Ph.D. in Electronic and Computer Engineering
Dept. of Electrical and Electronic Engineering
University of Cagliari

AN IMPLANTABLE MICRO-SYSTEM FOR NEURAL PROSTHESIS CONTROL AND SENSORY FEEDBACK RESTORATION IN AMPUTEES

Lorenzo Bisoni

Advisor: Dr. Massimo Barbaro
Curriculum: ING-INF/01 Elettronica

XXVII Cycle
April 2015

Ph.D. in Electronic and Computer Engineering
Dept. of Electrical and Electronic Engineering
University of Cagliari

AN IMPLANTABLE MICRO-SYSTEM FOR NEURAL PROSTHESIS CONTROL AND SENSORY FEEDBACK RESTORATION IN AMPUTEES

Lorenzo Bisoni

Advisor: Dr. Massimo Barbaro
Curriculum: ING-INF/01 Elettronica

XXVII Cycle
April 2015

Acknowledgements

With these few words I really want to thanks all the people that has been supporting me in this three long years and that in different ways had contributed to the achievement of the results here presented. I apologize if something is not written in English but I would like to thanks everyone in a more familiar and comfortable way.

Innanzitutto, vorrei ringraziare le persone che hanno creduto ed investito in me dandomi la possibilita' di mettere a frutto le conoscenze maturate in questi lunghi anni di studio. Un grazie per avermi dato la possibilita' di crescere, di cadere e rialzarmi con le mie gambe e di sbagliare, perche' e' proprio degli errori che si impara di piu'. Grazie per i tanti consigli e per avermi diretto per strade spesso tortuose ma sempre con traguardi davvero gratificanti.

Un doveroso e sentito grazie va a tutti i MENSAIOLI che navigando nello stesso mare e remando nella stesso CUBO hanno contribuito a rendere questo viaggio piu' sereno e piacevole. Grazie a chi con un EBBE ECCO e' stato capace di distrarti o farti sorridere perfino nei momenti piu' pesanti. Un grazie a.... perche' di FRKKY ce ne sono tanti, ma Lui non ha eguali ! Tra un DELIVERABLE e uno SCRUCCO, siamo pure riusciti a fare un po' di sport, che sudate vero.... ?!?! Si perche' si inizia con una pedalata e poi diventano due, tre, una sfida continua tra piscioni, con alternanza di salite, discese e poi salite, perche' quando si e' pazzi non si guardano maps, meteo ed orari. Certo, a volte si SBRUCCA ma poi, piu' uniti di prima, si ricomincia. Grazie anche per avermi supportato nei momenti peggiori perche' quando UBLOCCO sopraggiunge, non si sa mai come ci si risveglia. Grazie alla mia memoria esterna che e' sempre li', pronta a ricordarmi le scadenze, gli impegni e sopporta tutti i miei monologhi.... SCALLI! Ci sarebbero tante altre cose da rimembrare, ma il tempo stringe e il TRIGGHER incombe, per cui buona MENSA a tutti, Amici.

I thanks the whole team of the Laboratory for Biomedical Microtechnology at the University of Freiburg that received me as one of them and made me filling comfortable despite the long distance from my place. I really want to thanks each of you, for giving me part of your time, sharing your knowledge and introducing me in the fascinating world of the microtechnology. During my permanence in Freiburg, in addition to the satisfying scientific results I also met several friends. Even though I am Italian, you taught me how to make a tasteful handmade ice cream and a delicious Christmas sweet. I am also really happy to have had the chance to hike on the snow

in the moonlight, it was an unforgettable experience!!! Finally, I thank you for teaching me thousands of ways to open a beer and the Germans PROST!

Grazie a chi in mille modi non mi ha mai fatto mancare nulla, a chi in tutti questi anni mi ha sempre dato senza mai pretendere nulla in cambio. Non so proprio come avrei fatto senza il vostro supporto. Grazie per aver sopportato i miei silenzi, le mie assenze. Grazie per avermi sempre guidato e ricordato i valori importanti perche' alla fine e' soprattutto grazie a voi se ora mi trovo a scrivere questa tesi. Come si dice, una parola e' troppa e due sono poche, pero' ci tengo a ringraziarvi nuovamente per tutto quello che avete fatto e so che farete per me.

Un grazie speciale va alla persona che da poco si e' inserita nella mia vita stravolgendola. Ti ringrazio per avermi supportato e sopportato in questo lungo periodo, dalla permanenza all'estero alla scrittura di questa tesi. Grazie, grazie e grazie! Grazie per la tua capacita' di rendere piu' felici questi duri giorni di lavoro. Grazie ancora per tutte le cene PROKKI che si, hanno creato qualche problemino di bilancia, ma hanno sicuramente rallegrato l'animo.

Finally, I gratefully acknowledge Sardinia Regional Government for the financial support of my Ph.D. scholarship (P.O.R. Sardegna F.S.E. Operational Programme of the Autonomous Region of Sardinia, European Social Fund 2007-2013 - Axis IV Human Resources, Objective l.3, Line of Activity l.3.1.).

Abstract

In this work, the prototype of an electronic bi-directional interface between the Peripheral Nervous System (PNS) and a neuro-controlled hand prosthesis is presented. The system is composed of two Integrated Circuits (ICs): a standard CMOS device for neural recording and a High Voltage (HV) CMOS device for neural stimulation. The integrated circuits have been realized in two different $0.35\mu m$ CMOS processes available from AustriaMicroSystem (AMS). The recoding IC incorporates 8 channels each including the analog front-end and the A/D conversion based on a sigma delta architecture. It has a total area of $16.8mm^2$ and exhibits an overall power consumption of $27.2mW$. The neural stimulation IC is able to provide bi-phasic current pulses to stimulate 8 electrodes independently. A voltage booster generates a $17V$ voltage supply in order to guarantee the programmed stimulation current even in case of high impedances at the electrode-tissue interface in the order of tens of $k\Omega$. The stimulation patterns, generated by a 5-bit current DAC, are programmable in terms of amplitude, frequency and pulse width. Due to the huge capacitors of the implemented voltage boosters, the stimulation IC has a wider area of $18.6mm^2$. In addition, a maximum power consumption of $29mW$ was measured. Successful in-vivo experiments with rats having a TIME electrode implanted in the sciatic nerve were carried out, showing the capability of recording neural signals in the tens of microvolts, with a global noise of $7\mu V_{rms}$, and to selectively elicit the tibial and plantar muscles using different active sites of the electrode.
In order to get a completely implantable interface, a biocompatible and biostable package was designed. It hosts the developed ICs with the minimal electronics required for their proper operation. The package consists of an alumina tube closed at both extremities by two ceramic caps hermetically sealed on it. Moreover, the two caps serve as substrate for the hermetic feedthroughs to enable the device powering and data exchange with the external digital controller implemented on a Field-Programmable Gate Array (FPGA) board. The package has an outer diameter of $7mm$ and a total length of $26mm$. In addition, a humidity and temperature sensor was also included inside the package to allow future hermeticity and life-time estimation tests.
Moreover, a wireless, wearable and non-invasive EEG recording system is proposed in order to improve the control over the artificial limb, by integrating the neural signals recorded from the PNS with those directly acquired from the brain. To first investigate the system requirements, a Component-Off-The-Shelf (COTS) device was designed. It includes a low-power 8-channel acquisition module and a Bluetooth (BT) transceiver to transmit the acquired data to a remote platform. It was designed with the aim of creating a cheap and user-friendly system that can be easily interfaced with the nowadays widely spread smartphones or tablets by means of a mobile-based application. The presented system, validated through in-vivo

experiments, allows EEG signals recording at different sample rates and with a maximum bandwidth of $524Hz$. It was realized on a $19cm^2$ custom PCB with a maximum power consumption of $270mW$.

Contents

List of Figures

List of Tables

Introduction

The human body is often defined as a "perfect machine" in which hundreds of process run simultaneously and closely cooperate to reach a common goal: improve the body performance and let it survives against external threats. However, it undergoes the wear and tear of life and the unavoidable signs of time. Fortunately, where the body can't go, the science supplies its essential support to bring it back to an adequate performance level and to restore its basic functionalities. It is common today to substitute part of the human body in case of tissues damaging due to diseases or accidents, or simply to improve its beauty. Nevertheless, there is still space for science fiction movies to dream on cybernetic men or women having extra-powers and a perfect synergy with machines directly controlled by their brain. In fact, despite the great progresses that have been made in understanding the inner workings of the human machine many mechanisms are still unclear. Among these there is surely the complex neural network that from the brain diffuses to the most remote parts of the body delivering electrical commands and acquiring the correspondent feedbacks. Although research laboratories are already able to exchange signals with the Peripheral Nervous System (PNS), the technology behind the used instrumentation is too cumbersome, unstable and power hungry. Therefore, it is still far from a feasible integration with the human body closing the doors to a wide range of applications. For this reason, in the last years, many researchers are directing their efforts to miniaturize these bidirectional neural interfaces that is also the main topic of this thesis. It is part of a wider project aimed at developing a prosthetic hand controlled using neural signals. In particular in this thesis the focus has been put on the design of an implantable electronic device for neural signal acquisition and PNS stimulation. The commercially available prosthesis are based on Electromyographic (EMG) signals, their control implies unnatural movements and requires a great mental effort for the patient, especially during the first months after fitting, during which a special training to develop the control capabilities over the artificial limb is needed [159, 166]. As a result a number of patients give up the use of those devices very soon. On the contrary, the proposed approach offers several advantages. First, it is based on neural signals that are the same used to control the biologic limb, allowing a more comfortable solution for the amputee that will be closer to feel the robotic hand as the natural one. Secondly, placing different types of sensors on the limb surface, it is possible to trasduce the acquired information into electrical signals that can be injected into the PNS restoring the sensory feedback in the patient. The weakness of neural signals (neural spike amplitudes can span from few microvolts to hundreds of microvolts) makes their recording a critical operation and requires special care in terms of low noise and low power design. Neural spikes bandwidth lies in the frequencies from $500Hz$ to $10kHz$ with a peak around $2kHz$ and it partially overlaps with that of EMG

signals which have amplitudes several order of magnitude higher than that of neural signals. EMG signals are, for this reason, the most serious interference to cope with. Fortunately, the spectral signature of EMG decreases with frequency and, at $800Hz$ has an energy lower than that of neural signals. With a proper filter stage in the front-end circuit, it is then possible to isolate the neural signals and to prevent the EMG to mask them completely. On the other hand, the stimulation circuitry must provide current pulses whose amplitude, duration and frequency evoke the programmed stimulus without damaging the tissues. Typical neural stimulation patterns are bi-phasic current pulses with programmable amplitude in the range $10\mu A - 300\mu A$, period from $2.5ms$ to $1s$ and pulse width from $50\mu s$ to $150\mu s$. Bi-phasic pulses are needed since it has been demonstrated that the charge accumulation at the tissue interface can produce severe damages to the cells. To prevent these risks, bipolar active or passive waveforms should be used, in this way the charge accumulated in the first phase is compensated in the opposite phase. Another important issue is the high variability of electrode-tissue impedance whose value depends on the electrode placement inside the nerve and varies in the range $10k\Omega - 1M\Omega$ from electrode to electrode and during the lifetime of the implant. Therefore, reproducibility of the current stimuli requires the use of a high voltage supply and, thus, high voltage transistors in order to accommodate the large voltage drops required even by low stimulation currents. In this contest, the final goal is the development of a fully implantable device able to perform a bidirectional communication between the robotic hand and the patient. Due to small area, low noise and low power constraints, the only possible way to reach this aim is the design of full custom Integrated Circuits (ICs). Since they have different requirements and specifications, the idea is to use two separate ICs for recording and stimulation.

In the first chapter an overview on the main characteristics of the neural cells and on the electrochemical processes involved in the neural spikes generation is presented. A brief description of the project in which this research is part is also provided, finally an analysis on the state of art concerning the neural-machine interfaces is presented.

The recording IC is presented in the second chapter. It is the development of a previous research work in which a component-off-the-shelf (COTS) neural bidirectional interface was developed. The proposed IC is composed by the cascade of a preamplifier/ prefiltering block and a delta sigma modulator. The signal acquisition chain has been designed using a transistor level simulation model, developed in cadence environment, that describes precisely the circuit components and gives reliable information on the specification meeting. The task of the preamplifier/prefiltering block is first to amplify the signal in order to avoid its corruption due to noise and secondly to attenuate the huge EMG interferences avoiding the amplifier saturation. The signal is then digitalized by a 10bit resolution, third order, single loop, delta sigma modulator. The resulting 1bit data stream is finally sent to the decimator and stored in the pc for further processing. The chip was fully characterized and tested, first by electrical measurements and then by means of in-vivo experiments. The test outcomes proved the capability of the designed system to acquire the neural signals from the PNS and highlighted the need of improvements for a new future version of the recording chip.

The third chapter is aimed at the developing of the stimulation IC. The designed system can generate and inject into the nerve programmable current patterns in terms of amplitude, frequency and pulse width. As previously explained, due to the high impedance at the electrode-tissue interface, the $3.3V$ voltage supply is increased up to a maximum value of $20V$ by means of a programmable voltage booster to ensure a maximum stimulation current of $300\mu A$ for a maximum pulse width of $150\mu s$. Moreover, to control and limit the generated

high voltage, a voltage regulator has been designed. These two modules are shared between the eight stimulation channels, each of whose contains a programmable stimulation current generator and an output stage. The former is based on a $5bits$ current DAC generating current from $10\mu A$ up to $310\mu A$ into a low voltage domain whereas the latter converts the stimulation current from a low into a high voltage domain and delivers this current into the nerve. The designed device was fully tested and its functionalities were proved by means of in-vivo experiments on rats.

Since the aim of this work is to get a fully implantable bidirectional interface, the design and development of an implantable package for hosting the electronic parts is described in the fourth chapter. This part of the work has been carried on during my permanence at the *Institut fuer Mikrosysthemtechnik* (*IMTEK*) of the *Albert Ludwigs Universitaet* in Freiburg im Breisgau, under the supervision of Prof. Thomas Stieglitz. The proposed container embeds only the essential devices required to record and inject neural signals from/to the nerve. Thus, it will host the two custom ICs (recorder and stimulator) and very few external components such as by-pass capacitors. The reason for reducing as much as possible the number of components inside the package is essentially to reduce its dimensions so that it can be placed as close as possible to the nerve. In this way, the acquired neural signal will be less affected by external noise to the benefit of the overall system. Not only the size but also the shape of the container and the adopted materials are critical aspects that require a careful choice.

A wide-band and user friendly ElectroEncephaloGram (EEG) recording system for wearable applications was also realized. The EEG is a common technique for detecting symptoms of neurological diseases such as epilepsy, sleep disorders, anxiety and learning disabilities and in the recent years it has been applied also in developing the so called Brain Machine Interface (BMI). In the filed of neuroprosthesis, the EEG can be used as an additional channel for reaching a better control over the robotic limb, by integrating the information acquired from the PNS with those directly recorded from the brain. However, both applications require a long-term EEG monitoring, for example to follow the course of the disease, to prevent further degradations of the patient condition such as epileptic discharges or to constantly have a more fine control of the limb. Moreover, EEG acquisition during daily life activities is highly recommended to better reveal some pathologies. Traditional ambulatory EEG systems do not satisfy these requirements. In fact, patients can be continuously observed for only a few hours because of the costs and resource overheads and, in addition, they are forced to move from their natural environment. Therefore, they often feel uncomfortable and, depending on their pathology, this can affect the EEG acquisition, introducing undesired artefacts. Wearable EEG is aimed at overcoming these issues, allowing the recording of a longer temporal window that includes all stages of sleep and wakefulness, increasing the likelihood of recording typical symptoms in the medical applications and enabling a permanent control over the prosthesis. Even though many efforts have been already put on the realization of such EEG systems, some improvements are still needed. Most of them use proprietary radio links for data transmission requiring specific hardware to interconnect a remote back-end and they mainly operate in a bandwidth under $100Hz$ that may be enough to cover the most common diagnostic purposes, but a wider bandwidth, up to $600Hz$, is required to investigate some pathologies. Due to small dimensions and low power constraints, the best way to reach this aim is the design of a full custom IC. In particular, it is interesting to investigate the possibility of using the same neural recoding chip developed for the PNS with only few changes in terms of signal conditioning parameters, such as filter bandwidth

and gain. However, a preliminary evaluation of the key design features is necessary in order to define clear and precise design specifications. A low-cost and short implementation time device is then needed for this aim and the COTS approach seems to be the best solution for this purpose. In this work, a PCB with discrete components has been designed, developed and tested.

Chapter 1

Overview on bidirectional neural-machine interface

In this chapter the contest and the application field of this work of thesis is presented. First of all, a brief introduction on the project background is given and, since its main goal is to create a bidirectional interface between the human peripheral nerves and a robotic limb, an overview on the human nervous system and, in particular, on the neural signals' generation (Section 1.2) is provided. In addition, a short presentation on the different electrode's architecture used to directly contact the nerve for the neural information exchange between the two communication ends (brain and machine) is given in Section 1.3. Finally, the implementation issues connected to the development of the whole device, including the neural recording and stimulation unit and its implantable housing, are discussed in the last section of this chapter.

1.1 Project background: motivations and aims

The work described in this thesis is the combined result of different projects: *OPENHAND* (*OPEN neuro-prosthetic HAND platform for clinical trials*) and *HandBot* (*Biomechatronic hand prostheses endowed with bio-inspired tactile perception, bi-directional neural interfaces and distributed sensori-motor control*), both founded by the *Italian Ministry for University and Research* (*MIUR*) under, respectively, the *PRIN 2008* and *PRIN 2011* research programs, *NEMESIS* (*NEurocontrolled MEchatronic prostheSIS*) founded by the *Italian Ministry for Health* within the *Call for young researcher 2009* program and *NEBIAS* (*NEurocontrolled BIdirectional Artificial upper limb and hand prosthesiS*) founded by the *European Union* within the *Seventh Framework Programme* (*FP7*). The common objective of these projects is the development and the clinical evaluation of a neuro-controlled upper limb prosthesis intuitively controlled and felt by the amputee as the natural one. As a consequence, a novel neural interface able to provide a stable and very selective connection with the nervous system is required. The entire system combines microtechnology and material science and allows, on one side, recording of the neural signals governing the actions of the amputated hand/arm for the motion control of a mechanical prosthesis, and, on the other, providing sensory feedback from a variety of sensors (tactile and kinesthetic) placed on the skin of the

robotic limb through neuromorphic stimulation of the adequate afferent nerves within the residual limb. Moreover, reaching this goal requires also further studies in understanding the intrinsic way in which the human nervous system codes the efferent and afferent information in order to govern simple and complex hand/fingers movements.

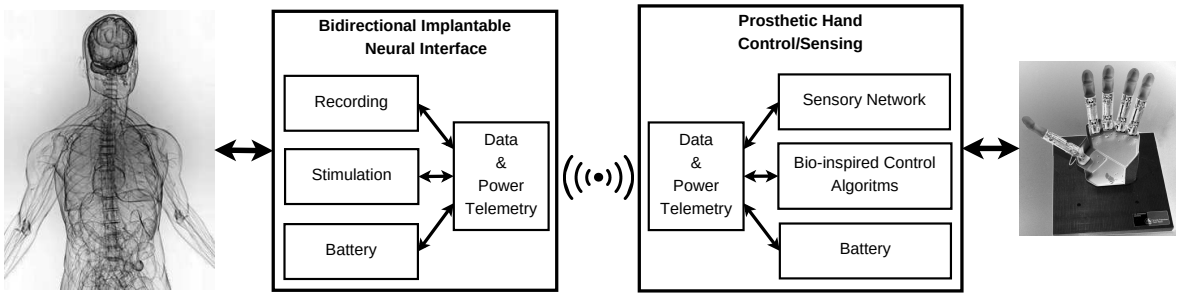


Figure 1.1: Architecture of the proposed neuro-controlled hand prosthesis.

In order to achieve the prefixed goals the systems depicted in Fig. 1.1 is proposed. Considering its complexity and the multidisciplinariety several partners has been involved in the projects and, referring to the NEBIAS project, a consortium of research groups from different European countries was created. Despite the huge variety of tasks included in the project, they are often quite overlapped requiring a strong cooperation between the involved partners. However, seven main topics had been identified in the project and assigned to each research group, on the base of its skills. In particular, the whole project is coordinated by the *Scuola Superiore Sant'Anna* (*SSSA*, Italy) that is also involved in the development of the mechanical limb and the coding and decoding algorithms respectively for the sensory feedback and motor information. Then, the *Albert-Ludwigs-Universitaet Freiburg* (*ALU-FR*, Germany) coordinates the design and realization of the implantable electrodes whereas the *University of Cagliari* (*UNICA*, Italy) is focused on the design of the embedded electronic that is the aim of this thesis. Moreover, the project involves other three universities in the clinical evaluation of the proposed system. The tests are first performed on rats at the *Universitat Autonoma de Barcelona* (*UAB*, Spain), followed by in-vivo experiments with non-human primates at the *Deutsches Primatenzentrum* (*DPZ*, Germany), to conclude with in-vivo trials with humans carried on at the *UniversitÃă Cattolica Sacro Cuore* (*UCSC*, Italy). The proposed prosthesis architecture has several advantages with respect to commercially available solutions based on EMG signals. In fact some studies reveal that 30 to 50% amputees do not use their prosthetic hand regularly, basically due to its low functionality, poor cosmetic appearance, and low controllability. On the contrary, the possibility to control the artificial limb with the thought clearly improves the amputee dexterity in using the prosthesis to perform tasks that are necessary for daily living activities and that cannot yet be done with the state-of-the-art robotic hands/arms. However, also in the neural prosthetics there are several possible approaches, the one pursued in these projects takes advantage by signals acquired by means of intraneural electrodes, thus allowing a stronger signal detection compared with extraneural recordings and a better selectivity, since the electrode insertion inside the nerve permits to discriminate among the single nerve fascicles within the nerve.

1.2 Nervous system

Each expression of our being such as the thoughts, the hopes, the dreams, the desires, the emotions, are due our nervous systems. It is the the mean through which we explore our self and interact with the surrounding environment. It has an architecture comparable to a personal computer (PC) with several input and output peripherals with which it continuously exchanges information. However even the most sophisticated PC is still far away from our nervous system in terms of interconnecting network complexity and cooperation between its different modules. The nervous system takes, elaborates and sends information related to the whole body in order to regulate all vital processes that continuously take place in it. The entire nervous tissue is part of the nervous system and it transfers information from one side to the other of our organism. The main functions of the nervous system include generating a feeling about the inner and outer environment, integrate the incoming sensory information, coordinate all voluntary and involuntary activities and control the peripheral apparatus.

The nervous tissue is composed of two main types of cells: nervous cells, also referred as neurons, and glial cells, sometimes called neuroglia or simply glia, that provide support and protection for neurons. In fact, the glial cells are more numerous than nervous cells and occupy almost the half of the nervous system's volume. Whereas the neurons are responsible for transferring and elaborating the information.

1.2.1 Neurons

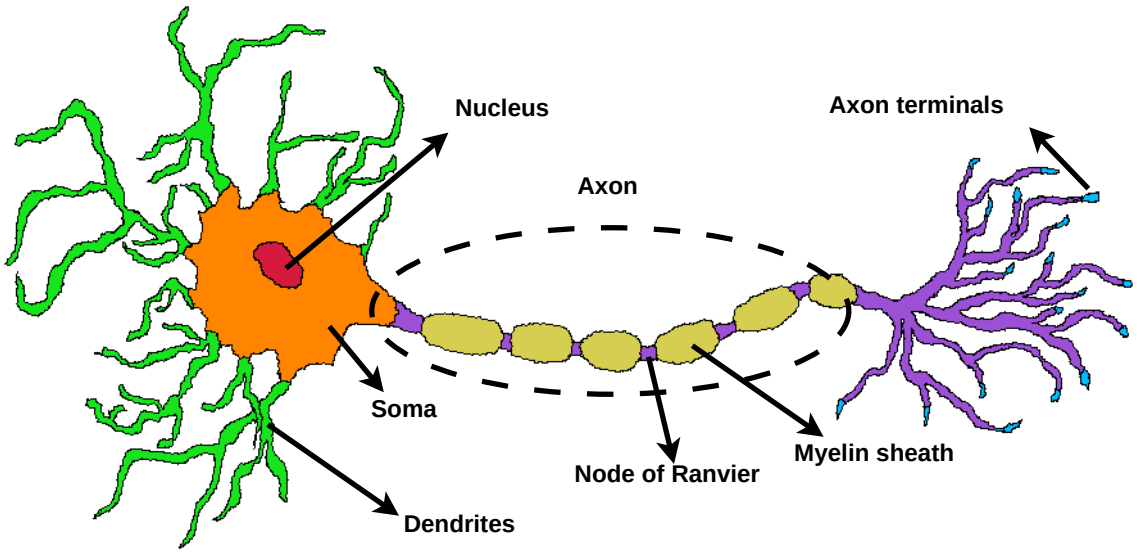


Figure 1.2: Nervous cell structure.

A typical nervous cell, depicted in Fig. 1.2, has a cell body (soma), dendrites, and an axon. Dendrites are thin structures that arise from the cell body, often extending for hundreds of micrometres and branching multiple times, giving rise to a complex *"dendritic tree"*. Thanks to their extension they have a wide surface to intercept the input signals coming from other neurons or from the external environment such as pressure, light, heat and smell stimulus. The soma is responsible of the neuron's vital functions and elaborates the signals acquired by the dendrites. In particular, it decodes the received signals and decides to generate or

not an action potential, the output signal of the neuron. Moreover, as any other cell, it synthesizes proteins, lipids, carbohydrates and coordinates all metabolic activities of the cell. Finally, the axon is a special cellular extension that arises from the cell body at a site called the axon hillock and travels for a distance, as far as one meter in humans or even more in other species. The axon transfers the action potentials generated from the cell body to the next neuron without a loss of the quality and intensity of the transferred signals. The cell body of a neuron frequently gives rise to multiple dendrites, but never to more than one axon, although the axon may branch hundreds of times before it terminates. At the of the axon there are the synapses where signals are sent from the axon of one neuron to a dendrite of another. There are, however, many exceptions to these rules: neurons that lack dendrites, neurons that have no axon, synapses that connect an axon to another axon or a dendrite to another dendrite, etc.

1.2.2 Neural signal generation in neurons

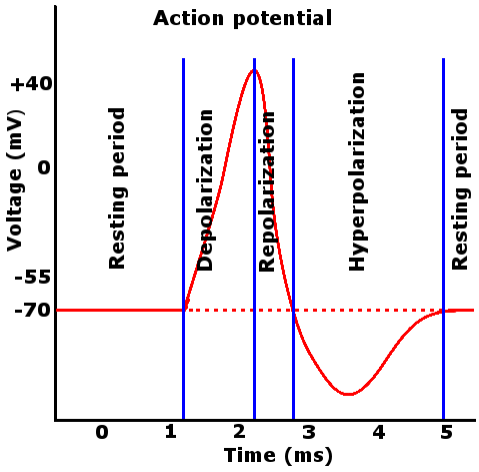


Figure 1.3: Typical action potential.

In Fig. 1.3 the shape of a classical neural spike is depicted, the changes of the voltage potential can be explained looking at the membrane cell configuration. In fact, the signal propagation across the nerve is possible thanks to the ion currents that flow across the cell membrane. Inside the cell there is a major concentration of potassium ions (K+) while outside the Sodium (Na+) concentration is prevalent. In resting conditions the internal side of the membrane is more negative than the external creating a resting potential of $-70mV$ (Fig. 1.4). When an over-threshold voltage stimulus (the threshold is around $-55mV$) is applied to the membrane the Sodium channels open, allowing the Sodium ions to enter inside the cell (Fig. 1.5), this causes the inside to become more positive that the outside increasing the membrane voltage up to $40mV$(depolarisation phase), due to this change of polarity the potassium channels open and ions flow out of the cell (Fig. 1.6), by this way a negative potential is restored inside the cell (repolarisation phase). The Potassium channels are slower than the Sodium ones, for this reason the number of Potassium ions flowing from the inner to the outside is higher than that of Sodium ions flowing in the opposite direction, as a result a hyperpolarization phase occurs. To restore the resting potential the Sodium-Potassium pump is needed, by this way potassium ions are bring back to the inside and Sodium ions

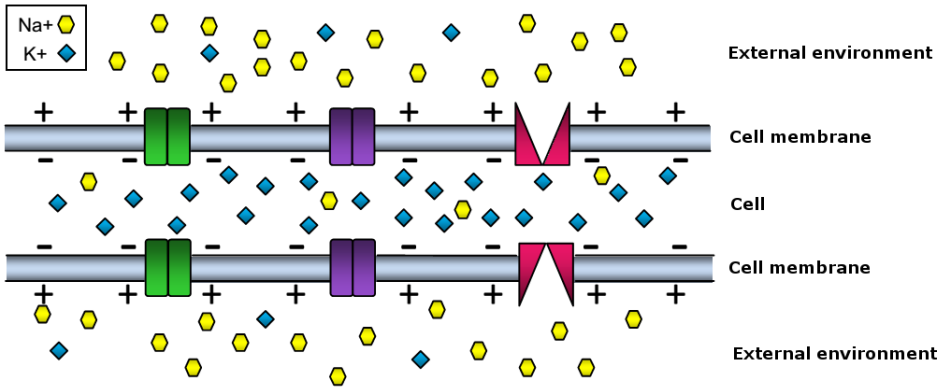


Figure 1.4: Ions cell concentration during the resting phase.

pushed out of the cell (Fig. 1.7). During this time interval, called refractory period, the action potential propagation is blocked. Note that the Sodium-Potassium pump is an active process because it moves ions against their gradients, so it requires energy to work that is provided by a co-enzyme called Adenosine triphosphate (AT P).

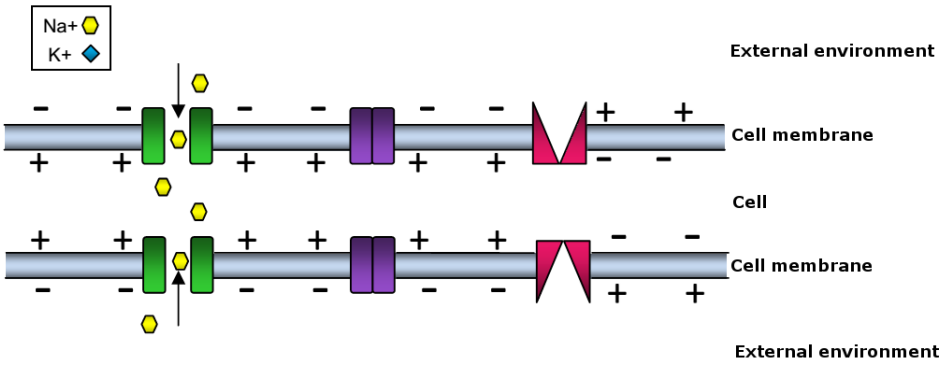


Figure 1.5: Cell membrane during depolarisation phase.

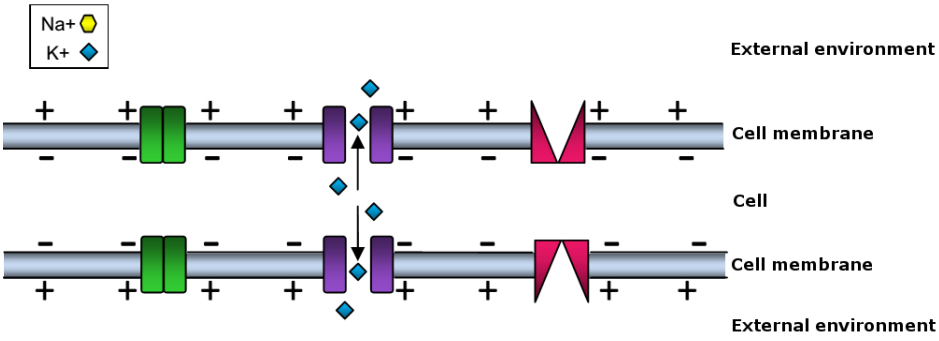


Figure 1.6: Cell membrane during repolarisation phase.

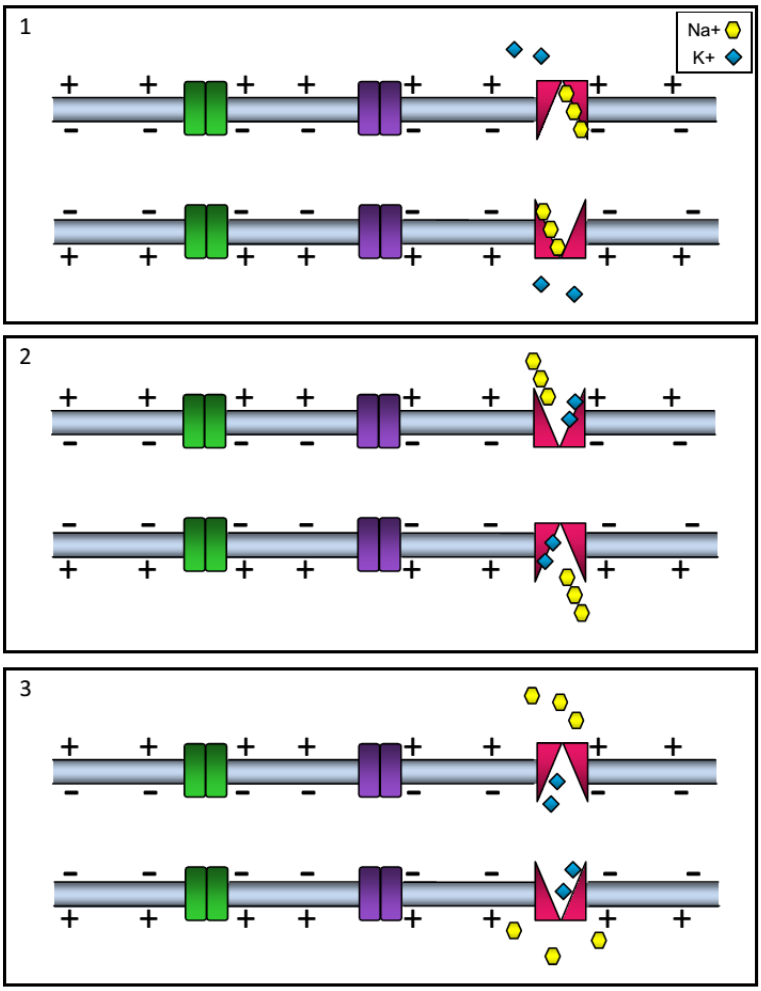


Figure 1.7: Cell membrane during hyperpolarisation phase.

1.2.3 The structure of the nervous system

The nervous system is organized in two main parts: the central nervous system (CNS) and the peripheral nervous system (PNS) (Fig. 1.8). The former is composed by the brain, inside the skull, and the spinal cord in the spinal column. Each section of the spinal cord is able to control specific motor functions. The CNS collects, elaborates and coordinates all sensory feedback and motor control signals. It also integrates more sophisticated functions, such as the intelligence, the memory, the emotions and the learning processes. With respect to the PNS, the CNS is able not only to acquire and to transmit but also to elaborate the information. The PNS includes all nervous tissues that are not part of CNS and, as main duty, transfers the afferent (input) and efferent (output) neural signals, from and to a peripheral organs, trough channels, called nerves. In particular, a nerve is an enclosed, cable-like bundle of axons (the projections of neurons) that provides a structured pathway that supports the electrochemical neural impulses transmitted along each of the axons. In the CNS, the analogous structures are known as tracts. Each nerve is a cable-like structure that contains many axons that are sometimes referred to as *fibers*. Within a nerve, each axon is surrounded by a layer of connective tissue called the endoneurium. The axons are bundled together into groups called fascicles. Each fascicle is wrapped in a layer of connective tissue called the

perineurium. Finally, the entire nerve is wrapped in a layer of connective tissue called the epineurium (Fig. 1.9). Moreover, nerves are bundled along with blood vessels, which provide essential nutrients and energy to the enclosed, and metabolically demanding, neurons [26]. Thus the PNS is composed by a wide network of nerves that connect the brain and the spinal cord to the all other body components including muscles and all the organs of the sensing, breathing, circulatory, excretory and digestive system.

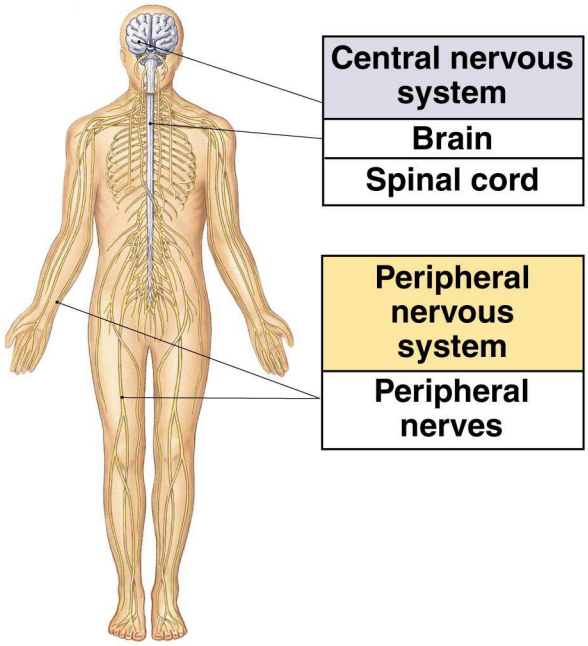


Figure 1.8: Human nervous system architecture: central nervous system (CNS) and peripheral nervous system (PNS) [3].

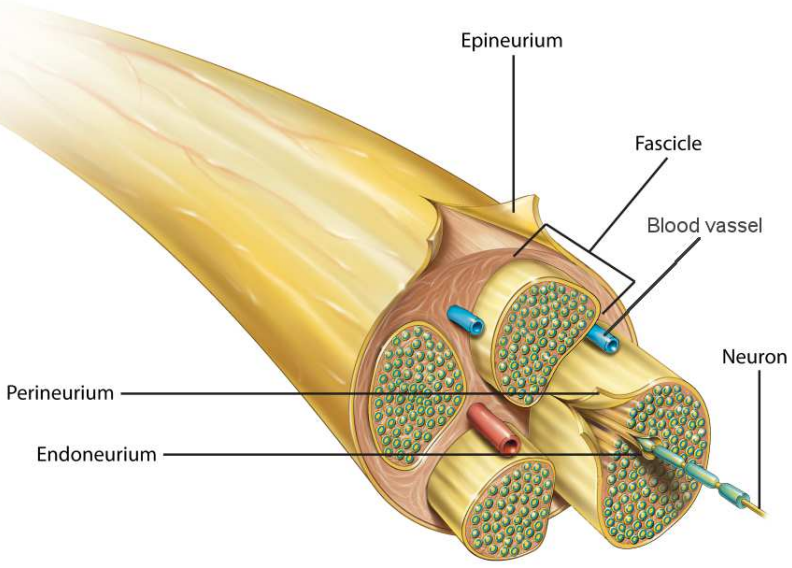


Figure 1.9: Nerve section [26].

The peripheral nerves contains the sensory neurons that transmit the sensorial feedback to the CNS and the motor neurons that transfer the information from the CNS to the organs

and muscles. The portion of the PNS involved in the body motor control is further divided in somatic nervous system (SNS) and autonomous nervous system (ANS). The motor neurons of the SNS are connected to the skeletal muscles and control the voluntary movements. Their cell body is in the spinal cord and their axon directly connects the controlled muscle. On the contrary, the motor neurons of the ANS control the involuntary actions and connect the heart, glands and smooth muscles.

1.2.4 Upper limb nerves

In the contest of this project, we are interested in the PNS and in particular in the arm and hand nerves that perform a substantial two-fold role: commanding the intricate movements of the arms all the way down to the dexterous fingers, while also receiving the vast sensory information supplied by the sensory nerves of the hands and fingers. The movements of the arms must be fast, precise, and strong to complete the diverse activities the body engages in throughout the day. Even the tiny hand muscles, which perform very delicate and precise movements, are driven by about 200.000 neurons. Rapid conduction of sensory nerve signals from the hands provides critical information to the brain and feedback during precise activities.

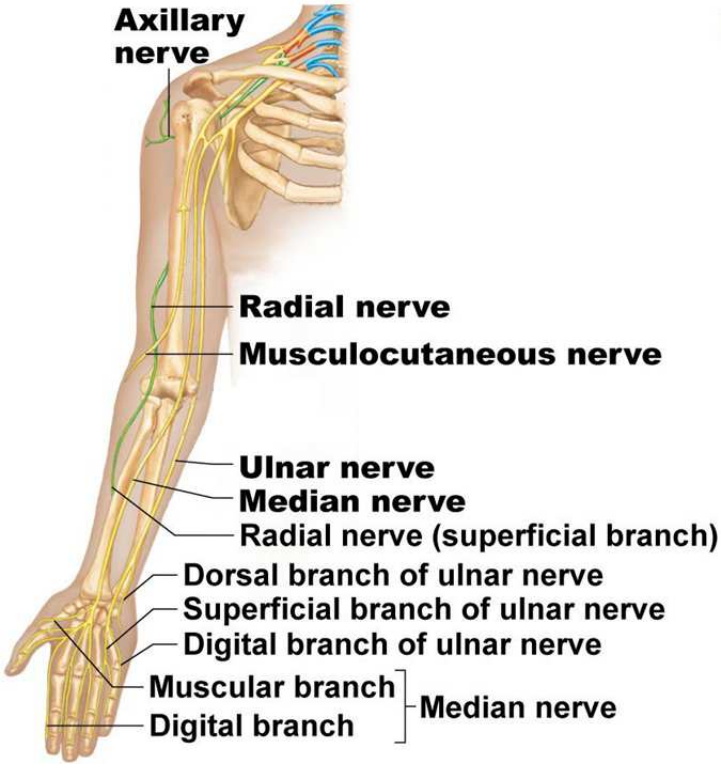


Figure 1.10: Peripheral nerve connection between the CNS and the upper limb.

Starting in the trunk of the body, the nerves of the arm and hand arise from the cervical and thoracic regions of the spinal cord as spinal nerves. These nerves merge to form a network called the brachial plexus before continuing into the arm. Five major nerves extend from the brachial plexus into the arm: the axillary, musculocutaneous, median, radial, and ulnar nerves (Fig. 1.10). Each of these nerves carries information in the form of nerve

impulses to and from a particular region of the arm and hand. Some of these impulses are sent from various parts of the brain and spinal cord, some come from sense organs located in the joints, ligaments, and tendons and others come from nervous tissue in the muscles themselves.

The forearm is served by several major nerves, including the radial, median and ulnar nerves. These nerves control the forearm muscles that move the hands and fingers through tendons that pass through the wrist. Skin in the posterior forearm and extensor muscles of the hand and fingers are supplied by the branches of the radial nerve. Along the anterior of the forearm, the median and ulnar nerves supply nerve signals to the skin and to the flexor muscles of the hand and fingers.

As major sensory components of the body, the hands are the destination for a majority of the nerves in the upper limb. The radial, ulnar, and median nerves, having already supplied connections to the arm and forearm, continue into the hand where they form a branching network of nerve fibers. These myriad nerve fibers work together to control many delicate, precise muscles of the hand and receive signals from millions of sensory receptors that detect touch, pressure, temperature, and pain. The median nerve supplies the muscles and sensory receptors of the skin in the lateral (thumb side) palm, first, second, and third digits (thumb, index, and middle fingers), and lateral half of the fourth digit (ring finger). Along the dorsum (back) of the hand, the radial nerve supplies the muscles and sensory receptors in the lateral dorsum, and the first, second, and third digits. On the medial side of the hand, the ulnar nerve supplies the sensory receptors and muscles in the medial palm, medial dorsum, medial half of the fourth digit, and the fifth digit (pinky finger).

The sum of these nerves and sensory receptors allows the peripheral nerves in the arms and hands to collect information about the external conditions in relation to the body's internal state; to analyze this information; and to initiate appropriate responses to satisfy the body's needs. The speed at which we can, for instance, remove our hand from a surprisingly hot surface exemplifies the power of the central and peripheral nervous systems in coordination within the upper extremities. Remarkably, the nervous system transmits such messages to the brain at speeds of 180 miles per hour.

1.3 Implantable neural electrodes

To achieve a neuro-controlled prostheses, a direct connection to the amputee nervous system is required. In particular, we are interested in controlling the artificial limb using the signals from the PNS. As a consequence, implantable electrodes are necessary to link the biological tissues, described in Section 1.2.3, and the sensing electronics. Moreover, to restore the sensory feedback too, the electrodes should support a bidirectional signals exchange. In fact, on one hand the device must allow to record neural signals, on the other hand to send stimulating signals from the external to the nervous system. Getting a bidirectional electrode is a challenging requirement since, as is later detailed, neural signal recording and stimulation have different electrode specifications to achieve an optimized solution. Moreover, since, in the nerves, the electrical conduction is based on ions, the electrodes play also the role of transducers from ions to electrons current flow and vice versa.

1.3.1 Modelling the electrical electrodes behaviour

The biological environment is mainly composed by water and electrolytes such as sodium chloride, potassium, calcium, and sodium bicarbonate. Due to their electrical polarity, the water molecules surround each dissolved ion creating a water shield that prevents a direct contact between the charge carrier and the metal electrode. As soon as the electrode is inserted in the solution, a first layer of water dipoles covers the metal surface creating an additional insulation layer called Helmholtz double layer which thickness is about $1nm$. Moving further into the solution, the next layer is composed by water encapsulated ions which centres of charge form a plane called outer Helmholtz plane (OHP). When a metal is inside a solution, depending on the metal Fermi level and on the electrolyte, rather a negative or a positive charge potential relative to the solution is developed. In addition, considering that water is a good insulator, the structure composed by OHP and the metal electrode behaves as a parallel plates capacitor named Helmholtz capacitance (C_H). The voltage across the C_H (V_{EE}) lies in the range of usually few mV up to $1V$, depending on the type of metal and electrolyte, and the inner electrical filed strength can reaches enormous levels of $1MV/mm$. This is a simplified model of the electrode/electrolyte interface, called phase boundary, depicted in Fig. 1.11.

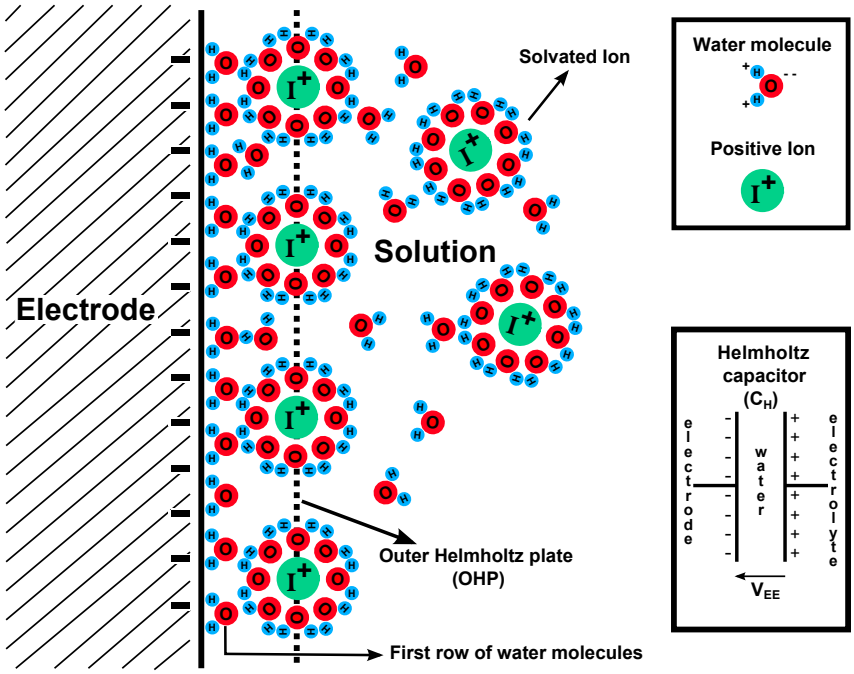


Figure 1.11: Simplified electrode/electrolyte interface.

The typical "communication" between the metal and the ions is based on electrical and chemical mechanisms. Changing the metal voltage potential is possible to modulate the charge accumulated on the electrode surface and, due to the capacitive coupling (C_H), the ions concentration on the OHP. This capacitive charge transfer does not involve any chemical reaction but unfortunately it allows only very small amount of charge to be transferred because exceeding a certain charge then the voltage increases too much and some chemical reactions can occur. Moreover, since it is a pure capacitive current flow, no charge carriers cross the Helmholtz double layer. Additionally to this electrical mechanism, other two electrochemical processes occur at the phase boundary: reversible and non-reversible faradic

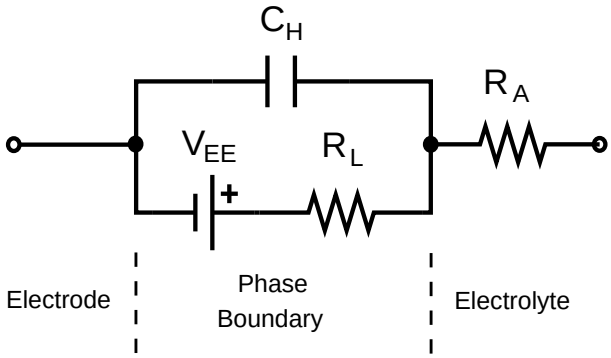


Figure 1.12: Simplified behavioural model of the electrode/electrolyte interface for tissue stimulation inside the water window.

reactions. They are both characterized by an alteration of the electrode surface due to chemical reactions with the electrolyte and by charge carriers crossing the C_H dielectric. However, in the first process the chemical reactions are reversible, so pushing current into the tissue some chemical reactions occur and pulling it out again the reactions are reversed and it is as nothing is happened. On the contrary, the non-reversible faradic processes cause permanent corrosion of the electrode surface and produce substances that diffuse or bubble into the electrolyte causing a pH shift of the biological environment and a consequent tissue irritation. These chemical reactions strongly depends on the metal and electrolyte properties, but since the electrolyte is fixed by the human body, the only way to control these processes is to carefully choose the proper metal. Furthermore, to avoid these undesirable side effects, the voltage potential applied to the electrode should stay inside a safe operation range called water window, putting a limit to the maximum injectable charge.

Material	**Resistivity** $\rho(\Omega * m)$
Fat	$15-10$
Brain	$3-9$
Muscle	2.4
Blood	1.4
Cerebrospinal fluid	0.89
$Pt_{80}Ir_{20}$	$3.1 * 10^{-7}$
Gold	$2.2 * 10^{-8}$

Table 1.1: Biological tissues and metals resistivity.

A simple behavioural model of the electrode/electrolyte interface is depicted in Fig. 1.12. The access resistance (R_A) is the ohmic electrical resistance in the path of the electrical current flowing between the current source and the electrolyte resulting in the sum of the electrode wire and solution resistance that usually dominates. The R_A increases with decreasing the electrode size and strongly depends on the electrolyte resistivity ρ. Typical biological tissues resistivity are collected in Table 1.1. The C_H, previously described, depends on the effective metal surface area and not on the geometrical one. Therefore, by increasing the roughness of the electrode surface the C_H increases allowing a higher amount of charge to be transferred. Finally, since the C_H is not ideal, a leakage resistance (R_L) to model the leak-

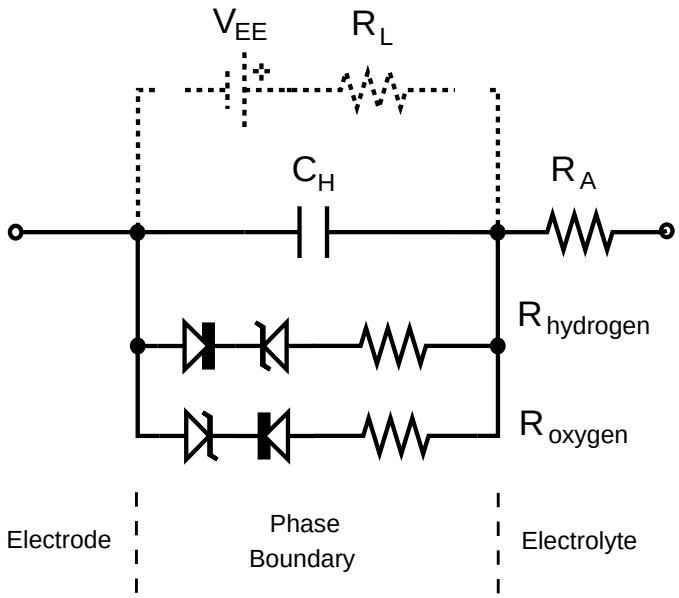


Figure 1.13: Simplified behavioural model of the electrode/electrolyte interface for tissue stimulation beyond the water window.

age of charge carriers through the C_H dielectric must be considered. The larger the effective electrode surface area, the smaller is the R_L. The presented phase boundary model well represents the tissue stimulation process when non-reversible chemical reactions occur.

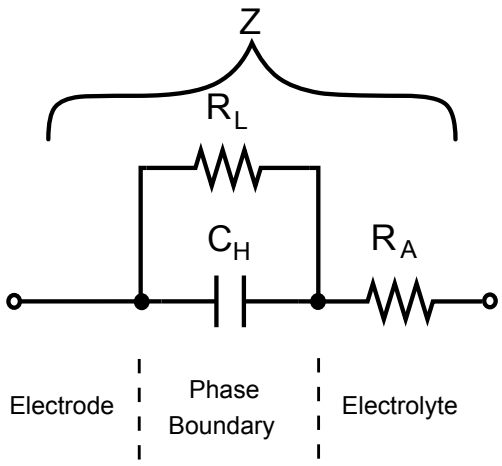


Figure 1.14: Simplified behavioural model of the electrode/electrolyte interface during signal recording.

Beyond the water window, tissue damages may occur and water dissociating process starts with consequent oxygen and hydrogen bubbling. In this case the whole interface shows linear current/voltage relationship and it is better represented by the circuit depicted in Fig. 1.13. In this new model, the zener diodes (Z_D) define the water window, becoming conductive when the applied voltage is besides that range, and the $R_{hydrogen}$ and R_{oxygen} model the current/voltage ratio observed respectively during hydrogen and oxygen bubbling. Since these resistance are smaller than R_L, they dominate and R_L and V_{EE} are usually neglected. Finally, with regard to the biological signal recording, the electrode/tissue inter-

face can be modelled with a complex impedance as depicted in Fig. 1.14. In this case, we are more interested to the signal variable component rather than their constant potential and due to the C_H, the interface acts as a high-pass filter, blocking the low frequency signals, with a cut-off frequency defined by the parallel between C_H and R_L. Therefore these two parameters must be carefully tuned considering the bandwidth of the biological signals to be acquired.

1.3.2 Electrode design

The design of electrodes involves different disciplines and strongly depends on the specific application. Recalling the target of this work, an implantable electrode to acquire/inject neural signals from/to the arm nerve is required. Since the electrode direct connects the inner body tissue, severe requirements in terms of biocompatibility and biostability put a strong limitation on the materials selection. The electrode must not be toxic for the organism and should last as long as possible in contact with the hostile biological environment to avoid frequent patient surgeries. All material's mechanical, chemical and electrical properties must be carefully considered to obtain an electrode that perfectly interfaces the organism without damaging the tissue and allowing good quality signal exchange between the body and the machine. For example, properties such as the mechanical robustness and the chemical corrosion refer to the material biostability and define how long the electrode will "survive" inside the body whereas the young modulus evaluation is important to obtain an electrode that imitates, as much as possible, the tissue's stiffness and elasticity avoiding tissue damages. Also the direction of the desired communication between the body and the machine should be taken into account since, as explained in Section 1.3.1, depending on whether we want to stimulate the tissue or to record signals from the organism, the electrodes behaves differently and a good compromise between the material's properties must be reached. Also the required electrode's selectivity and non-invasivity are critical aspects to deal with in order to define the electrode architecture and its geometrical configuration. In particular, because of the nerve bundle structure, the selectivity plays a key role in this specific application. In the inner part of the nerve, there are several fascicles and each fascicle contains different axons, therefore the electrode must be able to isolate a single neural signal from the other electrical activities around it. In this way, with electrodes placed close to neural fibers, it becomes possible to record a stronger signal, improving the Signal to Noise Ratio (SNR). From the patient point of view, it is suitable to minimize invasivity. These two requirements are clearly in contrast. In fact, if the aim is to have a high selectivity, than it is necessary to increase invasivity inserting the electrode into the body (non superficial electrode) or even within the nerve (intraneural electrode). In these years several categories of electrodes have been developed, they can be divided in two categories: extraneural (i.e cuffs) which are less selective but also less invasive, and intraneural (longitudinal, transversal, penetrative and regenerative) which are preferred for their better selectivity but imply a higher invasivity. A brief summary on the main electrode types is presented in the following.

1.3.3 Extraneural electrodes

Cuff electrodes

Cuff electrodes are among the most used extraneural electrodes. They have a cylindrical shape to completely envelope the nerve as depicted in Fig. 1.15.

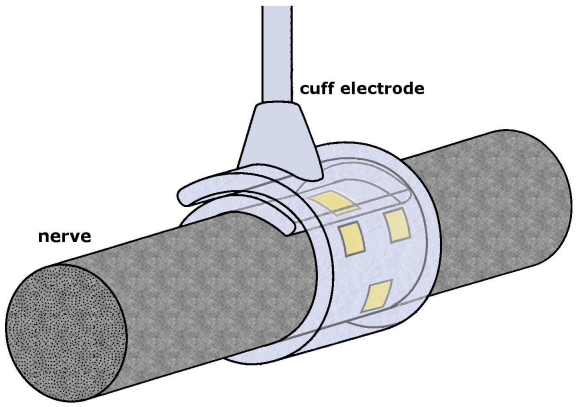


Figure 1.15: Extraneural cuff electrode.

The electrical contacts, which number depends on the specific application, are placed in the inner surface of the cylinder that directly contact the external nerve tissue. In this way the recorded signal is as strong as possible. There are two main types of cuffs: split-cylinder and spiral cuff. The formers have the shape of a semi-open cylinder that must be closed around the nerve with suture making them uneasy to implant. A common issue with split-cylinder cuff electrodes is their poor adaptability to the nerve diameter. In fact, a too large electrode does not allow a good contact with nerve and it will produce a too weak neural signal whereas a device too tight may cause nerve damages. In order to overcome these problems spiral cuffs have been introduced. They are fabricated with a stretch sheet that allows them to follow the nerve shape [125]. Compared to others extraneural electrodes, the cuff ones are reliable and robust and can be precisely placed around the nerve with a reduced invasiveness. Moreover, since the contacts are in the inside of the cylinder, the stimulation can occur with lower currents than those used in other extraneural electrodes. However, they suffer a low selectivity [182]. In fact, being wrapped around the nerve, they record the whole electrical activity of the nerve which is the sum of the signals from all axons. Furthermore, stimulating afferent axons from the outside of the nerve requires, anyway, high stimulation currents with respect to the intraneural electrodes.

Flat interface nerve electrodes

An evolution of the standard cuff electrodes to overcome their limited access to information from central fascicles is the flat interface nerve electrode (FINE). Due to its flat geometry, it presses the nerve forcing all nerve fascicles close to the epineurium [187]. The idea behind this design is to push the natural reshaping capability of the nerve in order to access most of the fascicles without compromising the blood-nerve barrier. This electrode has successfully shown recording selectivity in simulations and animal [210, 134] and human [161, 160] experiments. Finally, although the combination of low invasiveness and high selectivity makes

FINE electrode a promising neural interface, its long-term biocompatibility still needs to be proven in humans.

1.3.4 Intraneural electrodes

Intrafascicular electrodes

Electrodes able to penetrate the nerve have been introduced in order to allow higher selectivity with respect to extraneural electrodes. Being placed inside the nerve, the intrafascicular electrodes are in direct contact with tissue to be stimulated or from which neural signals are recorded. In this way, pulses with lower amplitude are required to get the same stimulation results of extraneural electrodes [211] and the signal-to-noise ratio (SNR) of recordings is increased. Moreover, stimulation through them allows to activate single fascicles inside the nerve with little cross-talk to adjacent ones. Several intrafascicular electrodes may be implanted for multiple stimulation and recording. For improving the selectivity and depending on the purposes, intrafascicular electrodes with different geometries were developed. Longitudinal electrodes get the name from their insertion way and are often indicated as LIFE (Longitudinal Intra-Fascicular Electrodes). In fact they are implanted throughout perinervium and placed, parallel to the axe of nerve, inside the nervous fascicles. They host multi-active sites composed of a thin conductor wire made of Platinum-Iridium (Pt-Ir) or fabricated with metallized Kevlar fibers, covered with an insulating sheath. Multi-channel structures allow understanding better the signal propagation along the nerve. They have been first tested in animals and later implanted for stimulation of the peripheral nerves in the human arm [113]. Nevertheless, LIFEs have some drawbacks regarding their radial symmetry [212], since the fixed distance between electrode and nerve limits selectivity. Moreover the electrode stiffness causes micro-movements that, in the long term, may damage the nerve. To overcome some of their flaws, new thin film Longitudinal Intra-Fascicular Electrode (tf-LIFE) were introduced. They are an evolution of LIFE composed of a double sided structure with contacts dislocated in different parts of the electrode. Due to its flexible structure, it allows a better compatibility with the tissue preventing possible nerve damages. The need for electrodes able to move within the nerve, approximating the electrical contacts to nervous fibers, have brought to a new generation of tf-LIFEs based on Shape Memory Alloy (SMA) materials. A serpentine shape can be memorized in the SMA, placing electrical contacts in the crests of serpentine. In this way, when the electrode reaches a determined temperature, its shape can be modified and active sites moved closer to the axon [25]. Anyway, due to their longitudinal placement inside the nerve, these intrafascicular electrodes are characterized by a low spatial resolution. To overcame this limitation, Transverse Intrafascicular Multi-channel Electrode (TIME) were developed. They are designed to be implanted transversally through the nerve, placing the active sites in a way that enhances the possibility of accessing a larger, spatially separated sub-population of different nerve fibers or fascicles. In theory, this is comparable to implanting several LIFEs in one nerve or several single fascicles. A complete description of TIME electrode is in [23]. Several studies have been conducted to compare the different performance of LIFE, tf-LIFE and TIME electrodes [16, 88]. In particular they prove the ability of a single TIME electrode to excite various muscles by stimulating through its different active sites.

Penetrating electrodes

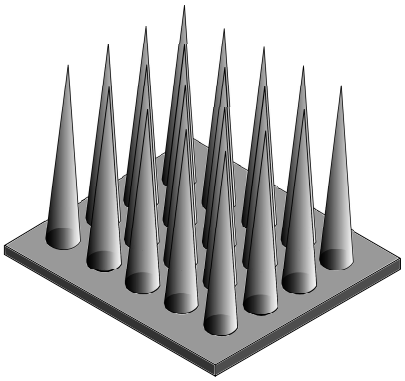


Figure 1.16: Penetrating electrode.

Penetrative electrodes are composed by a matrix of needles attached to a rigid substrate (Fig.1.16). In their simplest configuration they are called shaft electrodes and they are composed of only one needle. Structures with many electrodes are called MEA (Multi Electrode Array), a widely used version of MEAs has been developed at Utah University and it is called UEA (Utah Electrode Array) [110]. Penetrative electrodes were used primarily in the CNS, but there are also applications related to PNS although their stiffness and their difficult implantation does not make them particularly suitable for this purpose. When the electrode is used in CNS, needle can penetrate trough the skin in the skull reaching cerebral neurons. In the PNS, needles penetrate within nervous fascicles, implantation is facilitated by pneumatic insertion techniques that, increasing insertion velocity, allow preserving nerve integrity [28]. Recent studies show that a valid alternative, that can guarantee a better mechanical stability and a high biocompatibility, is in implementing MEAs with carbon nanotubes. Tests demonstrate that impedance in this electrode is one to two orders of magnitude smaller than that measured using traditional MEAs, thus significantly improving the performance of neural electrode [95]. Electrodes array have been used in numerous applications, implanted within acoustic nerve for auditory function restoring [204] and in the skull for recording brain signals in animals and also implanted in humans for robotic limb control [195]. Although high selectivity is a major design advantage of MEAs, their capability to discriminate single units has been observed to deteriorate over long periods of time [139]. Moreover, despite the reported functionality and safety of the MEAs, their implantation in the PNS compromises the perineurium and the blood-nerve barrier, carrying a significant risk of nerve trauma. This fact, together with a relatively complex implantation, and further stabilization, are the main drawbacks of this interface.

Regenerative electrodes

The last typology of intraneural electrodes that will be analysed in this contest is the regenerative electrode also referred as sieve electrode. It is transversally inserted in the nerve and is shaped as a grid that can be either circular or square. A possible architecture is depicted in Fig. 1.17. The grid plays a fundamental role because it allows the neural fiber regeneration through its holes, this is the reason why it is called regenerative electrode. This special structure confers to the electrode a double function. On one side it allows to contact single axons of the different nerve fascicles since the electrode active sites are placed inside

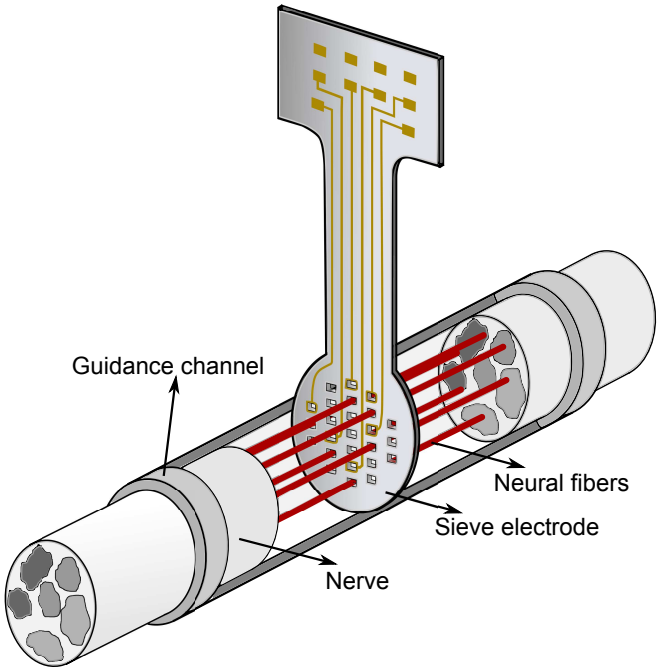


Figure 1.17: Sieve electrode.

the holes of the grid, making them the more selective among all presented electrodes. On the other hand, it makes the electrode very stable inside the nerve once the neural tissue regeneration has occurred. The number and the dimension of the grid vias is surely a crucial issue in designing such electrodes. In fact, different studies demonstrate that too small vias can inhibit neural tissue regeneration whereas, increasing their diameter, the distance between vias increases leading to an excessive deflection of neural fibers with a consequent difficulty in neural tissue regeneration. A good compromise seems to be the fabrication of electrodes with a diameter in the range $45\mu m - 60\mu m$ [126]. Moreover, for prosthesis control purposes, the electrode is usually divided in reference areas by shorting different vias to a unique electrical contact in order to record specific neural patterns [193]. The implementation of multi-via electrodes (some sieves contain 800 vias) is facilitated by the introduction of polyamide. This material is more flexible than silicon and allows to reduce the risk of nerve damages during implantation. Moreover the high biocompatibility degree of polyamide permits longer time implantation than that of silicon [89]. As previously introduced, the price of a high sensitivity is the high invasivity of the electrode. This aspect jointly to the fact that neural signals cannot be recorded until the regeneration is completed (usually about 12 weeks) are the main drawbacks of sieve electrodes. In particular, their high invasivity has not yet allowed their implantation on humans, although encouraging experiments have been carried out on frogs, rats and fishes [126]. Improvement on selectivity and cross-talk reduction is reached with the newer Regenerative Scaffold Electrodes (RSEs), a combination between sieve and cuff electrodes that better isolates nerve fascicles [117]. They are based on a thin-film sheet with micro channels that topographically guide the axons regenerating from a sectioned peripheral nerve across the electrode active sites. Different flexible materials such as polydimethylsiloxane (PDMS) [174] and nanofibers [43] have been investigated for RSEs fabrication in order to increase their tolerance to demanding mechanical handling such as twisting and bending. Moreover, some studies [58] demonstrates that embedding

substances such as extracellular matrix (ECM) proteins and neurotrophic factors (NF) in the nerve conduits enhances the nerve reconstruction. Many findings suggest that microchannel scaffolds are well suited for chronic implantation and peripheral nerve interfacing to promote organized nerve regeneration that lends itself well to stable interfaces.

1.4 Implementation issues

Today many devices are commonly and often quite easily placed inside the human body to restore some lost functionalities or simply to support the activities of the natural organ. In both cases, several strict requirements, defined on national and international directives, must be satisfied before the use of the medical device will be approved. In particular, the European Community has defined three main directives: the Medical Device Directive 93/42/EEC, the Active Implantable Medical Devices Directive 90/385/EEC and the In Vitro Diagnostic Medical Devices Directive 98/79/EC. The directive 90/385/EEC, introduced in the 1990, is the one that covers the placing on the market and putting into service of "active implantable medical devices" (AIMDs). Through these documents the European Union (EU) defines a series of conformity assessment procedures that all medical devices have to undergo. However, it is not economically feasible nor justifiable in practice to subject all implants to the most rigorous conformity inspections. Therefore, a medical device classification system was introduced to apply to medical device the appropriate check procedures only. The main classification criteria is the device potential risk defined considering some parameters such as the duration of use (transient, short and long term), the location of use (on central circulatory system, on central nervous system, outside of both), the level of invasiveness (non-invasive, invasive through body orifices, surgically invasive, implantable) and the energy supply (non-active, active). The EU legislation includes also several documents that contains a technical specification or other precise criteria designed to be used consistently as rules, guidelines or definitions, generally referred as "standards". There are national and international standards, created by bringing together the experience and expertise of all interested parties such as the producers, sellers, buyers, users and regulators of a particular material, product, process or service. Standards, harmonized internationally by the International Organization for Standardization (ISO), are designed for voluntary use without imposing any regulation and to increase the reliability and the effectiveness of goods and services. Moreover, following a common evaluation procedure, it is also easier to compare different solutions one with the other. Only after passing the related conformity assessment procedures, the device obtains the CE mark and can be commerced. What has been discussed until this point refers to the general procedures that has to be respected to produce any medical devices, whereas hereinafter more issues related to the specific goal of this thesis work will be addressed. The weakness of neural signals in the peripheral neural system is surely the major issue to face with in neural-machine interface designing. Moreover, especially for implantable devices, additional strict requirements in terms of system dimension, maximum power consumption and human safety make harder to find a suitable solution. The recoding of such low amplitude signals in a noisy and hostile environment as the inside of the body is, requires special care in designing a low noise and high-quality signal elaboration system. Furthermore, restoring the sensory feedback implies the use of a stimulator to inject current signals into the nerve without tissue damaging. Finally, the materials selected for developing the implantable devices must be totally biocompatible and biostable in order not to generate

infections and to obtain a device with a long expected life. These major implementation issues will be further discussed in the following.

1.4.1 Recording issues

The action potential directly measured at the cell membrane has an amplitude that can reach about $70mV$ as depicted in Fig. 1.3. Unfortunately, the cell surrounding layers act as a shield for the signal that is consequently attenuated. Nevertheless, it can still be detected, but its weakness makes it necessary to introduce in the recording circuit special techniques for low noise design. Signal amplitudes outside the epineurium can be lowered down to $1\mu V$ [150], whereas typical amplitudes for intraneural signals range from tens to hundreds of microvolts [70, 214]. In addition to the low signal amplitude, another critical recording aspect is the neural spikes bandwidth that, ling in the frequency from $500Hz$ to $10kHz$ with a peak around $2kHz$, partially overlaps with the Electromyographic signals (EMG) which have amplitudes several order of magnitude higher than that of neural signals. EMG interferences are, for this reason, the most serious interferences to cope with. Fortunately the spectral signature of EMG decreases with frequency and, at $800Hz$, it has an energy lower than that of neural signals [150, 69]. Using a proper filter stage in the front-end circuit, it is thus possible to isolate the neural signals and to prevent the EMG to completely mask them. In addition to the biological interferences, the noise due to the electronic devices must be considered too. The main noise contributions are flicker noise and thermal noise. The former is inversely proportional to the frequency (it is also called $1/f$ noise), and plays a key role in low frequency applications. In a MOS transistor it can be modelled as a voltage source in series with the MOS gate given by Eq. 1.1, where K_f is a constant depending on process parameters:

$$\overline{V_{n,flicker}{}^2} = \frac{k_f}{WLC_{ox}} \cdot \frac{1}{f} \tag{1.1}$$

Eq. 1.1 shows that flicker noise is reduced if wide area transistors are used. Physical causes of Flicker noise are not well known, the phenomena has been explained with charge fluctuation at oxide-semiconductor interface due to presence of traps. As the p-conduction occurs in depth while n-conduction is superficial, very close to the interface with the oxide, PMOS devices exhibit less flicker noise than NMOS ones. The thermal noise expression is given by Eq. 1.2, where γ represents the channel length modulation effect.

$$\overline{V_{n,th}{}^2} = \frac{4KT\gamma}{g_m} \cdot \Delta_f \tag{1.2}$$

The noise is reduced when g_m increases [145]. In terms of MOS size, this means that a large and short channel MOS minimizes thermal noise. A useful parameter for the evaluation of flicker noise incidence with respect to thermal noise is the corner frequency. It is the frequency at which flicker noise and thermal noise give the same contribute to the circuit. It can be calculated equating 1.1 and 1.2, obtaining 1.3.

$$f_{corner} = \frac{K_f}{WLC_{ox}} \cdot \frac{3}{8KT} \cdot g_m \tag{1.3}$$

Input Referred Noise (IRN) is the most widely used parameter to estimate the effect of noise in a circuit. It resumes all noise sources into a single voltage noise source, placed at the

input of the amplifier. By this way it is immediate to understand how much noise is degrading the input signal. A key role in neural signal acquisition is also played by low powering. Since the tendency is to acquire more signals simultaneously, the use of more amplifiers is required, causing the power reduction available for each of them. Unfortunately low-noise and low-power designs are in contrast since power scales as $1/\overline{V_{noise}{}^2}$ [198]. For this reason, the major effort of researchers is to find a good compromise between these two crucial issues. Noise Efficiency Factor (NEF) is an indicator used to compare the power-noise performances of different amplifiers. It has been introduced in [177] and describes how many times the noise of a system, with the same current drain and bandwidth, is higher compared to the ideal case. Its value is given by Eq. 1.4.

$$NEF = V_{rms,in} \cdot \sqrt{\frac{2 \cdot I_{tot}}{\pi \cdot U_t \cdot 4kT \cdot BW}} \tag{1.4}$$

The minimum value for NEF is reached by an amplifier with a single bipolar transistor, in this case without considering flicker noise, $NEF = 1$. Basically all practical circuits have higher values [70]. Amplifiers with lower NEF can achieve the same IRN with lower power dissipation [209].

1.4.2 Stimulation issues

Peripheral nerve stimulation, is a commonly used approach since the 1960s to treat chronic pain such as trigeminal neuropathic pain, nerve injuries, peripheral neuropathy, some headache syndromes and post amputation pain syndrome. Other applications include clinical treatment of epilepsy, tremors associated with Parkinson's disease, retinal and cochlear implants and multiple sclerosis [93, 81]. Recently, neural stimulation has been investigated also for sending sensory information back to the central neural system through the peripheral nerves [171, 35, 186]. Hand loss is a highly disabling event that markedly affects the quality of life. To achieve a close to natural replacement for the lost hand, the user should be provided with the rich sensations that we naturally perceive when grasping or manipulating an object. Ideal bidirectional hand prostheses should involve both a reliable decoding of the user's intentions and the delivery of nearly "natural" sensory feedback through remnant afferent pathways, simultaneously and in real time. Moreover, it is an essential instrument for neuroscientists to study the function of the nervous system by supervising the effects of stimulating neural tissue. The stimulation system must be capable of generating a wide range of electrical signals for nerve stimulation via implantable nerve electrodes. In addition, since this is a strongly patient dependent application, a reconfigurable and adaptable system is required. As a consequence, the generated neural signals must be programmable in terms of wave form, amplitude and frequency. However, generating the proper signals is not the only issue in designing a neural stimulator. The designer must also consider many other aspects that, for example, refer to the patient safety in normal-operation mode and in case of system failure.

From an electrochemical point of view when the stimulation signal is provided, a charge transfer between the electrons in the metal electrode and the ions in the biological tissue occurs. As discussed in the Section 1.3.1, the ionic flow can be induced by three primary mechanisms, the capacitive and the reversible and non-reversible Faradaic reactions. In the former no electrons transfer occurs, just a redistribution of charged chemical species in the

tissue. Whereas with the Faradaic reactions, an exchange of electrons across the electrode-tissue interface is involved, resulting in reduction or oxidation of some chemical species. In particular, the irreversible reactions are quite dangerous for the organism because they produce new chemical species that diffuse inside the body altering its normal chemical composition, for example inducing a pH shift. Then, to prevent this toxic reaction and tissue or electrode damages, in a neural stimulation system only reversible Faradaic processes are allowed for charge injection. Regarding safety during electrical stimulation, several analysis and models have been presented in literature. Some studies focus on electrode material and geometric area [151, 111], using as selection criteria the reversible charge injection limit of the material. Such quantity depends on the reversible processes that are available over the duration of the stimulus, as well as the stimulus waveform shape and frequency [152, 44]. Considering the methods of controlling charge injection, two categories are available: current-controlled and voltage-controlled. Several works consider the current controlled method the most effective because the effects of such stimulation take place near the electrode and can be directly calculated and easily understood [111, 41]. Current pulses allow to eliminate variations in the stimulation threshold even with changes in the electrode-tissue impedance and are commonly used for functional electrical stimulation of excitable tissue. However many researchers prefer voltage stimulation in terms of electrode safety. In fact, current pulses can cause high electrode voltages with a following electrochemical damage of the electrode [192]. Choice of stimulus parameters is then very important in the design of neural stimulation circuitry and depends on the type of stimuli to generate [65]. Charge-injection for neural stimulation is usually applied in the form of rectangular pulses but in the recent years different waveform types have been explored. The results obtained in [154] and [33], suggest that Gaussian waveforms, compared to rectangular stimulus, reduce the non-uniformity of the current density distributions on the electrode surface while maintaining stimulation efficacy and requiring the smallest electrode surface area.
The last but not the least problem to deal with in neural stimulator designing is the high impedance of the electrode-tissue interface. Its simplest model with discrete components is presented in Section 1.3.1, in which Fig. 1.12 and Fig. 1.13 respectively depicts the interface behaviour inside and outside the water window. The impedance of commercially available electrodes ranges from $10k\Omega$ to $1M\Omega$ [211, 213, 39, 23]. As a consequence, in order to inject enough level of charge into the nerve, the stimulation voltage needs to be increased with respect to the stimulator voltage supply that is typically lower then $3.3V$. For this reason, many implantable neural stimulators available in literature ([208, 78, 122]) embed a high voltage booster that properly increases the stimulation voltage before delivering the current pulse. Moreover, by analysing the different components of the electrode/tissue interface model, it results that the impedance's value strongly depends on, at least, three main factors, the electrode design (active sites geometry and selected materials), the in-body environment and the electrode positioning inside the tissue. Whereas the electrode parameters can be tuned to improve the signal injection on the base of the specific application, the last two factors are less controllable and patient dependent. In particular nothing can be done about the chemical composition of the organism and it is not easy to control how well the electrode had been implanted. In addition, the impedance tends to increase over the time due to the unavoidable body reactions to the implanted device and due to the irreversible Faradic processes that may occur at the electrode/tissue interface degrading the quality of the signal transfer [53]. In order to cope with this high variability of the impedance, programmable stimulator capable to adapt to the patient and to be tuned over the implant lifetime are often designed.

1.4.3 Packaging issues

The design of medical devices for human implantation always puts strict requirements on the system specifications limiting the range of materials that can be used. In particular, there are two main factors that influence an implantable system design: the biocompatility and the biostability. The former is the ability of a material to perform with an appropriate host response in a specific environment [2, 18], whereas the latter refers to the ability of a material to maintain its physical and chemical integrity after implantation in living tissue. A further distinction between structural and surface biocompatibility is also done. The structural biocompatibility is the adaptation of an implanted structure to the mechanical properties of the host tissue. This refers to the shape as well as to the inner structure of the implant that should mimic the tissue structure. The surface biocompatibility is a similar properties but refers to the chemical, physical, biological and morphological surface properties of an implant that should clinically promote itself interaction with the host tissue. The EU legislation refers to the ISO 10993 standard for the biological evaluation of medical devices. In particular, the standard details the procedures that should be applied to verify the device biocompatibility distinguishing between in vitro and in vivo tests. In vitro tests are performed with cells or biological molecules outside their normal biological environment. These tests are particularly useful to investigate the toxicity and compatibility of materials because there are not all those defensive mechanisms the normally act in a living organism. It is also possible to prove the effectiveness of production and sterilisation procedures. In vitro tests are followed by in vivo experiments that are usually performed first in animals and later in humans. In vivo tests are surely the most complete tests to really prove the device compatibility with the body. In particular, they allow to evaluate the real biological, chemical and mechanical interactions with the tissue and the long-term effects.
On one side placing electronics into a package protects the implant from water and vapour contained in the body and on the other side it protects the tissue from electrical currents. Galvanic corrosion of two dissimilar metal parts joined together, dissolution of inorganic passivation layers of semiconductors, evolution of gas by electrolysis, corrosion of thin-film metal tracks of semiconductors, high resistance shorting path for current in high-impedance circuits, electromigration of two adjacent metal tracks and swelling-induced mechanical stress of polymeric components are only some of the most common potential effects of liquid water on implanted electronics ([129, 4, 82, 32]). Moreover, in case the electronic circuits get in contact with saline solution, additional failure modes might occur such as low-resistance shorting of tracks by conductive saline or poisoning of semiconductor devices by sodium ions, resulting in greatly increased leakage in back-biased p-n junctions. For these reasons, an additional package property is always investigated: the hermeticity. It is defined over vapour leakage rate, based on gas permeability, specific to the material properties and its thickness. In addition, the maximum leakage rate for considering a package "hermetic" depends on the package volume. A possible way to evaluate the package hermeticity is described in [164], in which the maximum allowable level of vapour inside the package is fixed to $5000ppm$ since the dew point of water according to nomograph from Fig. 1.18 for packages with $1atm$ internal pressure at $0°C$ is reached when $6000ppm\ H_2O$ are present. By fixing the limit to $5000ppm$, the dew point is below freezing point ($0°C$) and any condensing water would build ice crystals instead of droplets, avoiding the risk of water-induced corrosion. Moreover, since the implants operate at $37°C$, not $0°C$, a higher moisture content is allowed and the limit of $5000ppm$ sets a large enough safety margin.

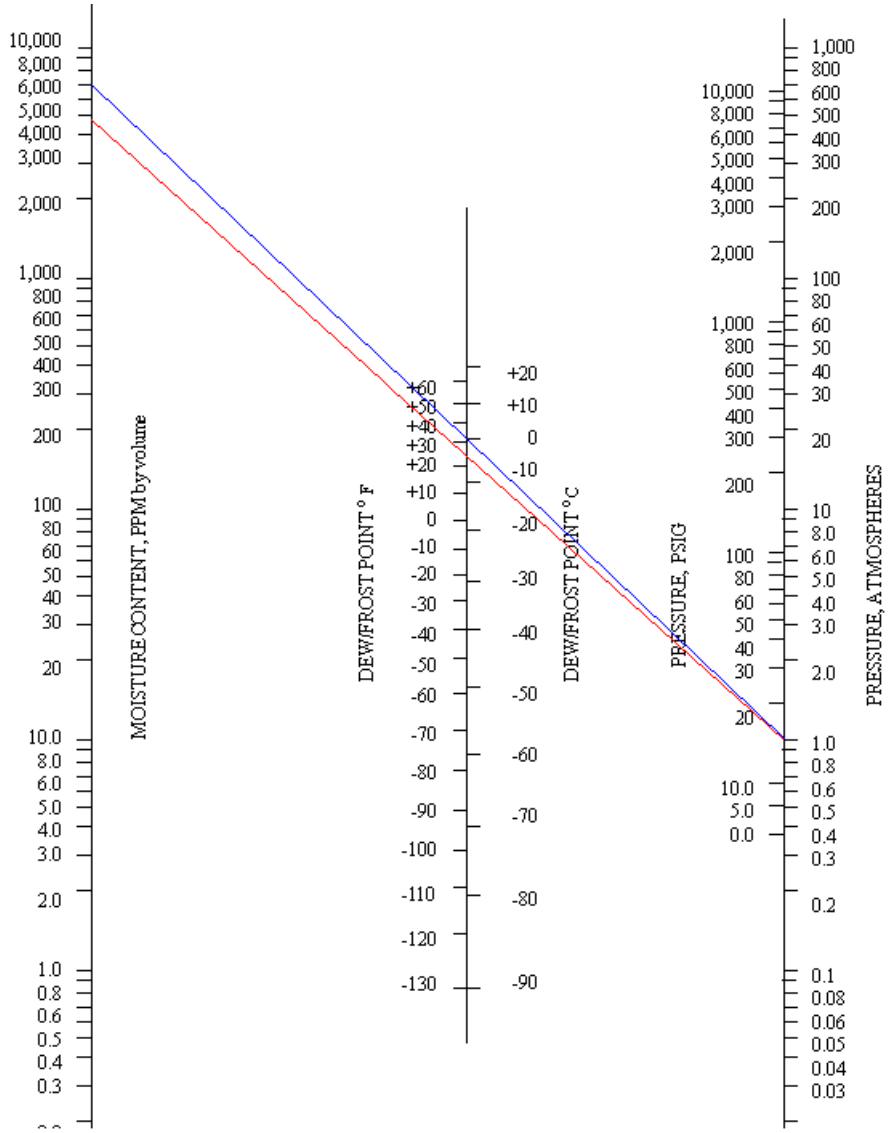


Figure 1.18: Nomograph for dew point and moisture content (PPMV) as a function of Pressure.

Other processes such as protein deposition, calcification and immune system reactions can cause the device encapsulation inhibiting or limiting its required interaction with the organism. The cooperation of all these mechanisms reduces the implant life-time and increases, consequently, the number of required surgeries for replacing the device. Moreover, depending on the importance of the restored body functionality, a system failure can also be fatal for the patient. Anyway, despite the in-body environment hostility, the implant can benefit of the constant temperature of the body ($37°C$) and of the relative stable pH of most of the tissues. In order to assure enough levels of biostability, biocompatibility and hermeticity, the materials selection is one of the key points in implantable package designing and since a huge range of materials is available, it is not an easy task. A typical package for housing an implantable medical device is generally composed by different parts such as the housing for the electronic and/or mechanical components, the cables for routing the electrical signals inside the body, the electrodes for connecting the electronic interface to the tissue and the

feedthroughs, i.e., the package opening to the outer environment. All listed elements, must be carefully designed, to avoid the failure of the whole implant and, depending on the part we are considering and on the specific application, only certain materials can be selected. Some of the most commonly used materials are collected in Table 1.2, they are metals, ceramics, polymers and glasses. Gold [112], stainless steel and its alloys [4], platinum and its alloys [162, 120], tungsten [139] and titanium [112] are stable metals adopted in AIMDs as electrical conductors and, seen they act as barrier against moisture, they are suitable for making the hermetic housing too. However, preventing any kind of wireless communication between the inner and the outer of the package, metal enclosures are not always the optimal solution. In this case, other materials transparent to electromagnetic fields should be adopted, for example, polymers, ceramics and glasses [68]. The last two, like the metals, are often used for making the electronic housing but, being quite brittle, they cannot be used in those applications where the package undergoes high continuous mechanical stress [104]. Metals, ceramics and glasses are used where high hermeticity levels are required, but, being quite hard, they often do not satisfy the structural biocompatibility requirements and, therefore, an additional encapsulation of polymer-based material is used. In fact, polymers have been chosen as housing but also as substrate and insulation material, because, being flexible, better match the Young's modulus of soft tissue. Quite diffuse implantable polymers are silicon rubber (Polydimethysiloxane-PDMS) [163], polyimide (PI) [84] and parylene C [72]. Moreover, they are quite diffuse in the fabrication of non-hermetic packages [80, 20] since polymers perfect surface adhesion does not allow space between the covering layer and the electronic circuits for vapour condensation, preventing all degenerative effects due to liquid water. Non-hermetic package are usually smaller, cheaper and require easier production steps with respect to the hermetic ones. To summarize, each material has its pros and cons and due to the huge variety of requirements to be satisfied, it is not easy to find a single material that perfectly fits the purpose. Many works in literature ([163, 112, 131, 85]) show that the only way to overcome the biostability, biocompatibility and hermeticity issues, is to proper combine different materials in order to exploit their advantages.

	Commonly used materials	Applications	Requirements	Degradation mechanisms
Metals	**P**latinum & Platinum/Iridium (Pt/Ir) **G**old **T**itanium **T**ungsten **S**tainless steel **M**P35N [87] **E**lgiloy	**Electrical conductors:** wires, feedthroughs, connectors, electrode contacts **Moisture barriers:** hermetic packages for electronics	**M**echanical robustness, **C**orrosion resistance, **B**iocompatibility, **G**ood conductivity	**G**alvanic corrosion, **C**revice corrosion, **P**itting corrosion, **C**orrosion fatigue, **F**retting corrosion, **E**lectrically driven corrosion
Polymers	**P**nynox **P**olydimethysiloxane (PDMS) **P**olycarbonate (PC) **P**olyimide (PI) **P**oly(p-xylylene) (Parylene) **P**olyethylenterer-phthalat(PET)	**Electrical insulators:** wires, feedthroughs, connectors, electrode contacts **Mechanical parts:** tines, mechanical mediators to tissues	**M**echanical robustness, **D**egradation resistance, **B**iocompatibility, **H**igh electrical resistance, **H**igh breakdown voltage	**U**nspecific hydrolyses, **O**xidative degeneration, **S**welling, **L**eaching, **P**lasticising effects, **E**nzymatic attack, **M**icrobiological attack, **L**ipid adsorption
Ceramics	**A**lumina (Al_2O_3) **Z**irconia (ZrO_2) **G**lass-Ceramics	**Electrical insulators:** feedthroughs **Mechanical parts:** implant housing	**M**echanical robustness, **D**egradation resistance, **B**iocompatibility, **H**igh electrical resistance, **H**igh breakdown voltage	**B**rittleness: risk of breakage, **F**atigue under load, **D**egradation in moist environments
Ceramics	**S**oda lime glass **B**orosilicate glass	**Electrical insulators:** feedthroughs **Mechanical parts:** implant housing	**M**echanical robustness, **D**egradation resistance, **B**iocompatibility, **H**igh electrical resistance, **H**igh breakdown voltage	**H**ydrolytic dissolution, **F**atigue under load

Table 1.2: Commonly used materials for implantable packages [178].

Chapter 2

Neural signal recording unit: design and test

In this chapter, after a brief overview on the state-of-the-art neural interfaces, the design of a custom IC for acquiring the neural signals from the PNS is described. Starting with the definition of the design specifications, the description focuses on the details of the system implementation. The device has been developed on two different levels: a high level behavioural model for a rapid evaluation of the specification meeting and a transistor model for a slower but more accurate analysis. Finally, the chip characterization tests, including electrical measurements and in-vivo experiments, are presented.

2.1 State of the art

Neural signals can be considered both in terms of voltages and currents. In fact, as explained in Section 1.2.2, voltage spikes are generated by means of ion channel currents. According to what reported in literature, in this thesis the main focus is on the neural voltage recording. Nevertheless an analysis and a high level implementation of a front-end circuit for ion channel current detection is also presented. For these reasons in this section the state of art related to both type of measures is presented, the voltage signal acquisition and the ion current readout circuits.

2.1.1 Neural voltage recording circuits

In last decades great advancements have been reached in biomedicine, in particular as described in Section 1.3 the introduction of intraneural electrodes has made it possible to work with stronger signals. Nevertheless, amplitudes remain in the order of magnitude of tens of microvolts, therefore the noise is still the major concern. A low noise front-end stage is then mandatory to prevent the signal destruction. Many researchers are currently working on low noise neural interfaces, aimed to different applications. This kind of devices indeed can be very useful for many purposes: to find a solution against neural-degenerative diseases like Parkinson and Alzheimer for instance, as well as for injured patients with permanent damages to the spinal cord and, as in the work presented in this thesis, to restore lost func-

tionalities in amputees thanks to neuroprosthesis. According to the pursued goal, different specifications drive the neural interface design. In the systems that record signals directly from the CNS, for example, also neural signals different from action potentials can be useful (*Local Field Potential (LFP)* for instance). Their amplitudes are in the order of magnitude of mV and their frequency overlaps with EMG interferences [83, 91, 183, 169]. However, the recording from CNS is still possible because EMG signals are not of a such importance, due to the fact that there are no muscles moving into the brain. For this kind of applications the bandwidth includes also very low frequencies (in the $mHz - 100Hz$ range) [168, 146, 100]. On the contrary, with respect to the acquisition of neural signals from the PNS, the EMG interference is a huge contribute to the overall background noise as explained in Section 1.4.1. Therefore, the neural signal weakness together with the strong interferences drive the designers to develop solutions capable to filter and amplify the signal as close as possible to the electrode, the miniaturization and optimization of electronics for neural activity registration seems to be then, the new challenge. Attempts to solve this issue are based on two different approaches: the use COTS electronics or the realization of a custom IC. The first approach is utterly useful for a preliminary analysis because it is a low-cost solution and has a rapid implementation time so it is suitable for short-term experiments, especially on animals [62, 105]. Moreover, since neural signal characteristics in terms of bandwidth and amplitudes are patient and electrode dependent, the possibility to easily modify the electronic configuration represents a great advantage in the first stages of research. The IC approach, on the contrary, allows the realization of low noise and compact devices, combining low power consumption and small sizes [71, 199] and is, therefore, more suitable for long-term implantation. Nevertheless, design time and prototyping costs are large and the custom device usually lacks flexibility and adaptability. To summarize, the typical approach is to start with a COTS device and, only once that the terms of the problem are better known, a custom integrated circuit can be developed on a solid ground.
Several works aimed at the realization of neural interfaces based on both, discrete and integrated circuit, approaches have been presented. For what concerns the integrated circuit approach, the majority refers to the processing of cortical neural signals [112, 106, 67, 218, 54, 199] including, sometimes, both recording and stimulation functionalities such as those presented in [146, 8, 189]. However, some integrated circuits for PNS have also been developed [148, 46, 165, 194, 92, 94, 150], but in most cases they do not include the Analog to Digital Converter (ADC) and are focused on cuff electrodes. The IC circuits have the great advantage on their discrete system counterpart, to allow the designer to have the complete control on all the system parameters, by this way it is possible to find a better fitting between the specifications and the prototype. The drawback is obviously a major project complexity due to the enormous degree of freedom that must be handled by the designer. In the following a survey on literature regarding the amplifier, the filter and the ADCs used in neural signal recording interfaces is presented.

Amplifiers

One of the key points concerning the recording module is to realize a low noise amplifier. Different choices have been made in this direction but the most pursued one has been to use a Symmetrical OTA topology of Fig. 2.1. Thanks to its simple circuitry, in fact, it guarantees the minimum IRN comparing with other topologies as Folded Cascade [199] and Miller OTA. Many papers present such solution for neural implementation in its single ended [204, 70,

15, 75] or fully differential versions [218, 92, 67].

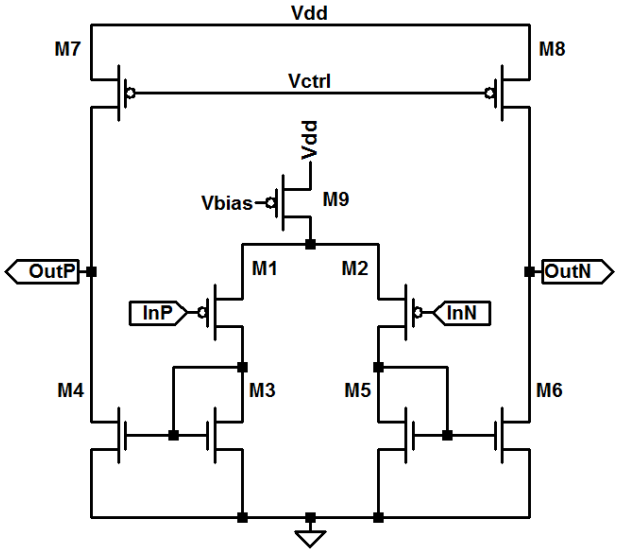


Figure 2.1: Simmetrical OTA in Fully differential configuration.

Using Symmetrical OTA architecture, thermal noise is given by Eq. 2.1.

$$\overline{V_{n,th}{}^2} = \left[\frac{16kT}{3g_{m1}} \cdot \left(1 + 2\frac{g_{m5}}{g_{m1}} + \frac{g_{m8}}{g_{m1}}\right)\right] \tag{2.1}$$

Where g_{m1} is the transconductance of the input differential pair, while g_{m5} and g_{m8} are the transconductances of the transistors in the output branch. In order to reduce noise, a designer must have special care in MOS sizing. Eq. 2.1 shows that thermal noise minimization requires $g_{m1} \gg g_{m5}, g_{m8}$. Since the g_m expression for a MOS in saturation region is given by Eq. 2.2, a low noise amplifier can be achieved by using large and short differential pair and narrow and long mirror transistors.

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}} \tag{2.2}$$

The consequence in choosing large transistor for input differential pair is that the device enters in weak inversion region. In such region g_m is maximized and becomes independent from MOS size, depending only upon drain current. Thus, once that the differential pair MOS is in weak inversion, the only way to further increase the transconductance is to increase the current with a consequent increase of power. Taking everything into account, the majority of papers choose to maximize g_{m1} by using a large input differential pair in weak inversion without increasing current, and to minimize g_{m5} and g_{m8} by putting $M5$ and $M8$ in strong inversion [115, 73, 98, 36]. This approach is not used only in Symmetrical OTA configuration but also in Folded Cascade [188, 198] and Miller OTA [194]. Such choice has advantages in terms of flicker noise reduction. As already shown in Eq. 1.1, this noise is in fact reduced when MOS dimensions are increased. Almost all researchers prefer a PMOS differential pair to NMOS for its lower sensitivity to flicker noise. Nevertheless, analysis carried out in [22] shows as such assumption is true only comparing NMOS and PMOS with the same g_m. The noise reduction, in this case, derives from a larger implementation area of

PMOS transistors. Considering the same biasing and area it is demonstrated that a NMOS amplifier presents higher g_m than a PMOS one and then a better figure noise. Another approach that has positive effects on noise is the use of a fully differential topology. Having two branches, in which the signal is mirrored and propagated, is an advantage in terms of common mode noise. Such noise spreads in the same way along the two differential paths of the circuit and is cancelled taking the difference of the two output voltages. These benefits are paid with a large occupation area due to the duplication of feedback networks of the filters and to the introduction of common-mode feedback (CMFB) blocks. For these reasons many papers adopt this strategy [218, 92, 67, 188]. Even if symmetrical OTA is the most widely used configuration, other topologies have been exploited. The modified folded cascade proposed in [198] allows to obtain a NEF of 2.67 which is one of the lower values reported today. This result is achieved reducing power by means of current reduction in folded branches (1/16 with respect to input branches) that may imply worse noise performance. This drawback is avoided using degenerating resistors in series with $M5$ and $M6$. An appropriate choice of these resistances may significantly reduce the contributions to total noise. First because thermal noise in resistors can be significantly lower than in MOS and second because the resistance gives no contributes to flicker noise. A folded cascade topology has been used by [141] that, taking advantage by the current-splitting technique, reaches a NEF of 3.09 with an $IRN = 3.07 \mu V rms$. Among the other topologies exploited in neural amplifiers, Wang et al., in [194], propose a preamplifier stage based on Miller OTA configuration. The circuit gives a gain of 20 dB and it is followed by an instrumentation amplifier that brings the gain to 80 dB. Sacristan and Oses [153] present instead a multi-stage architecture. In the design of the first stage, represented by a simple preamplifier, authors have paid particular attention in noise reduction and CMRR, using large area transistors and high biases current. The second stage takes advantage by a DDA (Difference Differential Amplifiers), composed by two pairs of differential inputs. Inputs are applied to the first pair while in the second two, feedback loops are implemented. One feedback loop imposes the gain, while the other introduces zero and poles for filter implementation. The third stage consists of a simple RC high-pass filter followed by a fixed gain amplifier, needed to adjust the gain to the level required by the ADC. This circuit solution allows to achieve particularly low noise levels ($0.35 \mu V$ in the bandwidth of $100 Hz - 5 kHz$), at the cost of a high power consumption ($2 mW$). In [92], a different solution employing an instrumentation amplifier has been proposed. In order to reduce the noise, a fully differential approach is used and the input stage is constituted by a PMOS differential pair with large area. Despite that, the noise at $1 kHz$ is about $0.73 \mu V / \sqrt{Hz}$. Integrated in the neural useful band ($250 Hz - 5 kHz$) an IRN value of $50 \mu V$ is obtained, still too high if compared with the weak amplitude of neural signals.

Filters

Several approaches in neural filter design have been implemented. The major degree of freedom in filter design is the choice of the filter type. In integrated systems, filter strategies can be classified in Continuous Time Filters (R-C or MOSFET-C and Gm-C) and Discrete Time Filters (Switched Capacitor) [6, 1]. The most used are MOSFET-C filters for their ability to reach very low cut-off frequencies useful for LFP recording [70, 198] as well as for Fast Ripples (FR) detection in epileptic patients [141]. Since the cut-off frequency is given by the inverse of the product of the MOSFET equivalent resistance and the capacitance, a very low value can be obtained using a high capacitor or a high resistance. But as both solutions

imply large area implementation, a widely used approach is to employ a MOSFET biased in triode region that emulates a resistive behaviour. By this way, the relationship between drain current and the drain-source voltage is linear, as expected from a resistor. This particular application requires large values of resistance (to achieve a mHz cut-off frequency with a capacitor in the pF range, it is necessary an equivalent resistance in the order of hundreds of $G\Omega$). For this reason, bipolar transistors compatible with CMOS process are used [24]. This technique allows achieving resistances of several hundreds of $G\Omega$. The discrete time approach is rarely used but it presents several advantages with respect to continuous time filters. In this case, cut-off frequency is set by the ratio of two capacitors. The ratio of parameters of the same kind of device is more precise than the ratio of a transconductance and a capacitor (Gm-C filters) since it is affected by statistical fluctuations of the same manufacturing process. Moreover, Switched Capacitor filters allow an effective use of silicon area, making possible to realize low cut-off frequencies with small areas. A great advantage is also given by the flexibility due to the dependence of the filter parameters on the clock frequency. In [92] a six order bandpass filter is proposed. The architecture consists in three fully differential biquad stages, in which the filter signal flow is based on ladder-type implementation. Gusmeroli et al., in [64] use a first order switched capacitor high-pass cell, changing the high-pass cut-off frequency in order to reduce the recovery time during stimulation. Trough switching capacitor technique, it is sufficient to increase the clock frequency to achieve a time recovery reduction. In the solution proposed in [203] the switching capacitor stages are preceded by a continuous time filter in order to avoid aliasing and to prevent input corruption due to switching noise. Regarding the heavy incidence of flicker noise in neural signal acquisition, some researchers [115, 157] have overcome this problem introducing a chopper stabilization technique. The working principle is to modulate input signal in order to translate it into high frequency where the flicker noise effect becomes irrelevant. The modulated signal is bandpass filtered and then demodulated in the baseband. Uranga et al. in [188] propose a signal chain composed by a modulator followed by a pre-amplifier stage and by a bandpass filter centred at chopping frequency. The pass-band removes the undesirable spikes introduced in chopping process due to non-idealities of switches. A post amplifier stage has been introduced after the bandpass, then a demodulator folds the signal into base band and finally a low-pass filter isolates the neural signal from noise. Both bandpass and low-pass continuous time filters have been designed using the Gm-C technique. The advantage of this approach is that the noise can be reduced simply increasing the chopper frequency. On the other hand, this implies an increase of the amplifier cut-off frequency that must be higher than the clock frequency, in order to avoid any harmonic distortion of the modulated signal. Gosselin et al. [61] present a multi-channel structure composed by a front-end stage and a mixed-signal compression module that uses an analog wavelet transform process followed by an ADC. The front-end stage is present for each acquisition channel while the wavelet signal processing block is shared among all channels. The frontend stage is based on Chopper Stabilization technique. After modulation, the signal is amplified with a rail-to-rail CMOS amplifier and filtered with a second order Gm-C stage. The signal is then demodulated into the baseband while the equivalent noise is added to the amplifier input after that the modulation process has occurred. Thus, noise is subject only to one modulation process (the same used for signal demodulation) that translates the noise out of the band of interest. Another technique, called auto-zeroing, has been exploited in order to reduce low-frequency noise and offset at the amplifier input. Between Chopper Stabilization and auto-zeroing there is a clear distinction: while the first is a modulation technique, the

latter is a sampling technique. The basic idea of auto-zeroing is to sample the offset voltage value and the noise and to hold them in a capacitor. Once that these values have been stored, the input is put into the amplifier and the unwanted quantities can be subtracted from the instantaneous input. With the offset voltage this process works well since offset is constant, the problem is a bit more complex considering time-varying and random flicker noise. The efficiency of auto-zeroing strongly depends on the correlation between the noise sampled and held in the capacitor and the instantaneous noise value from which such sample is subtracted. It can be stated that this process reduces also the flicker noise because the autocorrelation between two consecutive samples of flicker noise decreases slowly enough to allow the cancellation when the subtraction occurs. The main drawback of this approach is the aliasing. Since this is a sampling technique, the aliasing noise is folded into the base band [158]. Chan et al. [36] propose a neural amplifier based on auto-zeroing technique: the design consists of three stages. The first one is a variable gain amplifier composed by two differential pair, one for input recording and the other for offset-noise adjustment. The second stage is a low Gm-C high-pass filter and the third is a low-pass Gm-C amplifier. From the point of view of power consumption, auto-zeroing seems to give better performances than chopper. The modulation implies a wider amplifier bandwidth and to this aim, it is necessary to increase current and then power consumption. A summary on the main features of the neural recording system presented in literature has been reported in Tables **??** and **??**. It should be clear that each system has his own characteristics, thus a mere comparison of the parameters can be unfair. For this reason in the last column the number of channel to which the parameters are referred has been reported.

Analog-to-digital conversion and spike sorting

Once the signal has been properly amplified and filtered, the last operation is digitalization. At this regard, two main approaches have been proposed. The first consists in a traditional digital conversion, where the neural signal morphology is held and transmitted to external for processing and classification. The second approach consists in spike detection; in this case the signal morphology is lost and the only information kept is about spike occurrences. The A/D conversion is exploited in several works. In [204, 92, 153], an 8 bit successive-approximation register (SAR) ADC has been used. This solution involves low power consumption and small layout area. Watkins et al. in [197] make use of a $10bit$ SAR ADC but, since the signal is acquired from 100 different channels, it would be too onerous to convert all signals. The proposed solution converts only one channel, while for the others there is a spike detection block that recognizes if a spike has occurred or not. In this way there is a considerable reduction in bandwidth requirement for the external communication link. Horiuchi et al. [75] use the spike detection approach, but their circuit is more elaborate than a simple comparator and it is able to discern between peaks and troughs of spikes and gives also information about spikes amplitude. Another approach proposed is based on oversampling converters. Due to the low frequencies of the neural signals in fact, large OverSampling Ratio (OSR) can be achieved, without using high sampling frequencies. In [215] a first order delta sigma converter has been designed, reaching a 8 bit resolution with a 40 oversampling ratio over a $6.25kHz$ frequency. A second order delta sigma modulator that exploits a new superinverter amplifier has been proposed in [60] and allows to reach a $11bit$ resolution considering a $8kHz$ bandwidth.

Ref.	Tech.	Band [Hz]	Gain [dB]	V_{DD} [V]	Area	Power	IRN	NEF	Ch.
[204]	CMOS 0.5μ	$5-7.2k$	36	3	$2.25mm^2$	$99\mu W$	$9\mu V$	*n.a.*	64
[70]	CMOS 1.5μ	$25m-7.2k$	39.5	± 2.5	$0.16mm^2$	$80\mu W$	$2.2\mu V$	4	6
[198]	CMOS 0.5μ	$45-5.32k$	40.8	2.8	$0.16mm^2$	$7.56\mu W$	$3.06\mu V$	2.67	1
[91]	CMOS 0.18μ	$16-5.3k$	40	1.8	$2.7mm^2$	$89\mu W$	$18.9\mu V$	*n.a.*	8
[218]	CMOS 0.18μ	$0.38-5.1k$	$55-61$	1	$28.2mm^2$	$1.16mW$	$4.0\mu V$	1.9	100
[146]	CMOS 0.18μ	$0.64-6k$	54	1.5	$4mm^2$	$0.47mW$	$6.3\mu V$	3.76	4
[148]	CMOS 0.8μ	$310-3.3k$	80	± 2.5	$12mm^2$	$24mW$	$291nV$	*n.a.*	10
[71]	BiCMOS 0.6μ	*n.a.* $-5k$	60	3.3	$25.38mm^2$	$8mW$	$4.8\mu V$	*n.a.*	100
[112]	CMOS 0.35μ	$0.5-300$	<62	3.3	$178mm^2$	$75mW$	$1\mu V$	*n.a.*	64
[67]	CMOS 0.18μ	$0.25-10k$	$52-56$	0.45	$25mm^2$	$94\mu W$	$3.2\mu V-3.8\mu V$	1.76	100
[106]	CMOS 0.18μ	$0.5-6k$	$29-72$	1.8	$9.88mm^2$	$1.45mW$	$3.2\mu V$	3.08	52
[54]	CMOS 0.13μ	$<1-10k$	56	1.2	$25mm^2$	$6.5mW$	$2.2\mu V$	4.5	96
[92]	CMOS 0.35μ	$250-5k$	80	$3-4$	$4mm^2$	$2.25mW$	$0.73\mu V/\sqrt{Hz}$	*n.a.*	1
[94]	CMOS 1.5μ	$300-6k$	$40-60$	± 1.5	$41.84mm^2$	$1mW$	$1.95\mu V$	*n.a.*	1
[15]	CMOS 0.35μ	$10-10k$	$46-74$	3.3	$13.5mm^2$	$6mW$	$13\mu V$	*n.a.*	256

Table 2.1: Main characteristics of neural recording system presented in literature

Ref.	**Tech.**	**Band [Hz]**	**Gain [dB]**	V_{DD} **[V]**	**Area**	**Power**	**IRN**	**NEF**	**Ch.**
[75]	CMOS 1.5μ	$22-1.7k$	42.5	1.5	$81\mu m^2$	$0.8\mu W$	$20.6\mu V$	*n.a.*	1
[115]	CMOS 1.5μ	$100-5k$	38	5	$1mm^2$	$28mW$	$1.13nV/\sqrt{Hz}$	*n.a.*	1
[98]	CMOS 0.5μ	$73-2.18k$	70	± 2.5	$0.33mm^2$	$180\mu W$	$2.76\mu V$	*n.a.*	1
[36]	CMOS 0.18μ	$200-2k$	55	1.8	$0.245mm^2$	$26\mu W$	$4.24\mu V$	14	1
[188]	CMOS 0.7μ	$n.a.-3k$	74	5	$2.7mm^2$	$1.3mW$	$0.453\mu V$	5.3	1
[61]	CMOS 0.18μ	$100-6k$	80	1.8	$0.064mm^2$	$20\mu W$	$30nV/\sqrt{Hz}$	*n.a.*	100
[141]	CMOS 0.6μ	$250-486$	38.5	2.8	$0.45mm^2$	$4.5\mu W$	$2.46\mu V$	7.6	1
[153]	CMOS 0.7μ	$106-5.1k$ $119-5.1k$ $201-5.1k$ $352-5.1k$	$76-102$	± 2.5	$1.13mm^2$	$4mW$	$0.35\mu V$	3.6	1
[24]	CMOS 0.35μ	$2-20k$	64	± 1.65	$8.96mm^2$	$33mW$	$2.9\mu V$	*n.a.*	64
[64]	CMOS 0.35μ	$100-10k$	20	± 1.65	$5mm^2$	*n.a.*	$10\mu V$	*n.a.*	1
[203]	CMOS 0.5μ	$530-5.3k$	$61-73$	± 2.5	$15.96mm^2$	*n.a.*	$27.7nV/\sqrt{Hz}$	*n.a.*	17
[197]	CMOS 0.5μ	$1.1k-5k$	60.1	3.3	$27.3mm^2$	$13.5mW$	$5.1\mu V$	*n.a.*	100

Table 2.2: Main characteristics of neural recording system presented in literature

2.1.2 Patch clamp circuits for Ion channel current detection

As explained in Sec. 1.2.2, the generation of electrical signals in biological cells is possible thanks to ions that move across the cell membrane. In many applications it is important to record these currents in order to understand which electro-chemical processes are involved in the signal generation and to have a direct measurement of the ion channels involved in the reaction. Ion currents, in fact, play a key role in several physiological processes, in neural signal generation, as already discussed, but also in the maintenance of heartbeat and in muscle contraction [216]. The signal is recorded by means of a pipette, depending on the way the pipette is attached to the membrane. It is possible to record the electrical activity of the whole cell or of a small patch of channels (even a single channel current can be measured) [216, 66, 170]. The recording of a small cluster of channels is possible because the contact between the pipette and the membrane cell forms a Gigaohm seal [216, 191], allowing to isolate the electrical activity of a small area of the membrane. The patch clamp working principle consists in fixing the external membrane potential to a control voltage and in recording the current that flows across the membrane using proper electronic devices. These devices can be implemented, as in a wide number of paper presented in literature [216, 170, 200], as the cascade of an integrator and a differentiator (Fig. 2.2) or, as also proposed in this thesis, as a current feedback delta sigma modulator (Fig. 2.3) [185, 19, 17, 60, 121, 176]. In Fig. 2.2, it

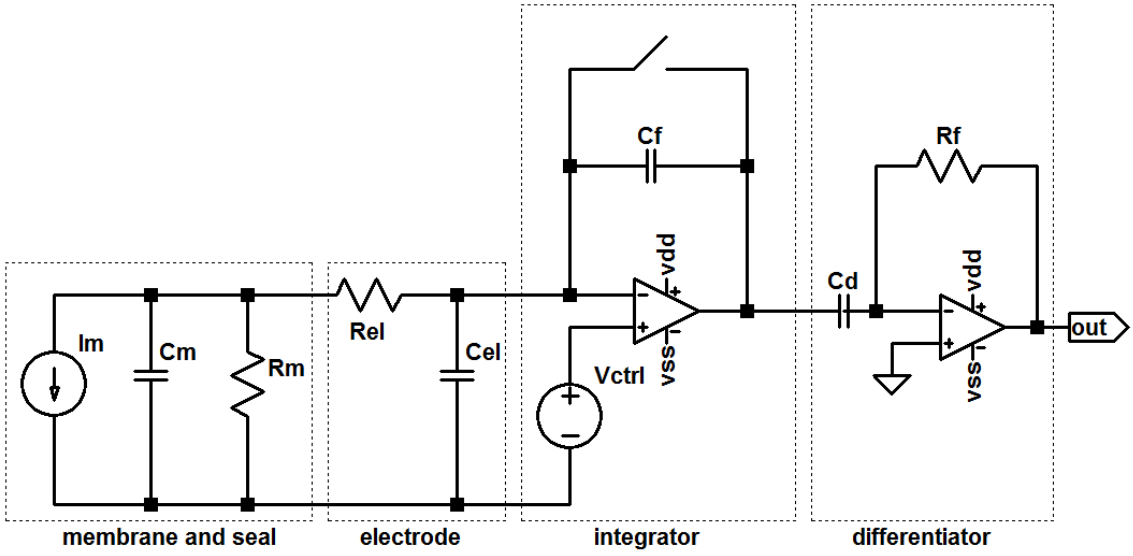


Figure 2.2: Patch Clamp circuit based on integrator-differentiator approach.

is also shown the equivalent electrical circuit for the membrane-seal connection and for the electrode. Typical values for these equivalent components are given in Table 2.3. The circuits traditionally used to detect ion channel currents, are very similar to potentiostats used to record redox current in electrochemical sensing devices [55, 14, 127]. In fact in both cases the aim is to detect a current in a range from hundreds of fA to few μA. The control voltage in the case of ion channel detection is used to set the membrane potential while in potentiostat it sets the redox voltage. The advantages of the delta sigma approach are that the current is directly recorded as a digital pattern without need of differentiator, and the reset switch of Fig. 2.2 can be avoided considering that the current, at the input node, is supplied or sank according to the feedback bit, avoiding the amplifier saturation.

C_m	$300fF$
C_{el}	$500fF$
R_m	$20G\Omega - 40G\Omega$
R_{el}	$10M\Omega - 140M\Omega$

Table 2.3: Equivalent electrical parameters for membrane and electrode

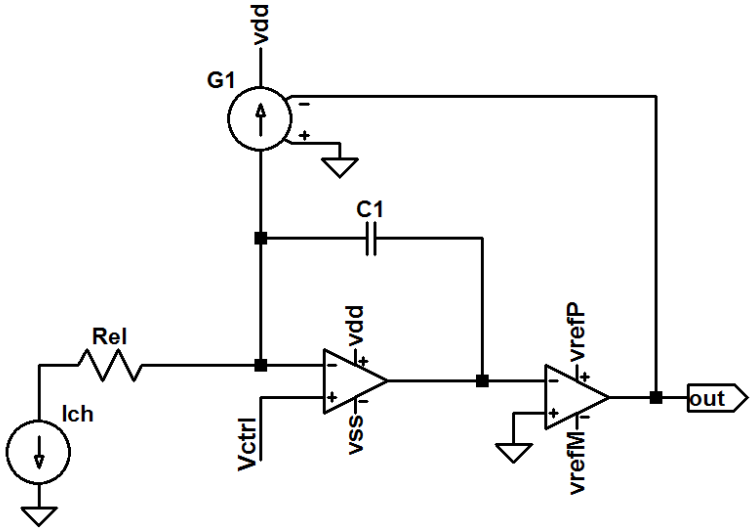


Figure 2.3: Patch Clamp circuit based on a sigma-delta approach.

2.2 Design specifications

As widely discussed in the first chapter, neural spikes are characterized by low amplitudes, that can vary in a range from few microvolts to hundreds of microvolts, and they are drowned in a noisy environment due to EMG interferences. The recording module should then provide a gain and a resolution capable to describe a microvolt level signal and should be able to filter the unwanted components. A first amplification-filtering stage is thus mandatory to amplify the weak signal for a proper ADC conversion and to eliminate the EMG interferences. The definition of the system specifications have been driven on side by the neural signal electrical features (such as frequency and amplitude) and on the other by considering works found in literature. In particular, among the consulted published papers, we considered the work presented in [105] in which a first prototype of the bidirectional neural interface was presented. It is a COTS based solution characterized by a first amplification/filtering stage with a programmable gain from $40dB$ to $54dB$ and passband from $800Hz$ to $3kHz$, followed by an ADC with $16bit$ of resolution. The system had been in-vivo tested highlighting some problems and possible improvements that have been taken into account in this work. In particular, the problems with the filter ringing described in [105], have driven us toward an implementation characterized by a lower selective filter in the analog domain. This fact implies a worse rejection of the EMG noise, the huge interferences will be however completely eliminated after the digital conversion, by filtering the signal in the digital domain. In this implementation we propose, in fact, to keep the analog part as simple as possible and to move all the complexity on the digital domain. It is then necessary to decrease the gain of

the analog filter in order to avoid the amplifier saturation; reasonable values for the gain are in a range from a minimum of $46dB$ to a maximum of $66dB$. The converter resolution requirements have also been changed, a $10bitADC$, with a $V_{ref} = 1V$ is enough to obtain an $LSB = 1.95mV$ which considering the maximum filter gain of $2000V/V$ results in a $977nV$ resolution referred to the input, which is lower than the noise floor of about $2\mu V$. Moreover, the filter bandwidth has been widen in order to investigate whether there is or not neural content even at frequencies higher than $3kHz$. The specifications for recording module of the IC design are summarized in Table 2.4.

Fixed Gain	$46dB$
Variable Gain	$20dB$
HPF order	1^{th}
HPF frequency	800 Hz
LPF order	1^{th}
LPF frequency	$8kHz$
ADC resolution	$10bit$
IRN	$< 2\mu V$

Table 2.4: Recording module specifications

2.3 System architecture

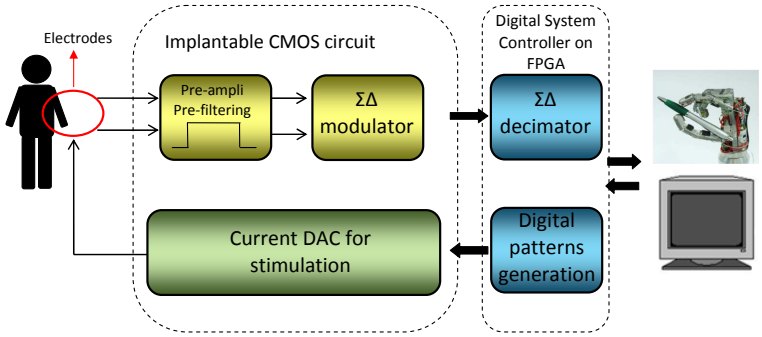


Figure 2.4: Block diagram of the recording system.

The block diagram in Fig. 2.4 shows the system architecture which is composed by two main blocks: the analog front-end and the digital processing unit. The front-end module implements basic signal conditioning on the incoming neural signal and includes also a low voltage module to send current pulses on the feedback path in case of low impedance at the electrode/tissue interface. The signal is, thus, filtered and amplified by the pre-filtering/pre-amplifier block as close as possible to the recording site. In this way, the noise due to long cables and connection paths can be avoided. The conditioned signal is then converted into a $1bit$ digital stream by the delta-sigma modulator and sent to the digital module for decimation and further processing. One of such signal's streams is needed for each input channel if the device is connected to a multichannel electrode. The digital module is hosted on

an external board; it implements the decimation block of the sigma-delta converter altogether with the highly selective bandpass filter. The digital module is also responsible for the generation of digital programmable stimulation waveforms and for the management of the communication between the artificial limb and the electrodes. The digital unit will be implemented on programmable logic (FPGA), hosted on the robotic limb. A further advantage of such approach, is the possibility of changing the selectivity of the filter on the fly by adjusting the digital parameters. Considering the stimulation direction, digitally programmed current pulses will be created by the FPGA and sent to the Current DAC in the analog board to generate current patterns to be injected into the electrode.
The work presented in this chapter is a part of the whole architecture design and concerns only the development of the analog front-end with eight independent channels containing the band pass filter, the delta sigma modulator and the low-voltage stimulator. Moreover an input multiplexer allows to choose which of the sixteen input signals connect to the eight channels. The recording module design has been carried out on two different levels: a behavioural model developed in Simulink and a circuital design in cadence environment. The first model, developed by my colleague, Caterina Carboni, during her PhD thesis work named *"Electronic bidirectional interfaces to the peripheral nervous system for prosthetic applications"*, is needed to provide a first rapid check on the system behaviour and to translate the specification of the whole system in the requirement that each single block must have, while for the physical realization of the device the transistor level simulation is mandatory. All the amplification chain has been designed using a fully differential topology, this approach in fact is the more suitable in a low noise design because helps in reducing the effect of the common mode noise sources in the circuit. Filter and modulator have been designed using a discrete time approach with switched capacitor circuits, this choice allows to reach a better precision in the filter cut off frequency realization compared to the continuous time approach.

2.4 Transistor level circuitry design

The transistor level circuit was designed in a $0.35\mu m$ CMOS process from AMS (Austriamicrosystems) with double-poly capacitors, $3.3V$ power supply and 4 metal layers. Area, power and noise constraints are particularly compelling since the chip must be integrated with the electrode and implanted in the patient stump, our main aim is then to find a good compromise among these requirements.

2.4.1 Bandpass Filter design

Fig. 2.5 shows the pre-amplifier/pre-filtering block that was implemented with a first order switched capacitor (SC) filter. The bandpass filter was realized cascading a high-pass filter with a low-pass filter; the high-pass is used as first stage in order to start rejecting the EMG interferences as close as possible to the electrode, before any amplification.

The filter specifications required a bandwidth between $800Hz$ and $8kHz$ and a minimum gain of $200V/V$. These parameters can be achieved choosing proper values for Capacitances and clock frequency according to the expressions of Table 2.5.

The gain value has been determined in order to maximize the amplification at neural frequencies avoiding the risk of amplifier saturation due to the high amplitude of EMG in-

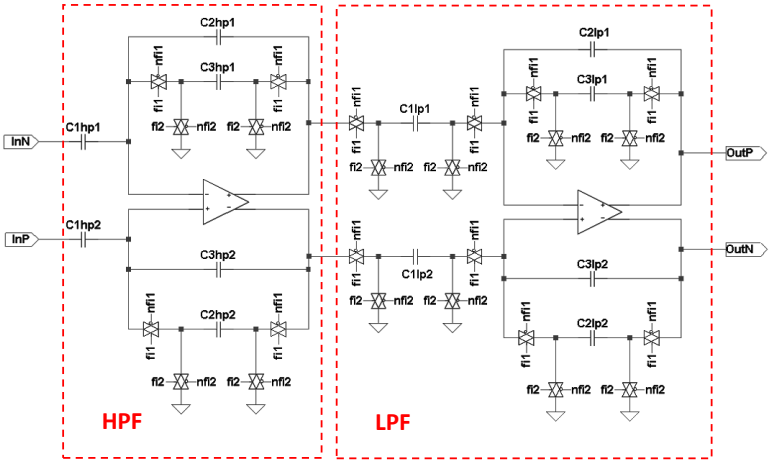


Figure 2.5: Band-Pass filter.

terferences. According to what reported in literature in fact, the EMG amplitude can reach, at $100Hz$ up to $50mV$ [149], since the maximum signal swing allowed is $2V$ (due to sigma delta reference voltage), the maximum acceptable gain at $100Hz$ is $100V/V$, resulting in a $200V/V$ gain in the neural bandwidth.

	HPF	**LPF**
Gain	$\frac{C1}{C3}$	$\frac{C1}{C2}$
cut off freq.	$\frac{f_s C3}{2\pi C2}$	$\frac{f_s C3}{2\pi C2}$

Table 2.5: Equations for filter gain and cut off frequency.

C	**Value [pF]**	**C**	**Value [pF]**
$C_{1hp1,2}$	70	$C_{1lp1,2}$	3.3
$C_{2hp1,2}$	17	$C_{2lp1,2}$	2.7
$C_{3hp1,2}$	0.06	$C_{3lp1,2}$	0.05

Table 2.6: Filter Capacitance values.

In Table 2.6 the capacitance values used in the minimum gain configuration are summarized. Since the reported value for the EMG interference is assessed in worst case conditions, a higher gain can be useful in order to increase further the neural signal level and to achieve a better resolution in normal case conditions. Hence, a programmable gain has been introduced, it is possible to modify the gain with 256 different levels reaching a maximum of $66dB$. For this purpose a switch network connects a rank of capacitors to the main components $C1_{hp}$ and $C1_{lp}$, $8bit$ are used to configure this network, 2 bits for the HPF, bringing the maximum $C1_{hp}$ value to $140pF$ and 6 bits for the LPF are used to increase the $C1_{lp}$ capacitance value up to $34.8pF$. In Fig. 2.6 the part of schematic regarding the filter programmability is reported, $C1_{hp}$ and $C1_{lp}$ values are respectively $70pF$ and $3.3pF$ (as indicated in Tables

2.6) while $Cvar_{hp} = 37pF$ and $Cvar_{lp} = 500fF$. All reported values have been realized using multiples of the minimum capacitance used in the stage (i.e. $60fF$ for the HPF and $50fF$ for the LPF)

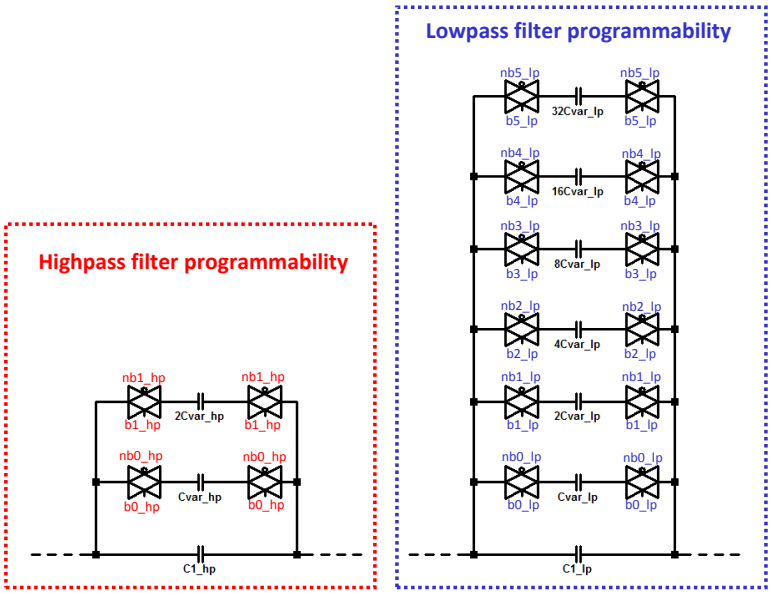


Figure 2.6: Circuitry design of flter programmability.

A simple cascade symmetrical OTA (Fig. 2.7) was chosen for the operational amplifier implementation and it was carefully dimensioned in order to minimize the input referred noise. Flicker noise is one of the major concerns, given the low frequencies of the neural signal, thus a p-type differential pair with large area was adopted to minimize this contribute [145]. Thermal noise was addressed using a large g_m for the differential pair and reducing the g_m of the output branch transistor [70] according to the formula 2.3.

$$v_{n,th} = \frac{16kT}{3g_{m1}}\left(1 + \frac{g_{m6}}{g_{m1}} + \frac{g_{m8}}{g_{m1}}\right) \tag{2.3}$$

where k is the Boltzmann constant, T the absolute temperature and g_{mx} the transconductance of transistor x. In Table 2.7 all sizes are reported, all transistors were biased with a $12.5\mu A$ current using the lower gain configuration, when the gain rises also the current can be increased proportionally in order to meet the GBW requirements. A passive SC common mode feedback block was used for power saving (Fig. 2.8), $4pF$ capacitance have been chosen in order to have a refresh time sufficiently long, this value also helps to have better performances in terms of stability.

2.4.2 Modulator circuitry design

The modulator was implemented with a SC circuit. The main components are the discrete time integrators shown in Fig. 2.9 (first stage) and Fig. 2.10 (second and third stages). It can be observed that all the feedback paths have been realized driving a switch with the quantizer output and connecting the corresponding capacitor to the reference voltages $V_{ref-} = V_{dd}/2 - 1$ and $V_{ref+} = V_{dd}/2 + 1$. Since the a and b coefficients are equals, in the first stage

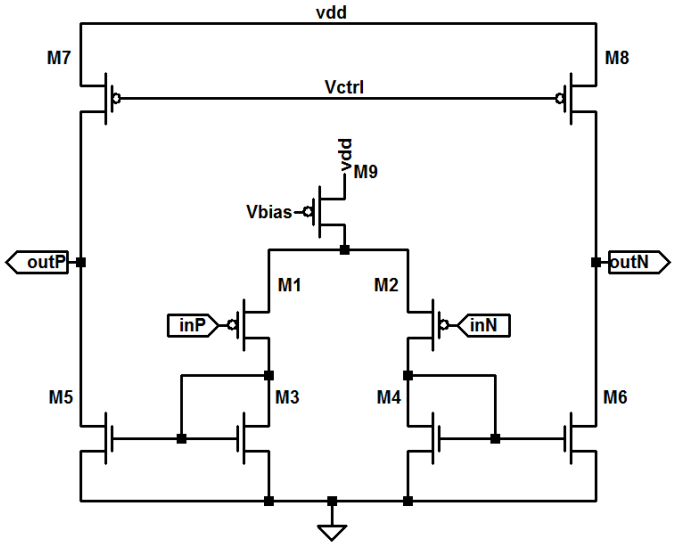


Figure 2.7: Symmetrical OTA

	$\frac{W}{L}[\frac{\mu m}{\mu m}]$		$\frac{W}{L}[\frac{\mu m}{\mu m}]$
$M_{1,2}$	$\frac{400}{2}$	$M_{7,8}$	$\frac{64}{21}$
$M_{3,4,5,6}$	$\frac{4}{8}$	M_9	$\frac{128}{21}$

Table 2.7: Dimensions of the OTA used in the filter.

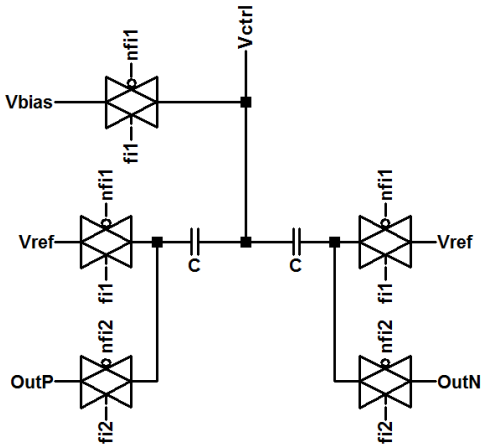


Figure 2.8: Common Mode Feedback schematic.

the same capacitor was shared for the two paths while in the second and third stage two different capacitors were used in order to implement coefficients a and c.

In Table 2.8 all the values used for the capacitors are reported. A simple symmetrical OTA was used to realize the operational amplifier (the same topology reported in Fig. 2.7 for the filter OTA has been used), it has been sized in order to meet the specifications determined with the behavioural simulation (in terms of DC gain, GBW, dynamic range and slew rate) the transistor sizes are reported in Table 2.9. The single bit quantizer has been designed with

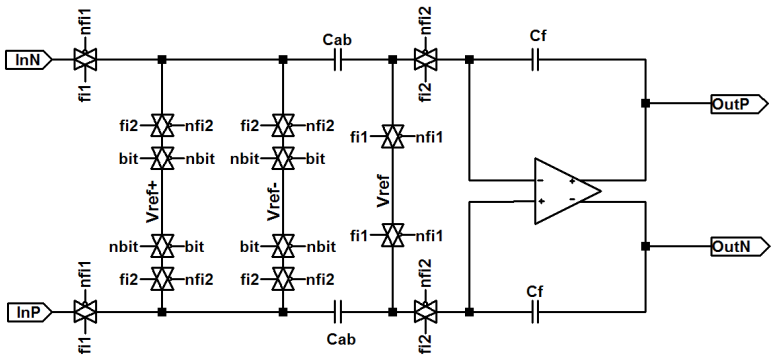


Figure 2.9: Sigma-delta modulator: first integrator schematic.

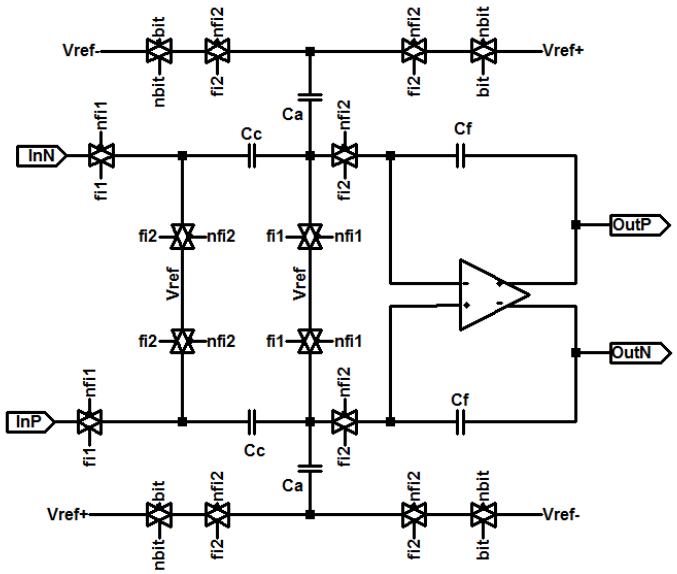


Figure 2.10: Sigma-delta modulator: second and third integrator schematic.

the track and latch circuit shown in Fig. 2.11.

C	Value [pF]	C	Value [pF]
$C_{ab,1st}$	0.4	$C_{f,2st}$	8
$C_{f,1st}$	8	$C_{a,3st}$	6.4
$C_{a,2st}$	2.4	$C_{c,3st}$	8
$C_{c,2st}$	8	$C_{f,3st}$	8

Table 2.8: Sigma-Delta modulator: capacitance values.

In Fig. 2.12 a global view of the modulator schematic with the cascade of the three integrators is depicted.

	$\frac{W}{L}\left[\frac{\mu m}{\mu m}\right]$
$M_{1,2}$	$\frac{107}{11}$
$M_{3,4}$	$\frac{1}{1}$

	$\mathbf{\frac{W}{L}[\frac{\mu m}{\mu m}]}$
$M_{5,6}$	$\frac{10}{1}$
$M_{7,8}$	$\frac{15}{5}$

Table 2.9: Dimensions of the OTA used in the modulator.

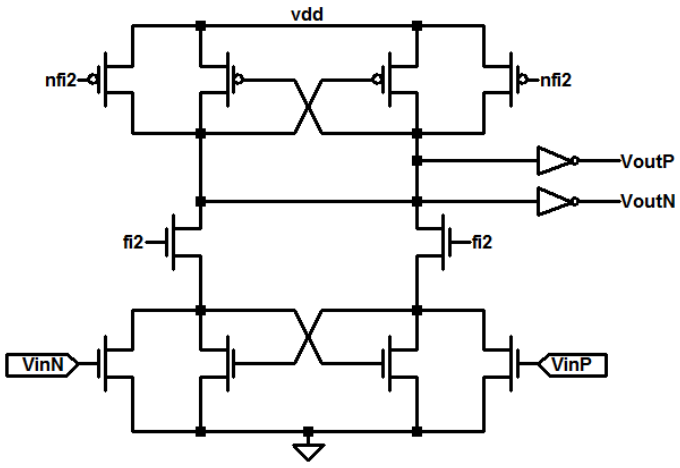


Figure 2.11: 1-bit quantizer circuital implementation.

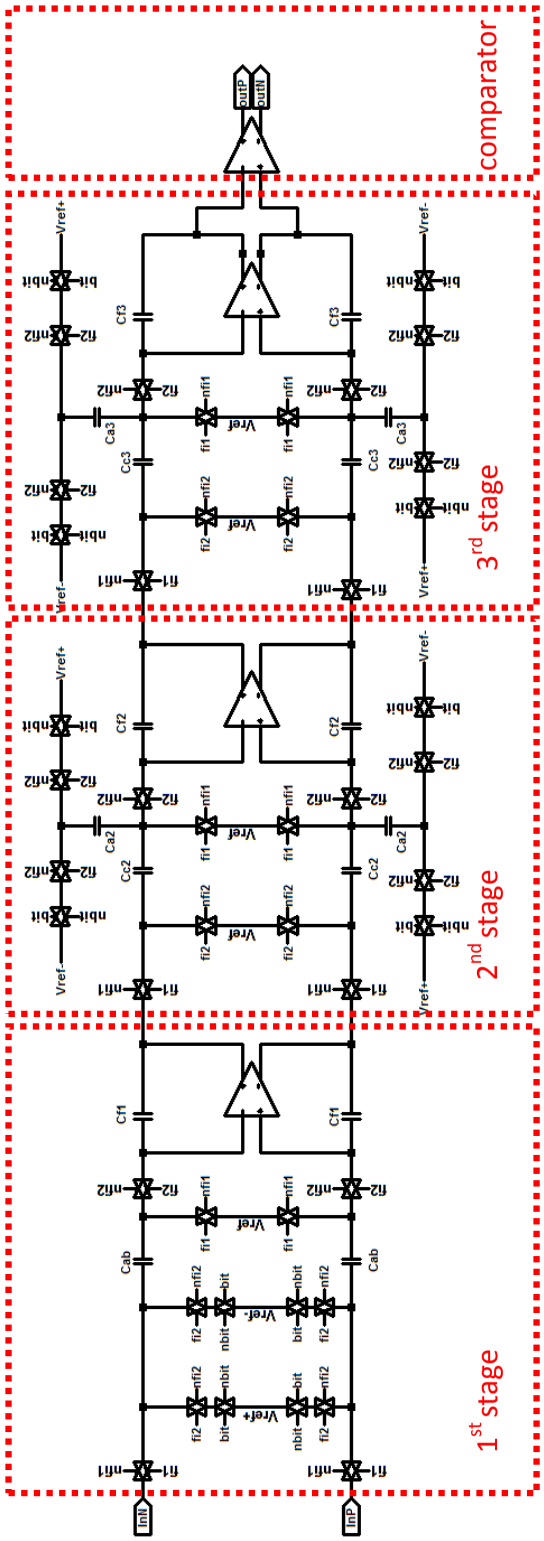


Figure 2.12: Sigma Delta Modulator: circuital schematic.

2.4.3 Low-voltage stimulator

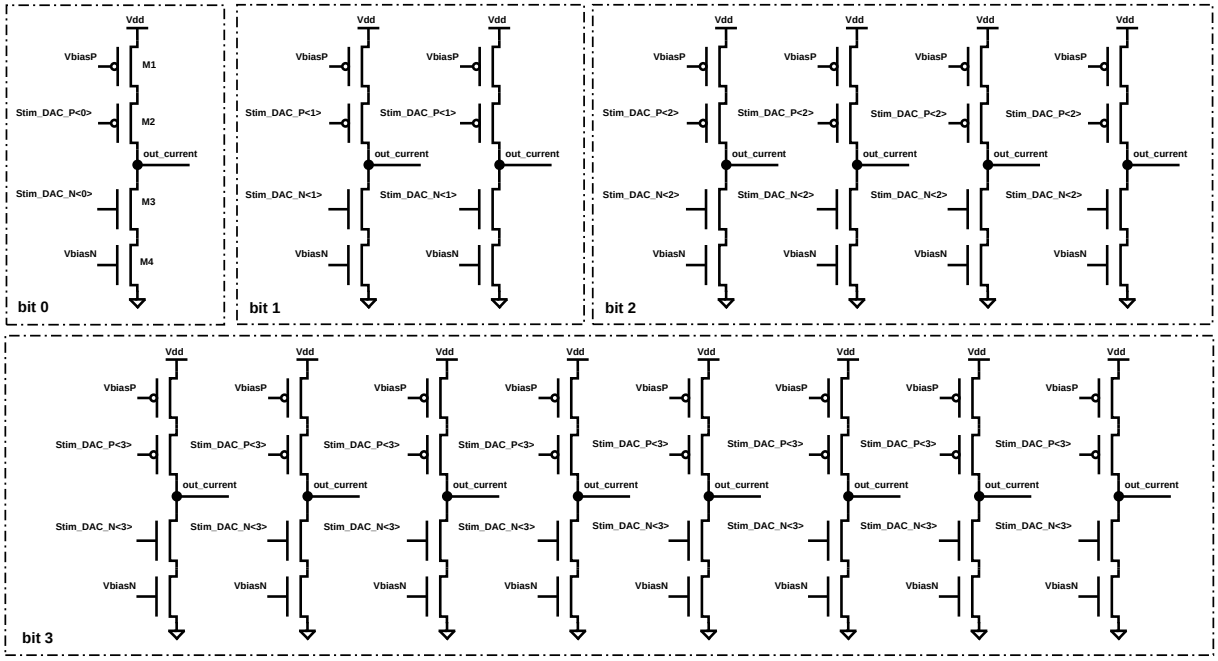


Figure 2.13: Stimulator: circuital schematic.

The low voltage stimulator, depicted in Fig. 2.13, has been implemented as a $5bit$ current DAC. The most significant bit (bit 4) is used to chose between positive and negative current, while the other 4 bit define the current amplitude. The positive part of the stimulator (made up of the PMOS transistors controlled by Stim_ DAC_ P< 0 : 3 > bit) sources the current to the electrode, while the negative part (NMOS transistors driven by Stim_ DAC_ N< 0 : 3 >) sinks the current from the electrode making possible the negative current flow. The transistors size is collected in Table 2.10, in particular, since in PMOS the carrier mobility is lower than in NMOS, PMOSs are three times bigger.

	$\frac{W}{L}\left[\frac{\mu m}{\mu m}\right]$
M_1	$\frac{60}{1}$
M_2	$\frac{60}{0.35}$
M_3	$\frac{20}{0.35}$
M_4	$\frac{20}{1}$

Table 2.10: Stimulator: transistors size.

2.4.4 Digital interface

The digital interface integrated in the chip is characterized by a bank of eight registers, each one of 16 bit. Seven registers encode the information concerning the chip configuration such as the gain value of the band-pass pre-filter, the input test set-up bypassing one of the various stages involved in the recording path, the stimulation current values, the electrodes selection. They can be either read or written. The last one is a read-only register used to store the eight $1bit$ generated by the $\Sigma\Delta$ modulators which must be applied in input to the multi-channel sigma-delta decimator. The communication between the custom designed IC and its hardware controller, presented in Section 2.6.1, is based on a custom SPI (Serial Peripheral Interface) link with four communication lines:

- **Serial Clock (SCK)**: It is a synchronization clock generated by the external digital controller;
- **Master Output Slave Input (MOSI)**: A data line from the master (external digital controller) to the slave (custom designed IC);
- **Master Input Slave Output (MISO)**: A data line from the slave to the master;
- **not Chip Select (nCS)**: This signal enables (active low) the communication between the master and the selected (usually more slave devices can be connected to the same SPI bus) salve.

The communication protocol consists of $20bit$ transactions as shown in Fig. **??** which involves that each communication pattern between the external digital part and the custom IC is performed with a frequency of $2MHz$. In detail, the first bit indicates whether the operation is intended to read or to write one of the chip registers, the next three bits are used to specify the address of which register is involved in the operation and the last 16 bits are the data which have to be read or written on the register. Using this protocol it is possible to perform different tasks on the chip:

- **Reset** of the internal registers to their default values;
- **Writing** one of the 7 chip registers for the configuration of the analog front-end;
- **Reading** one of the 8 chip registers;
- **Streaming** during which the bits generated by the eight $\Sigma\Delta$ modulators are continuously read at the frequency of $2MHz$ and sent to the digital decimator;
- **Stimulation** during which trains of biphasic pulses are generated as stimulation waveforms.

As specified before, write operations on the internal registers allow the user to reconfigure at runtime the following functionalities of the designed IC:

- The gain of the various processing sub-stages of the analog front-end (high-pass and low-pass pre-filtering) for all the eight channels;

- To give the test signal in input to one of the various stages in order to evaluate the frequency response of each of them or considering as input that coming from the neural electrodes for in-vivo experimental tests;
- To bypass or not the stage of bandpass pre-filtering;
- To set the value of the stimulation currents for each channel;
- To define which of the intermediate outputs of the processing flow connect to the test pins in order to verify the behaviour with an oscilloscope.

The custom IC digital interface was modelled and verified using Verilog Hardware Description Language (HDL). The system description was first made at Register Transfer Level (RTL) in terms of registers (flip-flops or latches) and later converted into a gate level description using the *Encounter* automatic synthesis tool by *Cadence*. Finally, the synthesized circuit was directly imported in Virtuoso Schematic Editor in which the logic ports were mapped on the digital ports from the Standard Cell library of the selected technology process.

2.5 Chip Layout

The complete transistor level schematic described in Section 2.4 was developed by continuously switching between circuitry implementation and simulation phases. The specifications, collected in Table 2.11, are the transistor level simulation results of the achieved system.

	Recording module characteristics
Total Gain	$46-66dB$
Bandwidth	$800Hz-8kHz$
IRN	$1.67\mu V_{rms}$
Power (1 ch.)	$2.5-3.4mW$
Area (1 ch.)	$0.8mm^2$

Table 2.11: IC recording module: main parameters summary after transistor level simulation.

Once the project constrains given in Section 2.2 had been met, the next and last step toward the IC fabrication was to draw the IC layout. It is the physical representation of the IC in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. The ICs are developed on a semiconductor substrate, normally silicon (Si), with additional layers on top to create all necessary structures that composed each single component of the circuit. The currently most diffused technology process to produce the ICs is the Complementary Metal-Oxide-Semiconductor (CMOS) which name is due to the fact that the typical design style uses complementary and symmetrical pairs of p-type and n-type Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) for logic functions. Two important characteristics of CMOS devices are high noise immunity and low static power consumption.

Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example the Transistor-Transistor Logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. Several CMOS technology processes are available, they differ in different factors such as the minimum MOS channel size, the substrate type, the maximum supported voltages and the number and type of the additional layers. Depending on these factors is also the variety of electronic components that can be realized on a certain technology, the most common are MOSFETs, resistors, capacitors and the Bipolar Junction Transistors (BJTs). The technology process used to make our device is the $0.35\mu mCMOSC35B4$ process from Austria-Micro-System (AMS), characterized by a minimum transistor channel length of $0.35\mu m$, a Si substrate of type *p*, 4-metal layers and a maximum operating voltage of $5.5V$ (further details on the selected technology process are in [180]).
The layout development of an analog circuit requires special care and has slight different specifications with respect to those of digital layout. In the digital domain, the main constrains are the area minimization and the minimization of parasitic capacitors in order to increase the working frequency. These two goals are obviously pursued in the analog circuit design too but in this case an additional constrain, that usually is in contrast with the others, is the maximization of the precision of all components and process parameters. This is not fundamental in digital circuits since the logic thresholds used by the logic ports to interpret and reconstruct the elaborated signals make negligible possible dissimilarities in the circuit parameters. On the contrary, the analog circuits strongly depend on the process parameters such as the oxide thickness, the MOSFET threshold voltage and the carriers mobility, and on the components geometrical dimensions, for example, the length (L) and width (W) of the MOSFETs' channel. There are two types of precision: the absolute and the relative precision. For what concern the absolute precision, the microelectronic design is characterized by errors in the order of 30% whereas it is possible to get quite high relative precision with errors in the range from 1% to 0.1%. For this reason is usually better not to let the circuit performance depending on the absolute values of the component parameters, but to design the system on the base of relative values such as the resistances or the MOSFET aspect-ratios or the capacitances ratio. Nevertheless, precision errors are always unavoidable due to the statistical fluctuations of the process parameters and due to the dissimilarities between the layout drawing and the effective component geometrical dimensions after the IC manufacture. For example, a huge difference is observed between the effective values of the parameters of two devices ideally designed with same parameters but placed on different sides of the wafer, in the same run and also in different runs. Moreover, depending on the nature of the phenomena that originates the error, the uncorrelated statistical fluctuations of a process parameter can be related to the device area, to its boundary or to both of them. Generally, the parameter variance is decreased by increasing the area and the boundary of the device since in this way the fluctuations are averaged on a larger surface. Therefore, as previously announced, in the analog circuit design the area minimization is not the best criteria to fix the device dimensions, as it is in the digital design.
However, by carefully drawing the layout it is possible to match the parameters of two devices placed in the same area of the substrate. Even though there is not the "best way" to draw a layout, some design rules, based on the specific technology process and on practical considerations, exist and can be followed to reach a good matching between similar compo-

nents. The most common are:

- **Same shape and dimension**: two matched devices with the same parameters should have the same shape and dimension (not minimum), whereas, in the case in which their parameters ratio is K, it is better to draw the devices as a multiple (with parallel or series connections) of a common unit device.
- **Minimum distance**: in order to reduce the process statistical fluctuations between one component and the other, the matched devices should be placed on the substrate as close as possible one to each other.
- **Symmetrical structure**: to maximize the matching between the devices, it is preferable to create structures that are as match symmetrical as possible. In particular, it is useful to compensate a process parameter fluctuation when it has a constant gradient in a specific direction. Possible solutions are the common centroid and the interdigitated structures.
- **Same orientation**: to avoid problems related to non-isotropic manufacturing steps and to reduce the silicon induced stress, it is better to have the current flowing in the same direction in matched components.
- **Same surrounding**: matched devices should have the same surrounding and, for this reason, some dummy components, typically connected to the circuit ground, can be placed next to the peripheral devices.
- **Same temperature**: in presence of on-chip high power dissipation components the matched devices should stay at the same distance from the heat source so that their parameters undergo the same temperature influence.

In addition to the "good-layout" design rules, many other drawing constraints are given by the manufacturer. Differently from the previous ones, these rules are due to the technology process capabilities and, therefore, must be respected otherwise the layout will be rejected by the manufacturer. For example, there are restrictions on the geometrical shapes (maximum and minimum area or aspect-ratio) on the minimum density of a certain metal layer and on the interconnection line minimum spacing. However, the respect of all presented rules does not guarantee a high performance chip, leaving a huge space to the designer experience. In fact, depending on how the elements are placed and interconnected, different parasitic components such as transistors, capacitors and diodes may be added to the designed circuit with possible consequent small or huge changes in the IC parameters. Sometime, the parasitics are unavoidable and, in case of a circuit performance decease, they cause the needs of changes on the device parameters or, even worst, on the circuit architecture. For these reasons, the analog layout design is a quite critical step in the project of an integrated circuit requiring the designer special care and experience.

Fortunately, modern IC layout is done with the aid of IC layout editor software, including place and route tools or schematic driven layout tools. In case of digital layout, since digital circuits mainly contain standard cells, the layout drawing is totally computerised and in few steps is possible to automatically generate the entire IC layout with high performance results. On the contrary, for the discussed reasons, the analog layout is not completely automatised and even though the layout of the single components (MOSFET, resistors and capacitors) can

be automatically generated, it does not often satisfy the precision constraints requiring several "by-hand" adjustments. Nevertheless, some support tools are available and the drawn layout must pass a series of checks in an automatic process known as physical verification. The most common checks in this verification process are:

- **Design Rule Checking (DRC)**: The main objective of DRC is not to validate that the design will operate correctly, but to verify that the structure meets the process constraints for a given design type and process technology. In fact, DRC software usually takes as input a layout and a list of rules specific to the semiconductor process chosen for fabrication. From these it produces a report of design rule violations that the designer may or may not choose to correct. Carefully "stretching" or waiving certain design rules is often used to increase performance and component density at the expense of yield. The DRC software used in this thesis is *Assura* by *Cadence Design System*.

- **Layout Versus Schematic (LVS)**: The LVS checking tool recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them. This netlist is compared by the "LVS" software against a similar schematic or circuit diagram's netlist. LVS Checking involves following three steps:

  1. **Extraction**: The software program takes a database file containing all the layers drawn to represent the circuit during layout. It then runs the database through many area based logic operations to determine the semiconductor components represented in the drawing by their layers of construction. Area based logical operations use polygon areas as inputs and generate output polygon areas from these operations. These operations are used to define the device recognition layers, the terminals of these devices, the wiring conductors and via structures, and the locations of pins (also known as hierarchical connection points).
  2. **Reduction**: During reduction the software combines the extracted components into series and parallel combinations if possible and generates a netlist representation of the layout database. A similar reduction is performed on the "source" Schematic netlist.
  3. **Comparison**: The extracted layout netlist is then compared to the netlist taken from the circuit schematic. If the two netlists match, then the circuit passes the LVS check. At this point it is said to be "LVS clean."

  In most cases the layout will not pass LVS the first time requiring the layout engineer to examine the LVS software's reports and make changes to the layout. Common errors are shorted and unconnected wires, component mismatches, missing components and parameter mismatch.

- **Parasitic extraction**: It is the calculation of the parasitic effects in both the designed devices and the required wiring interconnects of an electronic circuit: detailed device parameters, parasitic capacitances, parasitic resistances and parasitic inductances, commonly called parasitics.

- **Antenna rule checking**: The antenna basically is a metal interconnect, i.e., a conductor like polysilicon or metal, that is not electrically connected to silicon or grounded, during the processing steps of the wafer. During the manufacturing process charge

accumulation can occur on the antenna during certain fabrication steps like Plasma etching, which uses highly ionized matter to etch. If the connection to silicon does not exist, charges may build up on the interconnect to the point at which rapid discharge does take place and permanent physical damage results to thin transistor gate oxide. This rapid and destructive phenomenon is known as the antenna effect. Antenna errors can be cured by adding a small antenna diode to safely discharge the node or splitting the antenna by routing up to another metal layer and then down again. The Antenna ratio is defined as the ratio between the physical area of the conductors making up the antenna to the total gate oxide area to which the antenna is electrically connected.

- **Electrical Rule Checking (ERC)**: It involves checking a design for all electrical connections that are considered dangerous. This might include checking for well and substrate areas for proper contacts and spacings thereby ensuring correct power and ground connections, unconnected inputs or shorted outputs and gates connected directly to supplies. ERC checks are based upon assumptions about the normal operating conditions of the ASIC, so they may give many false warning on ASICs with multiple or negative supplies. They can also check for structures susceptible to electrostatic discharge damages.

When all verification is complete, the data is translated into an industry standard format, typically GDSII, and sent to a semiconductor foundry. The process of sending this data to the foundry is called tapeout due to the fact the data used to be shipped out on a magnetic tape. The foundry converts the data into another format and uses it to generate the photomasks used in a photolithographic process of semiconductor device fabrication. In case of huge and complex circuits is better to split the whole system in small blocks and to draw the layout of each single module separately. In this way, the verification procedure is quicker and it is easier to check and correct the possible resulting errors. However, a preliminary mapping of the overall system, also referred as IC floor-plan or outline, is required in order to define shape and position of the different blocks. This is an essential step to make the system as compact as possible and to arrange the blocks in a way that simplifies their interconnection and minimizes possible interferences among the parts. For example, unless it is unavoidable, mixing analog with digital layout is not recommended since the noise produced by the continuous switching of digital circuits can affect the analog circuit performance. Moreover, analog and digital circuits should have separate voltage supply lines and should be surrounded by proper rings shorted to ground to better insulate the two parts. In case of very complex IC, it is, of course, possible to iterate the splitting process and build up a multi-level hierarchical structure. This is the case of the designed IC that has been divided in the following top level blocks: the IC pads , the current and voltage reference generator (BIAS), the digital interface and the eight channels; each channel includes three second level modules: the bandpass filter (BPF), the $\Sigma\Delta$ modulator and the low voltage stimulator. Finally the bandpass filter has been further divided in two blocks: the high-pass filter (HPF) and the low-pass filter (LPF). The whole multi level floorplan is depicted in Fig. 2.14.

The layout of all modules was manually drawn with the tool Virtuoso Layout Editor by Cadence with the exception of the IC pads, whose layout already exist in the technology process libraries, and the digital interface whose layout was automatically generated with the Encounter Digital Implementation (EDI) tool by Cadence. Starting with the lower level

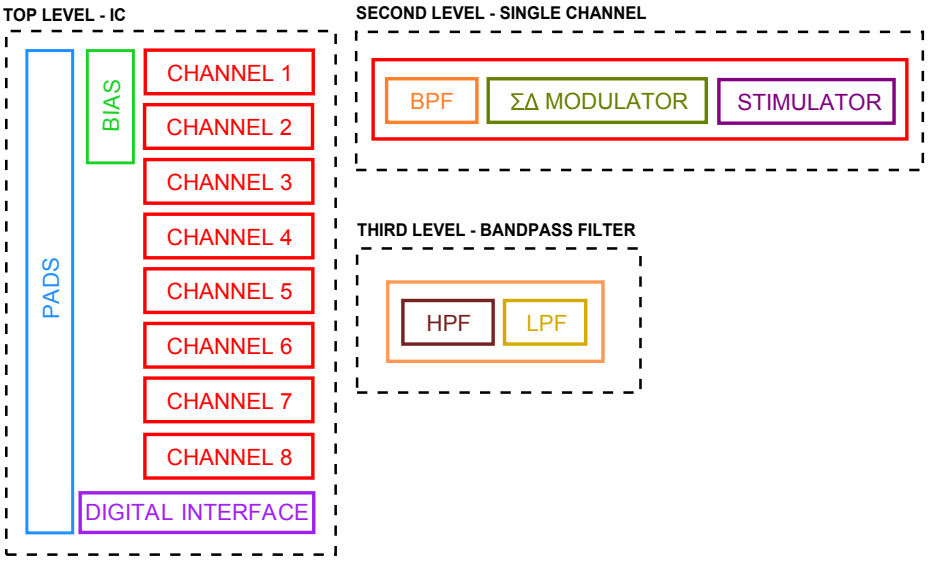


Figure 2.14: Complete outline of the designed recording chip.

blocks, the LPF layout, depicted in Fig. 2.15, was the first to be drawn. Since it has a fully differential structure, as depicted in Fig. 2.5, a high matching is required between the capacitors of the two symmetrical signal elaboration branches. In particular, the pairs $C1_{lp1}$-$C1_{lp2}$, $C2_{lp1}$-$C2_{lp2}$, $C3_{lp1}$-$C3_{lp2}$ from Fig. 2.5 and the gain programmability capacitor pairs from Fig. 2.6 have to match. For this reason, by joining the matching techniques previously presented, the capacitors were implemented as a parallel of several unit capacitors positioned by following the outline depicted in Fig. 2.18. Moreover, a ring of dummies was placed around the whole structure so that the peripheral capacitors have the same surrounding of the inner ones.

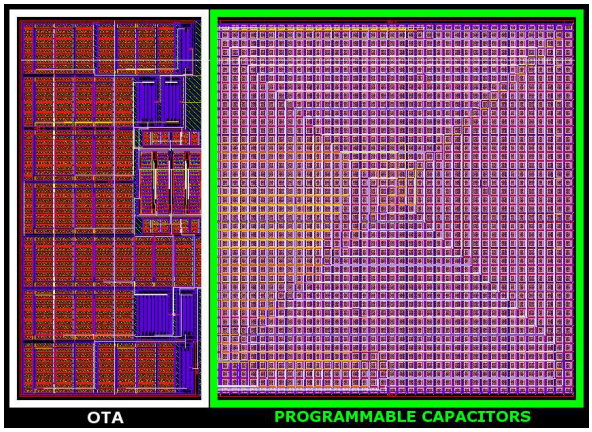


Figure 2.15: Low-pass filter layout.

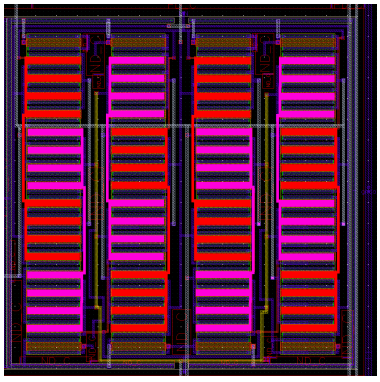


Figure 2.16: The layout of the input differential pair, M_1 (pink) and M_2 (red), of the LPF OTA (Fig. 2.7), each transistor was implemented as parallel of 32 interdigitated transistors.

The component matching rules were applied also for drawing the layout of the LPF OTA amplifier. The matched NMOSs and PMOSs were implemented as a multiple of unit transistors positioned with the same orientation and connected following the interdigitated schema.

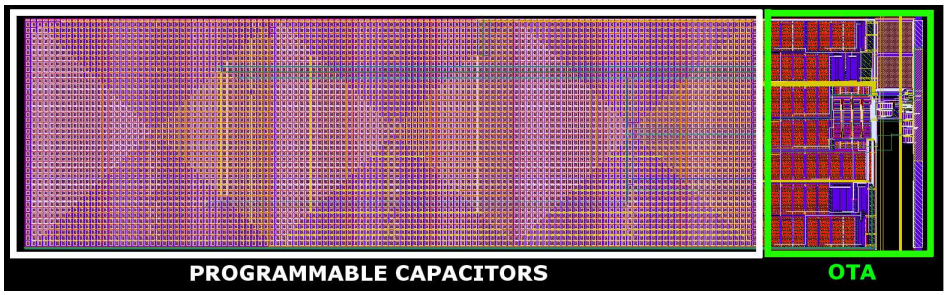


Figure 2.17: The HPF layout where the white box encloses the programmable capacitors and the green one contains the OTA.

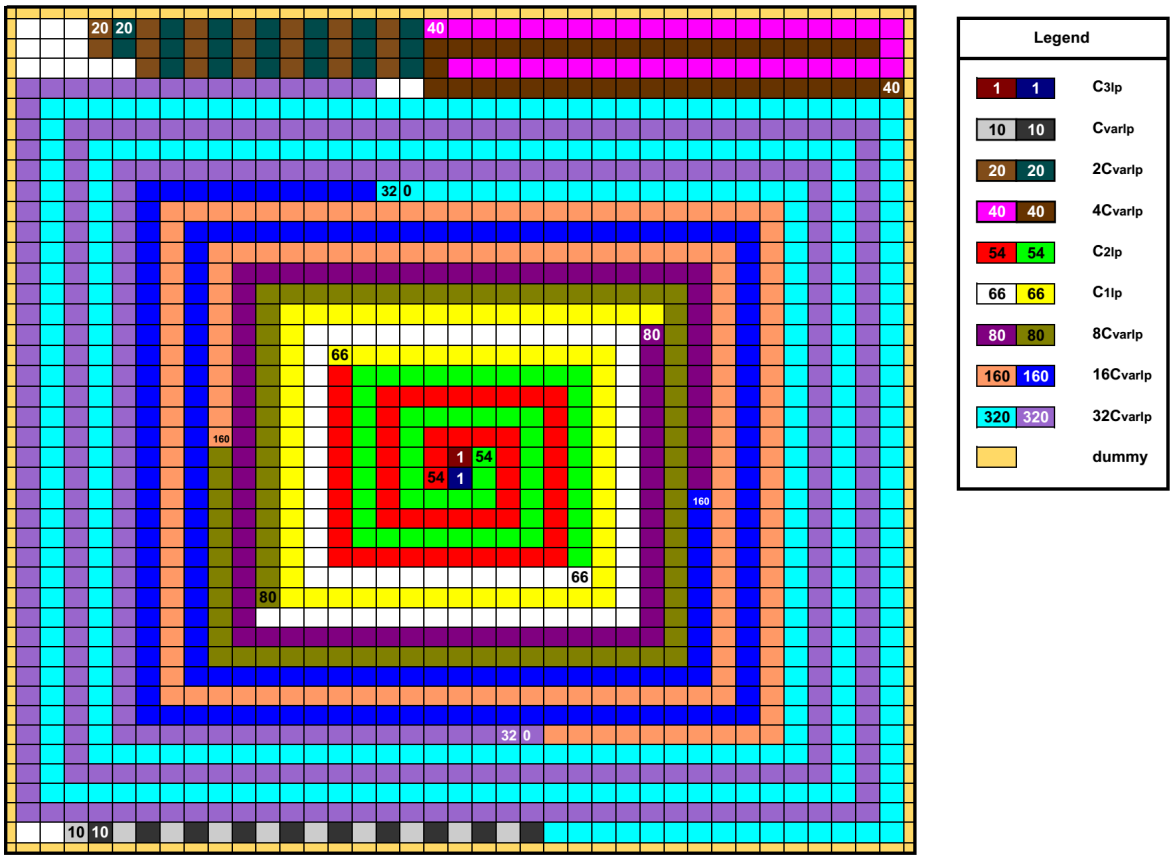


Figure 2.18: The outline of the LPF capacitors for reaching a good matching level.

For example, the matched structure of the input differential pair $M_1 - M_2$ of Fig. 2.7 is shown in Fig. 2.16: M_1 and M_2 with a $W/L = 400/2$ were designed as parallel of 32 PMOSs with a $W/L = 12.5/2$. The layout of all remaining modules was designed following the same methodology. Fig. 2.17 depicts the HPF layout in which the white box encloses the programmable capacitors and the green one contains the OTA. Then, the HPF and the LPF were cascade connected to form the BPF depicted in Fig. 2.19. In order to complete the single

channel, the ΣΔ modulator (Fig. 2.20) and the low-voltage stimulator (Fig. 2.21) layouts were designed and connected to the BPF as depicted in Fig. 2.22. Finally, by eight times copying the single channel layout and connecting it to the PADs, the digital interface and the polarization module (Fig. 2.23), the overall IC layout depicted in Fig. 2.24 was obtained. The resulting silicon die (Fig. 2.25), with a square shape and a total area of $16.81 mm^2$, has 34 pins that, from the top, have the following functions:

- **VDDA, GNDA**: analog power supply ($3.3V$).
- **OutTestP, OutTestN**: a network of switches was implemented in the IC to send to these two pads the output signals of a specific module of the recording channel. In particular it is possible to get the output of the following blocks: HPF, LPF, BPF and the first, the second and the third stage of the ΣΔ modulator. This is useful for testing purpose to better characterized each single block.
- From **elA0** to **elA7** and from **elB0** to **elB7**: these are the 16 input signals from the two electrodes, A and B.
- **GroundA, groundB**: they are the ground references of the two electrodes, usually placed inside the nerve, with respect to which is possible to recorded the input signals.
- **GroundExt**: this pad allows to record the input signals with respect to an external reference, for example placed on the patient body and outside the nerve.
- **InTestP, InTestN**: they allowed to provide some known input signals for testing purpose.
- **Vref, VrefP, VrefN**: they are the voltage references required by some IC modules.
- **gnd, vdd**: digital voltage supply ($3.3V$).
- **nCS, MISO, MOSI, SCK**: these are the four pads of the SPI communication port.

The silicon die was placed into a 84 pins package as depicted in Fig. 2.26.

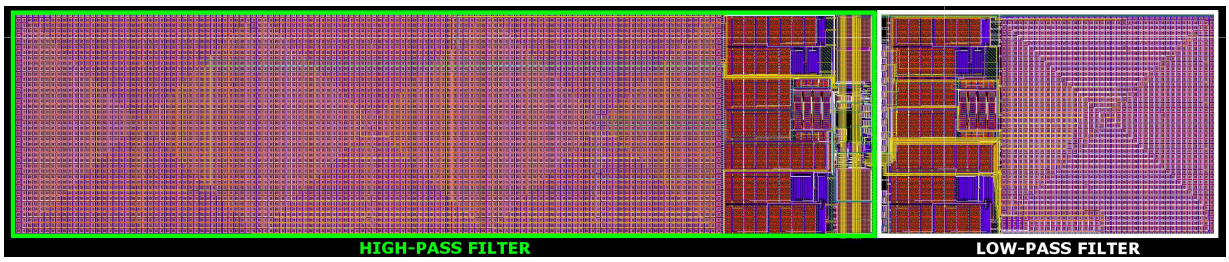


Figure 2.19: BPF layout as a cascade of the HPF and LPF.

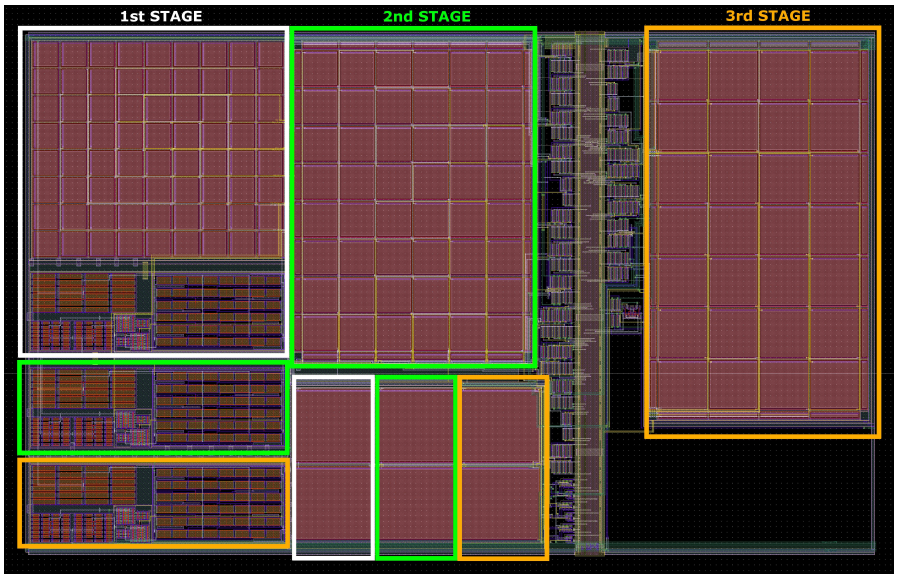


Figure 2.20: ΣΔ modulator layout.

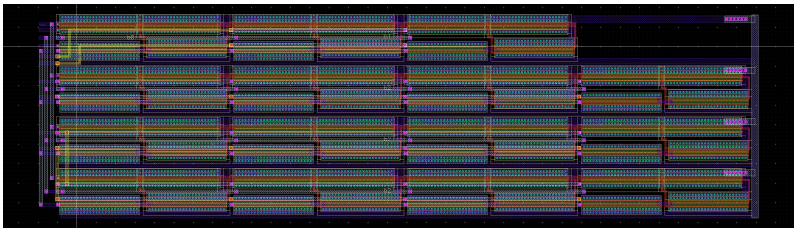


Figure 2.21: Low-voltage stimulator layout.

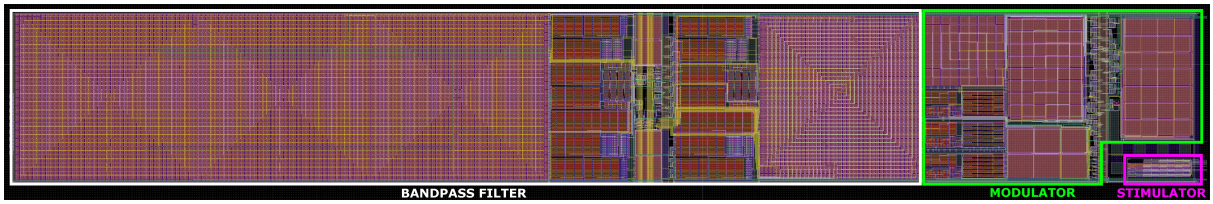


Figure 2.22: A signle channel layout including the BPF (white box), the ΣΔ modulator (green box) and the low-volatge stimulator (pink box).

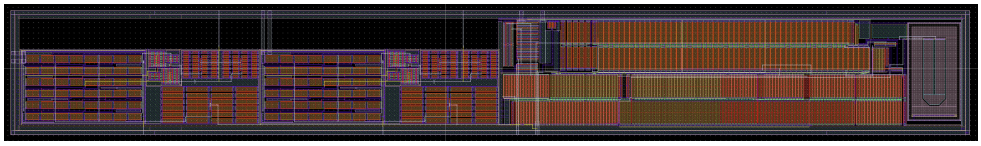


Figure 2.23: Layout of the voltage and current refernce generator.

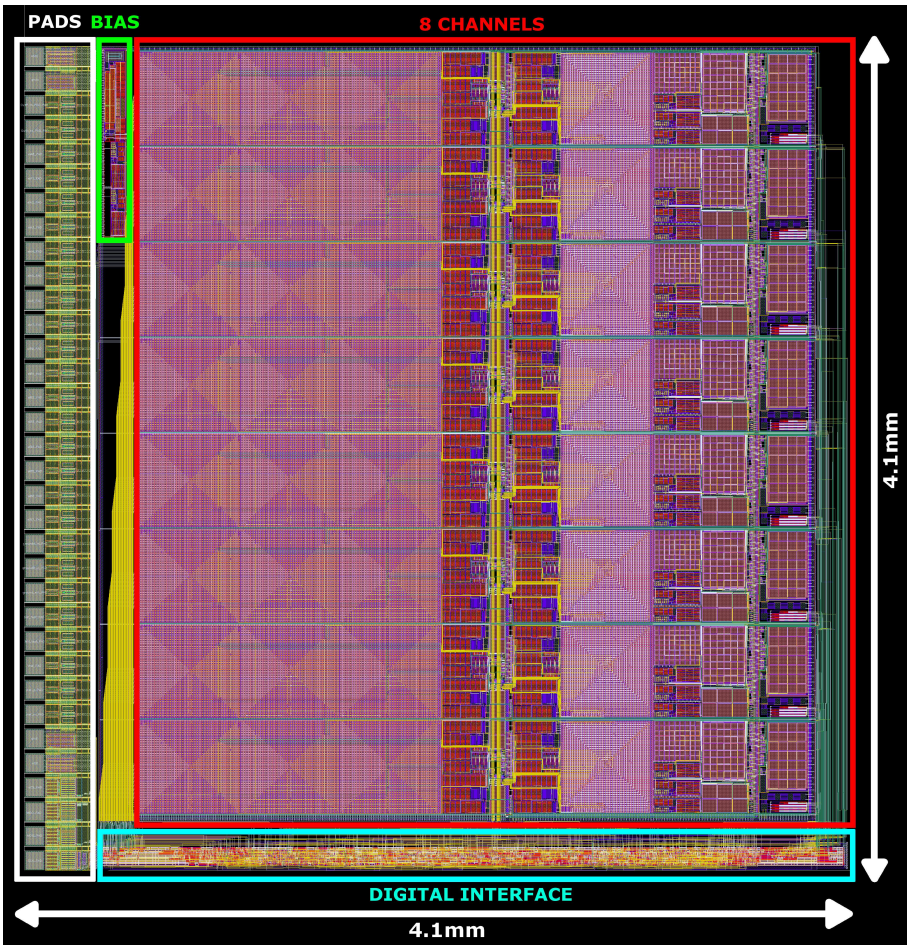


Figure 2.24: Complete layout of the designed 8-channels neural recording interface with low-voltage stimulator.

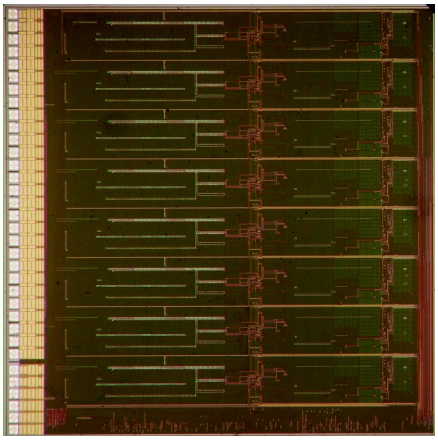


Figure 2.25: Designed silicon die.

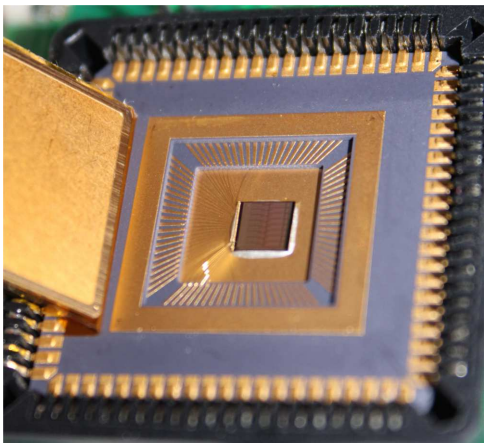


Figure 2.26: Designed IC into a 84 pins standard package.

2.6 Experimental results

In this Section, after a short presentation of the experimental set-up, the results of the IC experimental tests are shown: first the results obtained by means of laboratory measurements are discussed, then those achieved with the in-vivo tests.

2.6.1 Experimental setup

The developed IC is not a stand alone device and requires an additional frame to be hosted, configured and tested. Moreover, a digital system controller to manage the communication between the IC hosting frame and a PC is necessary. As a consequence, the Control System, depicted in Fig. 2.27, was developed. It is divided into two main parts: a custom designed Printed Circuit Board (PCB) and a digital system controller. Both parts are discussed in this Section even though only few details are given on the digital system since it was developed in collaboration with another PhD student, named Nicola Carta.

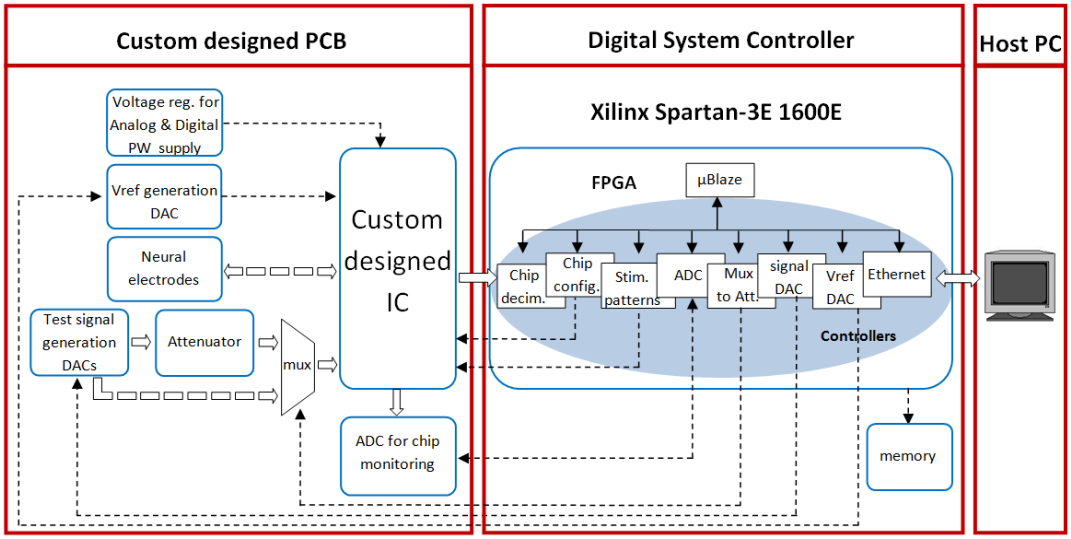


Figure 2.27: Architecture of the experimental setup.

The left part of the Control System contains the functional blocks that must be implemented in the PCB. The system core is the custom designed IC and its power supply is provided by two voltage regulators in order to separate the digital from the analog power supply. The Vref generation DAC block provides the voltage references needed for the chip proper working. The IC input signals can come from the neural electrodes or from a test module. The latter is made up of two blocks: the DACs for the sinusoidal signal generation, and an attenuator that reduces the sine amplitude in the microvolt range in order to make it more similar to the typical neural signals. An ADC has also been introduced in order to evaluate the intermediate output stages of the chip (HPF, LPF, 1st, 2nd and 3rd modulator integrator output as explained in Section 2.4). The right part shows the digital system controller, implemented on a prototyping board (Xilinx Spartan-3E 1600E) whose main tasks are the implementation of the digital decimator band pass filter for the $\Sigma\Delta$ converter, the control of the peripherals hosted in the PCB, and the communication management with the PC by

means of an Ethernet link. The on-board MicroBlaze processor has been used and, for each device hosted in the PCB, a custom controller has been developed. It is also possible to use a DDR memory available in the *Xilinx Spartan-3E 1600* in order to store temporary the data before being transmitted to the PC via Ethernet. Fig. 2.28 shows a picture of the two boards.

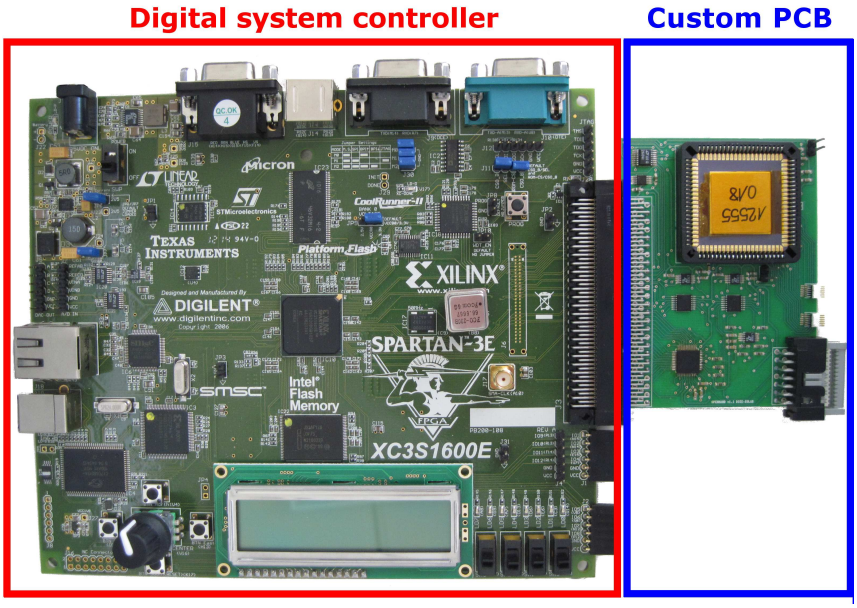


Figure 2.28: The control system.

Custom designed PCB

The board has been designed using the software *Cadence-Orcad Capture* for the schematic (Fig. 2.29) and *PCB Editor* for the layout (Fig. 2.30). Special care has been put on the layout, trying to minimizing the connections and keeping as symmetrical as possible the tracks carrying the most critical analog paths. Two different power supply were provided for the analog and the digital parts, in order to isolate the weak analog signals coming from the electrodes from the noise derived from the digital electrical grid. Wide ground planes have also been used as well as large tracks for ground and power supply paths.

As shown in Fig. 2.31, the board contains:

- **A**: A 84 pin socket hosting the custom designed chip.
- **B**: The electrode connectors.
- **C**: A 3.3V voltage regulator (*max1792*) for the analog power supply generation, (the digital one is generated in the *Spartan-3E 1600E* board).
- **D**: A DAC (*LTC2604*) for the reference voltage generation, three reference voltage are needed to provide the necessary voltages to the chip: 1.65V (Vref), 0.65V (VrefN) and 2.65V (VrefP). The last two are needed for the proper working of the sigma delta modulator.

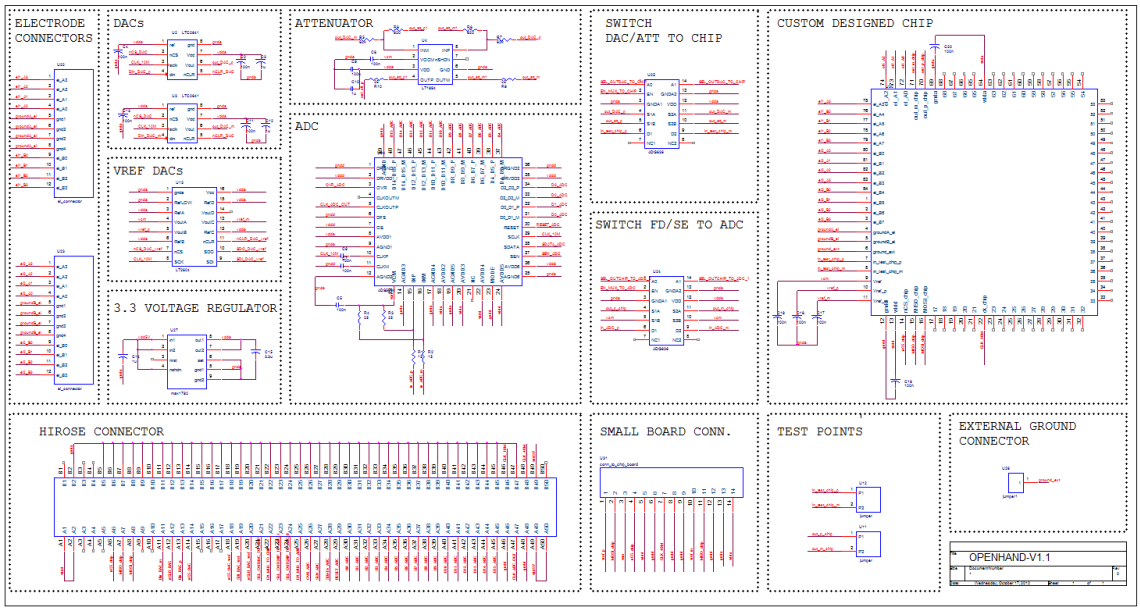


Figure 2.29: PCB schematic in *OrCAD-Capture* environment.

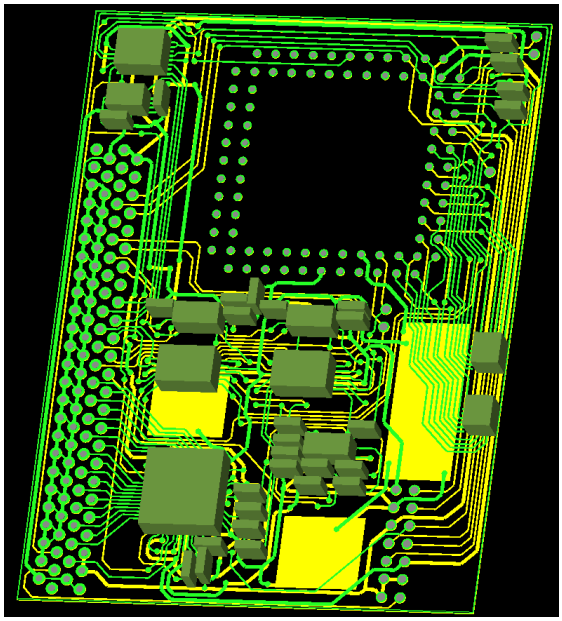


Figure 2.30: PCB layout in *OrCAD-PCB Editor* environment.

- **E**: Two 16 bit DACs (*LTC2641*) for the test signal generation. Two different DACs are necessary in order to generate a fully differential input signal.
- **F**: An attenuator implemented using a fully differential operational amplifier (*LT1994*) and a resistance network.
- **G**: A 16 bit ADC (*ADS5560*) has been inserted in order to verify the correct behaviour of the middle stages of the analog front-end of the chip.

- **H**: A 100 pin *Hirose* connector for the communication with the *Spartan-3E 1600E*.
- **I**: A further connection with a smaller board hosting only the electrode connectors and the chip. This feature will be particularly useful during in vivo tests and will allow to collocate the chip near to the implanted electrodes keeping the FPGA-board far away from the animal.
- **J**: A switch network used to send the DAC or the attenuator output to the test input pins of the chip (*ADG636*).

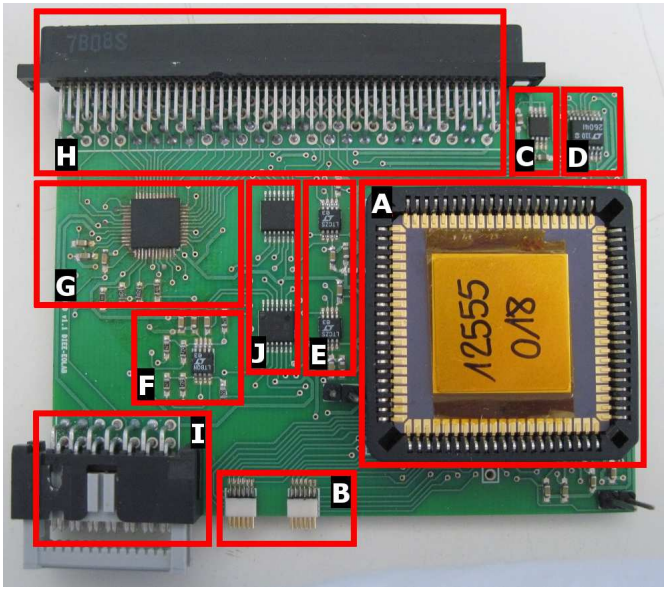


Figure 2.31: PCB modules.

Digital system controller

The Digital System Controller (DSC) has been implemented on a *Field Programmable Gate Array* (FPGA), in particular on a *Digilent Spartan 3E 1600 Development Board*. Main task of the system is to implement the digital part of the $\Sigma\Delta$ which removes by bandpass filtering the EMG noise at low frequencies and the quantization noise at high frequencies. At the same time, it must preserve the signal from aliasing effects before a subsequent downsampling at the Nyquist frequency. To evaluate the performances of the data acquisition system, it is necessary to create a test environment on FPGA characterized by a MicroBlaze processor used as microcontroller. In particular, the MicroBlaze is linked by PLB (Processor Local Bus) to the hardware interfaces that communicates using SPI (Serial Peripheral Protocol) with the components placed in the custom PCB, as we can notice in the Fig. 2.27, in order to:

- Apply the digital multi-channel bandpass filtering (IIR Butterworth $12th$ order BPF) between $800Hz$ and $8kHz$, using a defined fixed point quantization to represent the internal signals; at downstream it is necessary a downsampling stage to bring back the sampled signal at the Nyquist frequency;

- Set the value of the internal registers of the chip which permit to select among the different available configurations (electrode signal or test input selection, gain value, output signal selection, etc);
- Generate stimulation patterns as biphasic pulse trains with user-programmable amplitude, duration or frequency;
- Evaluate one of the intermediate outputs of the recording system acquired by the high resolution ADC (*TI-ADS5560*), reading in parallel way the 16 output-bits;
- Enable or not the attenuator;
- Select the frequency and the amplitude of two sine signals to be used as differential test input for the recording system, their samples centred at half of the main reference voltage and quantized with 16 bits are serially transmitted to the two DACs *LTC2641*;
- Define the three reference voltages needed by the custom designed IC, they are generated by the *LTC2604* component that receives a serial $24-bit$ word which determines in sequence the operation that must be done (4 bits), the address of one or more of the four integrated DACs (4 bits) and the equivalent decimal integer (16 bits);
- Acquire in real-time the samples coming from the different channels of the sigma-delta modulator and filtered by the digital band-pass decimator; the quantized output of this last stage are transmitted to the PC via Ethernet.

Moreover, it is necessary to generate the clock signals with frequency of $40MHz$ and $10MHz$ which must be sent in input, respectively, to the custom designed IC and to the *LTC2641*, *LTC2604* and *TI-ADS5560* components. They are generated from the system clock frequency of the digital board of $50MHz$ instantiating the opportune DCMs (Digital Clock Managers). With regards to the digital filter, it has been designed with a frequency bandwidth between $800Hz$ and $8kHz$ (the ENG signal bandwidth) allowing to remove the EMG noise at lower frequencies and the quantization noise, shaped by the sigma-delta modulator, at higher frequencies. The bandpass filtering, has been performed in the digital domain thanks to the possibility of exploiting the advantages of the integration capacity that allows to implement higher order filters. In this particular case, it has been designed a $12th$ order filter that meets our needs in terms of band attenuation. The filter order could be further increased by integrating the filter in the custom designed IC, in this case, in fact, the FPGA slice occupation should not be considered. The input sampling frequency is $16MHz$, it is given by the number of channels (8) multiplied by the output sampling frequency of the $\Sigma\Delta$ modulator ($2MHz$). Exploiting the timing division multiplexing (TDM) it has been possible to avoid the digital filter stages replication for each channel. A downsampler with a downsampling factor R of 125 has been implemented in order to bring back the eight output signals of the digital filter at the Nyquist frequency ($16kHz$).
Using the MATLAB environment, the user can select weather the input of the recording system is the differential sine signal generated by the two components *LTC2641* in testing mode or the ENG signal coming from the eight channel electrode connected to the custom designed PCB. In the first case, the user can send via *MATLAB* to the MicroBlaze processor, the frequency and the amplitude of the two sine signals. The maximum allowed frequency is

$80kHz$, due to the specification imposed by the component *LTC2641*, since the higher cut-off frequency is $8kHz$, such value is adequate to properly test the BPF filter.
The data coming from the different subblocks of the analog part as well as those coming from the digital anti-aliasing decimator filter, can be transferred to the PC by means of an Ethernet-based communication link, which determines the instantiation of a *Xilinx Controller* linked to the MicroBlaze by PLB. The MicroBlaze uses the *lwip*-1.3 library which implements the TCP-IP protocol stack optimized for FPGA. In this way, it is possible for the user to communicate with the MicroBlaze sending UDP packets, using MATLAB environment to define the configuration of the chip and of the various components in the PCB and to decide which operation mode must be performed by the custom designed IC:

- **RESET** of internal registers;
- **WRITING** of one of the possible internal registers;
- **READING** of one of the possible internal registers;
- **STREAMING** of the ΣΔ modulator and of the digital multi-channel filter with subsequent downsampling at Nyquist frequency;
- **STIMULATION** that is the generation of biphasic pulse trains of defined duration, amplitude and frequency to be sent to the electrodes.

On the PC side, MATLAB facilitates the use of a UDP communication because it takes care of managing the receipt and transmission of UDP packets to and from the FPGA as if they were simple readings from the input buffer and writes to the output buffer. An UDP connection between *MATLAB* and the FPGA is necessary in order to create a well defined communication socket between them. This is only possible if the *Instrument Control* toolbox is available.
On the FPGA side, the software library *lwip*-1.3 permits to the MicroBlaze to be always able to manage, at the same time, more requests from the user. This is possible thanks to the fact that the processor, for each request, defers the execution to the different hardware interfaces and waits for other UDP packets coming from the Ethernet controller. For example, if the user wants to set the *STREAMING* mode, the MicroBlaze reads continuously the value of a defined internal register and stores the relative samples on a buffer before sending it as the payload of a UDP packet. By this way, the real-time constraints can be satisfied allowing the audio streaming, the screen plotting and the data saving on the *MATLAB* workspace avoiding information loss. The processor is however able to handle in asynchronous mode the user requests and, for example, to stop the data sending to the PC, performing a callback function at the receipt of a particular UDP packet.
If the user wants to evaluate the output of one of the subblocks of the recording system, at the sampling frequency of $2MHz$, relatively to each single channel, converting it in a digital way, with 16 bits of resolution using the *TI-ADS5560*, we are not able to satisfy the real-time constraints. For this reason, it is necessary to save the relative samples on the DDR SDRAM memory, with high capacity ($64MB$), before they can be sent to the PC via Ethernet by subsequent UDP packets. A dedicated DDR SDRAM controller has been instantiated in the digital part and linked to the PLB in order to allow the processor to save several number of samples in output from the various channels of the ΣΔ modulator before transmitting them at off-line mode to the PC via Ethernet.
This problem does not occur during *STREAMING* state in fact, the downsampling stage brings

back the sampled signal to the Nyquist frequency so that the real-time constraints are relaxed. Nevertheless, it cannot be done without using some optimized techniques of buffering because of the latency on the software execution of the MicroBlaze, introduced by the sending of the UDP packets. In this particular case, to avoid the sample loss at the output of the digital filter, it has been necessary to use a bank of six registers for each channel. In this way, the hardware interface can sample the output of the eight channels of the digital filter at the Nyquist frequency and save them in circular mode in the register bank which is accessible to the MicroBlaze. It permits that the processor reads the value of the register bank only one time, by this way the sampling frequency in output of the digital filter is reduced by a factor of six with respect to the Nyquist frequency and the corresponding timing constraints caused by the latency of the sending of a UDP packet are relaxed.
Finally, during *STIMULATION* state, the Custom Designed IC is able to generate biphasic pulse trains as we can see in the Fig. 2.32.

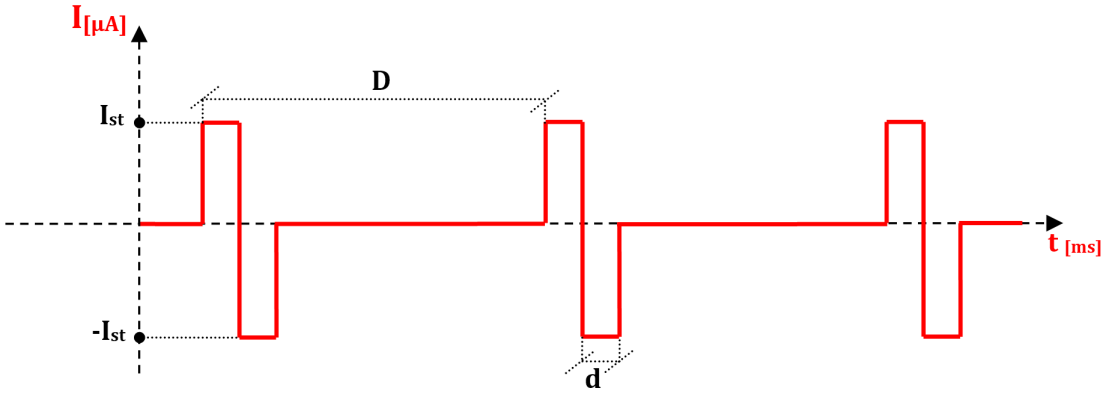


Figure 2.32: Biphasic pulse trains generated during *STIMULATION* state.

The user can communicate with the MicroBlaze processor, via *MATLAB*, the value of the various reconfigurable parameters which are showed in Fig. 2.32:

- The time period D between two subsequent biphasic pulses;
- The time interval d of each pulse phase during which the stimulation current on a defined channel corresponds to I_{st} or $-I_{st}$;
- The positive value of the desired current stimulation I_{st} applied in input to one channel of the electrode;
- The electrode channels to be stimulated.

Starting from these values, the MicroBlaze obtains the values which must be assigned to the accessible registers of the hardware interface. In particular, the processor converts I_{st} in Sign-Magnitude representation using only 5 bits for each channel so that the interval of possible integer values is $[-15;+15]$ which corresponds to a defined value of stimulation current between $-412.5\mu A$ and $412.5\mu A$ with a resolution of $27.5\mu A$. The period D of the biphasic pulse train can vary in the $[3.3ms - 100ms]$ range, while the pulse duration d ranges from $10\mu s$ and $300\mu s$. The MicroBlaze checks, for each stimulation parameter, whether the value entered by the user is acceptable or not. The two temporal parameters must be converted

in two integers which correspond to the values of two hardware counters, instantiated in the hardware interface and synchronized with respect to a clock signal of $2MHz$, which controls the operation of a Finite State Machine (FSM) for the pulse generation.
The stimulation pulse is generated by the hardware interface with the following operations: first, the representation of the positive I_{st} is written on a defined internal register of the custom designed IC, then the negative value is stored in the register and, finally, a recovery period with 0 current is obtain by making a reset write operation. During the recovery period, the operation state of the custom designed IC can be changed to *STREAMING* state in order to continue to acquire samples from the recording system.
Due to the MicroBlaze code size, it is necessary to link code and data of the application to the DDR SDRAM, characterized by a greater capacity. Moreover, it is possible to create a bootloader and to store it on the FLASH memory of the FPGA, this makes possible to load the MicroBlaze code and data on the DDR SDRAM at the power-up state and to configure the FPGA. This feature is particularly useful because allows the user to utilize the system even without installing on the PC the *Xilinx* tool chain. In this way, the PC should have only *MATLAB* application for the communication with the processor and, indirectly, with the custom designed IC.

2.6.2 Laboratory measurement results

The first tests of the chip were aimed to verify its proper functioning from an electrical point of view. The test signals were generated by the two DAC (*LTC2641* component) collocated in the control board described in Section 2.6.1. The system is provided with two output test points used to monitor the system behavior, a switch network inside the chip allows to select which intermediate output connect to the test points. By this way it is possible to see the signal at the HPF, LPF, first, second and third modulator stage output. The signals were acquired using the *MSO6054A* oscilloscope from *Agilent technologies* as shown in Fig. 2.33.

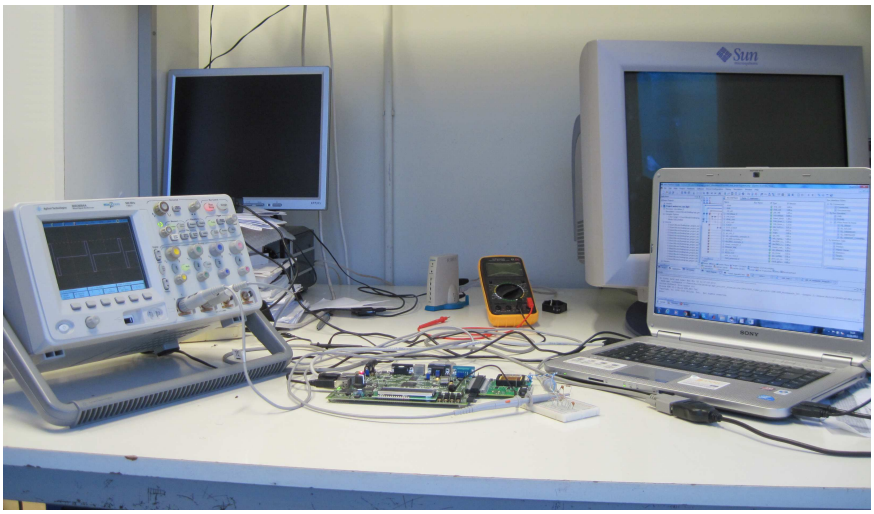


Figure 2.33: Measurement setup.

Recording analog front-end test

The filters parameters, the gain and the frequency bandwidth, were verified setting a differential sinusoidal signal at different frequencies at the filter input. The chosen frequency range is $[100Hz - 80kHz]$ which is enough to test the $[800Hz - 8kHz]$ BPF. In Fig. 2.34 and Fig. 2.35 the results respectively obtained for the HPF and the LPF are reported. In Fig. 2.34 it can be noted that the frequency response starts dropping for frequencies higher than $10kHz$, this is due to effect of the OpAmp pole.

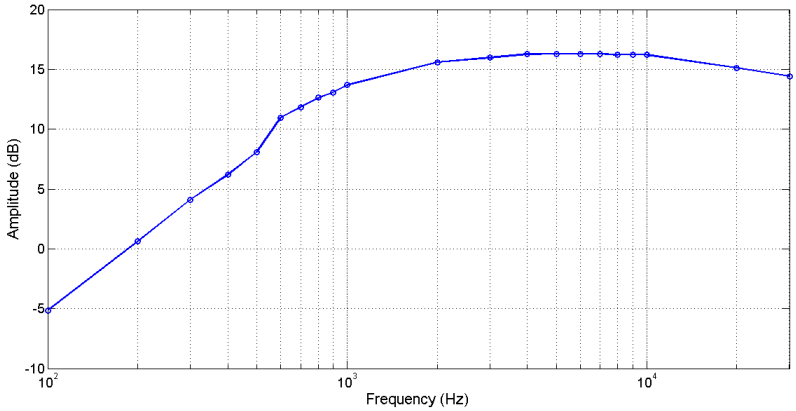


Figure 2.34: HPF Bode diagram.

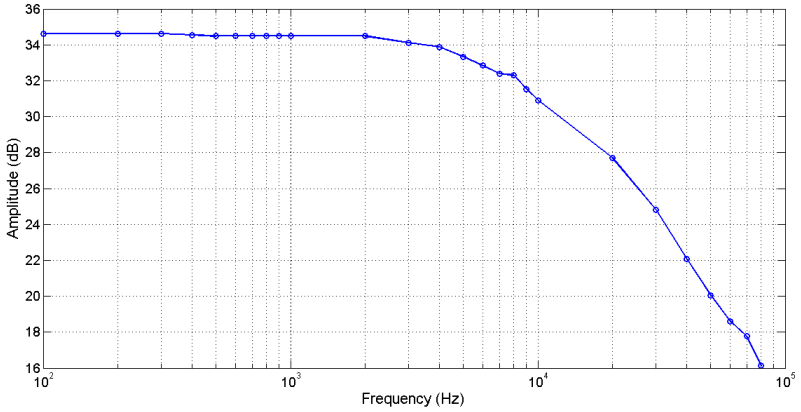


Figure 2.35: LPF Bode diagram.

The values of gain and cut off frequencies for the HPF and for the BPF are resumed in Table 2.12. Then, the frequency response of the whole analog $1st$ order BPF has been verified. Fig. 2.36 shows the results, the blue curve was obtained with the lowest gain while the red one with the highest gain configuration. The filter parameters, in terms of gain and bandwidth for the maximum and the minimum gain configuration, are reported in Table 2.13.

With respect to the simulation result we have a lower gain in the high gain configuration, the values match those obtained with post-layout simulation. The differences from the simulated results can thus be justified as a consequence of the parasitic effect in the layout.

	GAIN [dB]	CUT OFF FREQUENCY [kHz]
HPF	16.3	0.9
LPF	34.4	10

Table 2.12: HPF and LPF parameters.

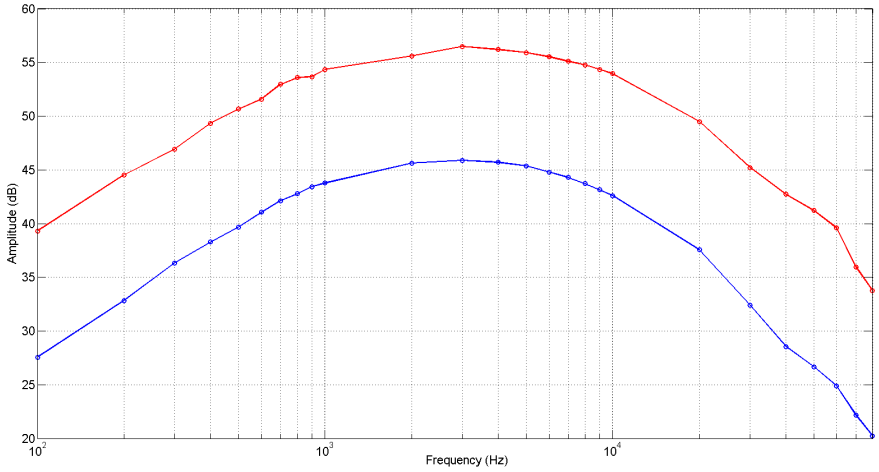


Figure 2.36: BPF Bode diagram. Red curve: higher gain configuration, blue curve: lower gain configuration.

Moreover, it should be clear that, even though there is a slight difference with respect to the design specification ([$800Hz-8kHz$]) it does not represent a problem since the out-of-band frequencies will be completely rejected by the high selective BPF of the digital decimator stage.

	GAIN [dB]	BANDWIDTH [kHz]
High gain	56.5	0.8 – 11
Low gain	45.9	0.8 – 9.5

Table 2.13: BPF parameters.

Fig. 2.37 demonstrates the possibility to program the gain of the pre-filter: the traces were obtained stimulating the chip with a fully-differential sinusoidal signal with a $280\mu Vpp$ amplitude at $3kHz$. The weak amplitude has been obtained thanks to the attenuator cascaded to the DACs. The DACs generate a $28mVpp$ signal that, attenuated by a factor of 100, gives the desired input signal. The result has been achieved with five possible gain configurations; nevertheless, the gain can be configured with a total of 256 values between the minimum and the maximum values.

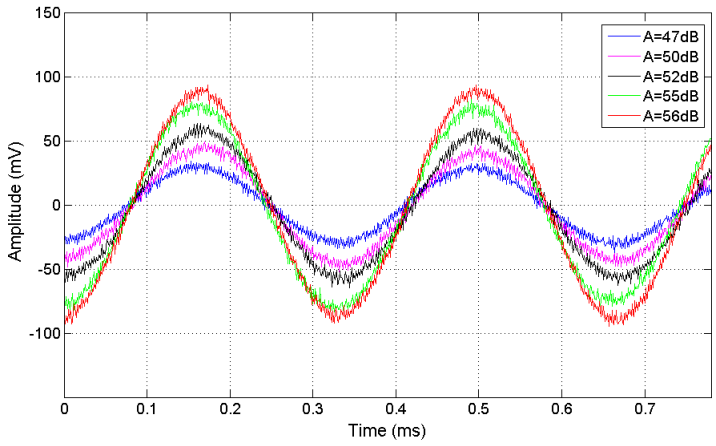


Figure 2.37: BPF: gain programmability.

ΣΔ modulator test

The bit stream generated by the sigma delta modulator is acquired, by means of a SPI interface, by the digital system implemented in the *Xilinx Spartan 3E 1660E* prototyping board. The serial signal is the interlaced results of the eight channels. The decoded bit stream for a single channel is shown in Fig. 2.39a, the signal has been obtained with a input sinusoidal signal with a $0.5V@5kHz$. The analog bandpass filter has been bypassed (thanks to a switch network embedded in the chip), and the sine has been sent directly to the modulator input.The resulting Power Spectral Density (PSD) is reported in Fig. 2.39b and confirms a predominant signal component at $5kHz$. For an input signal with this amplitude the signal to noise ratio is $59.6dB$, corresponding to a Effective Number Of Bits (ENOB) of $9.6bit$ that can be considered the real resolution of the developed converter. The plot shows also the noise shaping effect generated by the ΣΔ modulator. This high frequency noise, as well as the low frequency interferences, will be removed by the sharp digital decimator filter.
The ΣΔ modulator output signal of Fig. 2.39a, is an oversampled $1-bit$ stream. The original

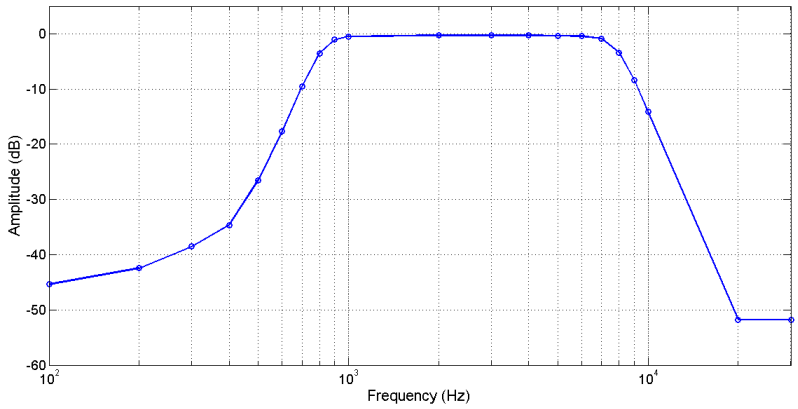
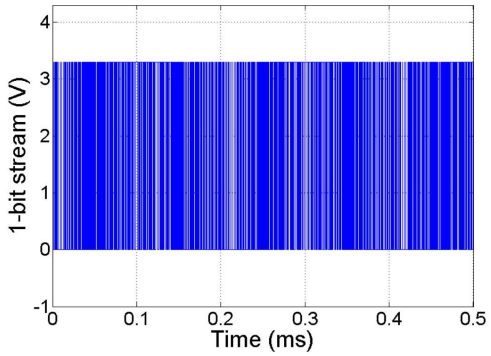


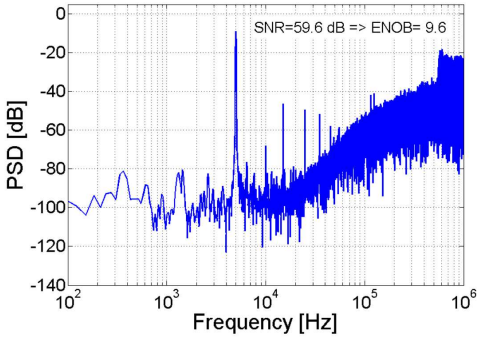
Figure 2.38: Frequency response of the 16^{th} order digital BPF.

signal can be reconstructed by filtering the stream and downsampling it to obtain a Nyquist

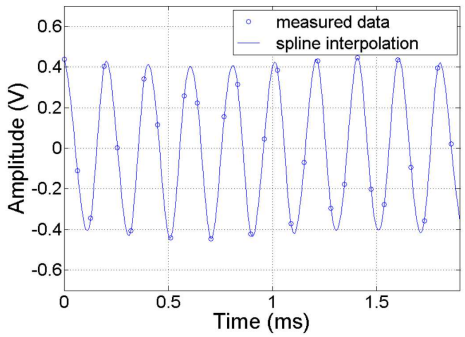
rate sampled signal. In our case a band pass filter has been used, in this way it is possible to reject both the low frequency biologic interferences (EMG - ECG signals) and the high frequency quantization noise. The $16th$ order digital BPF frequency response is represented in Fig. 2.38. It can be noticed the filter sharpness that allows to deeply attenuate all the out-of-band interferences, a $200Hz$ signal, for instance, that is a frequency in the EMG range, will be attenuated by more than $100V/V$.
The digital filter output is reported in Fig. 2.39c and Fig. 2.39d, respectively in the time and in the frequency domain. The digital decimator brought back the sample frequency to the Nyquist rate, the sine is thus sampled at $16kHz$. Therefore, it has only about 3 samples for each period, for that reason in Fig. 2.39c the spline interpolation of the measured samples has also been reported. The $5kHz$ input signal has been converted in a digital signal with a SNR of about $60dB$ as it can be observed in Fig. 2.39d.



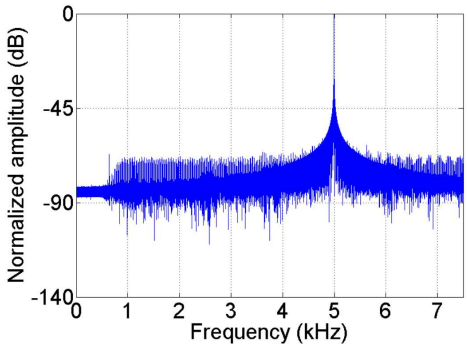
(a) Time domain: bit-stream.



(b) Frequency domain: Power Spectral Density.



(c) Time domain: digital decimator output.



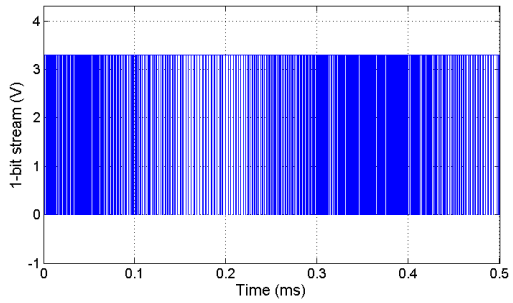
(d) Frequency domain: digital decimator output.

Figure 2.39: Results at the modulator and at the decimator output with a sinusoidal input with $0.5V$ in amplitude at $5kHz$.

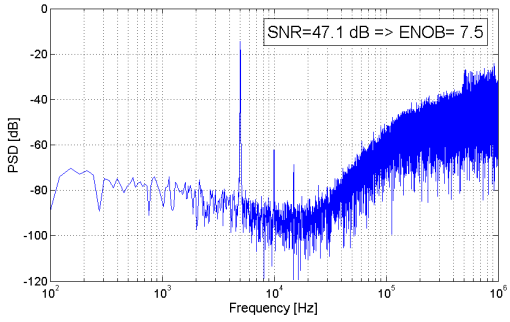
The full recoding chain test

In this subsection, the results obtained using all that recording chain (i.e. the analog filter, the $\Sigma\Delta$ modulator and the digital decimator filter) are presented. The signals depicted in Fig. 2.40a and Fig. 2.40b represent the modulator output, respectively in the time and in the frequency domain, in response to an input sinusoidal signal with a $3.6mVpp@5kHz$. First, the sine is amplified by the analog filter configured in low gain mode, the modulator

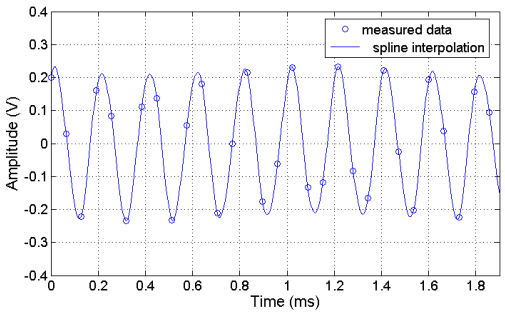
input has thus a $667mVpp$ amplitude. The PSD of Fig. 2.40b shows that, for an input signal



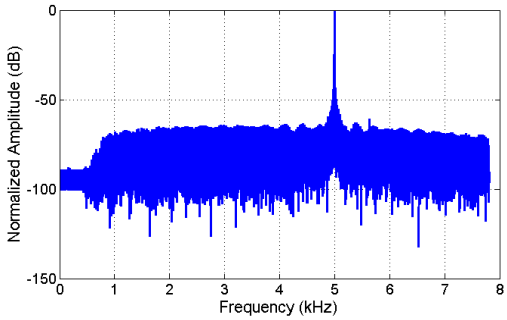
(a) Time domain: bit-stream.



(b) Frequency domain: Power Spectral Density.



(c) Time domain: digital decimator output.



(d) Frequency domain: digital decimator output.

Figure 2.40: Results at the whole recording chain output with a sinusoidal input with $0.5V$ in amplitude at $5kHz$.

with such amplitude, the signal to noise ratio is $47.1dB$, corresponding to a Effective Number Of Bits (ENOB) of $7.5bits$. The filter output signals have been reported in Fig. 2.40c (time domain) and Fig. 2.40d (frequency domain), from both plot it is clear how the input signal has been correctly reconstructed. As in the previous case, a spline interpolation has been reported together with the real samples, just to facilitate the waveform understanding. Looking at the underlying noise in Fig. 2.40d, it is possible to see the filter shape that confirms the $[800Hz - 8kHz]$ bandwidth.
The relation between the signal amplitude (referred to the analog filter input) and the SNR calculated from the PSD at the modulator output has also been evaluated. The result is shown in Fig. 2.41, a typical $\Sigma\Delta$ characteristic has been obtained, the SNR increases with the increasing of the input amplitude up to a threshold (in this case $3.6mV$ referred to the input) corresponding to about half the reference voltage at the modulator input. For higher amplitudes the signal saturates and the corresponding SNR starts to drop.

Since the system has been designed to work with neural signals, it has been also tested the capabilities of the whole recording chain to work with amplitudes in the order of tens of microvolts. A $18\mu V$ signal at $3kHz$ has been generated as input signal (the attenuator cascaded after the two DACs has been used for this purpose). In Fig. 2.42a, the time $1-bit$ stream is reported, while Fig. 2.42b presents its PSD, even though such signal is particularly weak it is still detectable. This is even more evident if the output of the digital filter is analysed: Fig. 2.42c shows the acquired signal in the time domain, the result has been obtained

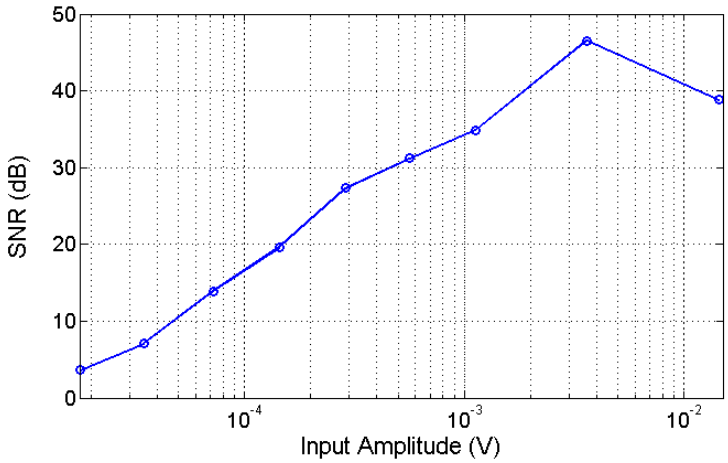
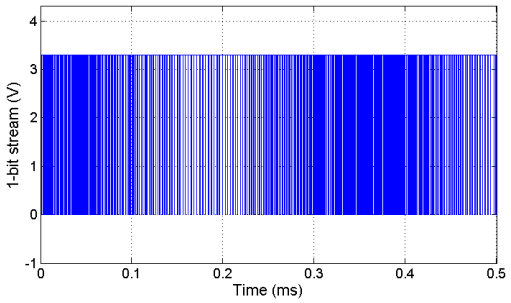
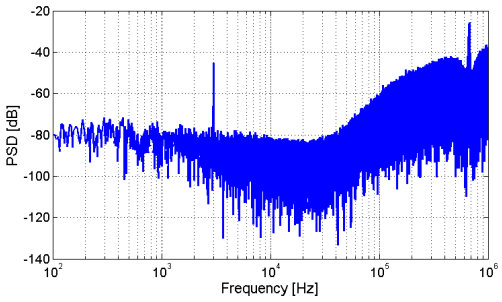


Figure 2.41: SNR vs. Input Amplitude.

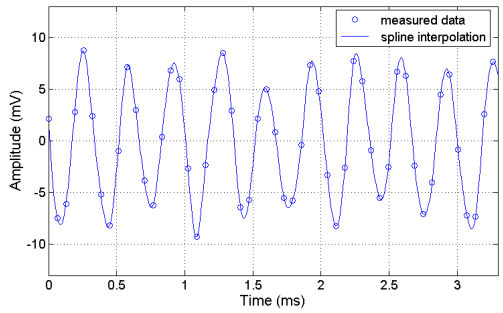
using the higher gain configuration for the analog bandpass pre-filter in order to amplify the weak signal as much as possible before the digital conversion. The frequency spectrum, reported in Fig. 2.42c confirms this result, showing a peak signal at $3kHz$ as expected. Looking at the underlying noise shape in Fig. 2.42c, it is evident how the interferences below $800Hz$ are deeply attenuated.



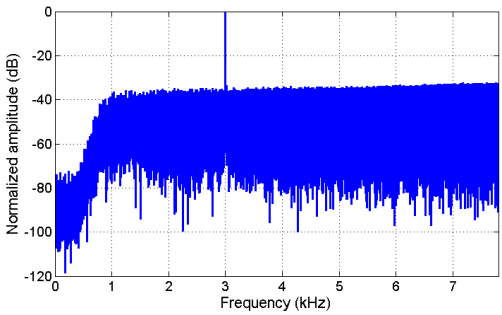
(a) Time domain: bit-stream.



(b) Frequency domain: Power Spectral Density.



(c) Time domain: digital decimator output.

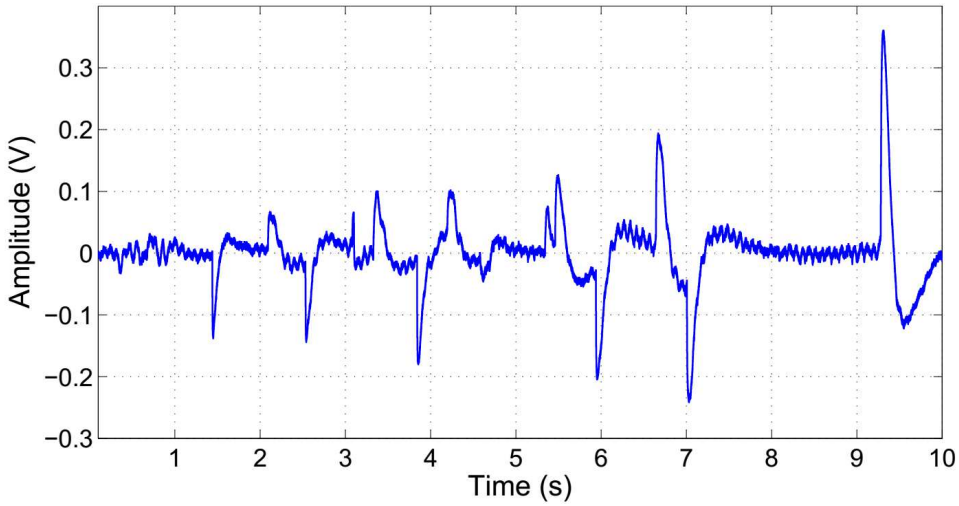


(d) Frequency domain: digital decimator output.

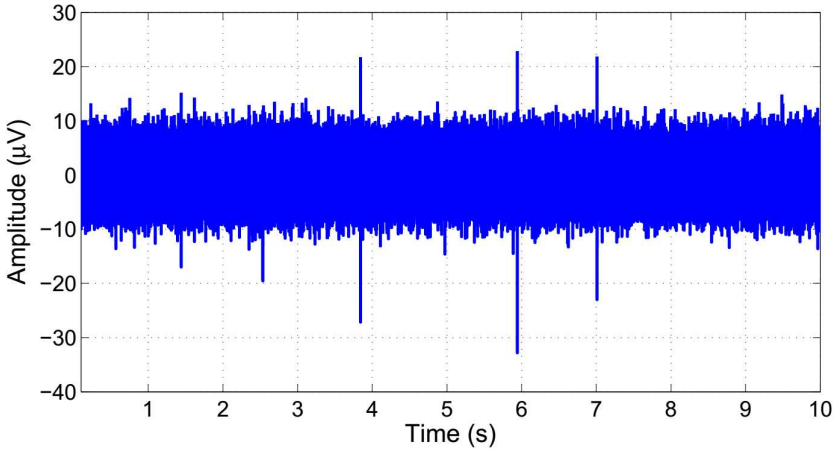
Figure 2.42: Recording system results in high-gain configuration with an input signal of $18\mu V$ at $3kHz$.

Finally, the system has been tested with a pre-recorded neural signal acquired during

previous clinical trials with rabbits. The animal was subjected to vibrations at $50Hz$ and $100Hz$ in cutaneous afferent fibers for 10 seconds. The results show how the system is capable of rejecting the huge low noise components visible in the input signal (Fig. 2.43a) and to highlight the neural spikes (Fig. 2.43b).



(a) Input signal.



(b) Output signal.

Figure 2.43: Pre-recorded neural signal processed by the recording module.

Low-voltage stimulator test

The stimulation module has been tested using the system presented in Section 2.6.1 that permits to generate biphasic pulse trains with variable current, pulse width and period. A $10k\Omega$ resistance connected between the input pin and the reference voltage was used to emulate the impedance introduced by the target neural electrodes. Fig.2.44 shows the possibility to

vary the current amplitude which, considering this output impedance, can range from $20\mu A$ to $100\mu A$. Higher currents can be achieved with lower impedances.

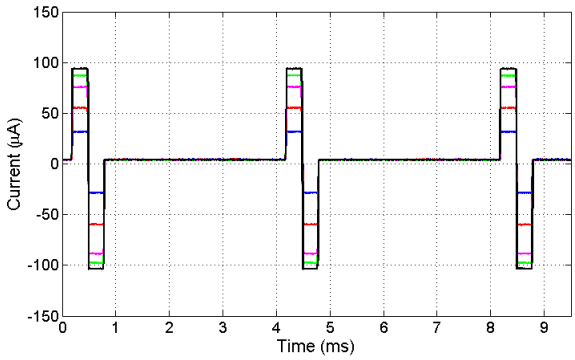
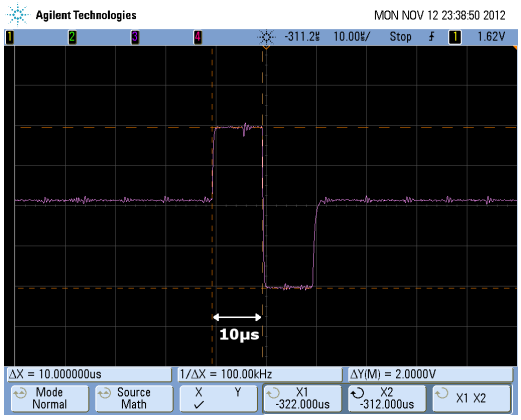
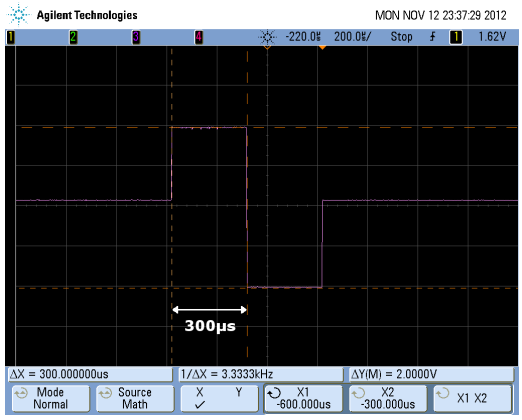


Figure 2.44: Stimulation current amplitude programmability.

Fig. 2.45a and Fig. 2.45b show how it is possible to change the pulse width W, in fact it can be programmed in a range from $10\mu s$ to $300\mu s$. The signals depicted in the figures have been acquired with the oscilloscope and they therefore represent the voltage signal drops across the equivalent input resistance connected at the electrode terminals. To obtain the corresponding current, the signals should be divided for the $10k$âĎę resistance value.



(a) Pulse width $W = 10\mu s$.



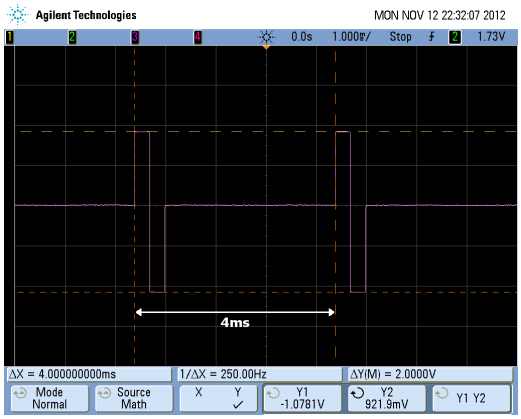
(b) Pulse width $W = 300\mu s$.

Figure 2.45: Stimulation biphasic pulses varying the relative phase width.

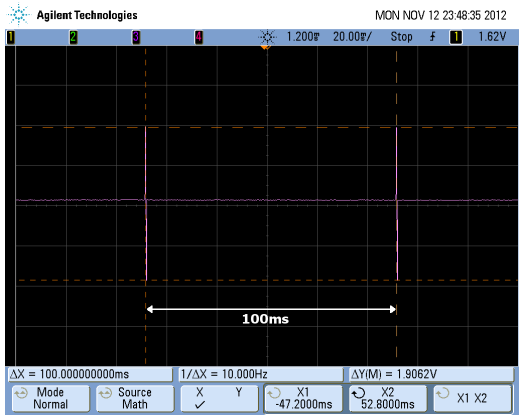
The possibility to change the biphasic pulse period T has also been provided, it can span from a minimum of $4ms$ to a maximum of $100ms$. Fig. 2.46a and Fig. 2.46b confirm the proper functionality of the stimulator also in this case.

2.6.3 In-vivo experiment results

The in-vivo measurements have been performed on sedated rats at the Ecole Polytechnique Federale de Lausanne (EPFL) (Switzerland). An eight-channels TIME (Transverse Intra-fascicular Multi-channel Electrode) was chronically implanted in the sciatic nerve of the animal. All



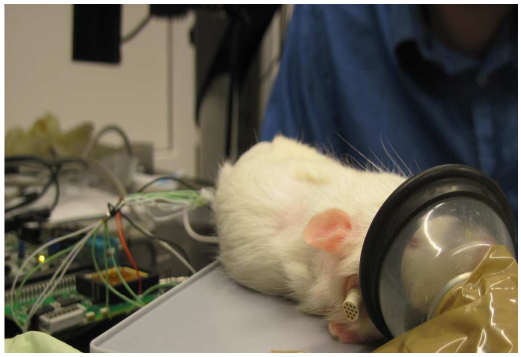
(a) Train period $D = 4ms$.



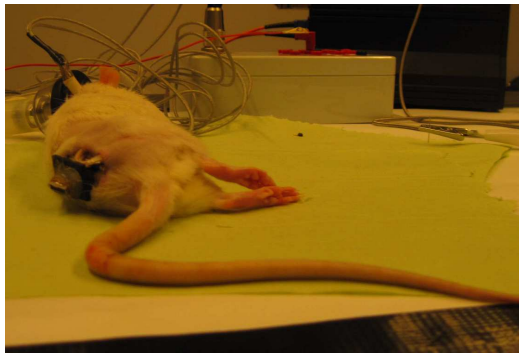
(b) Train period $D = 100ms$.

Figure 2.46: Stimulation biphasic pulses varying the relative period.

processes were performed using a protocol approved by the local Ethical Committee. The tests were performed after a month from the electrode implantation, therefore the results should be considered highly representative of what can be obtained in a long-term implant, when the electrode-tissue interface is already degraded. In Fig. 2.47 two pictures of the experimental set-up with the chip connected to the neural electrode chronically implanted in the rat is shown.



(a) Experimental set-up.



(b) Chronic TIME implantation.

Figure 2.47: In-vivo tests at the EPFL laboratories.

During the tests the hind pow of the animal has been subjected to flexo-extensor movements. The results, concerning seven different channels, have been reported in Fig. 2.48.

The presence of neural spikes with amplitudes of few tens of microvolts is evident as well as the correlation between the near channels. The test successfully confirms the system capabilities of recording neural signals with an input referred noise of less than $10\mu Vpp$. Fig. 2.49 shows a single spike recorded with the proposed system. As expected for a neural signal, it is characterized by an amplitude of about one hundred of μV and a duration of $300ns$.

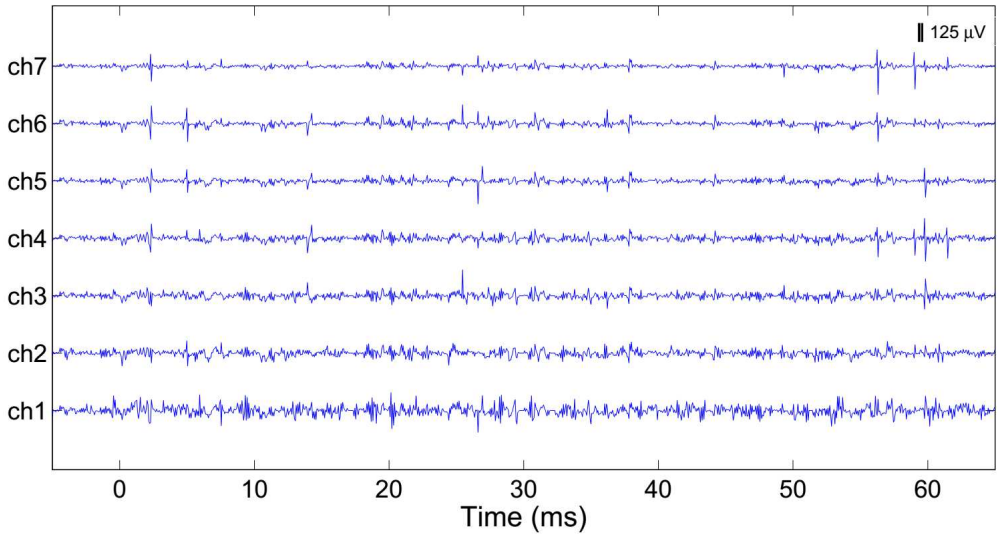


Figure 2.48: In-vivo recording results with seven channels.

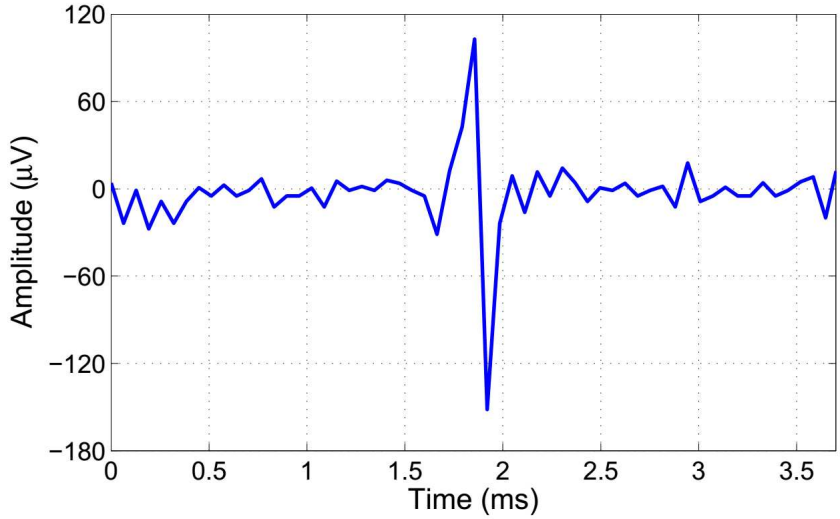


Figure 2.49: In-vivo recording results: zoom on a single spike.

2.7 Results discussion

The proposed IC for neural signal recording embeds both the front-end amplifier and the sigma-delta modulator on chip, therefore the signal provided to the external is a robust digital signal with high immunity to noise and that grants an Equivalent Number Of Bit (ENOB) of 10.9 bit. This fact is a significant advantage over works [148] and [46] that do not include the ADC and over [153] and [9] which use respectively an ADC from a cell library of the used technology and a 8-bit converter. The drawback is an increase in power consumption, that is slightly higher than in the other works. This is mainly due to the eight delta-sigma modulators, that are based on switched capacitor circuits that work with a $2MHz$ sampling frequency and require, therefore, OTAs with larger bandwidth and consequently higher bias

currents. Nevertheless, comparing the pre-amplifier circuits of a single channel in low-gain mode, the power consumption is considerably lower than almost all the other papers, with the exception of [9], in which the power has been optimized and reduced to $0.3mW$. Nevertheless, in such paper the corresponding noise has not been reported and, therefore, it is not possible to evaluate the impact on the IRN. The power scales with $1/v_n^2$ where v_n is the IRN [198]; power optimization, therefore, leads to the increase of noise levels. Since the background noise due to the electrode and to the spontaneous neural activity is about $10\mu V$ [9], the electronic noise of $1.8\mu V_{rms}$ is perfectly acceptable and allows to save power with respect to [153, 46, 148] that present excellent results in terms of noise but with a relative higher power consumption. Moreover, the bandpass high selective filter ($\Sigma-\Delta$ decimation filter) is provided by the digital part of the system implemented along with the digital system controller in a *Xilinx Virtex 5 LX330 FPGA*. The in-vivo tests on the embedded low voltage stimulator highlighted that poor capability of the system to activate action potentials in the peripheral nervous fibers due to the high impedance of the electrode-tissue interface. For this reason the high voltage neural stimulator, presented in the next chapter, had been realized.

Chapter 3

Peripheral nerve stimulation module: design and test

After a brief introduction on the state-of-the-art of neural stimulation circuitries, an integrated neural stimulator for prosthetic applications, realized with a High Voltage (HV) CMOS 0.35μm process, is presented in this chapter. The device is able to provide biphasic current pulses to stimulate 8 electrodes independently. A voltage booster generates a 17V voltage supply in order to guarantee the programmed stimulation current even in case of high impedances at the electrode-tissue interface. Pulse parameters such as amplitude, frequency and width can be programmed digitally. The device has been successfully tested by means of both electrical and *in-vivo* tests and the results show its capability to provide currents in the order of hundreds of μA with impedances in the order of tens of $k\Omega$.

3.1 State of the art

Neural electrical stimulation has been widely used in the latest years in different biomedical applications, from cochlear implants to neurological disorders treatment [130]. In neural prosthetics, the stimulator is needed to provide sensory feedback to the patient, who will have thus more chances to feel the robotic limb as a natural extension of his/her body. The work presented in this chapter belongs to this latter field and proposes an integrated neural stimulator aimed to restore the sensory feedback in patients with upper limb amputation.
In Section 1.4.2, the main implementation issues related to the neural stimulation were discussed. Depending on the specific application several strategies to solve or to partially overcome some of the mentioned problems have been developed over the years. In fact, different ways to generate and to transfer stimulation patterns to the tissue are available and an overview of the state of the art of the main blocks contained in a neural stimulator is presented in the next paragraphs. In particular, the most diffused architectures of the voltage booster, the output stage and the current pulse generator are detailed. Finally, the main features of some of the state-of-the-art neural stimulator are collected in Table 3.1.

3.1.1 DC-DC booster converter

An important issue concerning the tissue stimulation, presented in Section 1.4.2, is the high variability of electrode-tissue impedance whose value depends on the electrode placement inside the nerve and varies in the range $10k\Omega - 1M\Omega$ [39] from electrode to electrode and during the lifetime of the implant. Therefore, the reproducibility of the current stimuli requires the use of a high voltage supply which is not always possible for low power implantable devices. Therefore, a DC-DC booster converter (or step-up) is essential to generate a voltage higher than the nominal supply retrieved from the power source. Despite different classes of DC-DC converter exist, only switching converters may provide an output greater than the input voltage. Several high-voltage-compliant neural stimulators can be found in literature such as those presented in [201, 206, 78, 124, 102, 123, 147, 13]. The switching DC-DC converters are divided into two types depending on how the conversion is performed: magnetic and capacitive converters. Since the on-chip inductors occupy a large area and, often, have a limited quality factor, only DC-DC switched-capacitor converters, also called charge pumps, are considered in this work.
The first voltage booster circuit was introduced by Cockcroft and Walton in the late 1932. It is composed of a voltage multiplier ladder network of capacitors and diodes to generate high DC voltages from a low voltage AC or pulsing DC. A new architecture, to improve its conversion efficiency and its output impedance, was developed in 1976 by Dickson [47]. It is a series of diodes with a capacitor connected at each node, properly controlled by two clock signals ($\Phi, \overline{\Phi}$) with opposed phases as depicted in Fig. 3.1. In particular, the diodes were implemented with diode-connected NMOS (i.e. the NMOS gate is shorted to its drain). This architecture is the base for the majority of today's charge pumps. When the clock Φ is high

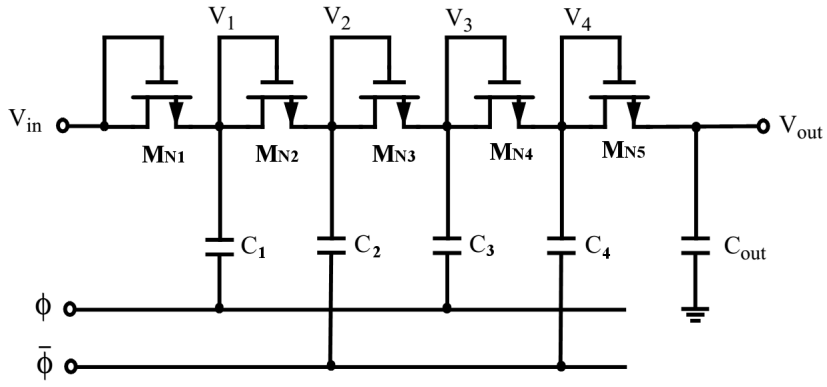


Figure 3.1: A 4 stages Dickson charge pump.

($\Phi = V_\Phi$) and, therefore, $\overline{\Phi}$ is low ($\overline{\Phi} = 0$), the voltage at the opposite terminal of odd capacitors (in this case V_1 and V_2) is increased of a V_Φ. At this time, the even transistors (M_{N2i}) are on and transfer the charge from one node to the next one whereas the odd transistors (M_{N2i+1}) are off. In the next cycle ($\Phi = 0, \overline{\Phi} = V_\Phi$), it happens the opposite: the odd transistors lead the charge whereas the even ones are off and so on. The result is a continuous moving of charge from the input to the output of the chain. Moreover, between each stage, there is a theoretical voltage increase of $V_\Phi - V_{th}$, in which V_{th} is the NMOS threshold voltage. Taking into account the parasitic capacitance C_p between each stage and the output current

I_{out} dissipated by the load, the output voltage can be computed as in Eq. 3.1.

$$V_{out} = V_{in} + N \cdot \left(\frac{C}{C + C_p} \cdot V_\Phi - V_{th} - \frac{I_{out}}{(C + C_p) \cdot f_{osc}} \right) - V_{th} \tag{3.1}$$

where N is the number of stages, f_{osc} is the clocks frequency and C is the C_i capacitance [140]. Then, the Eq. 3.2 can be used to compute the voltage gain A_V of a single booster cell.

$$A_V = \Delta V - V_{th} = \frac{C}{C + C_p} \cdot V_\Phi - \frac{I_{out}}{(C + C_p) \cdot f_{osc}} - V_{th} \tag{3.2}$$

However, due to the CMOS supply voltage scaling, the V_Φ decreases and, according to Eq. 3.2, the same happens to the pumping gain A_V. In addition, due to the body effect, V_{th} increases as the voltage at a given stage is increased, which means that the single stage gain A_{V_i} decreases with N. Thus, it is obvious that the Dickson charge pump is not at all suitable for low voltage operation. To overcome these problems, several changes to the charge pump architecture have been proposed over time. In [205], an improvement to the Dickson charge pump is proposed by cancelling the A_{V_i} reliance on the V_{th}. Its architecture, commonly referred as *NCP-2* (New Charge Pump - 2), with four stages is depicted in Fig. 3.2. This circuit, with slight changes at the output stage, was used by Nadeau et al to imple-

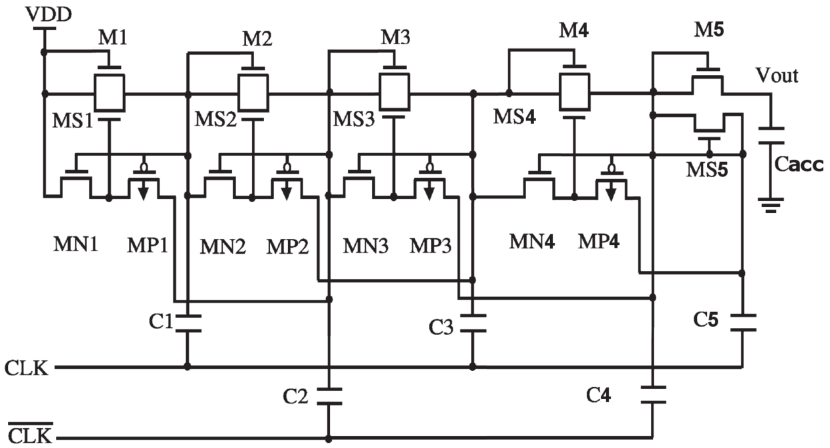


Figure 3.2: A four stages NCP-2 booster by [205].

ment a peripheral nerve stimulator described in [122]. Another technique to improve the load charge transfer of Dickson architecture is the dynamic control of the substrate voltage of diode connected MOS transistors, proposed by Shin et al in [167]. As shown in Fig. 3.3, the NMOS transistors have been replaced by PMOS which are isolated from the substrate in the N-type wells. The bias voltage of the wells is dynamically controlled by the other two transistors according to the cycle, significantly reducing the V_{th} reliance on the body effect and improving the voltage increase at each stage of the charge pump. It can be noticed that in the architectures presented so far, the output stage delivers the charge to the load only for a half-cycle. To maximize the effectiveness of the voltage conversion, an implementation with two independent paths whose clocks are inverted has been presented in [135]. In this way, the output stage receives the charge in each half cycle, ensuring a shorter rise time and supporting larger output currents. Pelliconi et al presented in [137] a new architecture that is

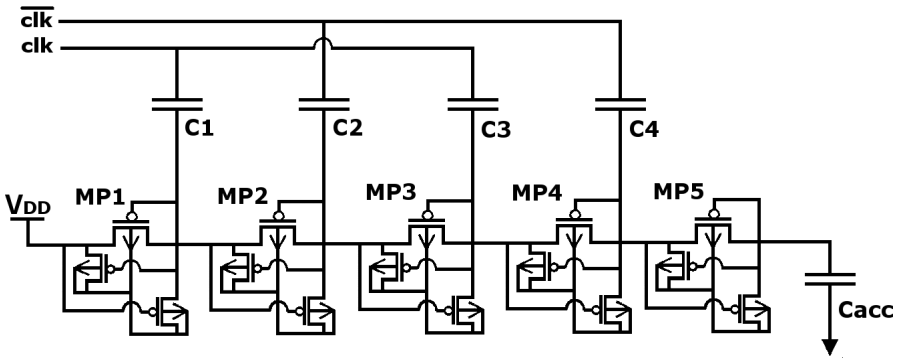


Figure 3.3: A four stages booster with dynamic substrate polarization, [167].

not directly derived from the Dickson charge pump. Each stage, depicted in Fig. 3.4, consists of two NMOS and two PMOS connected to create two paths controlled by two clock phases, maximizing the charge transferred per cycle. Moreover, since charge pump circuits are of-

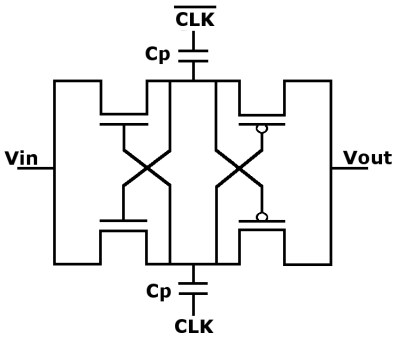


Figure 3.4: One stage of the Pelliconi charge pump described in [137].

ten implemented with high voltage transistor characterized by a thick gate-oxide, a common strategy in voltage booster design is to double the clock amplitude in order to better activate the transistors and to increase the voltage gain at each stage. An example of clock doubler circuit, introduced by Huang et al in [77], is depicted in Fig. 3.5. Several works which implement this kind of circuits are described in literature, such as those presented in [207, 38]. Another possible charge pump architecture introduced by Saiz et al is the Two-Phase Voltage Doubler (TPVD) whose boosting cell is depicted in Fig. 3.6. It consists of four switching transistors ($M0-M3$), a flying capacitor Cp and a load capacitor CL ([155]). At least two different switching stages are needed in order to make the TPVD circuits working. The main drawback of this architecture is that it cannot produce negative voltages. The main problem related to the negative voltage boosters is the need to produce voltages that are lower than the one of the substrate. To overcome this limitation, a triple-well technology which supports multiple supply voltages has to be adopted. The majority of the presented architectures supports the generation of negative voltage virtually unchanged. Usually, it sufficient to reverse the input and the output of the DC-DC converter that means to connect the output to ground and the input to the load capacity. The direction of the charge flow is unchanged, therefore the charge is pumped into the ground and a negative voltage is generated at the input capacitance. However, some precautions must be taken when drawing the layout to avoid short circuits and triggering of parasitic thyristors (latch-up)([21, 207]).

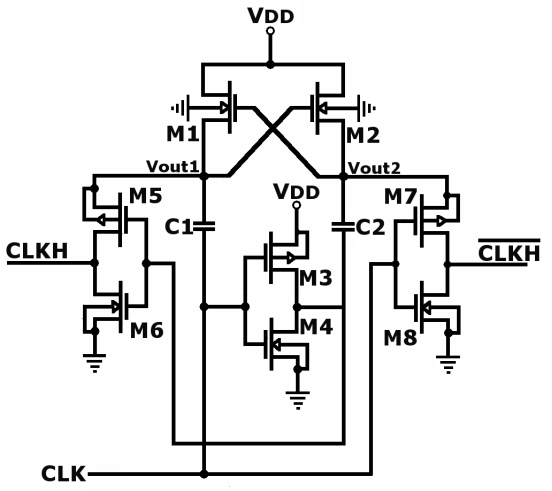


Figure 3.5: Clock doubler introduced by Huang et al in [77].

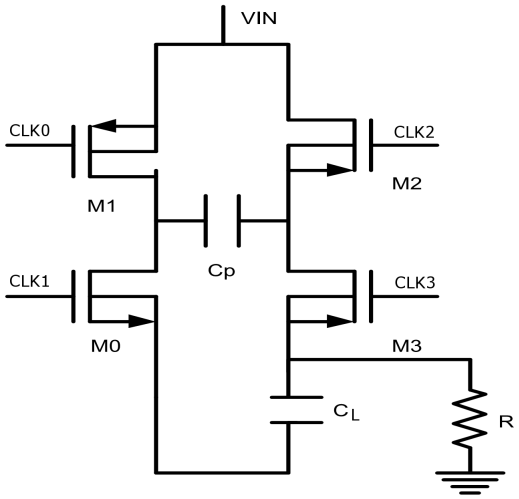


Figure 3.6: One boosting cell of the TPVD charge pump from Saiz et al, [155].

Following the listing of various charge pump architectures, a summary is required to be able to compare them. The requirements to be met in order to properly evaluate the performance of a DC-DC converter include among others the output voltage, the current that can be delivered to the load, the efficiency of conversion, the occupied silicon area and the complexity of the circuitry. These results depend on a multitude of parameters including the manufacturing process used, the voltage supply, the number of stages, the clock frequency, the pumping and output capacitors. A fair comparison is not feasible in practice, because each of the circuits described above has been implemented in the context of its own to achieve a specific goal. We must therefore consider the various parameters and the overall results to make a comparison. All the charge pumps mentioned above generates only positive voltage with the exception of the *Pelliconi* charge pump. It can generate negative voltages but it suffers from latch-up issue which hugely decrease the chip performances. For what concern the Dickson charge pump, the NCP-2 and the substrate dynamic polarization architectures, the output stage receives the charge during only half of the clock period. Moreover, the effect of V_{th} causes a significant drop of the output voltage and a consequent loss of the single cell

gain. These problems, with the exception of the V_{th} effect, have been solved by introducing the dual path charge pump that, however, is characterized by an increase of the circuit complexity and by a reduction of the booting performance by increasing the number of stages.

3.1.2 Output stage

In neural stimulator the output stage is the unit that is directly connected to the tissue to deliver a certain amount of electrical energy for either activating or deactivating particular areas of the brain. As introduced at the beginning of Section 3.1, different ways to inject or sink the electrical energy to/from the tissue are available and each of them is functional for a specific application. As discussed in Section 1.3.1, the electrode tissue interface can be modelled by an RC network (Fig. 1.12). In order to "communicate" with the tissue, the stimulator charges the (non ideal) capacitance with a consequent change of the voltage in the tissue. When enough charge is delivered, the potential in the tissue reaches a certain threshold voltage, leading to (de)activation of the neural cells. This means that what it is important in the stimulation is the delivered amount of charge and thereby controlling the charge during stimulation should be the best way to proceed. However, most traditional stimulators do not use charge as the output steering quantity, but they implement a constant voltage stimulation (CVS) or a constant current stimulation (CCS). In both approaches the objective is to transfer a given charge through the electrode. While the generation of voltage pulses can be very efficient in terms of power consumption, the actually delivered charge depends on the highly variable electrode-tissue interface impedance that typically increases due to reactive tissue response [138]. Therefore, it has poor performances in terms of amplitude resolution of the stimulus. On the contrary, with current-mode stimulation (for example [11, 90, 147, **?**]) the amount of delivered charge depends entirely on controllable parameters (injected current and duration of the pulse), thus it can be designed with excellent amplitude resolution and high safety for the patient [59]. A general architecture for current-mode stimulation is depicted in Fig. 3.7a whereas the counterpart voltage-controlled is depicted in Fig. 3.7b.
Note that, regardless of which technique is chosen, the absolute value of the output quantity

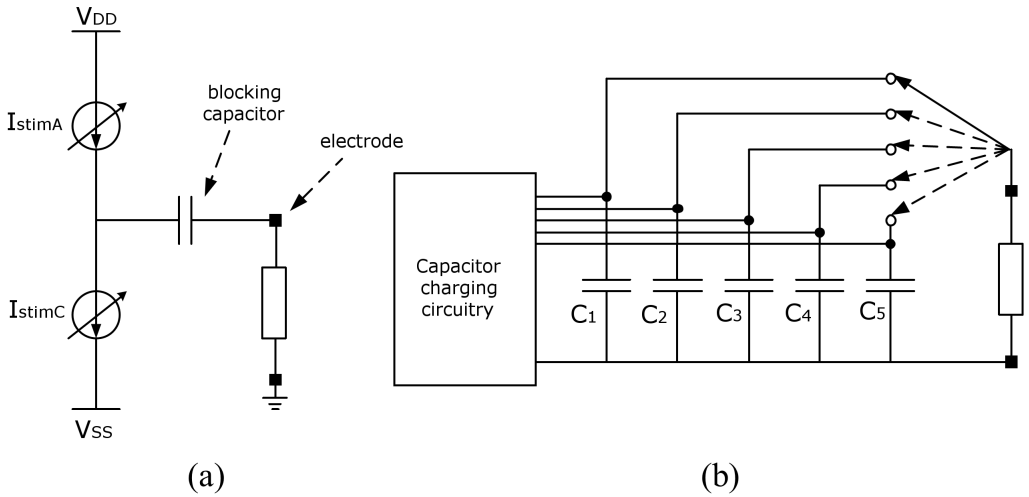


Figure 3.7: Possible stimulation architecture: (a) current-mode, (b) voltage-mode. From [98].

is not important. Since the electrode-tissue interface is very different from subject to subject

(due to the incorporation of the electrode in the body by means of connective tissue), the absolute value of the stimulation parameter is of no significance. The subject should only indicate if the stimulation must be stronger or weaker.
The choice of the stimulus waveform is another important issue to deal with when designing the output stage. It depends on the type of electrode employed as well as the intended physiological effect. In fact, several publications have shown that different types of applications need different stimulation waveforms in order to produce an optimum stimulation effect [63, 12, 27, 122, 119, 30]. Asymmetric biphasic pulses have been proven to limit channel interaction between adjacent stimulation sites [108, 109], and avoid new excitation during the discharge phase [132]. Studies conducted by [52, 181] found that the non-rectangular shape such as Gaussian, linear and exponential decrease could provide stronger stimulation effects. A recent study proved also that flexible stimulation such as step-down current pulse shape, could reduce the required electrode voltage by $10\% - 15\%$ [65]. The above shows the advantages of having flexible stimulation waveforms for different degrees of tissue degeneration and for maximizing the application range of the stimulator chip. Nowadays, the CCS is preferred and mostly uses symmetrical or asymmetrical, biphasic, cathodic-first current pulses [111]. This is because of the ease of the implementation [12, 27, 122, 206], and in order to achieve first order charge balanced stimulation. In the cathodic phase, the stimulus current depolarizes nearby axons and initiates the action potential. The succeeding anodic phase cancels the charge accumulated in the cathodic phase on the electrodes. Sometimes an inter-phase delay separates the two stimulation phases slightly so that the anodic phase does not block action potential propagation initiated by the cathodic phase. Usually the leading cathodic phase is active (with a programmed shape) while the following anodic phase can be either active (with a programmed shape) or passive (exponential decay). In active discharge phases the discharging current is fixed by the stimulator [206, 124, 45, 147], whereas in the passive discharge the capacitance is discharged through a resistive pathway [103, 99, 90, 101].
Fig. 3.8 shows the general architecture for implementing a stimulation with active cathodic phase followed by a passive anodic phase. The current *Istim* is injected from the anodic lead to the cathodic one by closing switches S_1, then, by opening these switches and closing S_2, the passive discharge is enabled. Whereas, in order to generate biphasic waveform with both active phases, a single or a dual voltage supply topology can be implemented as depicted in Fig. 3.9a and Fig. 3.9b. In the former, the driver circuitry reverses the current direction through the electrode and the tissue by interchanging the two electrode leads (closing/opening the switches S_2 in Fig. 3.9a) as presented in [206, 147, 102]. On the contrary, the dual voltage driver produces the biphasic stimulus by sourcing and sinking currents from/to one electrode lead that means, referring to Fig. 3.9b, by alternatively closing the switches S_1 and S_2. In this case one common ground electrode (the lead named C in Fig. 3.9b) acts as the return path for the stimulation currents through the tissue. Furthermore, as discussed in Section 1.4.2, in order to prevent electrolysis to happen at the electrode tissue interface, the net charge delivered to the tissue needs to be as close to zero as possible. As previously said, this is only partially assured by the use of a biphasic stimulation scheme. In fact, due to mismatches and non linearities, the second pulse will never cancel out the injected charge perfectly. Therefore, additional circuitry needs to be designed to assure enough charge cancellation. The easiest method to establish a zero charge injection is the one proposed in the diagrams of Fig. 3.9 in which a third switch S_3 was added to periodically (for example after each stimulation pattern) shortcircuit the electrode leads. For this reason, this technique

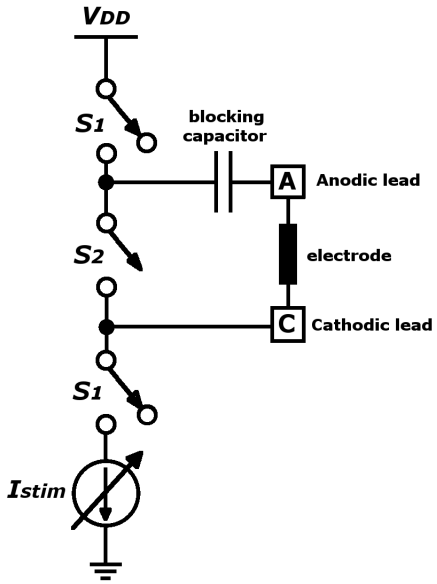
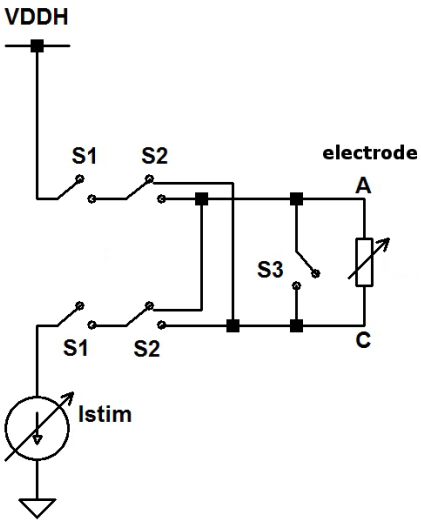
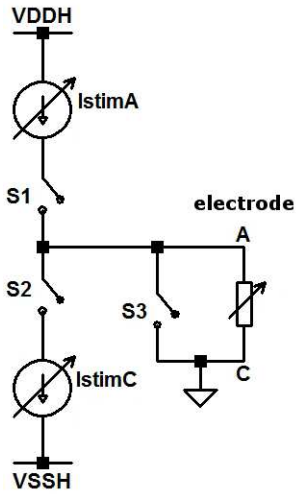


Figure 3.8: Stimulation architecture with a single supply, active cathodic phase and passive anodic phase.



(a) Single supply.



(b) Dual supplies.

Figure 3.9: Stimulation architecture with a single (a) or a dual (b) voltage supply characterized by both active phases.

is often referred as electrode shorting. During the shortening, the remaining charge on the electrodes gets a chance to leak away through the short. For N stimulation sites, the number of tissue-electrode interfaces required is $2N$ and $N+1$ in single-voltage and dual-voltage topologies respectively. In many prosthetic applications only a small amount of space is available, inside the body, for placing the electronic interface and, therefore, the device dimension is one of the major bottle-neck. So minimizing the number of electrode leads is essential. On the other hand, since increasing the number of stimulation sites directly im-

proves the quality of the prosthesis, the number of stimulation sites should be maximized for a given number of interface leads. For these reasons, in works such as [172, 40, 118], a dual-voltage architecture was chosen.
Independently from how the stimulation pattern is generated, a basic problem encountered in the clinical use of brain stimulators is the adaptive behaviour of brain tissue. In fact, the impulses given by the stimulator are an unnatural phenomena from the brain's perspective and, therefore, the brain will adapt itself in order to ignore the artificial pulses and neutralizing the possibility to give sensory feedbacks anymore. One way to solve this problem is to frequently change pulse shape, duration, intensity, repetition rate and other parameters, so it is harder for the tissue to adapt itself. Therefore the adjustability of the pulse parameters of the output stage is an important property. Moreover, besides the increased robustness against adaptation, the pulse parameter adjustability also determines the flexibility of the stimulator: the more parameters are adjustable, the more applications the stimulator will have and the more it can accommodate individual patients who may have different reactions to and perceptions of the injected pulses with the same configuration. In addition, the stimulation parameters rely also on the electrode implantation and can vary over the time due to changes in the quality of the electrode-tissue interface. In the following the most important pulse parameters and their influence are discussed. An overview of the pulse parameters denoted in an example pulse is given in Fig. 3.10.

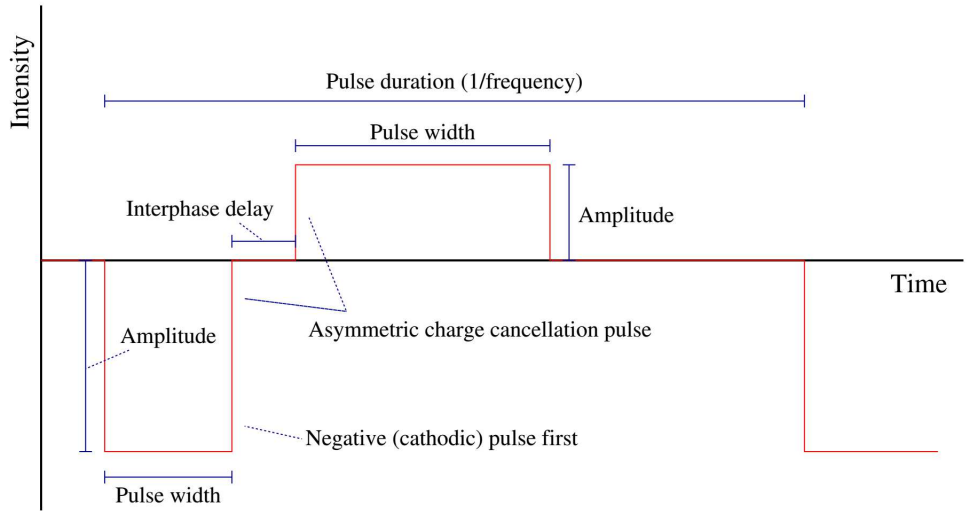


Figure 3.10: Main stimulation pulse parameters.

- **Amplitude and pulse width**: The combination of the amplitude and pulse width of the stimulation pulse determines the charge applied to the tissue ($Q = \int I dt$). The more charge is injected, the higher the tissue voltage will become and the more cells will be activated. Both the maximum amplitude and pulse width (the maximum injectable charge) and the resolution determine the applicability of the device. In terms of adaptation redundancy it is important to realize it is possible to vary the amplitude and pulse width, while still injecting the same charge into the tissue. This means that for different pulse shapes, still the same charge is injected, leading to the same tissue voltage.

- **Interphase delay**: It is defined as the delay between the first and second pulse in a biphasic stimulation pattern. A small delay between the two pulses is required to allow the tissue to react on the voltage change of the first stimulation pulse (due to the latency of the neural cells). The tissue must first be activated, before the tissue voltage can be lowered by the second charge cancellation pulse. The minimum delay time is set by the time it takes for the tissue to activate and the maximum time is defined by safety constraints: the maximum allowed time to keep charge on the tissue.

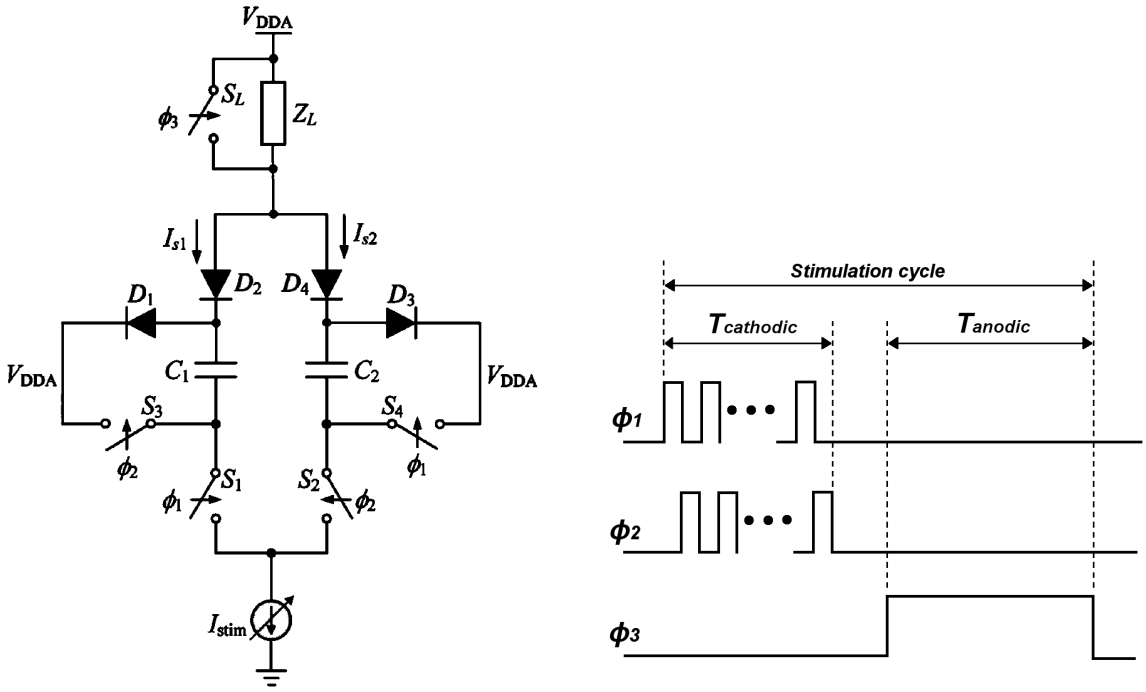
- **Frequency**: It is the repetition rate of the stimulation. Two types of frequency are distinguished: the burst frequency and the stimulation frequency. The former is the repetition rate of the pulses within the same pulse train (burst). Only after all the pulses of the train are sent the charge can be cancelled. Whereas, the stimulation frequency is the repetition rate of one complete stimulation pattern, including the charge cancellation pulse. The frequency applied in stimulation is mostly application specific: each application requires more or less a fixed frequency. Therefore the frequency cannot be changed in order to increase the adaptation robustness, but it determines the number of applications the stimulator can be used for.

- **Pulse sequence**: As was shown before the first pulse in a biphasic stimulation scheme is the pulse used to stimulate the tissue, while the second pulse is only used for charge cancellation. The polarity of the first pulse determines what kind of stimulation is used. In fact, using cathodic stimulation the voltage at the electrode is made more negative during the first stimulation pulse. In this case the cells are depolarized, yielding an activation mechanism. Cathodic stimulation is therefore used when a desired mechanism in the brains is absent or when a certain mechanism needs to be paced in a rhythm. Whereas, using anodic stimulation the voltage at the electrode is made more positive during the first stimulation pulse. In this case the cells are hyperpolarized, yielding deactivation. This type of stimulation is used if a certain activation of the brain needs to be suppressed.

- **Pulse symmetry**: When using a biphasic stimulation scheme, the second pulse does not need to have necessary the same shape as the first pulse. The only requirement is to inject the same amount of charge into the tissue, thereby the pulse area has to be the same. Reasons concerning minimizing the tissue damage or power consumption might lead to a different pulse shapes for the second pulse as for the first pulse.

Another important feature that the stimulator should include is the possibility to deliver sub threshold prepulses. They are low-amplitude pulses which are injected just before the "real" stimulation pulse. Using sub threshold prepulses, due to their low amplitude, only the nervous fibers nearby the stimulation electrode can be effected and thus slightly depolarized or hyperpolarized. Due to this deviation from their equilibrium, they will need a lower (de)polarizing pulse to be deactivated (activated). This means that due to this lower amplitude only cells more close to the electrode are (de)activated resulting in an increase of the stimulation selectivity inside the nerve.
The last aspect discussed in this dissertation with regard to the design of the output stage is the patient safety. As discussed in Section 1.4.2, it is one of the major issue in designing implantable devices that exchange electrical signals with the body. In case of neural stimulator, the danger is usually diminished and made acceptable by placing a capacitor (often referred

as blocking-capacitor) in series with each stimulating electrode. The blocking-capacitor limits the charge on the electrodes to $Q_{max} = C \cdot V$, where C is the capacitance and V is the stimulation voltage. Q_{max} should be chosen so that the charge density can not exceed the safety limit which depends on the electrode material. Typically, for functional electrical stimulation (FES) applications, these capacitors are in the order of a few μF each [217, 31, 184] and, therefore, they are not physically small components that could be integrated on silicon with the rest of the stimulator circuitry. Different works in literature solve the problem of the huge blocking-capacitors using the High Frequency Current Stimulation (HFCS). This stimulation technique is based on small blocking-capacitors that are alternatively charged and discharged several times during the same pulse in order to deliver the desired amount of charge to the nerve. In this way, the stimulation current is not continuous but composed by a sequence of small pulses. Their frequency essentially depends on the size of the blocking-capacitors and thus on the time required for their charging and discharging. An example of this architecture, depicted in Fig. 3.11, is presented in [101]. Apart from protection against



(a) Output stage architecture.

(b) Stimulation cycle.

Figure 3.11: (a) Stimulator output stage with small blocking-capacitors utilizing the HFCS technique and passive discharge with the related (b) timing waveforms. From [101].

electrolysis following semiconductor failure, the use of blocking-capacitors provides also a simple solution to maintaining charge-balance ([42]) during normal stimulation [101].

3.1.3 Stimulation pattern generator

Once the stimulation mode has been defined (voltage or current), another design variable to be defined is the output generation. Since a certain waveform is desired for stimulating and different output intensities are needed, it is not possible to simply connect a source

directly to the tissue. The traditional way to construct a certain waveform is by using Digital to Analog Converters (DACs). The pulse shape is constructed using digital logic and is then converted to an analog signal to stimulate the tissue. In most traditional stimulators only square shaped waves are used. Using this scheme the DAC is set at a certain constant output intensity end subsequently the DAC is enabled for a certain period of time. Several DAC based designs are reported in literature. A classical DAC based architecture can be found in [217]. Some modifications are found in literature, each focusing on a certain aspect of the DAC:

- To improve the resolution in [172] the design is modified to have a variable maximum current. When low intensities are required, the DAC current is reduced. In this way a high resolution can be obtained, even when the output current is small.
- When designing a stimulator with many output channels, the area of the stimulator becomes important. In [175] the area reduction was mainly obtained by introducing a more efficient current source implementation. In [45] the area reduction if obtained by introducing a multibias scheme: instead of using $2N-1$ transistors to generate the binary weighted currents, only N transistors are used, each of them biased differently to generate the binary weighted currents.
- To assure monotonicity, the DAC can be chosen to be made thermometer based instead of binary weighted [96].

An alternative to the use of a DAC is to do all signal processing in the analog domain. This technique can be used to obtain a very low power consumption. Recent publications mostly show applications in cochlear implants [57]. Input signals from a microphone is filtered and processed to create the stimulation pulses in an analog way. Publications show this can significantly decrease power consumption using sub-threshold operation compared to using DSPs. The drawback of this scheme is the limited flexibility. An analog circuit is in most cases only applicable for a certain application. A little more flexibility while still having the low power consumption is to add a little digital control to the analog circuitry [56].

Ref.	Tech.	Output I [mA]	Output V [V]	Load [$k\Omega$]	Stim. Freq. [Hz]	# of Chs	Area[mm^2]	Power [mW]
[206]	COTS	< 35	[0.05;3]	[0.8;2]	[1;200]	2	506	20
[124]	COTS	< 0.8	–	100	1	–	–	–
[147]	CMOS 0.18μ	[0;4.2]	–	15.4	–	10	4	0.5
[103]	HV-CMOS 0.6μ	< 8	[0;+17.25]	< 2	< 50	4	27.3	30.1
[45]	CMOS 1.2μ	< 0.4	–	–	–	–	4.84	0.26
[40]	CMOS 0.18μ	[0;0.005]	[−12;+12]	10	–	256	27	6.8
[90]	SOI-CMOS 0.6μ	[1;16]	[+6;+24]	–	–	–	0.31	–
[99]	SOI-CMOS 0.6μ	< 10	< 12	1	–	–	4	–
[101]	SOI-CMOS 1μ	0.15	[+5;+18]	[1;10]	–	4	2.7	60
[172]	CMOS 1.5μ	< 0.6	[0;+6.5]	10	50	8	4.84	1
[201]	HV-CMOS 0.18μ	[0;0.5]	[+3;+11.5]	–	80	8	5.4	–
[78]	CMOS 0.18μ	[0;0.32]	[0;+8]	–	–	–	1.27	3.8

Table 3.1: Main characteristics of neural stimulation system presented in literature.

3.2 Design specifications

In this chapter, the design of a stimulation unit aimed to restore the human sensory feedback is described. The device interfaces the peripheral nervous system of an hand-amputee and should be capable to proper generate action potentials in the nervous fibers of the nerve in order to transmit to the brain the sensory information acquired by the sensors placed over the artificial limb. As discussed in Section 1.4.2 and Section 3.1, the environment in which the device is intended to work in is hostile and not totally known, therefore, it is not easy to get very well defined design specifications. In fact, a suitable and functional neural stimulator should be as much flexible as possible even though the flexibility usually goes in opposite direction with respect to implementation simplicity, costs and system dimension. As a consequence, when defining the stimulator specifications, a good compromise between all these factors together with the patient safety has to be reached. However, due to the complexity of the system, only the most essential requirements are considered in designing the first prototype here presented.
The first not negligible issue concerns the high impedance at electrode-tissue interface that impose the development of a high voltage compliant system. In particular, since the target is a totally implantable device, the high voltage source and so a voltage booster to increase the stimulation voltage above the low voltage power supply is included in the stimulator. The remaining fundamental blocks are the module to generate the stimuli and the output stage that delivers them to the nerve.
The definition of the system architecture and specifications have been driven on side by the neural signal electrical features (such as frequency and amplitude) and on the other by considering works found in literature. As widely discussed in Section 3.1, different stimulation strategies are available and, in particular, the CCSs have been proved to be a good trade off between implementation complexity and system performance. For this reason a current-mode stimulation is selected as a way to control the charge exchange between the stimulator and the tissue. Therefore, the device should generate programmable current waveforms [144, 105] with amplitude resolution of $10\mu A$ and a time resolution of $0.8\mu s$. As

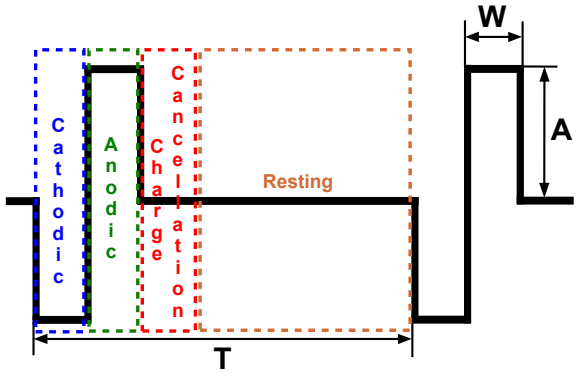


Figure 3.12: Stimulation pattern.

previously discussed (Section 1.4.2 and Section 3.1), typical neural stimulation patterns are biphasic current pulses, shown in Fig. 3.12, with programmable amplitude (A) in the range $10\mu A - 300\mu A$, period (T) from $2.5ms$ to $1s$ and pulse width (W) from $50\mu s$ to $150\mu s$ and therefore these parameters were selected as the target for our device. Biphasic pulses are needed since it has been demonstrated that the charge accumulation at the tissue interface

can produce severe damages to the cells [76]. To prevent these risks, bipolar active or passive waveforms should be used, in this way the charge accumulated in the first phase is compensated in the opposite phase. Any residual charge due to mismatch between the pulses must be eliminated by connecting the terminals through a resistor or using other techniques such as blocking capacitors [101]. As shown in Fig. 3.12, each pulse is therefore characterized by 4 phases: cathodic, anodic, charge-cancellation and a final resting phase in which the electrode terminal is disconnected from the stimulator. The pulse phases are independently generated and can differ in duration if necessary. A complete integration of the stimulator is required to reduce the encumbrance of the electronics and let the patient move freely, without impeding connections to lab instrumentation. The electronics will be connected by transcutaneous wirings to the implanted TIME electrodes as those used in [144]. Finally, considering typical electrode-tissue impedance in the range of tens of $k\Omega$ ($50k\Omega$ was fixed as maximum value) and the need to deliver currents in the order of hundreds of μA (maximum $300\mu A$), the required high voltage was fixed to $17V$. Moreover, in order to adapt the system to a lower impedance of the electrode-tissue interface, the stimulation voltage should be programmable starting from at least $4V$ that is slightly over the $3.3V$ power supply. The specifications for the IC design are summarized in Table 3.2.

Simulation method	current-mode
Pulse Amplitude (A)	$10\mu A - 300\mu A$
Pulse Width (W)	$50\mu s - 150\mu s$
Pulse Frequency $(1/T)$	$1Hz - 400Hz$
Stimulation voltage	$4V - 17V$

Table 3.2: Stimulator specifications.

3.3 System architecture

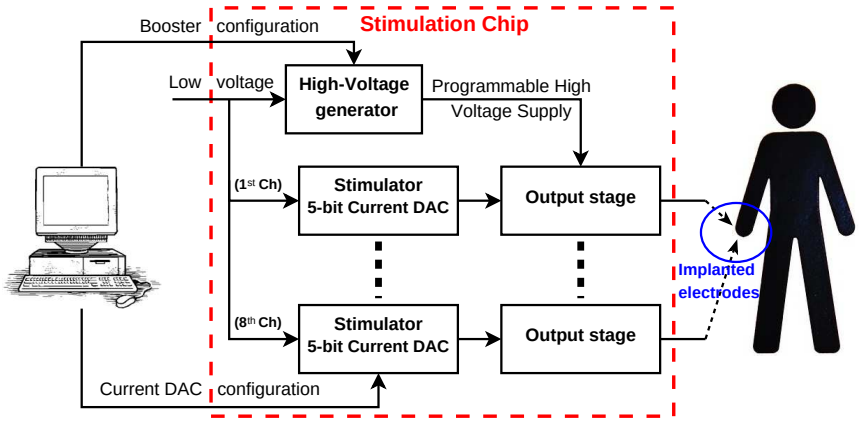


Figure 3.13: Block diagram of the stimulation system.

The architecture of the proposed neural stimulator is presented in Fig. 3.13. The device embeds a programmable voltage booster that increases the stimulation voltage up to $17V$

starting from a $3.3V$ power supply. The generated high voltage is shared between 8 independent stimulation channels. Each channel includes a low voltage pulse generator based on a $5-bit$ current DAC followed by an output stage that converts the generated pulse from a low into a high voltage current stimulus ready to be injected/sunk to/from the nerve.
The IC was realized in a $0.35\mu m$ HV CMOS process from AMS including both low voltage and

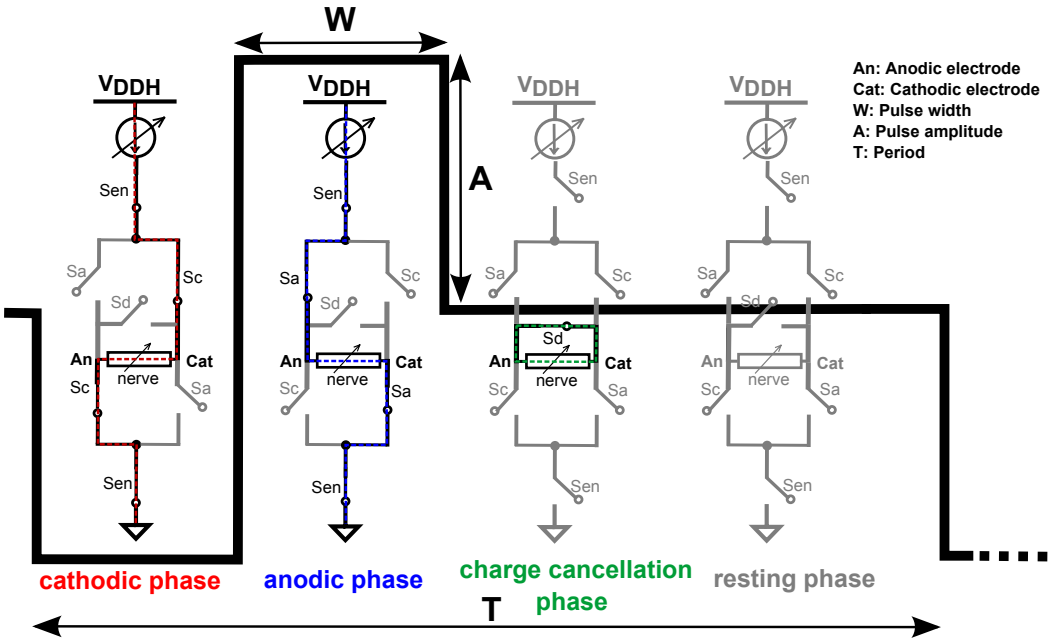


Figure 3.14: Implemented stimulation architecture.

high voltage transistors able to support up to $50V$. The stimulation circuits and the switch configuration used to generate each phase have been represented in Fig. 3.14 overlapped to the corresponding pulse phase. The stimulation is enabled by closing switches S_{en}; when also switch S_c is closed, the cathodic phase is started; closing S_a and opening S_c the anodic current is delivered to the electrode. Switches S_{en} stay open in the last two phases: during charge-cancellation S_d is closed to short the electrode terminals and, finally, when all the switches are open the electrode is disconnected from the stimulator (resting state).
The anodic electrode in Fig. 3.14 is shared by all the 8 stimulation channels (the catodic electrodes) and represents a reference electrode properly placed inside the nerve or in the patient body. All the switches are driven by a digital controller hosted on an external board; it handles the different pulse phases through a $16-bit$ SPI interface clocked at $20MHz$. The SPI clock frequency sets the time resolution of the stimulus pattern at $0.8\mu s$ which is the time required for a single write operation. Moreover, the digital module is responsible for the setting of the stimulus parameters (amplitude, width and frequency) and the stimulation voltage generated by the voltage booster. All the settings are stored into an on-chip digital interface which directly control the entire chip. The external digital unit will be implemented on programmable logic (FPGA), that together with the recording IC digital interface will be hosted on the robotic limb.
The work presented in this chapter is a part of the whole architecture design and concerns only the development of the analog front-end with the high voltage generator and the eight independent channels containing the stimuli generator and the output stage. In particular, the high voltage generator is composed of two independent programmable voltage boosters

each of which is responsible for the generation of the high voltage required during the stimulus's anodic or cathodic phase. As will be detailed in the following section, each booster is implemented with a switched capacitors charge pump that accumulates the charge on an off-chip $22nF$ capacitor. The accumulated charge is that used for generating the cur-

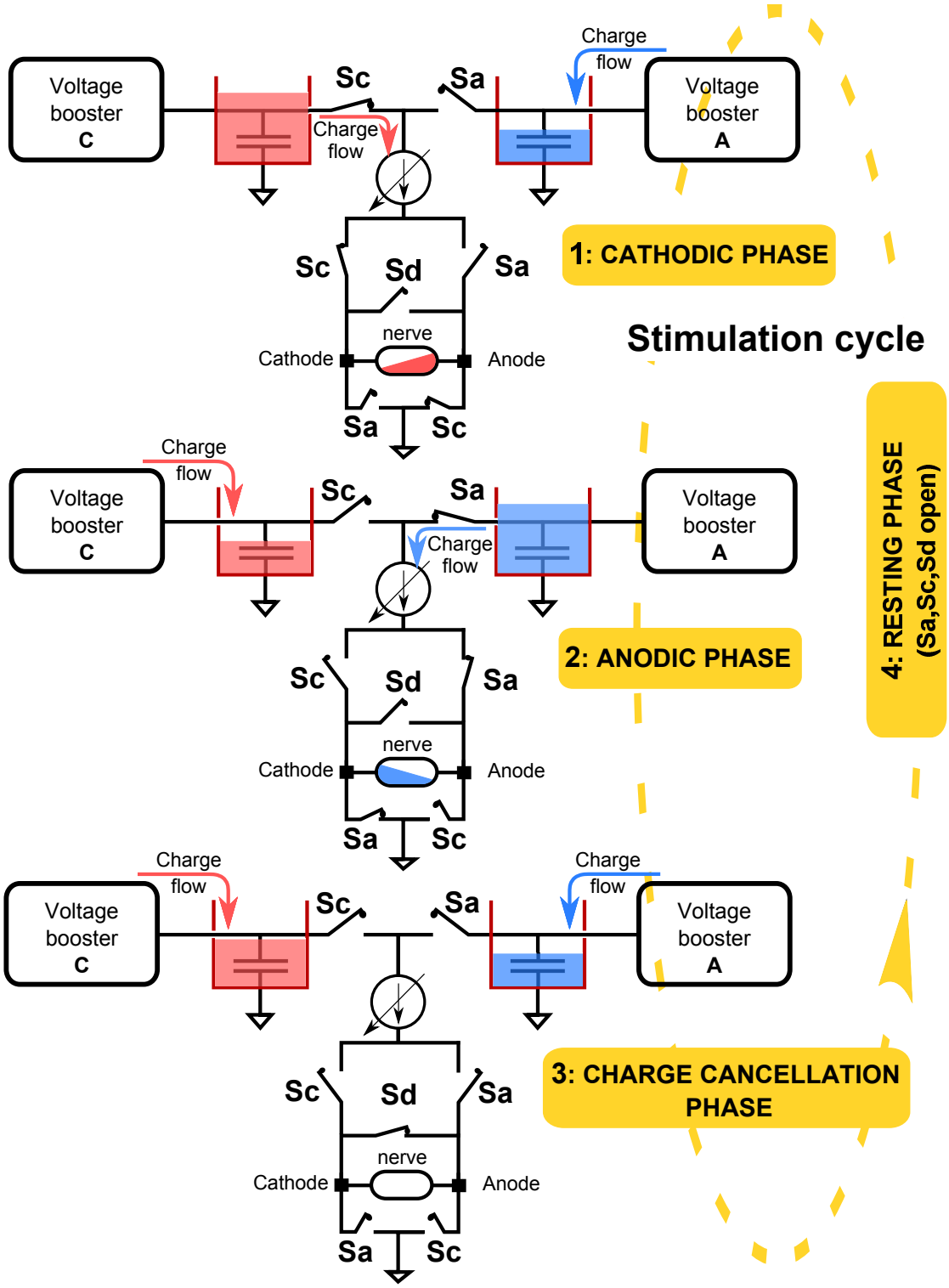


Figure 3.15: Volateg boosters behaviour during the stimulation cycle.

rent stimulus and, therefore, injected into the nerve. In this way we assure that, in case of system failure, no more than the charge stored in the capacitor can be delivered to the tissue, protecting it from a permanent damage. Acting in this way, the main drawback is that, during the charge delivering, the high voltage drop across the capacitor and thereby the stimulation voltage decreases. This problem is solved by using separate boosters for the two stimulation phases (anodic and cathodic). As depicted in Fig. 3.15, during the cathodic phase the charge flows from the *C*thodic booster to nerve and the *A*nodic booster recharges the previously discharged accumulation capacitor. The same charge exchange but in opposite direction happens during the anodic phase. Finally, during charge cancellation and resting phases, both boosters recover the delivered charge. Of course, in order to make this mechanism working, the system has to be properly sized. In particular, in worst case condition (maximum stimulation frequency), the booster should completely recover the delivered charge otherwise the desired stimulation voltage will be not reached at the time of the next cathodic/anodic stimulation phase. The most critical parameters are the charge pump switching-capacitor frequency, the number of stages of the boosting chain and the size of the accumulation capacitor. The sizing of these parameters and the detailed booster implementation is discussed in the following section along with the description of all other modules that compose the designed IC.

3.4 Transistor level circuitry design

The transistor level circuit was designed in a High Voltage (HV) CMOS 0.35μm process from AMS (AustriaMicroSystems) characterized by a p-type substrate, 4 metal layers and 2 polysilicon layers. In addition, the selected technology supports:

- The standard 3.3V and 5V process including *PMOS* and *NMOS* transistors, *CPOLY* (POLY1-POLY2) capacitors and *RPOLY1/2* and *RPOLYH(igh-resistive)* sheet resistors.
- Isolated low voltage (3.3V and 5V) transistors, *NMOSI(solated)* and *PMOSI(solated)*, created into a n-well.
- High voltage (50V) transistors called *NMOS50(T,M,H)* and *PMOS50(T,M,H)*. The last letter of the name indicates whether the transistor has a thin (T), a medium (M) or a thick (H) gate-oxide and the related maximum supported gate-source and source-body voltages (V_{GS} and V_{SB}) that are 3.6V for the *NMOS50T*, 5.5V for the *NMOS50M* and 20V and 5.5V for the *NMOS50H* V_{GS} and V_{SB} respectively, whereas all transistors support a maximum drain-source voltage (V_{DS}) of 50V.
- Symmetrical high voltage (50V) transistors, *NMOS50HS* and *PMOS50HS* that with respect to the non-symmetrical ones support V_{SB} up to 50V.
- Isolated high voltage (50V) transistors and in particular, since a p-type substrate is used, only n-type isolated high voltage transistor, NMOSI50(T,M,H) are implemented using a n-type well. This transistors with respect to the non-isolated ones have the advantage to support body-substrate voltages ($V_{B-substrate}$) up to 50V.
- Other components are also implemented such as the *CPM* (using the PLOY1-Metal1-Metal2-Metal3 layers) and *CWPM* (using the DNTUB-PLOY1-Metal1-Metal2-Metal3 layers) sandwich capacitors and PNP and NPN bipolar transistors.

These are only the main components and their correspondent main parameters extracted from the technical datasheets of the selected technology process. Each components has its specific features, advantages and disadvantages, therefore an accurate selection was made before starting with the IC design. In particular, since the high voltage transistors occupy a wider area and have wider parasitics than the low voltage ones, the strategy adopted in the IC design was to minimize as much as possible the use of the HV transistors. Area, power and patient-safety constraints are particularly compelling since the chip must be integrated with the electrode and implanted in the patient stump, our main aim is then to find a good compromise among these requirements.

3.4.1 Programmable high voltage generator

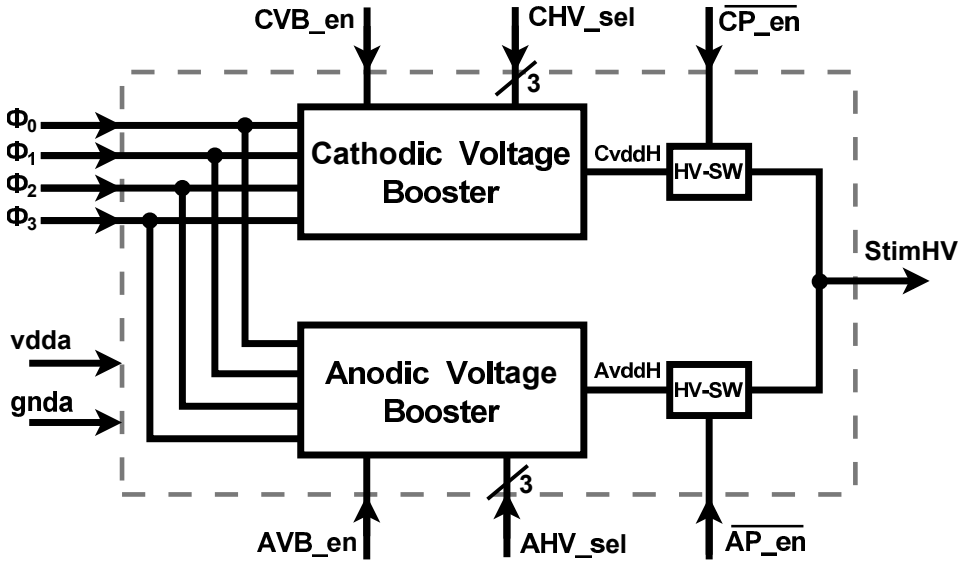


Figure 3.16: High voltage generator block diagram.

The complete high voltage generator scheme is depicted in Fig. 3.16. As introduced in the previous section, it includes two independent voltage boosters for the cathodic and anodic stimulation phases that generate the stimulation voltage (*StimHV*) starting from the $3.3V$ power supply (*vdda*). Moreover, two High Voltage SWitches (*HV-SW*) controlled by the $\overline{CP\_en}$ (Cathodic Pulse enable) and $\overline{AP\_en}$ (Anodic Pulse enable) active-low signals are introduced to respectively connect the Cathodic Voltage Booster (CVB) or the Anodic Voltage Booster (AVB) to the output depending on the stimulation phase. Each voltage booster is controlled by the following signals:

- **AVB_ en / CVB_ en**: Anodic / Cathodic Voltage Booster enables. They are active-high signals to turn on/off the boosters.
- **AHV_ sel / CHV_ sel** (Anodic/Cathodic High Voltage selection): Each of them is a $3-bit$ signals to set the desired stimulation voltage for the anodic and cathodic phase respectively.
- Φ_0,Φ_1,Φ_2,Φ_3: These are four clock signals to control the switched-capacitors charge pumps. Further details are given in the following.

All control signals are generated by the external digital interface on the FPGA board as introduced in Section 3.3.

In order to interrupt or close a high voltage path, the switch depicted in Fig. 3.17 was de-

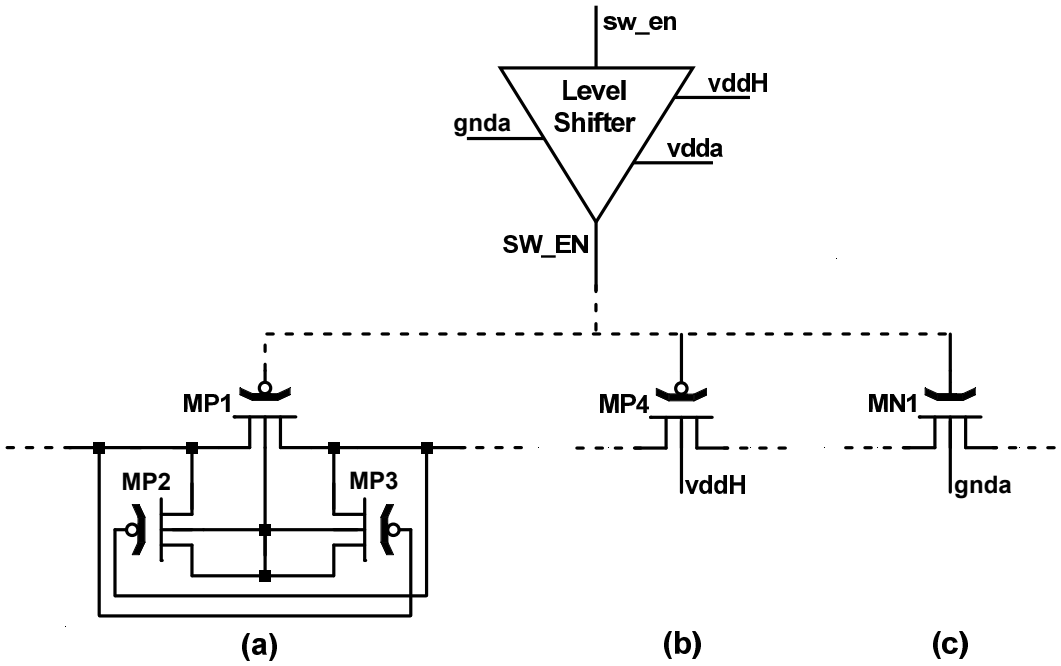


Figure 3.17: High Voltage SWitch (HV-SW) implementation with (a) dynamic or (b),(c) fixed control of the switch-transistor's body contact.

signed. It consists of a symmetrical HV transistor (*MP1* or *MP4* or *MN1*) that, depending on the type of the HV path to be controlled (a HV ground or a HV source), can be either a PMOS or a NMOS (*NMOS50HS*, *PMOS50HS*). In this case, both HV switches are implemented with a

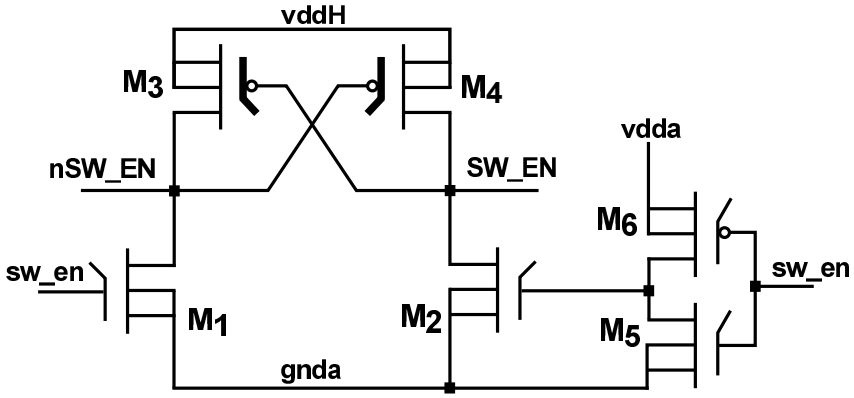


Figure 3.18: Level shifter implementation.

p-type switch-transistor. Differently from the n-type transistors which body is connected to the lower voltage in the circuit and thereby to ground (*gnda*), the p-type body contact has to be connected to the higher voltage. In this specific module, the two high voltage switches are connected in a critical path in which both voltages on the drain and on the source vary over

the time. In fact, for example, the upper *HV-SW* in Fig. 3.16 is connected on one side to the CVB which output increases to create the desired cathodic stimulation voltage whereas on the other side the voltage can be either lower, in the cathodic phase, or higher, in the anodic phase. For this reason, other two *PMOS50HS* transistors are added to create a dynamic body contact connection. These are the transistors *MP2* and *MP3* in Fig. 3.17 which function is to constantly keep the *MP1* body contact to the higher voltage between those at *MP1* drain and source. The dimensions of the transistors are reported in Table 3.3a and vary from a PMOS to a NMOS due to their different carriers mobility. In this case the only requirement is to have transistors wide enough to carry the required current. Since the have a thick gate-oxide and due to high voltage connected to their source and drain, a high voltage signal is required for controlling their gate. However, the piloting signals are generated in a low voltage domain since, as explained in Section 3.3, the low voltage transistors allow to save area and have small parasitics. For this reason, a level shifter was implemented to convert the gate piloting signal from a low voltage into a high voltage domain. Fig. 3.18 shows the level shifter implementation and Table 3.3b contains its transistors' size. The designed level shifter generates two high voltage signals: the *SW_ EN* that is the equivalent of the low voltage input *sw_ en* signal and the *nSW_ EN* that has opposed phases. The high voltage generator specifications

MOS	**size** $\frac{W}{L}\left[\frac{\mu m}{\mu m}\right]$
MP1, MP4	$\frac{200}{2.8}$
MP2, MP3	$\frac{100}{2.8}$
MN1	$\frac{200}{4}$

(a) *HV-SW*'s MOSs parameters.

MOS	**type**	**size** $\frac{W}{L}\left[\frac{\mu m}{\mu m}\right]$
M1, M2	*NMOSI50T*	$\frac{20}{0.5}$
M3, M4	*PMOS50H*	$\frac{20}{1.4}$
M5, M6	*NMOSI,PMOSI*	$\frac{10}{0.5}$

(b) *Level Shifter*'s MOSs parameters.

Table 3.3: Transistors size of the (a) high voltage switch and of the (b) level shifter.

require a programmable output voltage in the range $4V - 17V$ with step of $2V$. As explained in Section 3.2, the voltage range has been determined in order to be able to inject a maximum current of $300\mu A$ into the nerve even in case of high electrode-tissue impedance up to $50k\Omega$. The same implementation diagram depicted in Fig. 3.19 was used for both Cathodic and Anodic Voltage Boosters. The voltage booster is comprehensive of a charge pump and a voltage regulator. The former is the core module that generates the required voltage level programmed through the $3-bit$ signal (*HV_ sel*). It is based on a Dickson charge pump circuit [47] in which each cell contains a MOSFET-based diode and a charge-transfer capacitor. The specifications for the voltage booster were calculated trying to minimize the chip area and to reduce the boosting time. In order to reach the target output voltage of $17V$ and to minimize the area, 9 stages are required as computed in Eq. 3.3 [133].

$$N = 2 \times \left(\frac{V_{out}}{V_{dd}} - 1\right) \tag{3.3}$$

Moreover, considering that in the worst case, which is stimulating at the maximum frequency ($400Hz$ and thereby $T = 1/f = 2.5ms$) with the maximum pulse width ($150\mu s$), only $2.35ms$ are available to recover the charge between two subsequent pulses, one more stage was added to reduce the recovery time. The whole boosting chain is depicted in Fig. 3.20

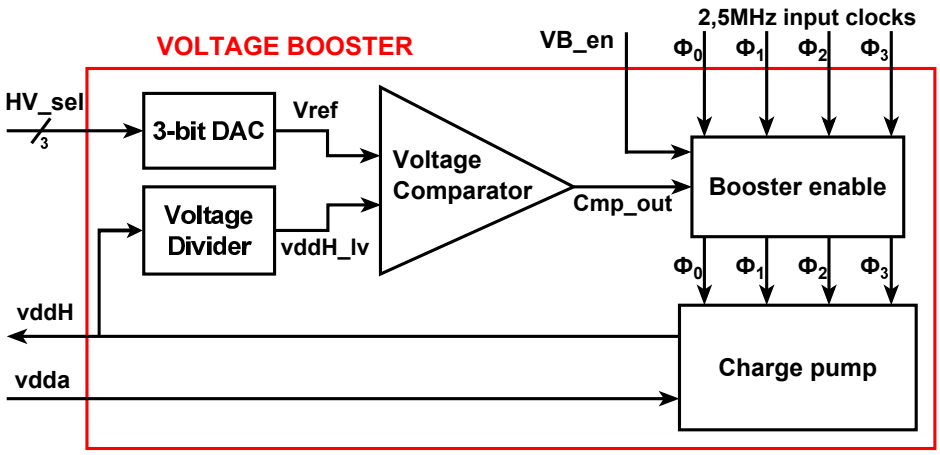


Figure 3.19: Voltage booster implementation.

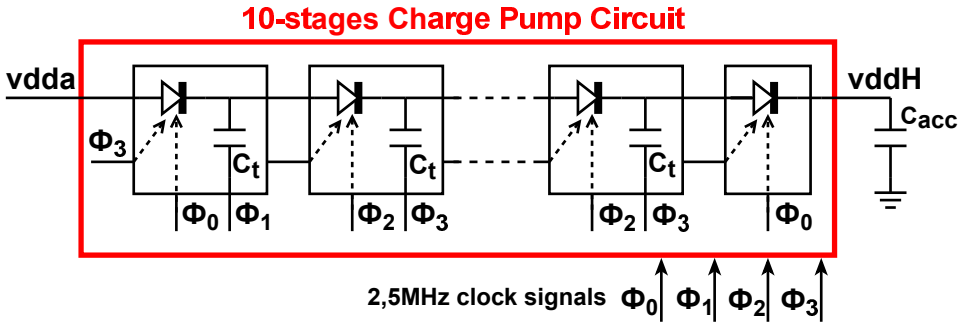


Figure 3.20: Block diagram of the implemented charge pump.

whereas Fig. 3.21 shows two cells of the charge pump connected together. The diodes are implemented with symmetrical HV p-type transistors (*PMOS50HS*) [207]: M_1 is the transistor responsible of the charge transfer, M_2 and M_3 implement the dynamic connection of the M_1's body contact to the maximum voltage between those at M_1's drain and source. M_4 with the C_g capacitor guarantees that the V_{gs} of M_1 does not exceed the $3.3V$ power supply so that the transistor M_1 can be turned on/off by means of a low voltage ϕ_i signal. The gate of M_4 is controlled by the clock signal ϕ_2, for the first cell and, for all the other stages, by the clock at the M_1 gate of the previous stage. These connections allow to open M_1 diode connection during the charge phase and to connect it in diode-mode during charge transfer to the subsequent cell. The operating principle of the boosting chain is the turnover of two different phases by means of four $2.5MHz$ clocks $(\phi_0, \phi_1, \phi_2, \phi_3)$ depicted in the inset in Fig. 3.21. Clock frequency was chosen for compatibility with the requirements of the recording chip (Chapter 2) driven by the same signal that completes the bi-directional interface. Clocks ϕ_0 and ϕ_1 drive to the odd cells while ϕ_2 and ϕ_3 control the even cells. In Fig. 3.21 the circuit of the first two Booster's cells is shown in details: during phase 1, $\phi_0 = 0V$ and $\phi_1 = 0V$ the transistor M_{1a} is on and current flows from V_{in} charging C_{ta}. In phase 2, $\phi_0 = 3.3V$, M_{1a} turns off, isolating C_{ta} from V_{in} and $\phi_1 = 3.3V$ forces the C_{ta} charge to move through M_{1b} on C_{tb}, this is allowed by the clocks ϕ_2 and ϕ_3 in cell b that are both low. The charge transfer described for the first cells is replicated for all cells. Continuously switching the two phases, small amounts of charge are transferred from one stage to the next one until when the charge reaches the final accumulation capacitor (C_{acc}). Its dimension has been

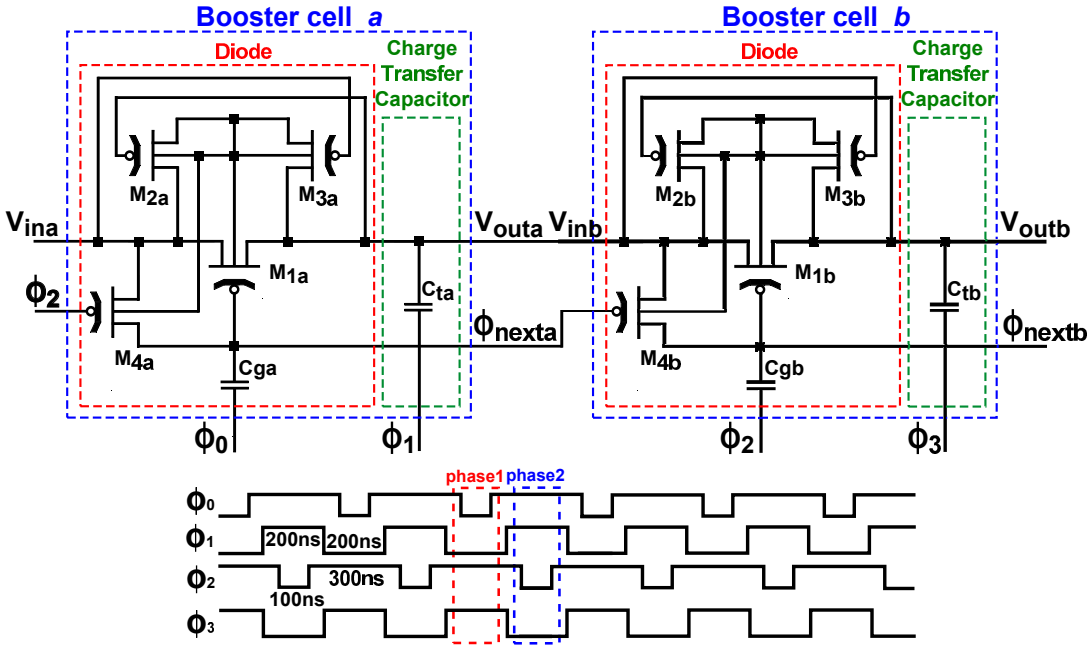


Figure 3.21: Schematic diagram of the charge pump cells.

chosen considering the maximum stimulation current of $300\mu A$ and the maximum pulse width of $150\mu s$, in this case, the maximum amount of charge to be delivered to the nerve is $45nC$ for each pulse side (positive and negative). As a consequence and for a given electrode impedance of $50k\Omega$ the booster needs to charge an accumulation capacitor C_{acc} of, at least, $20nF$. Due to its huge capacitance, it requires a too wide area to be integrated in the IC and, therefore, we opted for an off-chip capacitor. Among commercially available components with small package, a $22nF$ capacitor was selected. The transfer capacitance has been chosen minimizing the area, according to [133], the optimum value is calculated as Eq. 3.4 that results in a $C_t = 62pF$, we tuned this value simulating the circuit and obtained the same boosting rate using a $C_t = 50pF$.

$$C_t = N \times \frac{I_L T}{[(N+1) \cdot V_{dd} - V_{out}]} \tag{3.4}$$

The size of the diode-transistor M_1, has been chosen considering the charge delivered dur-

MOS	type	size $\frac{W}{L}\left[\frac{\mu m}{\mu m}\right]$
$\mathbf{M_1}$	*PMOS50HS*	$\frac{300}{2.8}$
$\mathbf{M_2, M_3}$	*PMOS50HS*	$\frac{100}{2.8}$
$\mathbf{M_4}$	*PMOS50HS*	$\frac{35}{2.8}$

(a) Voltage booster's MOSs parameters.

MOS	type	value
$\mathbf{C_g}$	*CWPM*	$9.5pF$
$\mathbf{C_t}$	*CWPM*	$50pF$
$\mathbf{C_{acc}}$	off-chip	$22nF$

(b) Voltage booster's capacitors value.

Table 3.4: Selected (a) transistors and (b) capacitors parameters of the voltage booster.

ing each stimulation pulse and the minimum time between two subsequent pulses. As al-

ready mentioned, within a stimulation pulse, the maximum charge delivered to the electrode is $45nC$ for each phase (with current amplitude of $300\mu A$ and duration of $150\mu s$). Since the maximum work frequency is $400Hz$ ($T = 2.5ms$), in the worst case, the charge transferred to the nerve must be recovered in $2.35ms$. During this time, with the booster clock frequency of $2.5MHz$, 5875 clock cycles occur, therefore $7.6pF/cycle$ are transferred to recover the consumed charge ($45nC$). This corresponds to a current of $76\mu A$ (since $T_{on} = 100ns$). Considering the technology parameters, to achieve such current a $W/L = 25$ has been calculated. This is valid for a single channel stimulation, to allow the parallel simulation of at least 4 channels a $W/L = 100$ was used. Since for the HV transistors $L_{min} = 2.8\mu m$ a $W = 300\mu m$ was chosen. The chosen parameters for all charge pump's components are collected in Table 3.4. The voltage booster is regulated by means of a voltage regulator that compares the booster

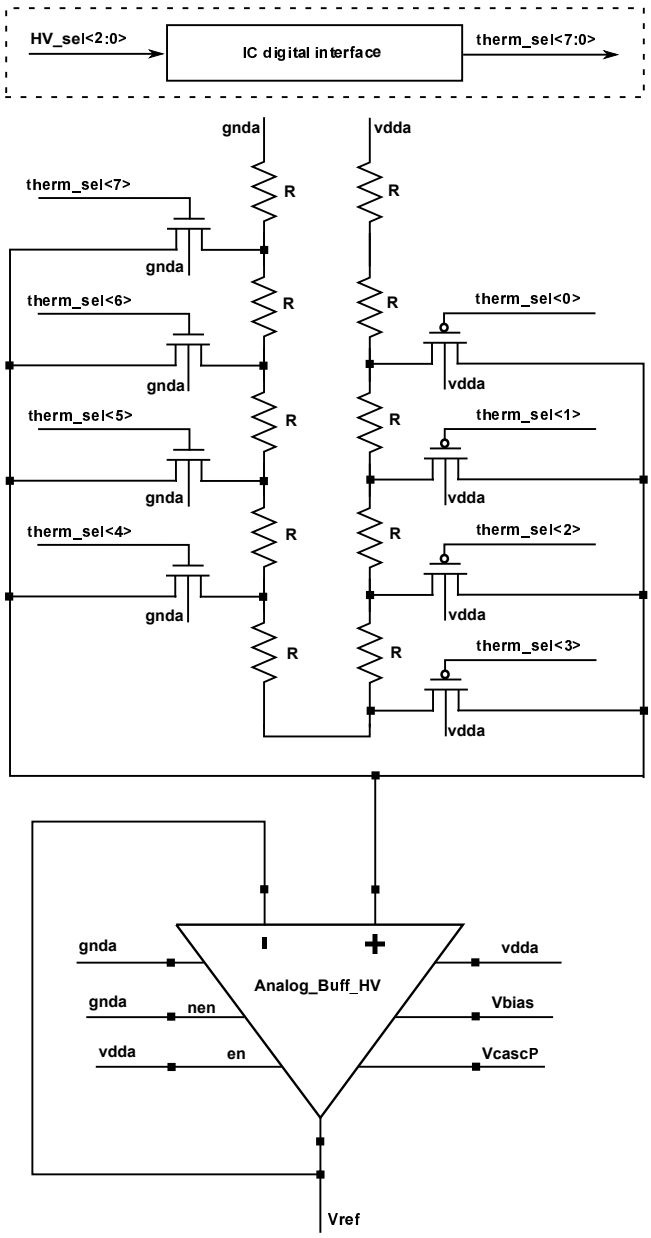


Figure 3.22: Schematic diagram of the $3-bit$ DAC.

HV_ sel <2:0>	Therm_ sel <7:0>	Target voltage [V]
000	1000 1111	3
001	0100 1111	5
010	0010 1111	7
011	0001 1111	9
100	0000 0111	11
101	0000 1011	13
110	0000 1101	15
111	0000 1110	17

Table 3.5: $3-bit$ DAC: target voltage coding.

name	type	size
nmos	*NMOSI*	$\frac{W}{L} = \frac{0.5\mu m}{0.35\mu m}$
pmos	*PMOSI*	$\frac{W}{L} = \frac{1\mu m}{0.35\mu m}$
R	*RPOLYH*	$300k\Omega$

Table 3.6: Parameters of the DAC's components.

output with a target voltage generated by a $3-bit$ DAC according to the first and the third columns of Table 3.5. The converter is based on a resistive divider network (Fig. 3.22) controlled by an $8-bit$ thermometric code generated by the IC digital interface starting from the $3-bit$ input selection code (*HV_ sel*) (according to the first two columns of Table 3.5). The transistors, whose gate is directly piloted by the input code, act as switches and are designed with a minimum dimension whereas the resistor's value was chosen as a trade-off between power consumption and area occupation; the adopted values are collected in Table 3.6. Moreover, since there are no special constrains for the output voltage buffer, a standard component (*Analog_ Buff_ HV*) from the technology process libraries was selected. In order to save area, the regulation circuitry was completely designed with low voltage transistors and, as a consequence, the booster high voltage output is scaled into a low voltage range between $0V$ and $3.3V$ before being compared. The conversion is based on a simple resistive divider (R_1,R_2) as depicted in Fig. 3.23. The resistors' value (Tab. 3.7) are determined in order to limit at $5\mu A$ the current derived from the high voltage path and thereby from the accumulation capacitor C_{acc}. As for the voltage buffer, also the comparator (*Comparator_ HV*)

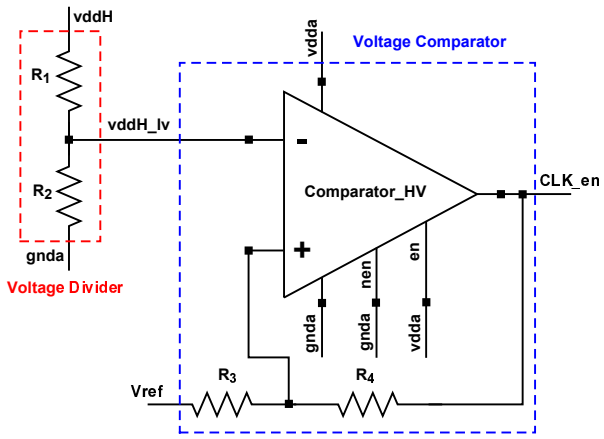


Figure 3.23: Schematic diagram of the voltage comparator.

name	type	size
R_1	*RPOLYH*	$3M\Omega$
R_2	*RPOLYH*	$500k\Omega$
R_3	*RPOLYH*	$6.67k\Omega$
R_4	*RPOLYH*	$400k\Omega$

Table 3.7: Voltage comparator and voltage divider resistors' value.

was selected from the process libraries. The comparison result (*Cmp_ out*) is a signal that indicates whether the charge pump has reached ($0V$) or not ($3.3V$) the programmed value and it is supplied to the *Booster enable* module along with the "master" enable (*CVB_ en* and *AVB_ en* for the cathodic and anodic voltage booster respectively) generated by the external control unit on the FPGA board. The *Booster enable* uses the master enable as a high priority signal. In fact, if the master enable is low ($0V$) the booster is disabled setting the four clock signals to $3.3V$, regardless the voltage comparator output. On the contrary, when the master enable is high ($3.3V$), the booster is (de)activated according to the *Cmp_ out* signal. This strategy is implemented with the diagram depicted in Fig. 3.24 using one *NAND* and four *OR* logic ports. The *NAND* port compares the master enable with the *Cmp_ out* generating the final active-low enable signal ($\overline{CP\_en}$ - Charge Pump enable) according to Table 3.8a. This signal is then supplied to each *OR* port to effectively (de)activate the charge pump by (pulling up) forwarding the clock signal (Table 3.8b).

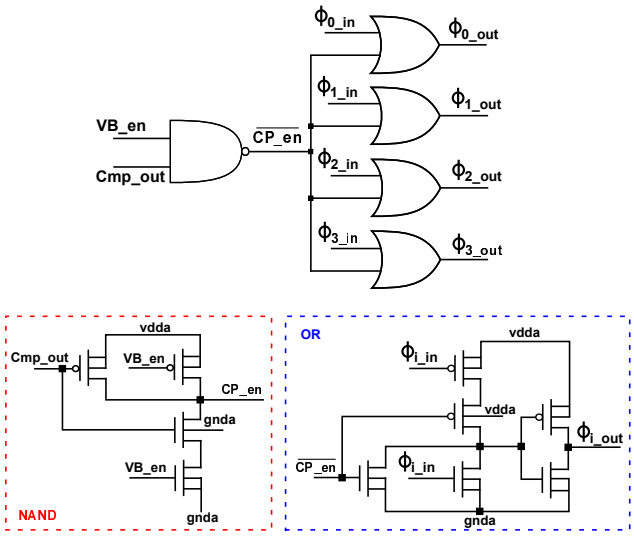


Figure 3.24: Booster enable logic network and logic ports' implementation.

VB_ en	Cmp_ out	CP_ en
0	x	1
1	0	1
1	1	0

(a) *CP_ en* generation (NAND port).

$\overline{CP\_en}$	Φ_{i_in}	Φ_{i_out}
0	0	0
0	1	1
1	x	1

(b) Booster clock enabling (OR port).

Table 3.8: Booster enable logic tables.

3.4.2 Stimulator: $5-bit$ current DAC

This module generates the stimulation current pattern in a low voltage domain on the base of the selection bit programmed by an off-chip controller. The stimulator is based on a $5-bit$

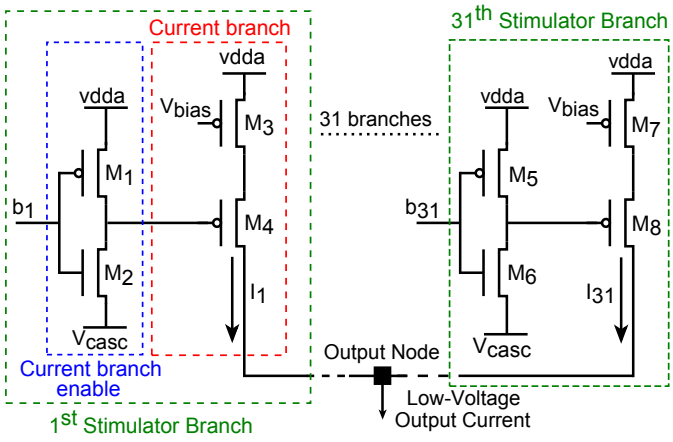


Figure 3.25: Schematic diagram of the stimulation current generator.

name	type	size $\frac{W}{L}\left[\frac{\mu m}{\mu m}\right]$
M_1, M_5	*PMOSI*	$\frac{1.5}{0.35}$
M_3, M_7	*PMOSI*	$\frac{5}{1.2}$
M_4, M_8	*PMOSI*	$\frac{5}{0.7}$
M_2, M_6	*NMOSI*	$\frac{0.5}{0.35}$

Table 3.9: Stimulation current generator transistors' size.

current DAC that can generate currents in a range from $10\mu A$ up to $310\mu A$ with a resolution of $10\mu A$. The stimulator diagram is depicted in Fig. 3.25. The base current is generated by a common bias circuit and mirrored into 31 equal branches (thermometric code) switching the gate voltage of the enabler pmos transistor (M_4 and M_8 in Fig. 3.25) from *vdda* to V_{casc}. Both voltages, V_{bias} and V_{casc}, are generated by the on-chip bias circuit.

3.4.3 Output stage

The output stage converts the stimulation current from a low into a high voltage domain using the high voltage generated by the boosters. It is implemented as a current mirror that copies the low voltage current from the stimulator in a branch with high voltage transistors connected between the high voltage (*vddH*) and *gnda* as depicted in Fig. 3.26. In particular, a cascode architecture was adopted in order to increase its output impedance. The transistors' size whose fixed considering the maximum stimulation current ($310\mu A$) and reducing, where possible, the current flow from *vddH* to *gnda*. For this reason, the transistors from M_3 to M_6 are smaller than those that deliver the charge to the electrode. The dimensions of the implemented transistors are collected in Table 3.10. The voltage V_{cascH} used to polarize the HV NMOS transistor is generated by the on-chip common bias circuit. This module includes also the high voltage switches to implement S_c, S_a and S_d from Fig. 3.14 whose functionalities are described in Section 3.3. The high voltage switches are implemented as described in Section 3.4.1 with the architecture depicted in Fig. 3.17.

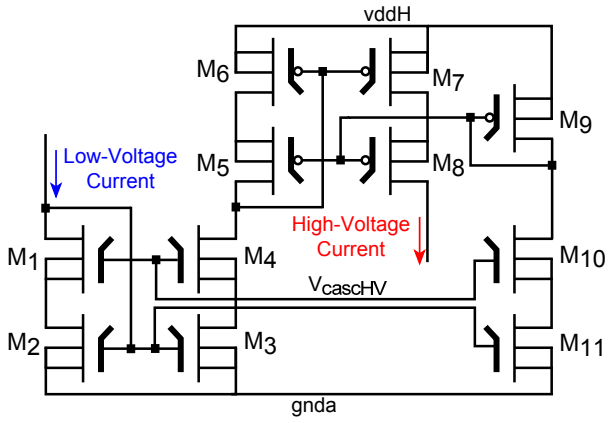


Figure 3.26: Schematic diagram of the output stage.

name	type	size $\frac{W}{L}\left[\frac{\mu m}{\mu m}\right]$
M_1, M_2	*NMOSI50H*	$\frac{1600}{0.5}$
M_3, M_4	*NMOSI50H*	$\frac{80}{0.5}$
M_5, M_6	*PMOS50H*	$\frac{80}{1.4}$
M_7, M_8	*PMOS50H*	$\frac{1600}{1.4}$
M_9	*PMOS50H*	$\frac{20}{1.4}$
M_{10}, M_{11}	*NMOSI50H*	$\frac{1600}{0.5}$

Table 3.10: Output stage transistors' size.

3.4.4 Digital interface

A minimal digital interface to coordinate the different IC's analog blocks was designed for the stimulation chip too. It is characterized by a bank of seven registers, each one of 12 bit as depicted in Fig. 3.27. With the exception of register 0, that is a read-only register, all the others can be either read or written. The communication between the custom designed IC and its external hardware controller is based on a custom $20MHz$ SPI (Serial Peripheral Interface) link with four communication lines:

- **Serial Clock (SCK)**: It is a synchronization clock generated by the external digital controller;
- **Master Output Slave Input (MOSI)**: A data line from the master (external digital controller) to the slave (custom designed IC);
- **Master Input Slave Output (MISO)**: A data line from the slave to the master;
- **not Chip Select (nCS)**: This signal enables (active low) the communication between the master and the selected (usually more slave devices can be connected to the same SPI bus) salve.

	11	10	9	8	7	6	5	4	3	2	1	0
0									CCmp_out	ACmp_out	CCP_en	ACP_en
1			CVB_en	AVB_en			AHV_sel			CHV_sel		
2		pulse_config	pulse_opcode		selected_electrodes							
3			stim_current_0					stim_current_1				
4			stim_current_2					stim_current_3				
5			stim_current_4					stim_current_5				
6			stim_current_6					stim_current_7				

Figure 3.27: Registers of the stimulation IC digital interface.

- **Register 0**: it is a read only register used to store and read same signals for testing purpose. The stored signals are:
  - **ACP_ en, CCP_ en**: (Anodic Charge Pump enable, Cathodic Charge Pump enable) a low level on these signals indicates that the anodic and cathodic boosters are active, respectively. They are the output of the NAND ports contained in the *Booster enable* modules (Fig. 3.24).
  - **ACmp_ out, CCmp_ out**: (Anodic Compare output, Cathodic Compare output) they are the output signals of the anodic and cathodic voltage comparators (Fig. 3.23), respectively. The signals assume a low level ($0V$) when the relative booster output voltage reaches the programmed value.
- **Register 1**: it is a read/write registers in which the voltage booster enable signals (**CVB_ en** and **AVB_ en**) and the desired output voltage selection codes (**CHV_ sel** and **AHV_ sel**), according to Table 3.5, for the cathodic and anodic boosters are stored. The enable signal is active-high, thus a high value indicates that the booster must be activated. This is the high priority booster enable generated by the external digital controller on the FPGA board.
- **Register 2**: it contains information related to the stimulation type and to the actual stimulation phase.
  - **pulse_ config**: If zero, it indicates that the stimulation is between an electrode active site and the reference electrode, otherwise it is between two normal active sites inside the nerve.

  - **pulse_ opcode**: It is a $2-bit$ code that indicates the actual stimulation phase (00 - resting phase, 01 - cathodic phase, 10 - anodic phase and 11 - charge cancellation phase) and it is used by the digital interface to (de)activate the switches S_a, S_c and S_d (from Fig. 3.14) according to what explained in Section 3.3.
  - **selected_ electrodes**: it is a $8-bit$ field used to specify which electrodes among the eight available have to be stimulated. Each bit refers to a specific electrode. If the bit is zero, the correspondent electrode is excluded from the stimulation.

- **Register 3 to 6**: These registers are used to store the stimulation pulse amplitude for each of the eight stimulation channel. The amplitude value is fixed by a $5-bit$ binary code (*stim_ current_ i*) and ranges from $10\mu A$ (00001) to $310\mu A$ (11111) with step of $10\mu A$.

The custom IC digital interface was modelled and verified using Verilog Hardware Description Language (HDL). The system description was first made at Register Transfer Level (RTL) in terms of registers (flip-flops or latches) and later converted into a gate level description using the *Encounter* automatic synthesis tool by *Cadence*. Finally, the synthesized circuit was directly imported in Virtuoso Schematic Editor in which the logic ports were mapped on the digital ports from the Standard Cell library of the selected technology process.

3.5 Chip Layout

Table 3.11 summarizes the transistor level simulation results of the achieved system. The final step toward the IC manufacturing is the layout drawing. It was developed following the same "good-layout" rules presented in Section 2.5 and, of course, using the new design rules imposed by the different technology process. The adopted $0.35\mu m50VCMOSH35B4$

	Stimulation IC characteristics
Stim. pulse amplitude	$10\mu A-310\mu A$
Stim. pulse frequency	$1Hz-400Hz$
Stim. pulse width	$50\mu s-150\mu s$
Stim. voltage	$4.5V-17V$
Max electrode-tissue impedance	$50k\Omega$

Table 3.11: IC stimulation module: main parameters summary after transistor level simulation.

process from Austria-Micro-System (AMS) is characterized by a minimum transistor channel length of $0.35\mu m$, a Si substrate of type *p*, 4-metal layers and a maximum operating voltage of $50V$ (further details on the selected technology process are in [180]). Since, as described in Section 3.4, it supports both low and high voltage transistors, special attention is required when both components are integrated in the same silicon die. In this case, it is suggested (in [180]) not to mix low and high voltage MOSs but to place them in well separate islands by using special voltage barriers.
The same tools presented in Section 2.5 were used to draw the layout of the stimulation

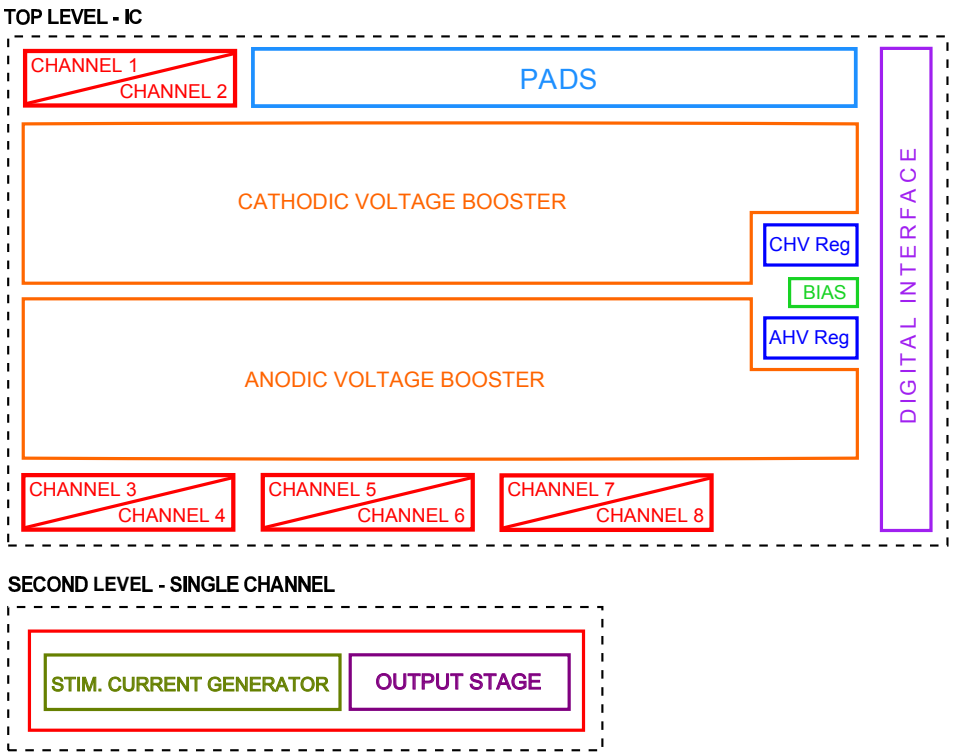


Figure 3.28: Complete outline of the designed stimulation chip.

chip starting from the IC floorplan depicted in Fig. 3.28. The layout of all modules was manually drawn with the tool Virtuoso Layout Editor by Cadence with the exception of the IC pads, the voltage buffers (Fig. 3.22), the voltage comparators (Fig. 3.23), whose layout already exist in the technology process libraries, and the digital interface whose layout was automatically generated with the Encounter Digital Implementation (EDI) tool by Cadence. Starting with the single stimulation channel, the $5-bit$ current DAC (Section 3.4.2) layout was the first to be drawn. Fig. 3.29 shows the zoom on a single stimulator branch in which

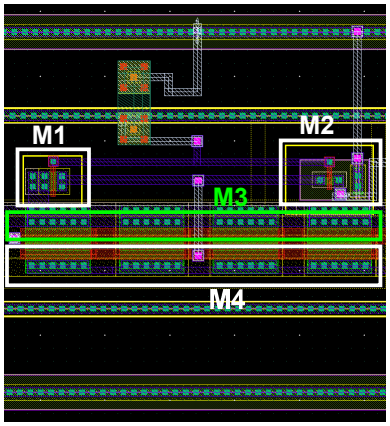


Figure 3.29: A single stimulator branch lyout.

the correspondent transistors to the schematic of Fig. 3.25 are highlighted. In particular, M_3

was realized as a parallel of four smaller transistors in order to increase its matching with the transistor that generates the V_bias in the IC biasing module. The component matching

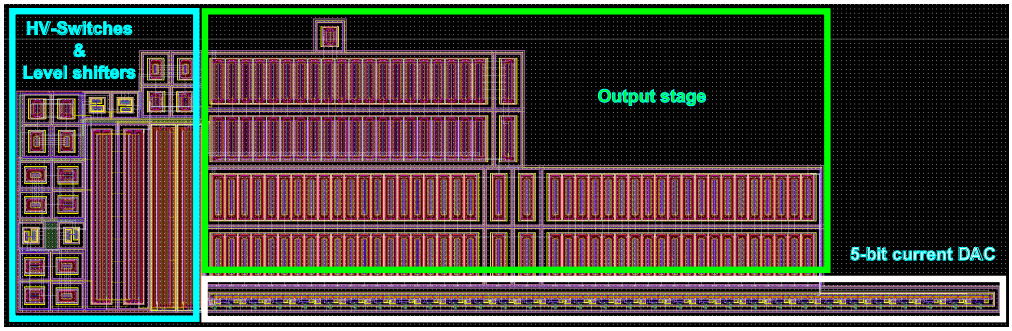


Figure 3.30: Single stimulation channel layout.

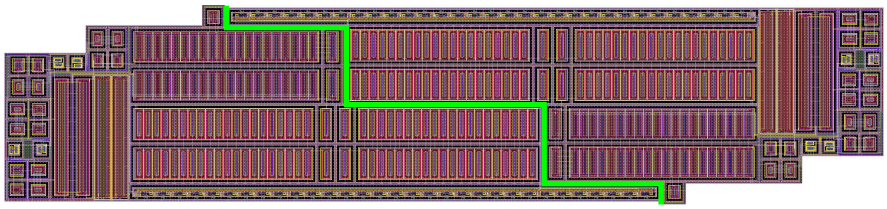


Figure 3.31: Two stimulation channels block.

rules were applied also for designing the layout of the high voltage current mirror of the output stage. The matched NMOSs and PMOSs were implemented as a multiple of unit transistors positioned with the same orientation and connected following the interdigitated schema. The layout of all remaining modules was designed following the same methodology. Fig. 3.30 depicts the layout of a single stimulation channel in which the white box encloses the entire stimulation current generator, the green box contains the output stage and the light-blue rectangle contains the high voltage switches (S_a, S_c and S_d). The shape of the single channel layout is due to the fact that by rotating of 180° another channel, is possible to perfectly match two channels creating a compact rectangular block as depicted in Fig. 3.31. The voltage regulator layout is depicted in Fig. 3.32 where its main blocks are highlighted: the analog voltage buffer, the voltage comparator, the high voltage divider and the $3-bit$ DAC to generate the reference voltage. In Fig. 3.33, where the complete booster layout is depicted, it is possible to notice as most of the designed IC area is occupied by the C_g and C_t capacitors of the charge pump. By duplicating this block and adding the 8 stimulation channels (Fig. 3.30) with the polarization circuit, the whole analog IC layout is obtained. Finally, Fig. 3.34 shows the complete designed IC layout where the digital interface and the PADs are connected to the analog block. The silicon die has a total area of $18mm^2$ ($3.4mm \times 5.3mm$), with 23 pins that, from the top, have the following functions:

- **SCK, MOSI, nCS, MISO**: these are the four pads of the SPI communication port.
- **vdd, gnd**: digital voltage supply ($3.3V$).
- **VDDA, GNDA**: analog power supply ($3.3V$).

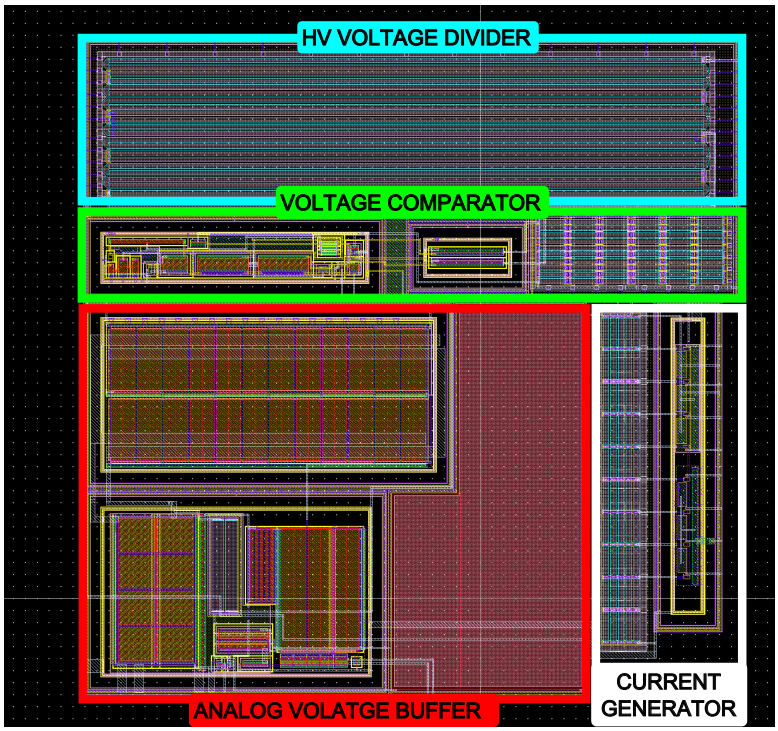


Figure 3.32: Booster's voltage regulator layout.

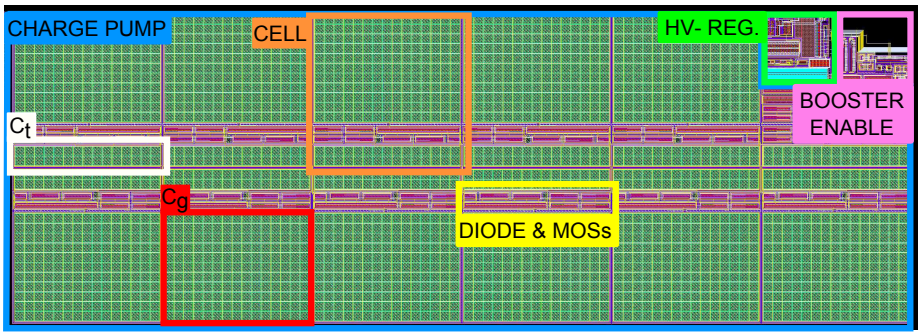


Figure 3.33: Voltage booster layout.

- **VSUB**: the substrate voltage ($0V$).
- **vddHC, vddHA**: cathodic and anodic high voltage pins to connect the $22nF$ off-chip capacitors to the correspondent charge pump output.
- **OutBstC, OutBstA**: test pads to measure the voltage before the HV-SW.
- **vddH**: test pad to measure the voltage after the HV-SW.
- **elref**: connection for the stimulation reference electrode.
- From **el7** to **el0**: these are the 8 output electrodes to be stimulated.

The silicon die (Fig. 3.35) was placed into a 84 pins package as depicted in Fig. 3.36.

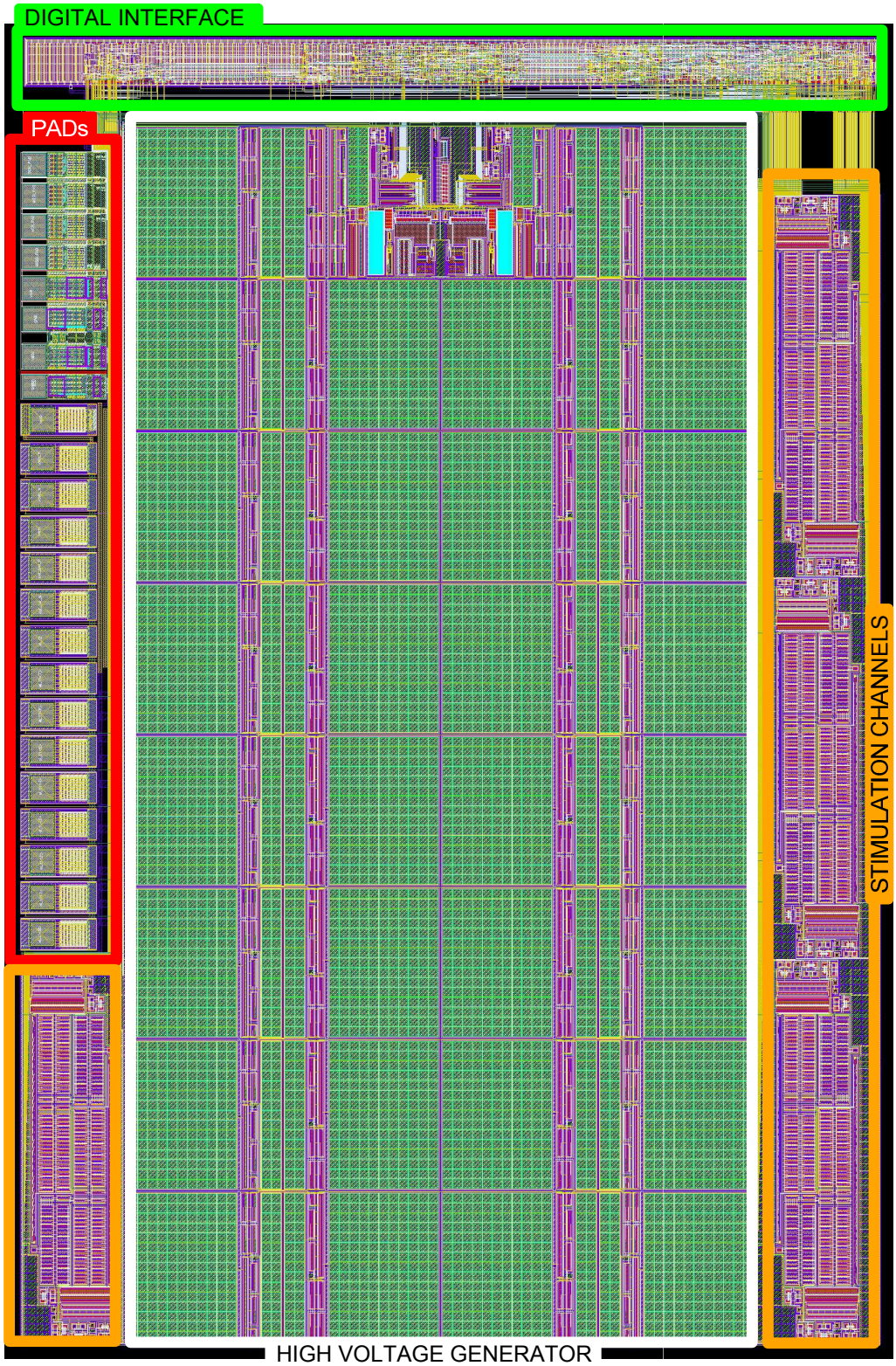


Figure 3.34: Complete layout of the designed 8-channels high voltage neural stimulator.

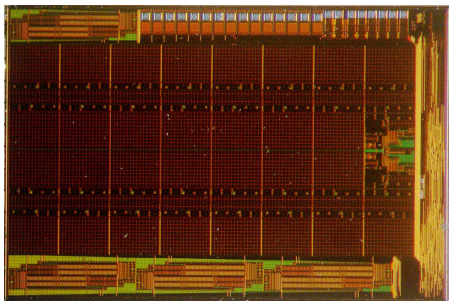


Figure 3.35: Designed silicon die.

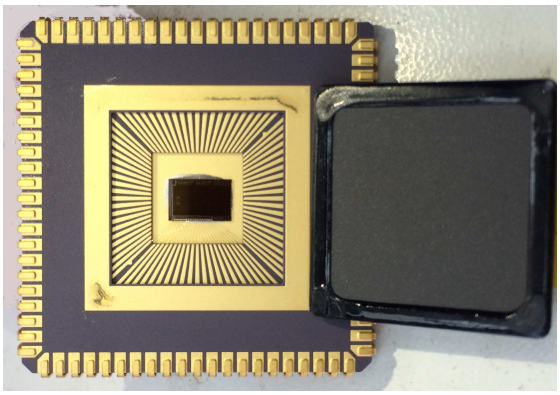


Figure 3.36: Designed IC into a 84 pins standard package.

3.6 Experimental results

In this Section, after a short presentation of the experimental set-up, the results of the IC experimental tests are shown: first the results obtained by means of laboratory measurements are discussed, then those achieved with the in-vivo tests.

3.6.1 Experimental setup

The developed IC is not a stand alone device and requires an additional frame to be hosted, configured and tested. Moreover, a digital system controller to manage the communication between the IC hosting frame and a PC is necessary. As a consequence, the Control System, depicted in Fig. 3.37, was developed. It is divided into two main parts: a custom designed Printed Circuit Board (PCB) and a digital system controller. The PCB is discussed in this section since the digital system was developed by another PhD student, named Nicola Carta.
The left part of the Control System contains the functional blocks that must be implemented

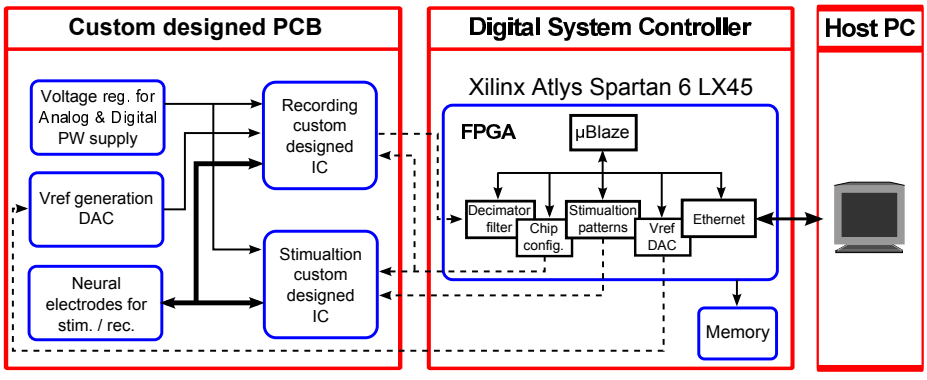


Figure 3.37: Architecture of the experimental setup.

in the PCB. The system core is composed by the two custom designed ICs: one for recording, described in Chapter 2, and the other for stimulation, presented in this chapter. The two chips have separate power supplies for the analog blocks and the digital interfaces. The digital power supply is derived from the digital control system board whereas the analog one

is provided by two independent voltage regulators embedded in the custom PCB. The Vref generation DAC block provides the voltage references needed for the chip proper working. Since the recording IC was previously tested, all modules for testing purposes are removed from the PCB and therefore the recording input signals can come from the neural electrodes only.
The right part shows the digital system controller which is an extension of the previously presented module in Section 2.6.1. In particular, some functionalities to control the stimulation chip were added and a wider FPGA board was selected. The whole digital system is implemented on a prototyping board (Xilinx Atlys Spartan-6 LX45) which main tasks are the implementation of the digital decimator band pass filter for the ΣΔ converter, the control of the peripherals hosted in the PCB, and the communication management with the PC by means of an Ethernet link. The on-board MicroBlaze processor has been used and, for each device hosted in the PCB, a custom controller has been developed. It is also possible to use a DDR memory available in the *Xilinx Atlys Spartan-6 LX45* in order to store temporary the data before being transmitted to the PC via Ethernet. Fig. 3.38 shows a picture of the two boards.

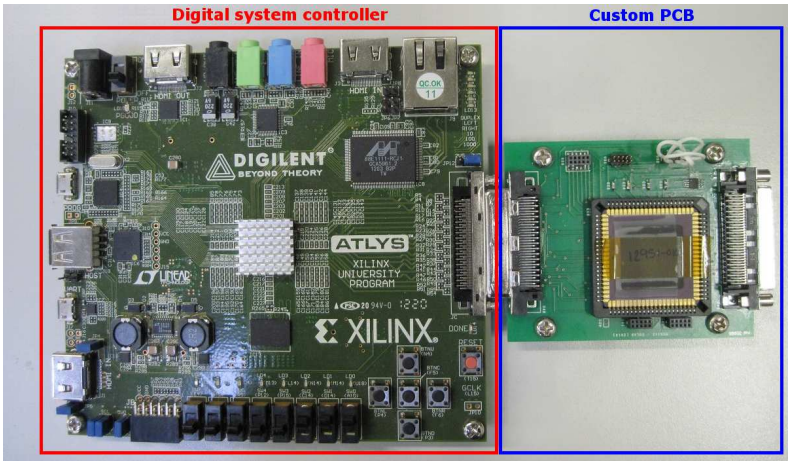


Figure 3.38: The control system.

In order to reduce the prototype dimensions a dual-face PCB was created and only essential components had been placed on it. As depicted in Figure 4 the PCB top face (a) hosts the stimulation chip and the bottom plate (b) hosts the recording chip. In addiction the board contains two 3.3V voltage regulators to generate the ICs' analog power supply, a voltage DAC to generate recording chip reference voltages and electrode and test connectors. Then a male VHDCI connector was placed on the left side of the PCB to directly connect the frontend to the FPGA (Figure 5, left) and a female VHDCI connector is hosted on the right side to connect the PCB via-cable to the FPGA (Figure 5, right). The via-cable interconnection is useful during in-vivo experiments to place the anolog frontend as far as possible closed to the test animal and so far from the noisy lab equipments.

Custom designed PCB

The board has been designed using the software *Cadence-Orcad Capture* for the schematic (Fig. 3.39) and *PCB Editor* for the layout (Fig. 3.40). In order to reduce the prototype size, a

dual-face PCB was created and only the essential components had been placed on it. Special care has been put on the layout, trying to minimizing the connections and keeping as symmetrical as possible the tracks carrying the most critical analog paths. Two different power supply were provided for the analog and the digital parts, in order to isolate the weak analog signals coming from the electrodes from the noise derived from the digital electrical grid. Wide ground planes have also been used as well as large tracks for ground and power supply paths. As depicted Fig. 3.41 the PCB top side (a) hosts the stimulation chip whereas the

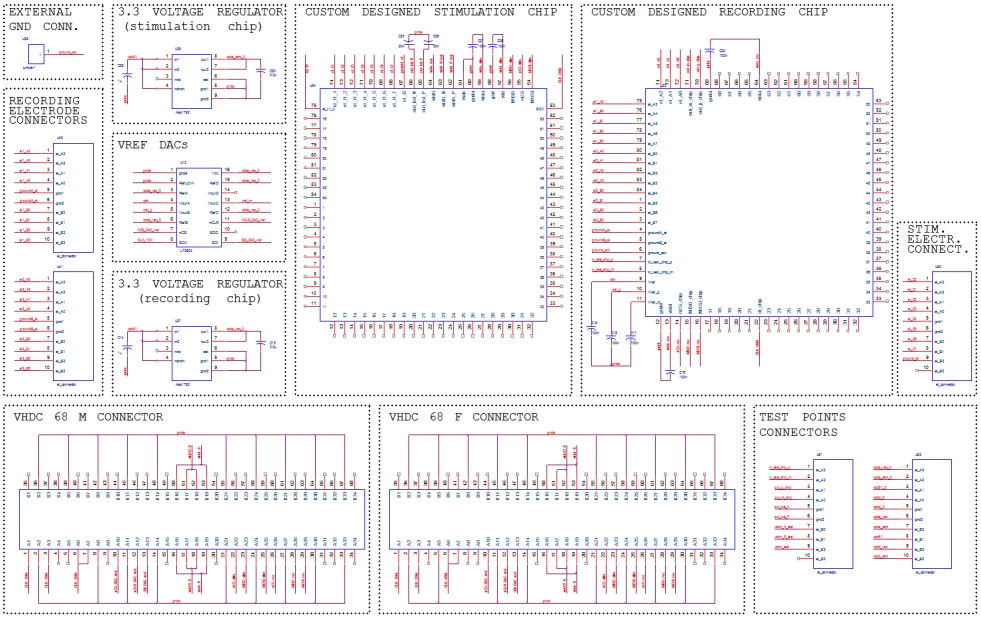
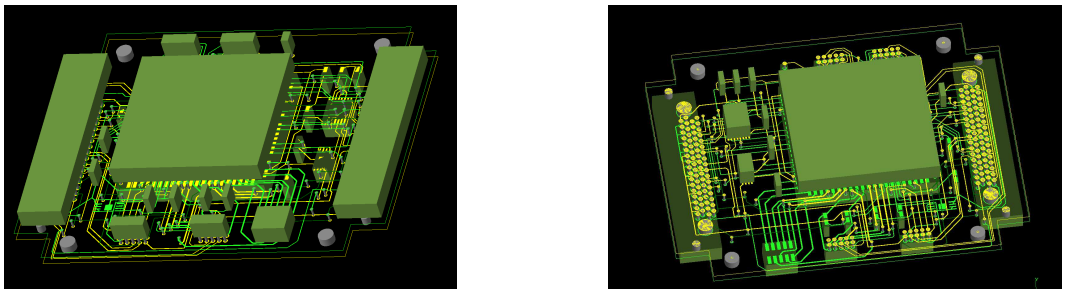


Figure 3.39: PCB schematic in *OrCAD-Capture* environment.



(a) Top side

(b) Bottom side

Figure 3.40: PCB layout in *OrCAD-PCB Editor* environment.

bottom (b) hosts the recording chip. In particular, the board contains:

- **A**: A 84 pin socket hosting the stimulation chip.
- **B**: A male *VHDCI* connector for the direct PCB connection to the FPGA board. All control signals exchanged between the two modules (the custom PCB and the digital system controller) transit through this link.

- **C**: A male *VHDCI* connector for the via-cable connection to the FPGA board. This additional link is useful during in-vivo experiments to place the anolog frontend as close as possible to the test animal and, therefore, far from the noisy lab equipments.
- **D**: An 8 pin connector for connecting the stimulation electrode.
- **E**: An 8 pin connector for testing purpose.
- **F**: The two off-chip accumulation capacitors of the stimulation chip's charge pumps.
- **G**: A 3.3V voltage regulator (*max1792*) for the stimulation chip's analog power supply generation, (the digital one is generated in the *Xilinx Atlys Spartan-6 LX45* board).
- **H**: Two 8 pin connectors for connecting the neural recording electrodes.
- **I**: A 84 pin socket hosting the recording chip.
- **J**: A 3.3V voltage regulator (*max1792*) for the recording chip's analog power supply generation, (the digital one is generated in the *Xilinx Atlys Spartan-6 LX45* board).
- **K**: A DAC (*LTC2604*) for the reference voltage generation, three reference voltage are needed to provide the necessary voltages to the chip: 1.65V (Vref), 0.65V (VrefN) and 2.65V (VrefP). The last two are needed for the proper working of the sigma delta modulator.

The whole designed bidirectional interface is depicted if Fig. 3.42.

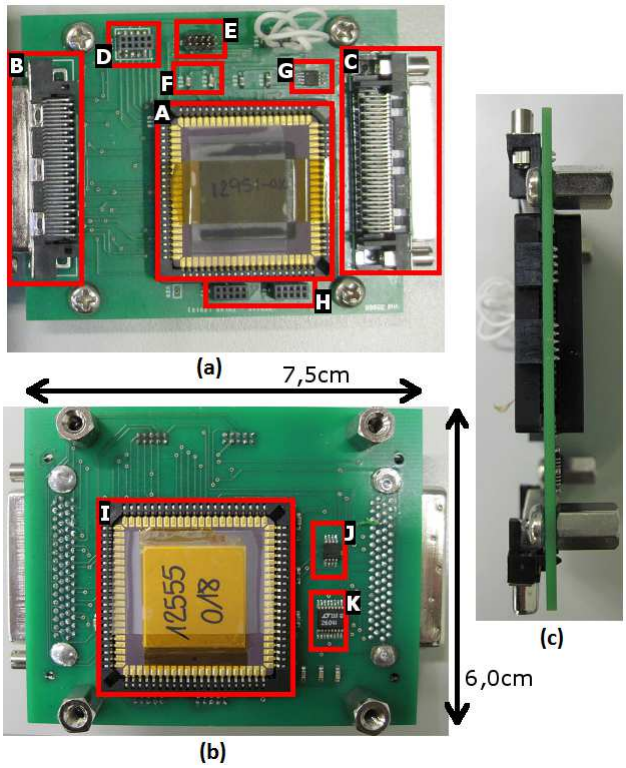


Figure 3.41: PCB modules.

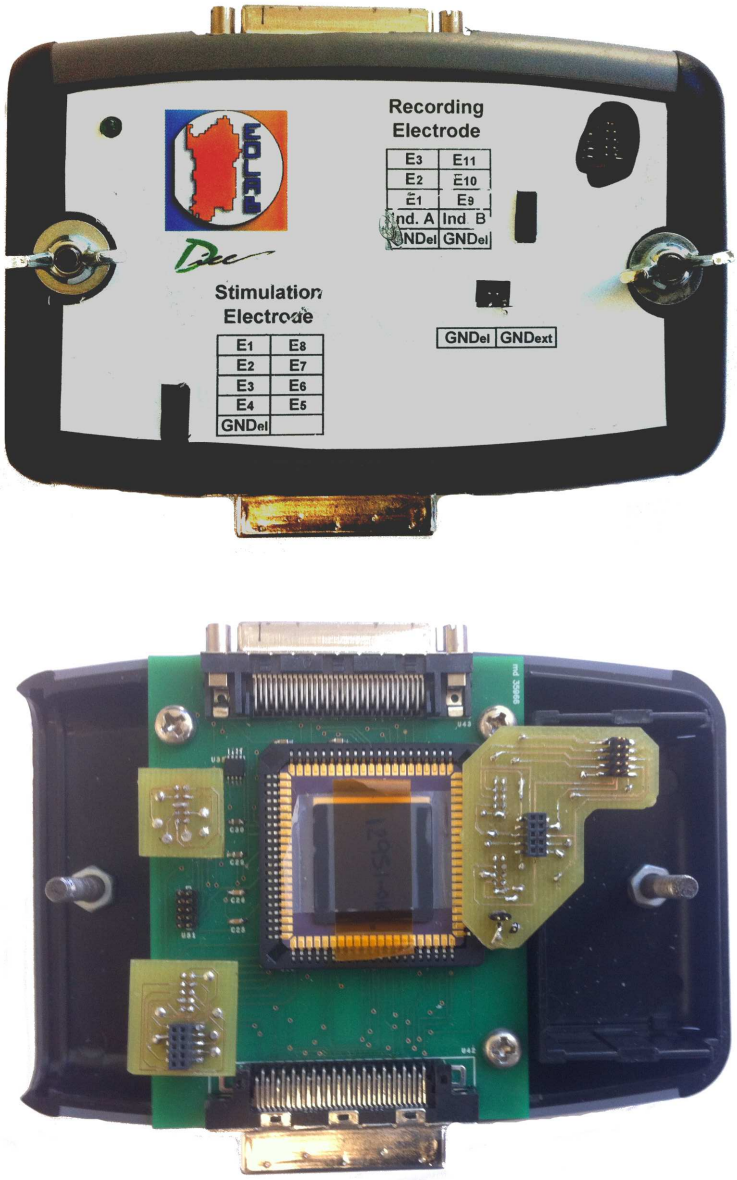


Figure 3.42: The complete developed prototype: bidirectional neural interface with both high and low voltage stimulation module and a recording unit.

3.6.2 Laboratory measurement results

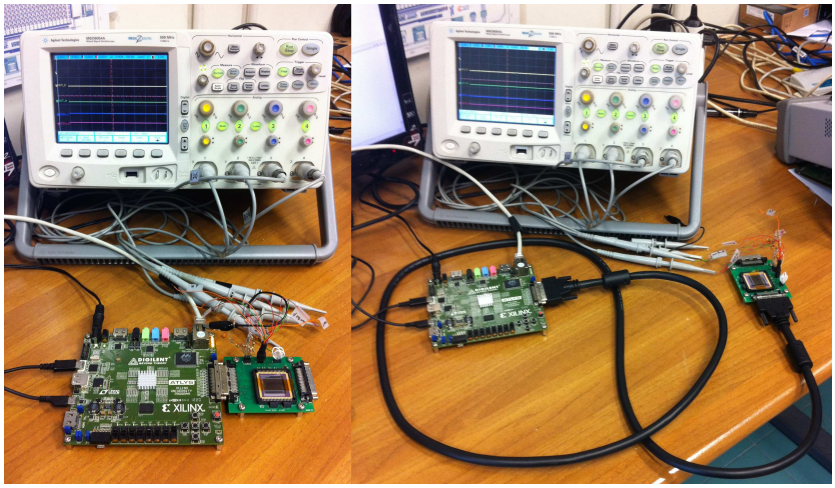


Figure 3.43: Measurement setup.

The first tests of the chip were aimed to verify its proper functioning from an electrical point of view. The measured power consumption of the whole developed prototype, including the voltage regulators, the voltage reference DAC and the two developed ICs (turning off the two voltage boosters), is $51.25mW$. After this preliminary test, more accurate measurements were performed to better characterized the different parts of the high voltage stimulator using the *MSO6054A* oscilloscope from *Agilent technologies* as shown in Fig. 3.43. To start with, both boosters were completely characterized in terms of high voltage programmability and boosting time. As depicted in Fig. 3.44, they can effectively generate an output voltage in the range $4.69-17V$ with steps of about $2V$, showing a boosting time of $9ms$ to reach the maximum voltage level (Table 3.12). Then, each stimulation channel was tested generating

Output Voltage [V]	Boosting time [ms]
4.65	1.80
6.78	2.68
8.92	3.23
11.15	4.94
12.91	5.66
15.03	7.78
17.03	10.08

Table 3.12: Boosting time of the designed high voltage generator.

and delivering different current patterns to resistors with different values chosen to emulate

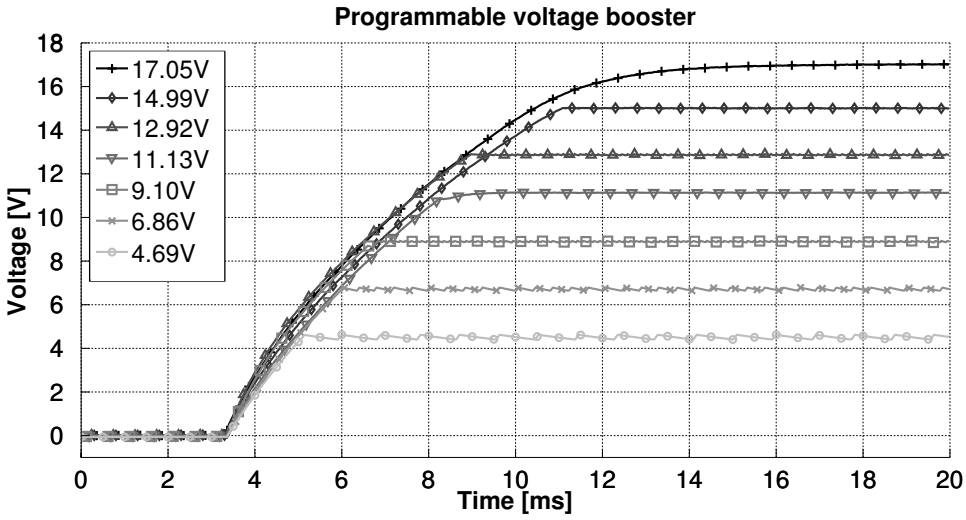


Figure 3.44: Booster programmable output voltage.

the electrode impedance. Fig. 3.46a refers to the injection of current pulses with an increasing amplitude into a $33k\Omega$ resistor and shows a stimulation current programmability from about $10\mu A$ to $310\mu A$ with steps of $10\mu A$, as expected. Moreover, a $400Hz$ pulse train with $152\mu s$ cathodic and anodic phase duration (worst conditions) was delivered to a $33k\Omega$ resistor. The complete pulse train with the C_{acc} discharge in correspondence of each cathodic (lower plot) and anodic (upper plot) phase is depicted in Fig. 3.46b. The same test was performed changing the electrode resistance to characterized the stimulator behaviour with an increasing load. A current saturation phenomena is encountered in the experimental result depicted in Fig. 3.45 in which a $400Hz$ train pulse with a phase width of $152\mu s$ is delivered to a $67k\Omega$ resistor with an increasing amplitude. In fact, it is possible to notice as the two curves at $220\mu A$ and $230\mu A$ are totally overlapped meaning that no more than $220\mu A$ can be delivered with this electrode impedance. If the resistance is further increased, the saturation phenomena occurs at a lower current value as shown in Fig. 3.47. In this case, a $400Hz$ pulse train with a pulse width of $56\mu s$ was delivered.

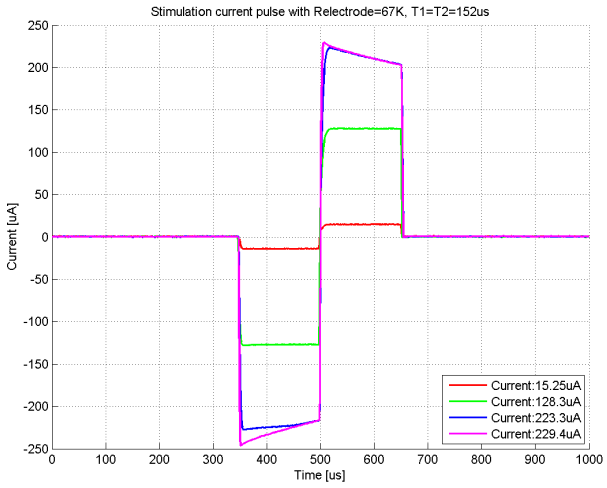
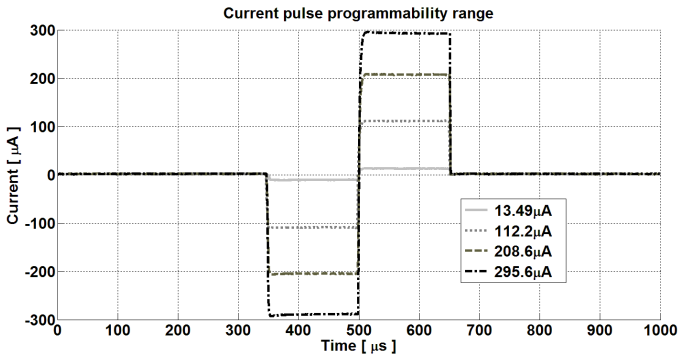
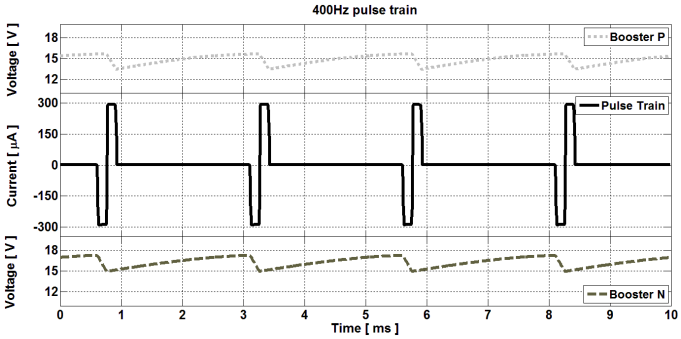


Figure 3.45: Current saturation phenomena with a $67k\Omega$ electrode resistance.



(a) Increasing stimulation current



(b) A 400Hz pulse train

Figure 3.46: Current stimulus delivered to a $33k\Omega$ resistor with $152\mu s$ anodic and cathodic phases: (a) current programmability range and (b) a $400Hz$ pulse train (central plot) with the correspondent booster discharges (top and bottom curves).

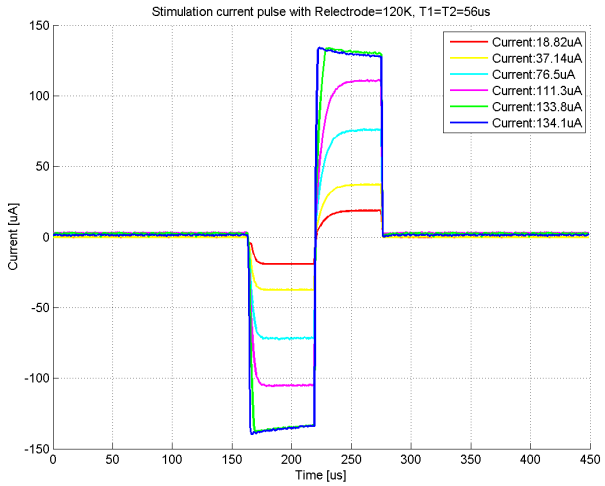
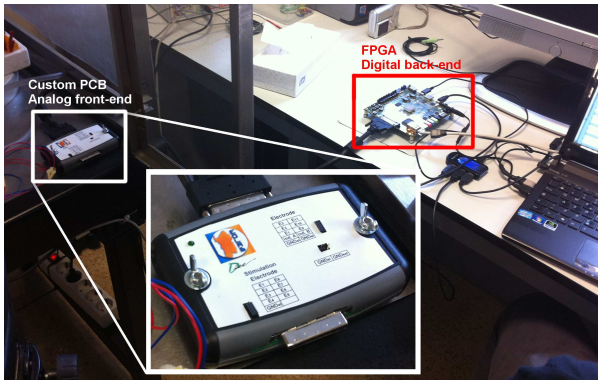


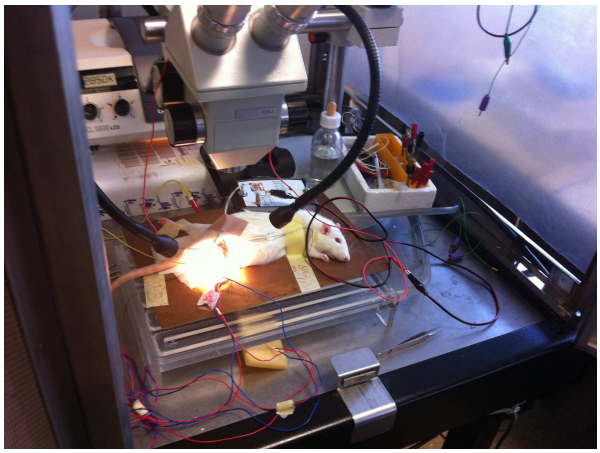
Figure 3.47: Current saturation phenomena with a $120k\Omega$ electrode resistance.

3.6.3 In-vivo experiment results

The in-vivo measurements have been performed on sedated rats at the Universitat Autonoma de Barcelona (Spain). An eight-channels TIME (Transverse Intra-fascicular Multi-channel Electrode) [23] was chronically implanted in the sciatic nerve of the animal. All processes were performed using a protocol approved by the local Ethical Committee. The tests were performed after a month from the electrode implantation, therefore the results should be considered highly representative of what can be obtained in a long-term implant, when the electrode-tissue interface is already degraded. In Fig. 3.48 two pictures of the experimental set-up with the chip connected to the neural electrode chronically implanted in the rat is shown. Moreover, two different needles were placed in the tibial (TA) and plantar (PL) mus-



(a) Bidirectional neural interface via-cable connected to the digital system controller.



(b) A 400Hz pulse train

Figure 3.48: In-vivo stimualtion setup.

cles to record the electromyographic response to the neural stimulation. The stimulation was generated with the chip while the muscle reaction was being recorded with commercial laboratory equipment. The nerve was subjected to electrical stimulation in each channel as depicted in Fig. 3.49, where the electrode 0 is the reference electrode and the electrodes

$1-8$ are the active stimulating sites. Train current pulses with a width of $50\mu s$, a period

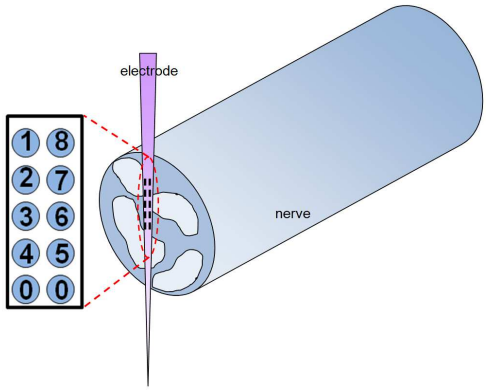


Figure 3.49: Electrode position in the nerve.

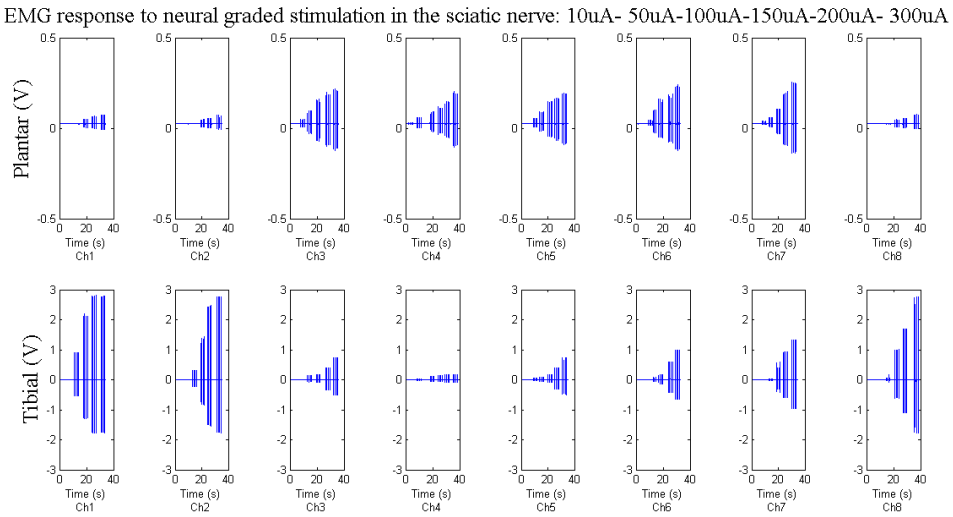


Figure 3.50: In-vivo stimulation results: electromyographic activity recorded in the tibial and in the plantar muscle in response to neural current stimulation.

of $1s$ and graded amplitudes in the range $10\mu A \div 300\mu A$ were injected the nerve. The results, presented in Fig. 3.50, show the reaction in the PL (upper plot) and in the TA muscles (lower plot): for all channels a graded muscular reaction was recorded coherently with the stimulus injected. It is relevant to note that the upper channels of Fig.3.49 (channels 1-2-8) evoke a major reaction in the tibial muscle while the lower ones (channels 3-4-5-6) are more devoted to stimulate the plantar muscle, while only the 7^{th} channel seems to be able to stimulate both muscles. This is a clear proof of the excellent stimulator selectivity that can elicit different neural fascicles with different active sites within the same electrode. This is even clearer looking at Fig. 3.52a where the Selectivity Index (SI) [190] for each channel is reported. It has been calculated as:

$$SI_i = \frac{\mu_i}{\sum_{j=1}^{m} \mu_j} \tag{3.5}$$

where m is the number of muscles involved in the experiment and μ_i is the percentage of recruitment of muscle i, calculated as the normalized value of the Compound Muscular

Action Potential (CMAP) [143]. The results confirm that channels 3-4-5-6 are dedicated to PL stimulation and, in particular, channel 4 is almost completely devoted to stimulate the PL while channels 1-2 and 8 are able to selectively elicit the TA muscle. The SI calculation helps also for channel 7 classification, even though in Fig. 3.50 it seems to induce a good reaction also in TA muscle, the correspondent SI is lower than 50% and channel 7 should be, therefore, classified as addicted to stimulate mainly the PL muscle. The capability of increasing the fibres elicitation using more channels contemporary has also been verified. In Fig. 3.52b, the percentage of fibres recruited versus the channels involved in stimulation is presented. In the inset of Fig. 3.52b, the channels involved in seven different trials are indicated. In all experiments a biphasic pulse waveform with a $50\mu s$ pulse width and an amplitude of $100\mu A$ was used. It can be observed that increasing the number of stimulating channels, the CMAP increases and, when almost all channels have been activated, saturates. It can also be noticed that different channels cause different increase rates in the CMAP response, this is a further confirmation of the stimulator selectivity. The introduction of channel 5, for instance, generates the higher step for the PL muscles but it does not affect in a significant way the TA muscular fibres. On the contrary, channel 2 has a deep impact on TA muscle but it does not cause any reaction on PL. Finally, the fibres recruitment in response to the pulse amplitude was evaluated. A graded stimulation with biphasic pulse amplitude in the range $10-300\mu A$ was used to stimulate channel 1, for TL muscle and channel 3 for PL muscle. The results, presented in Fig. 3.52c, show the progressive recruitment of all the muscular fibres for the PL (blue curve) and for the TA (pink curve) muscle, the plateau of the CMAP amplitude occurs, for both muscles, at $200\mu A$. In particular, Fig. 3.51 shows the increasing recorded response from the rat TL muscle.

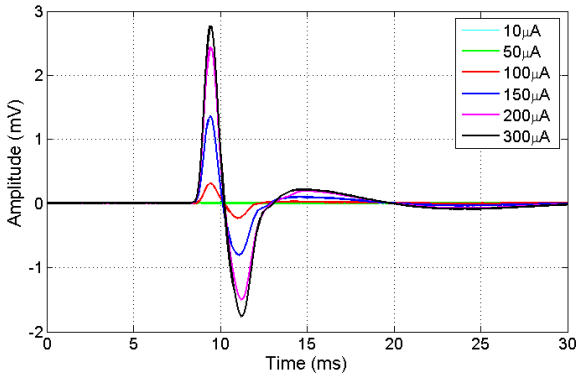
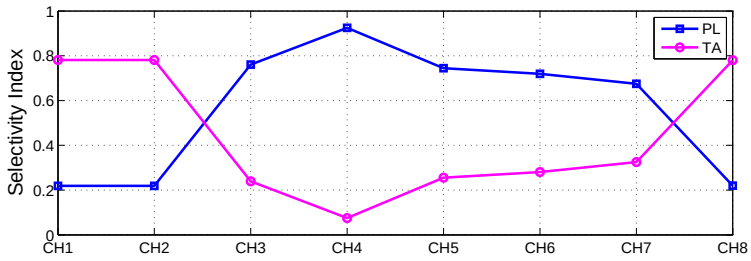


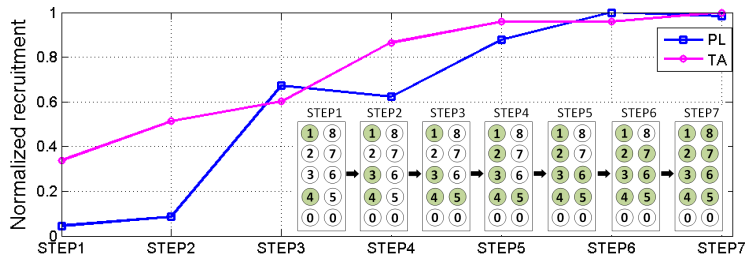
Figure 3.51: In-vivo test: tibial EMG response obtained by increasing the stimulation current of a single TIME active site.

3.7 Results discussion

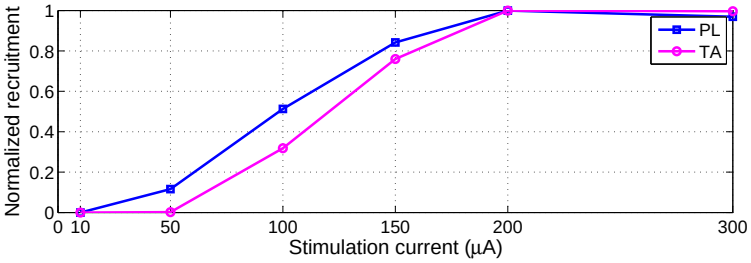
The proposed stimulation chip can deliver relatively high currents to impedances up to $50k\Omega$ which is a considerably higher value than that achieved with other approaches. The electrode contact impedance is a crucial aspect in peripheral neural stimulation, considering that it increases during the implant lifetime due to electro-chemical reactions at the tissue interface. Even a few days/weeks after the implant the impedance can grow up to tens of $k\Omega$[144], thus silencing the active site. In order to keep most of the electrodes alive, the



(a) Selectivity Index



(b) Normalized Recruitment vs Channels. The channels used in the different steps are indicated in the inset.



(c) Normalized Recruitment vs current

Figure 3.52: Stimulator performances.

supply voltage should be increased properly. This was the main aim of the proposed work and it was achieved thanks to the high voltage generator that provides voltages up to $17V$ in a boosting time of $9ms$. The programmable voltage regulator allows to increase the desired supply voltage following the degradation of the contact and preventing saturation of the output current. The drawback of such approach is the higher power consumption mainly due to the large number of stages in the Dickson charge pump. Power consumption was measured in different working conditions: the static power is $5mW$, while the total power (static and dynamic), measured during a biphasic pulse stimulation of $300\mu A$ in amplitude and a duration of $150\mu s$, is $29mW$. More than 50% of such power is lost in the transfer capacitors C_t, because of the large number of stages. Moreover, a large amount of power is dissipated because the chosen HV-CMOS process has large parasitic capacitances: around 30% of power

is dissipated by the bottom-plate parasitics of transfer capacitors. The achieved power efficiency is slightly lower than 10% which is the theoretical efficiency limit of a charge pump with 10 stages realized in a process with bottom-plate capacitors equal to 14% of the main capacitor, as calculated in [74]. Anyhow, power efficiency was not the main concern of the current implementation, which is aimed at experimental sessions with human volunteers lasting no more than 6-8 hours. Therefore, the design was not optimized in terms of power consumption, but rather in terms of delivered current, boosted voltage, area and recovery time. Nevertheless, even with present power consumption levels the device could be continuously operated for more than 70 hours with commercially available rechargeable batteries with a capacity in the order of $650 mAh$.

Chapter 4

Implantable package

Since the designed neural interface has to be implanted in the human body, a hermetic package to host the whole system is required. After an introduction on the state of the art of implantable packages, the specific requirements of the developed electronic encapsulation are discussed. As described in Section 4.4.2, a first 3D model of the container was created in order to better define and investigated the proposed solution before its realization. Finally, in the last part of the chapter, the entire package fabrication process is described along with some electrical test results to prove the system assembly.

4.1 State of the art

The package of an implantable system plays a fundamental role in protecting the host body and the implant device from harm. As fully discussed in Section 1.4.3, in order to protect the host body, there are a few important requirements and challenges:

- The implant should not have any toxic material and is sterilized;
- The surface of the implant should be biocompatible so that the implant will not irritate surrounding tissues;
- The implant surface temperature should not be much higher than the tissue temperature (less than $2^{\circ}C$ difference).

On the other hand, in order to protect the implant device, the package should satisfy the following:

- Protect the implant from water vapour and ionic chemicals to permeate through to cause current leakage and low resistance paths that degrade the function of the electronics;
- Protect the implant from mechanical damages in the body or during the implant operation;
- Insure the proper function of the implant over the desired lifetime.

The implantable package described in literature can be divided in two main categories: the hermetic and the non-hermetic containers. The formers protect the inner electronics assuring a low gas and ions permeability. Typical materials used for hermetic packages are metals, ceramics, and glasses. Metallic packaging generally uses a biocompatible metal capsule that is either machined from a solid piece of metal or deep drawn from a piece of sheet metal. Moreover, the signal exchange between the inner and the outer of the package is guaranteed by hermetic feedthroughs. They are often based on a ceramic or glass insulator that allows one or more conducting wires to exit the package without coming in contact with the package itself. This method has been successfully used for implantable pacemakers [51], cardioverter defibrillators [48], implantable multichannel neuromuscular stimulators [179], and CNS recording modules [112]. The main drawback of metal-based packaging is that they are not transparent to electromagnetic fields and, therefore, requires an external coil or antenna for power and data transmission increasing the overall system size. For this reason, other materials, such as biocermics and biograde glasses, are often used as alternative to the metals. They have been used as the main packaging materials for brain machine interfaces [163], vision prosthesis [131] and cochlear implants [202]. Typical ceramic materials used for structural applications are alumina [131] and zirconia [86]. Many different types of biocompatible glass have been successfully used for implantable medical devices such as the *BION* microstimulators [85]. However, even though the package is made of ceramic or glass, the use of metals for the feedthroughs is unavoidable. Thus, hermetic bonding between the ceramics or glasses and metallic/conductive components is essential requiring fusion welding methods, such as laser welding and electron-beam welding. Moreover, since these techniques typically require the use of high bonding temperatures, sometimes, they are too much high to be supported by the hosted system. As a consequence, alternative methods based on ceramic or glass metallization are used. The package constraints, such as its shape and dimension, strongly depend on the application and vary in order to perfectly match the specific body requirements. A common and efficacious design rule is to imitate the in-body surrounding environment in terms of materials hardness in order to reduce the risk of the body or of the package damage. For this reason, metallic, ceramic and glass packages are often covered by polymer-based materials that better match the Young's modulus of soft tissue. For example, Mestais et al. [112] use this approach in developing a CNS recording system hosted in a $50mm$ diameter silicone-coated titanium cylinder. A similar work that uses a silicon rubber encapsulation is described by Schuettler et al. in [163].

Other materials, often used to fabricate implantable packages, are polymers and due to their properties, the resulting container is non-hermetic. Typical materials are epoxy, silicone and parylene. Non-hermetic encapsulation is often used when the hosted system is composed by discrete components that are compactly arranged and "potted" in a mold with leads or conductive feedthrough pins penetrating through the polymeric encapsulation wall. Due to the simplicity, the low-cost and the relatively low processing temperature of this approach, it is often a good option for short term implants. In addition, the resulting packages are smaller compared to the hermetic ones. However, since polymers do not provide an impermeable barrier against the in-body moisture, in long term implants, some corrosive degradation processes with a consequent system failure can occur. Moreover, in general, polymer encapsulation is unsuitable for high-density and high voltage electronics circuits. From this discussion, it is clear that each material has its pros and cons and due to the huge variety of requirements to be satisfied, it is not easy to find a single material that perfectly fits the purpose. In fact, many works in literature ([163, 112, 131, 85]) show that the only way to

overcome the biostability, biocompatibility and hermeticity issues, is to proper combine different materials in order to exploit their advantages. Several materials commonly used for fabricating implantable packages are discussed in Section 1.4.3 and collected in Table 1.2.

4.2 Design specifications

In order to complete the realization of the bidirectional neural interface, a hermetic implantable package for housing the developed system was designed. First of all, since the package has to be implanted in humans, special care is required in the materials selection. As for all implantable devices, the materials have to be biocompatible and biostable in order to protect the container itself and the surrounding tissues from damages.
As introduced in Section 1.4.1, the signals we want to acquire from the nerve are very weak compared to the noisy surrounding environment. Therefore, a good solution is to place the electronic interface as close as possible to the source of the signals, thereby close to the nerve in which the electrode are implanted, in order to reduce the noise injection in the interconnection wires from recording unit to the implanted electrodes. Since the target application of our system is to restore the hand functionalities of an amputee by directly connecting the nerves of the limb, only a few space is available to accommodate the electronic interface. In this case, the system miniaturization is one of the main constraint in the package design. Nevertheless, the system has to be large enough to host the developed interface with the minimal surrounding components that it requires for properly working. Considering all these factors, a non-hermetic package could be a good choice to obtain a compact solution. However, as introduced in the previous section, non-hermetic packages are not suitable for long term implants that is another constraint of our application, moving the attention on the hermetic containers.
The bidirectional interface proposed in this thesis is a preliminary solution and therefore it does not include all the features that the final system would have such as a wireless module for power and data transmission that is here based on a wired link. However, in order to get a package that might be used also in a future version of the device, a container, transparent to electromagnetic fields, is required considering the possible integration of a coil or an antenna for power and data transfer. Table 4.1 summarizes the package design specifications.

Package Design Specifications
Biostability
Biocompatibility
Hermeticity
Small dimensions
Transparent to electromagnetic fields

Table 4.1: Package design specifications.

4.3 System architecture

Since a minimum-size interface is required, only the essential components are included in the implantable package, as depicted in Fig. 4.1. Its main body includes the two designed ICs, for neural signal recording and stimulation, the two off-chip accumulation capacitors required by the stimulation chip, a humidity and temperature sensor and some bypass capacitors for stabilizing the voltage supply of the different modules. The humidity and temperature sensor was embedded for testing purpose only. In fact, it is useful to monitor the package inner environment during the hermeticity tests and the accelerated life-time experiments in order to evaluate the time in which the critical humidity concentration is reached. This allow to predict how long the package will last inside the hostile body environment. In addition, 31 hermetic feedthroughs allow the device communication with the external

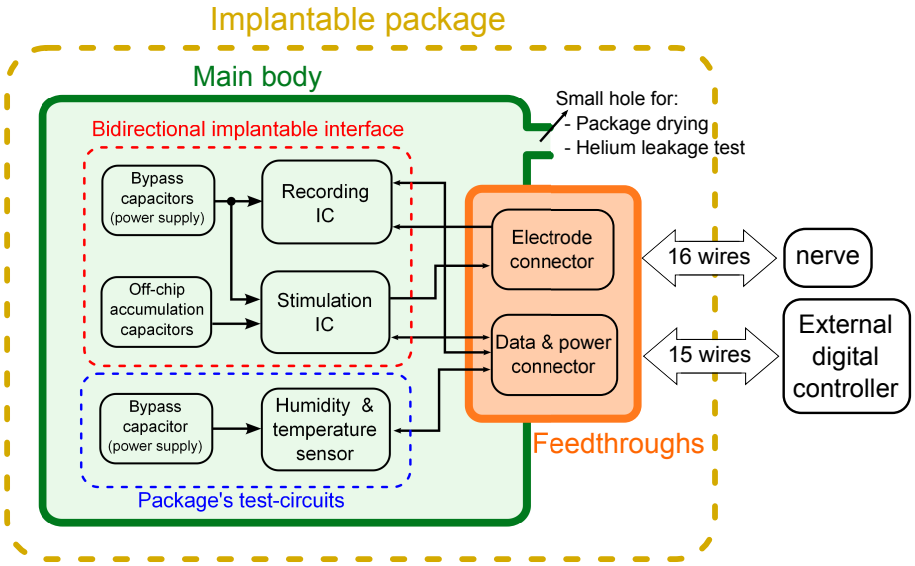


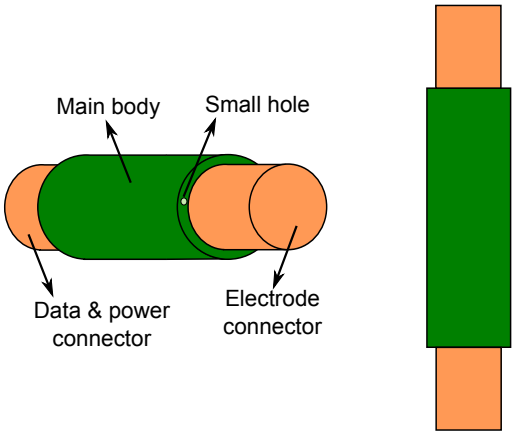
Figure 4.1: Block diagram of the whole system.

environment. Even hough the developed interface has only eight channels for both recoding and stimulation, a 16 pins electrode connector is included considering a future system expansion by developing 16 channels recoding and stimulation ICs or simply doubling the already developed interface. A further 15 pins connector is necessary for delivering the low voltage ($3.3V$) power supply and the reference voltages (required by the recording IC) to the device and for the data exchange between the analog front end and the remote controller including the custom ICs' SPI bus and the humidity sensor's data and control lines.
Once the whole package had been assembled, only a small opening has still to be closed. It is the tiny hole in the package's main body (Fig. 4.1), required for serving two main tasks: first of all it allows the residual water vapour to get off the container during the package drying step and secondly it allows the helium molecules to enter the package before being completely sealed. The package sealing in helium atmosphere is the preliminary phase required by the helium backfilling technique. It is a common methods for evaluating the package hermeticity. In particular, after the package was filled by the helium and the tiny hole was closed by a small soldering ball, the next step is to measure the helium leakage rate (L_{He}) by using a mass spectrometer. This value is then converted into the correspondent water vapour leakage rate (L_{H_2O}) according to $L_{H_2O} = 0.471 \cdot L_{He}$. The L_{H_2O} parameter with the package inner volume

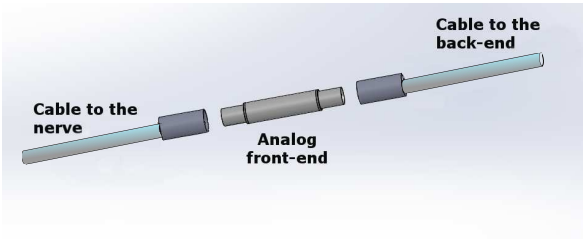
V can be used to estimate, according to Eq. 4.1 ([5]), the necessary time t to reach, inside the package, a certain amount of water vapour Q_{H_2O} that is considered dangerous for the hosted system. The Q_{H_2O} value can be computed with the following formula $Q_{H_2O} = c \cdot P_i$, where c is the maximum moisture concentration allowed in side the package (see Section 1.4.3) and P_i is the pressure inside the package, whereas the parameter Δpi_{H_2O} is the partial pressure of water in the human body ($\Delta pi_{H_2O} = 61.81 mbar$).

$$t = -\frac{V}{L_{H_2O}} \left[ln\left(1 - \frac{Q_{H_2O}}{\Delta pi_{H_2O}}\right)\right] \tag{4.1}$$

In order to minimize the system impact in the human body, the package depicted in Fig. 4.2a was designed. It must be wide enough to host all components of Fig. 4.1 and has a prolate shape that, reproducing the human arm form, better fits the small space available in the host body. Since the developed interface is very compact, it allows to get a tiny package that can be considered as a small rigid insertion along the cable that goes from the implanted electrode (in the nerve) to the remote digital controller, as shown in Fig. 4.2b. The pack-



(a)



(b)

Figure 4.2: Model of the proposed package.

age main body consists of a rigid tube that contains the developed electronic interface with two caps hermetically sealed at its extremities that serve also as support for the hermetic feedthroughs. Moreover, one of the two caps contains also the small hole for the package drying and sealing in helium atmosphere. Having a ceramic rigid structure, the package is able to protect the inner electronics against human arm movements or hits, but it is to

hard compared to the surrounding tissues Young's modulus. For this reason, a further covering with a proper polymeric material is required in order not to hurt the tissue. For what concern the hosted system, a custom PCB was designed to accommodate all the electronic components of Fig. 4.1. The PCB is fixed inside the container and wired to the package feedthroughs.

4.4 System implementation

In the following section, more details on the materials selection and on the system implementation are provided. In addition the complete fabrication process of all different parts that compose the package is described.

4.4.1 Materials and components selection

As introduced in Section 4.2, even though this first prototype of the system uses a wired connection for powering and data transmission, a package that enables a future integration of an electromagnetic coupling with the external controller has to be developed. Thus, materials, transparent to electromagnetic fields, such as glasses and ceramics are possible solutions for our package. Considering also the biocompatibility and the biostability requirements, suitable materials typically used in literature are Alumina (Al_2O_3), Zirconia and different type of glasses. As depicted in Fig. 4.2b, the proposed neural interface connects on one side the electrode implanted in the nerve and on the other side the remote digital controller. Due to the lack of real implantable microconnectors and in order to simplify the realization of this first prototype, a commercially available nano-connector from Omnetics was selected. Being non-implantable, a proper structure, described in the following, was designed to make it suitable for the human implantation. These connectors are mainly composed of polymeric materials that do not support working temperature above $125°C$ and allow mounting temperatures up to $360°C$ for no more than $10s$. Therefore, a limit to the maximum assembling temperature of the whole package is imposed. This excludes the possibility of using typical non-metals fusion welding methods that often require temperatures above $1000°C$. In this cases, others joining techniques based on material metallization are used. They allow to join materials, even of different nature, by "simply" soldering together the two metallized parts at relative low temperatures between $300°C$ and $400°C$ and, therefore, suitable for our application. By considering all these factors and the considerable laboratory expertise in fabricating Alumina packages, this material was chosen for the package's main body and its side caps. Whereas, about the metallization of the ceramic joint parts, a commonly used platinum/gold alloy was selected. It is a paste that can be easily processed with a good adhesion on Alumina substrates and with a soldering temperature of $250°C$. In addition, to better match the surrounding tissues softness, the silicon rubber was chosen as material to completely cover the package after being hermetically assembled. The silicon rubber is a biocompatible material often used in implantable devices and has a high adhesion with the ceramic surface reducing the risk of water vapour condensation at the interface. For what concern the PCB aimed to accommodate the electronics of the hosted system there are no strong requirements in the materials selection since it is hermetically enclosed by the package. However, different solutions are available among flexible and stiff materials. A flexible Polyimide PCB is not the best choice since, in order to reduce the hosted system size, we decided to use the bare silicon

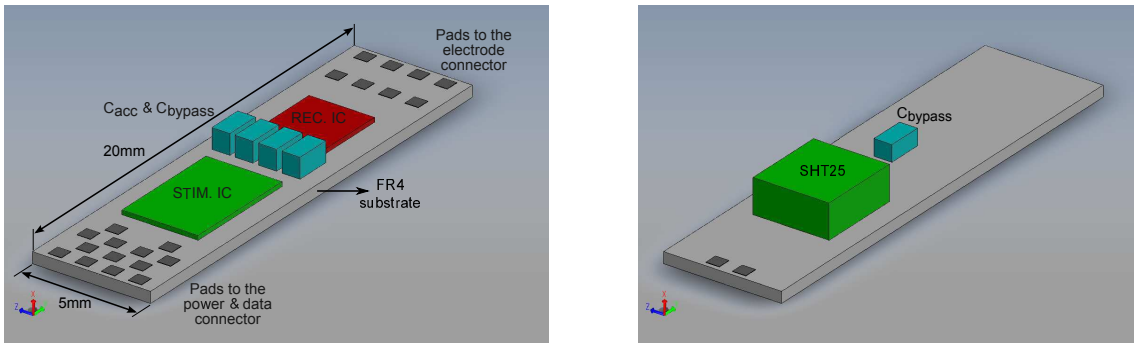
die, of the developed ICs, directly wire-bonded to the PCB. Therefore, due to the fragile interconnections, a rigid substrate is preferable. Among the possible solution a standard $FR4$ substrate was selected. All electrical components were chosen with high electrical safety margins and with a minimum package size. In particular, a $22nF-50V$ and a $100nF-25V$ ceramic capacitors with a 0402 ($1mm \times 0.5mm \times 0.5mm$, LxWxD) package were selected for the charge-accumulation (C_{acc}) and the bypass (C_{bypass}) capacitors, respectively. Finally, the compact device ($3mm \times 3mm \times 1.1mm$, LxWxD), *SHT25* by *Sensirion*, which includes both temperature and humidity sensors was included in the design. To conclude with the materials selection, the *MP35N* Nickel-Chromium alloy (35% Ni, 35% Co, 20% Cr, 10% Mo) was chosen for the interconnection wires between the PCB and the package feedthroughs. Being a high combination of strength, high modulus values and good corrosion resistance, it is often used in medical field and it results also suitable for our application. All the selected materials with their correspondent application in designed package are collected in Table 4.2.

Material	**Application**
Alumina (Al_2O_3)	Package main body & lateral caps
Pt-Au paste	Metallization of ceramic joint parts
Silicon rubber	External package covering
MP35N	Interconnection wires (PCB-feedthroughs)
FR4	PCB

Table 4.2: Selected materials and their application.

4.4.2 Package 3D model

Before proceeding with the package realization, in order to guide its design and to define the fabrication steps, a real-scale 3D model of all different parts was realized with the *SolidWorks* Computer-Aided Design (CAD) software. The first modelled component is the hosted system and, therefore the PCB, since it defines the minimum package size. Considering the size of the developed ICs and all the other components to be fixed on it, the model, depicted in Fig. 4.3, was created. It is a minimum-size ($5mm \times 20mm$) double face FR4 PCB, containing all components specified in the system diagram of Fig. 4.1. The two developed ICs, their bypass capacitors (C_{bypass}) and the stimulator's accumulation capacitors (C_{acc}) along with the pads to connect the package feedthroughs are placed on the PCB's top face whereas the humidity and temperature sensor with its bypass capacitor are placed on the bottom face. The defined components displacement is due to the decision of keeping all parts of the 8 channels bidirectional neural interface on the same PCB's face and the electronics for the package testing on the other side. In this way, after the package will be completely tested, the testing-purpose components can be removed, completely freeing the PCB's bottom face that can be used for hosting a second bidirectional neural interface, obtaining a 16 channels device. Once the hosted device had been defined, the model of the package's main body was designed as depicted in Fig. 4.4. It is a cylinder with an inner diameter of at least $5.5mm$ and a length of $21mm$ to accommodate the micro PCB and the package feedthroughs with the related interconnection wires. Moreover, both extremities of the tube are metallized to



(a) Top face (b) Bottom face

Figure 4.3: Model of the micro PCB for hosting (a) the bidirectional neural interface and (b) the electronics for the package testing-purpose.

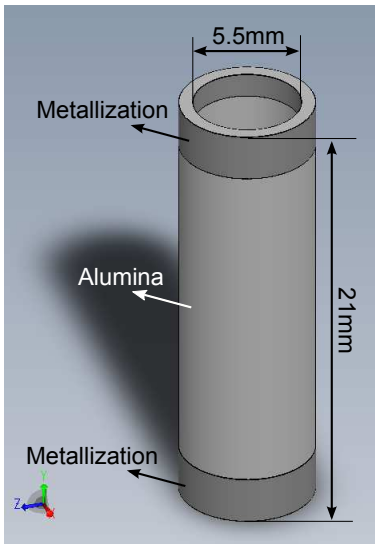


Figure 4.4: Model of the package's main body.

enable a low temperature joint with the two side caps. In order to accommodate the female Omnetics connectors which model is shown in Fig. 4.5, the ceramic caps depicted in Fig. 4.6 and Fig. 4.7 were designed. They have an external circular metallization to be hermetically soldered to the package's main body. Moreover, 16 metallized through-holes are placed on each cap so that the Omnetics connector's pins can reach the inner part of the package and be soldered to the cap it self, creating the hermetic feedthroughs. The cap in Fig. 4.6 has a diameter of $5.35mm$ so that it can pass through the $5.5mm$ tube simplifying the package assembly as will be later discussed, whereas the one in Fig. 4.7 has a step lateral profile with a inner diameter of $5.35mm$ and an outer diameter of $6.5mm$. In this way, the thinner side of the cap partially goes inside the tube guiding the cap alignment to the centre of the tube, whereas the opposite wider surface can better accommodate the metallized through-hole for the package drying and sealing at helium atmosphere (for more details see Section 4.3). The design of the cap's through-holes for accommodating the Omnetics connector's pins required special attention and it was realized with the collaboration of the PhD student Paul Cvancara from the BMT-IMTEK laboratory. Each hole has a diameter of $0.3mm$ to let the Omnetics pin go through it and a bottom through-hole thin channel to host the *MP35N* wire

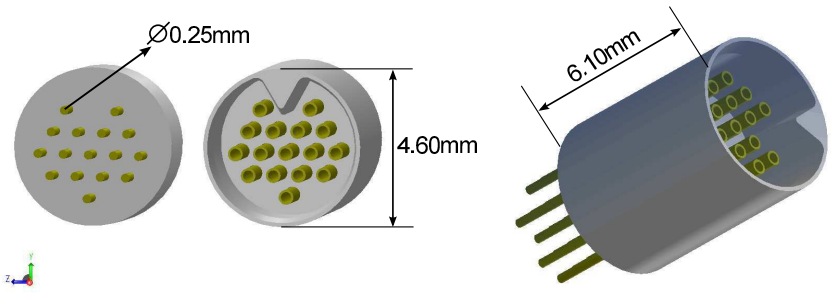
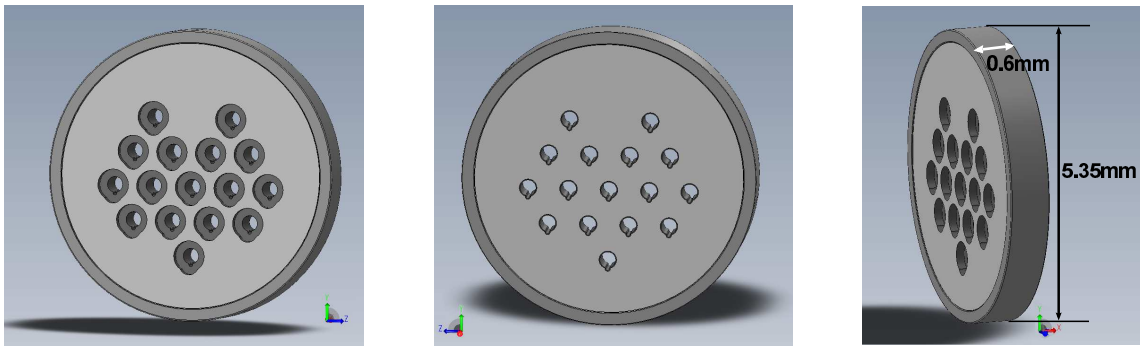


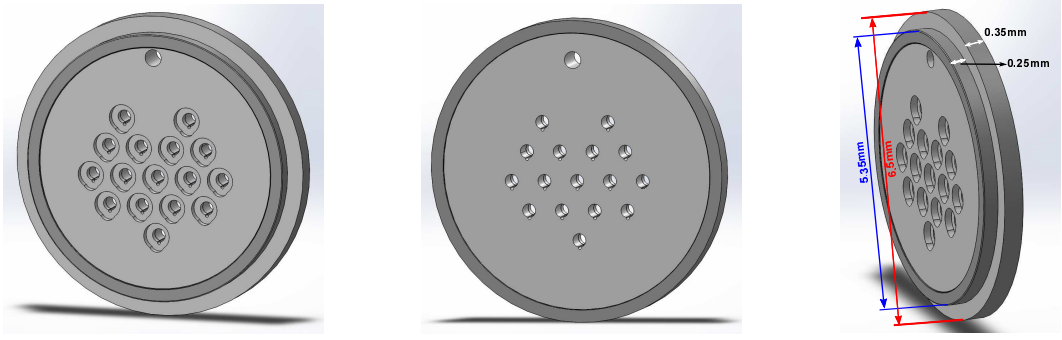
Figure 4.5: Model of the 16pin female Omnetics connector.

that connect the package feedthrough to the internal PCB. In addition, from Fig. 4.6a and Fig. 4.6b it is possible to notice the different shape that the holes have in the two sides of the cap. In particular, on the internal side, where the interconnection wire and the Omnetics pins have to be soldered, a wider ring was created around each hole to accommodate the metallization layer and the solder. The ring has a diameter of $0.5mm$ and a depth of $80\mu m$, as depicted in Fig. 4.8.



(a) Internal side (b) External side (c) Lateral view

Figure 4.6: Model of the package's ceramic cap with the small diameter: (a) the package-internal side, (b) the package-external side, (c) a cap lateral view.



(a) Internal side (b) External side (c) Lateral view

Figure 4.7: Model of the package's ceramic cap with lateral step profile: (a) the package-internal side, (b) the package-external side, (c) a cap lateral view.

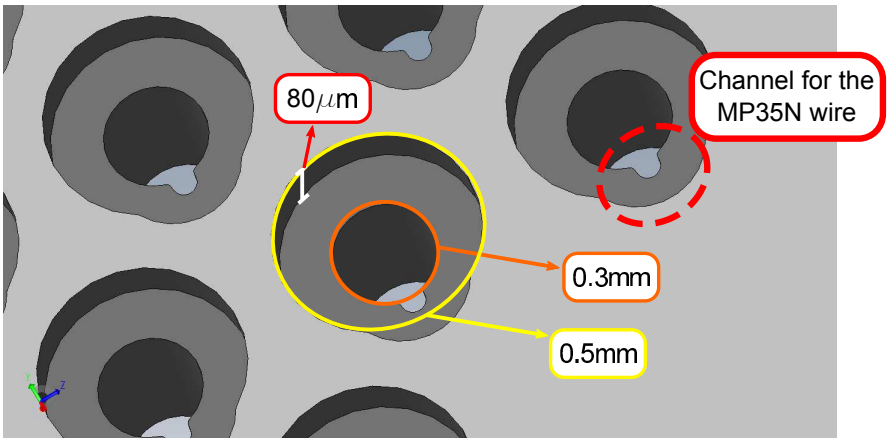


Figure 4.8: Zoom on the cap's feedthroughs.

The section view of the whole package model is depicted in Fig. 4.9. It has an overall length of 33.2mm and an internal diameter of 5.5mm. The external diameter has not be fixed at this first stage of the package design since it depends on the constraints of the technological process of the ceramic manufacturer. As previously introduced, the Omnetics

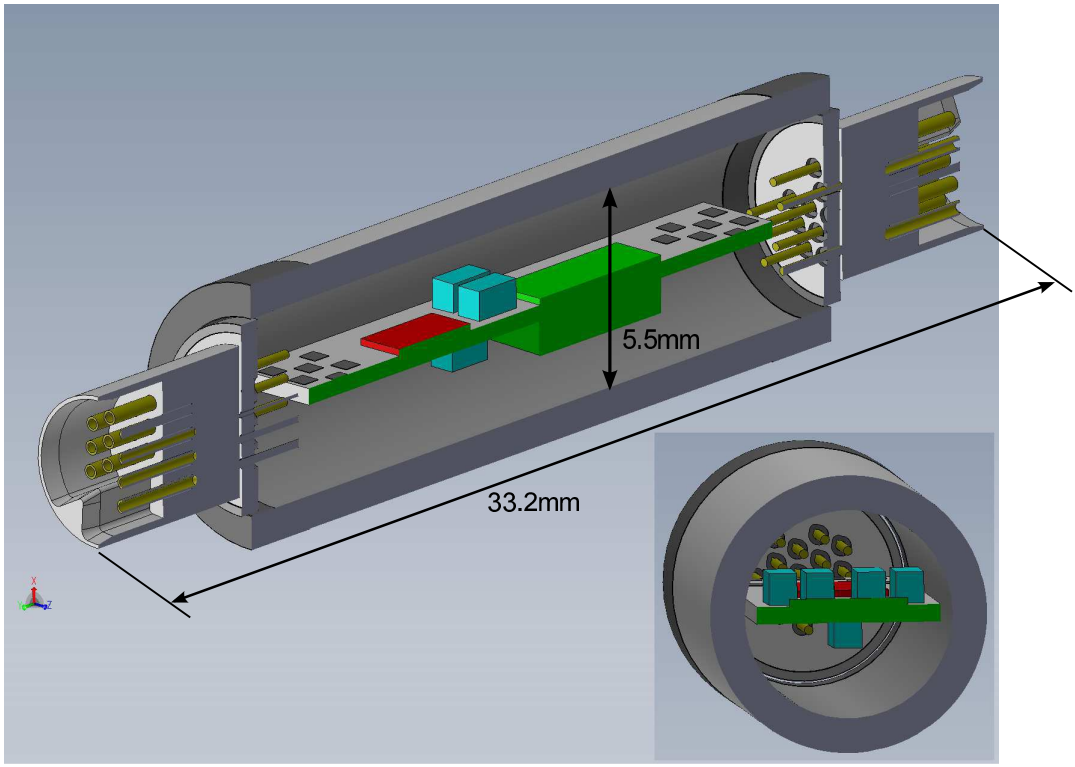


Figure 4.9: A section view of the complete designed package for the neural interface.

connectors suit our application because they are very small, but they are not implantable. For this reason, an additional encapsulation for protecting both female and male (Fig. 4.10) (on the cable side) Omnetics connectors has been developed, taking inspiration from the already designed package. The proposed connector's package is depicted in Fig. 4.12. It consists of an Alumina cylinder (Fig. 4.11) with an internal diameter 300μm wider than the

external diameter of the neural interface's package. Both tube extremities are metallized to be soldered, on one side, to the ceramic (Al_2O_3) cap, depicted in Fig. 4.11, that hosts the male Omnetics connector, and, on the other side, to the external metallization of the neural interface's package as depicted in the section view of Fig. 4.13. Finally, the complete section view of both designed packages is depicted in Fig. 4.13, in which the package of the neural interface is highlighted by a green rectangle. The developed 3D model was use not only to

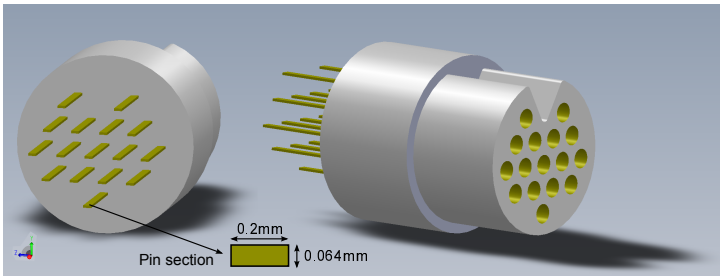


Figure 4.10: Model of the 16pin male Omnetics connector.

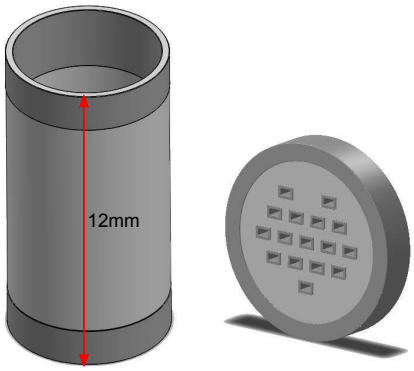


Figure 4.11: Different parts of the connector's package: the Alumina tube on the left and the Alumina cap on right.

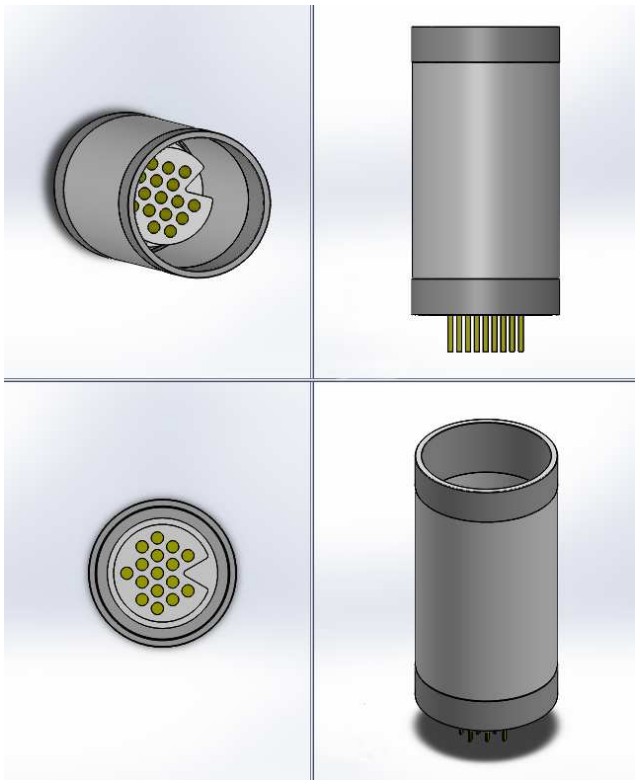


Figure 4.12: Different views of the complete package for the Omnetics connector.

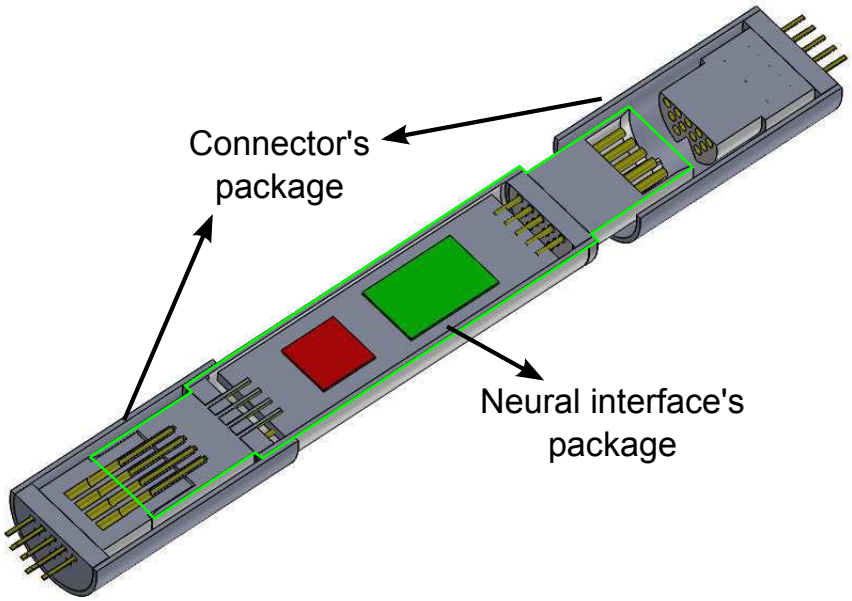


Figure 4.13: A section view of the complete designed package.

define the dimensions of the package's components but also to determine the more convenient way to assembly the whole structure. The resulting mounting phases are depicted in Fig.s 4.14, 4.15, 4.16, 4.17, 4.18. The first two steps, that respectively consist in mounting all electronic components on the PCB and fixing the Omnetics connectors to the ceramic caps, can run simultaneously. At a later stage, the Omnetics connectors are connected to the PCB by means of the *MP35N* wires. At this point the whole assembly is inserted inside the tube on the side of the Omnetics connector with the smaller cap. This is the reason why one of the two caps was designed in a way that it can go through the ceramic tube. At this point, the two ceramic caps are soldered to the ceramic tube keeping open the small hole on the larger cap. It is closed only in the final step, after the package had been dried and filled with helium. Even though both packages had been designed, only the one that host the bidirectional neural interface was developed. Its main fabrication steps are described in the following section.

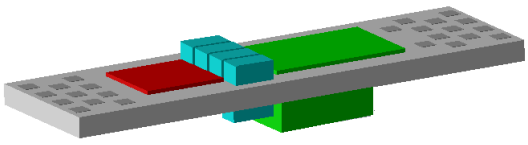


Figure 4.14: Package assembly, phase 1: hosted system assembly on the micro PCB.

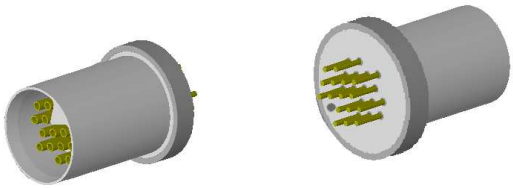


Figure 4.15: Package assembly, phase 2: make the hermetic feedthroughs.

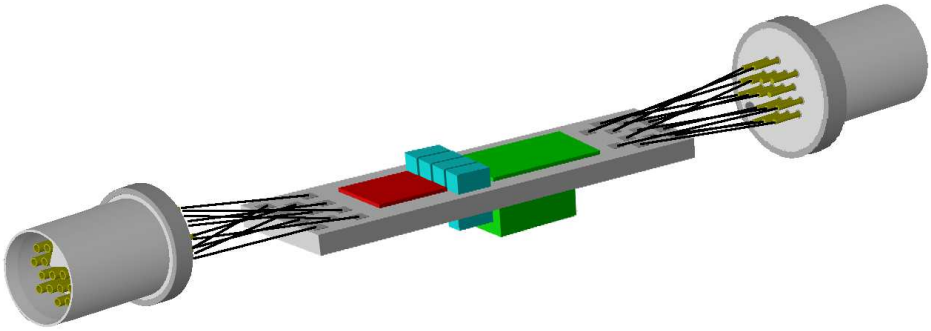


Figure 4.16: Package assembly, phase 3: connect the hosted system to the hermetic feedthroughs.

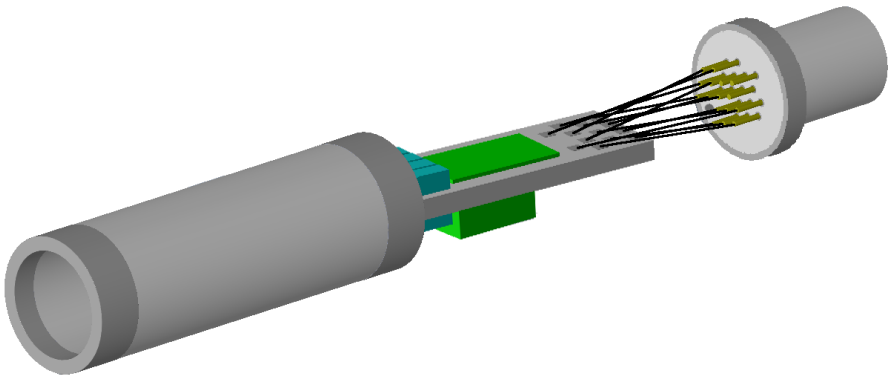


Figure 4.17: Package assembly, phase 4: insert the hosted system in the ceramic tube.

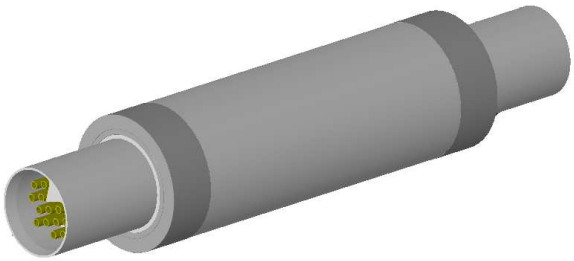
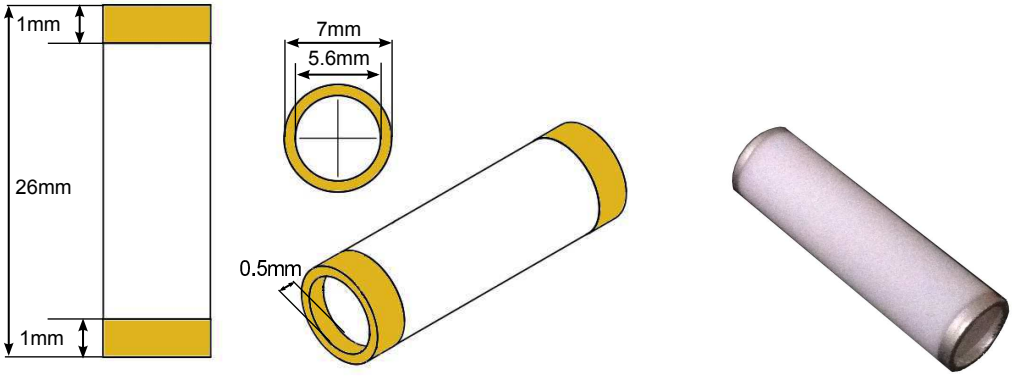


Figure 4.18: Package assembly, phase 5: solder the tube to the side caps.

4.4.3 Manufacturing process

In this section the complete manufacturing process of the package for hosting the 8channels bidirectional neural interface, described in Chapters 2 and 3, is presented. The assembly of the whole package and the Alumina cap fabrication were completely processed in the BMT-IMTEK laboratory and, therefore, they are fully detailed in the following. Whereas, the Alumina tube (Fig. 4.19b) and the Omnetics connectors (Fig. 4.20) were bought from external suppliers. According to the technology process of the *BCE Special Ceramics GmbH* company, the ceramic tube, depicted in Fig. 4.19a, was designed with an inner diameter of $5.6mm$, a wall thickness of $0.7mm$ and a Pt-Au annular metallization of $1mm$. For what concern the micro PCB, it was designed and assembled in the lab and manufactured by the Multi Circuit Boards company. Thus, only the first two steps are described in this section.



(a) Drawing (b) Manufactured part

Figure 4.19: Alumina tube: (a) drawing and (b) manufactured part.

Figure 4.20: A 16pins female Omnetics connector.

The hosted system

Since the hosted system was implemented on a micro PCB, this is the first element here presented. The board has been designed using the software *Cadence-Orcad Capture* for the schematic (Fig. 4.21) and *PCB Editor* for the layout (Fig. 4.22). Special care has been put on the layout, trying to minimizing the connections and the overall PCB size. As previously discussed (Section 4.4.2), all elements that composed the bidirectional neural interface (the two custom ICs and the accumulation and bypass capacitors) are placed on the PCB top face, whereas the electronics for monitoring the environment inside the package (the temperature and humidity sensor with its bypass capacitor) are on the bottom face. As shown in Fig. 4.23, the board contains:

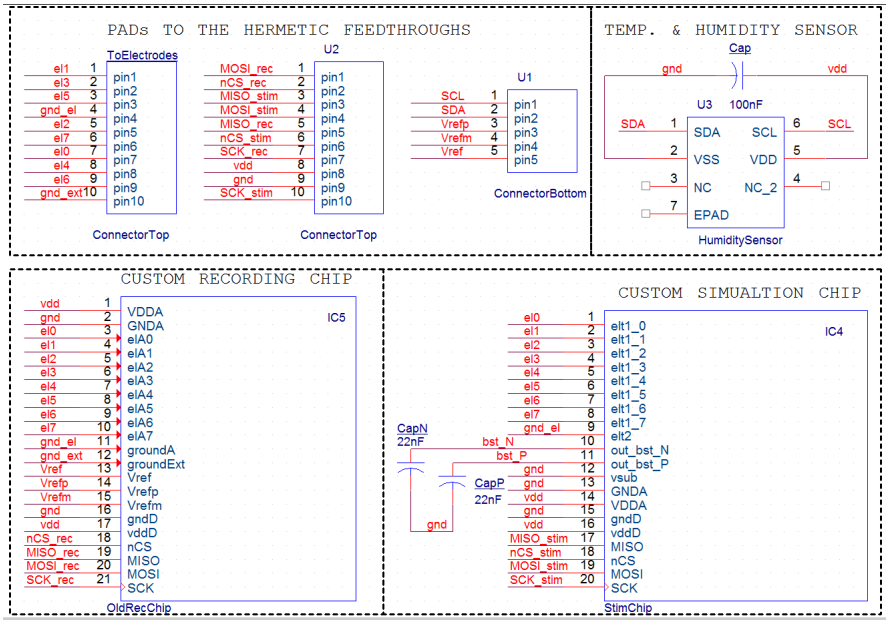


Figure 4.21: PCB schematic in *OrCAD-Capture* environment.

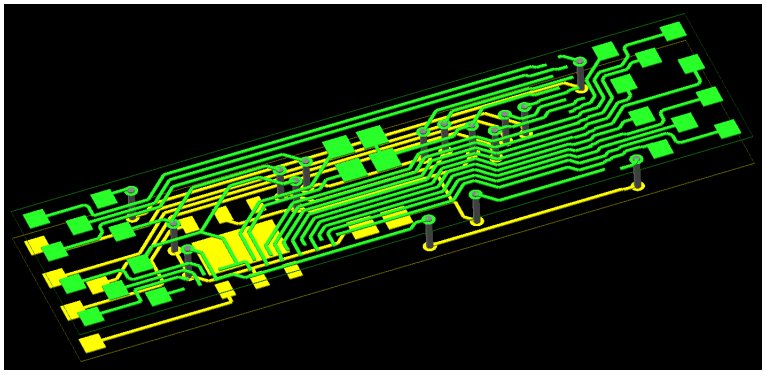


Figure 4.22: PCB layout in *OrCAD-PCB Editor* environment.

- **A**: The *SHT25* temperature and humidity sensor by *Sensirion*.
- **B**: The pads for bonding the custom stimulation chip.
- **C**: The pads for bonding the custom recording chip.
- **D**: The accumulation capacitors for the stimulation IC.
- **E**: The bypass capacitor for the power supply.
- **F**: The pads to connect the package feedthroughs.

As introduced in Section 4.4.1, in order to reduce the hosted system size, the two custom ICs are directly bonded on the PCB saving the extra space required by the IC's package. In order to proceed with the bonding two important steps are necessary: the cleaning of both the ICs and the PCB and the IC glueing on the PCB substrate. Since the cleaning solvents can

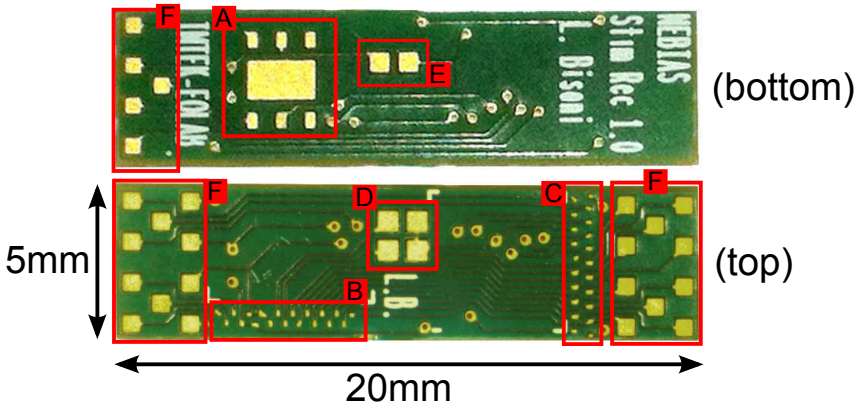


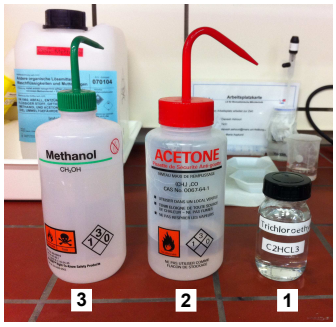
Figure 4.23: Manufactured micro PCB.

damage the glue used to fix the IC, it is recommended to do first the cleaning. It consists in the removal of any organic residual that can compromise the bonding itself, by reducing the wire adhesion on the pads, and the chip operation. This can be achieved by the sequence of 3 baths in different solvents with a decreasing aggressivity, in the following order:

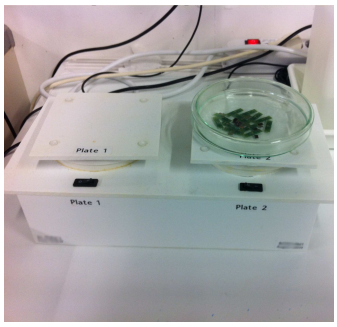
1. Trichloroethylene (C_2HCl_3), at room temperature for 10 – 15 minutes;
2. Acetone ($(CH_3)_2CO$), at 50°C for 10 – 15 minutes;
3. Methanol (CH_3OH), at 50°C for 10 – 15 minutes.

Moreover, a shaking machine (Fig. 4.24b), to continuously move the solution during the bath, was used to make it more effective. The last step in the cleaning process, to guarantee a good electrical contact between bonded wires and the IC's pads, is the removal of the aluminium oxide that have been eventually generated on the ICs pad due to their contact with the oxygen contained in the air. For this reason, the ICs were immersed for 10 minutes in a 1 : 100 solution of sulphuric acid (H_2SO_4) with deionized water ($1:100/H_2SO_4:(DI)H_2O$). The pictures in Fig. 4.24 show different moments of the cleaning process.

After being cleaned, the ICs were carefully fixed on the PCB using the *UHU PLUS endfest*



(a) The solvents

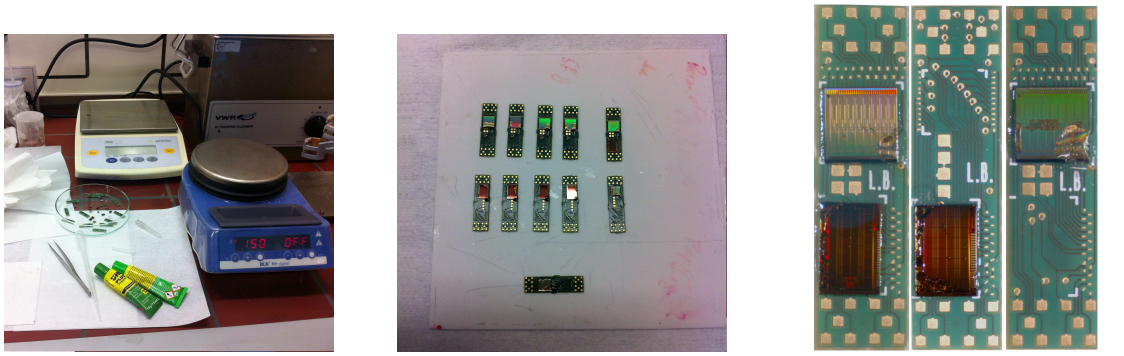


(b) Shaking machine

(c) The hot plate

Figure 4.24: The ICs and the PCB cleaning process: (a) the 3 different solvents, (b) the shaking machine and (c) the hot plate used for the acetone and methanol baths.

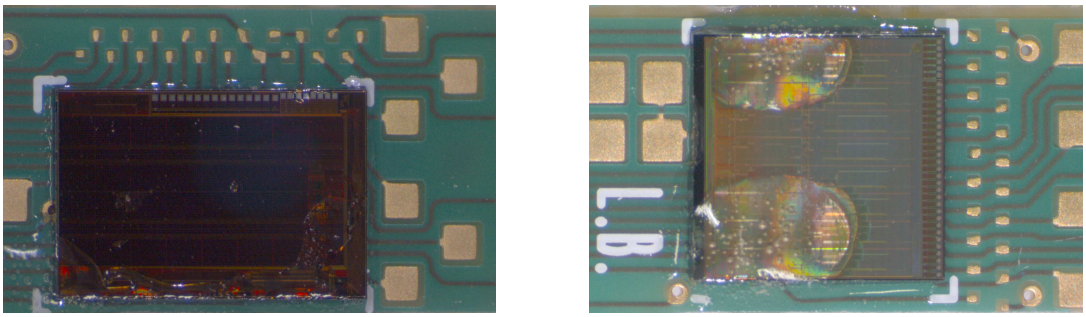
300 glue. It is a solvent free two-part epoxy resin adhesive for heavy-duty requirements (up



(a) The gluing materials (b) The glued ICs (c) A zoom on the glued ICs

Figure 4.25: The ICs gluing on the micro PCB

to $300 kg/cm^2$). The ICs gluing requires special care in order to perfectly align the ICs on the PCB substrate and to avoid any glue on the pads. At room temperature (20°C) the glue dries in approximatively 12 hours, but to speed up the process, as specified in the glue's datasheet, the ICs were glued on the hotplate at 150°C requiring less then 10 minutes to completely dry. The ICs were bonded in a semi-cleaning room with the *Kulicke and Soffa 4526* wire bonder,



(a) Stimulation chip (b) Recording chip

Figure 4.26: A zoom on the glued (a) stimulation and (b) recording ICs.

depicted in Fig. 4.27. Using a $15 \mu m$ gold wire, the machine can perform a single gold ball on the pad or a two steps bonding characterized by a first ball-bonding and a final wedge-bonding. In the second modality, which is the one that fits our interest, the wire bonder can execute a semi-automatic or a manual bonding. Since only few prototypes were going to be developed, the manual bonding was selected. Even though the two steps bonding was chosen, since the wedge-bonding is more fragile than the ball-bonding, an additional ball was created on each wedge connection. Several hours of practice in wire bonding on dummy samples (Fig. 4.28a) had been spent before reaching an adequate level of experience and additional time was required to tune the different bonding parameters. The adopted parameters' value are collected in Table 4.3. Moreover, during some bonding tests, it resulted more effective to execute the first step of the bond (ball-bonding) on the IC's pad and the second step (wedge-bonding) on the PCB's pad. Fig. 4.28 collects some pictures taken during the bonding process whereas Fig. 4.29 and Fig. 4.30 show some details of the bonded recording and stimulation chip respectively.
After the bonding, the ICs' electrical connections were tested with the experimental setup

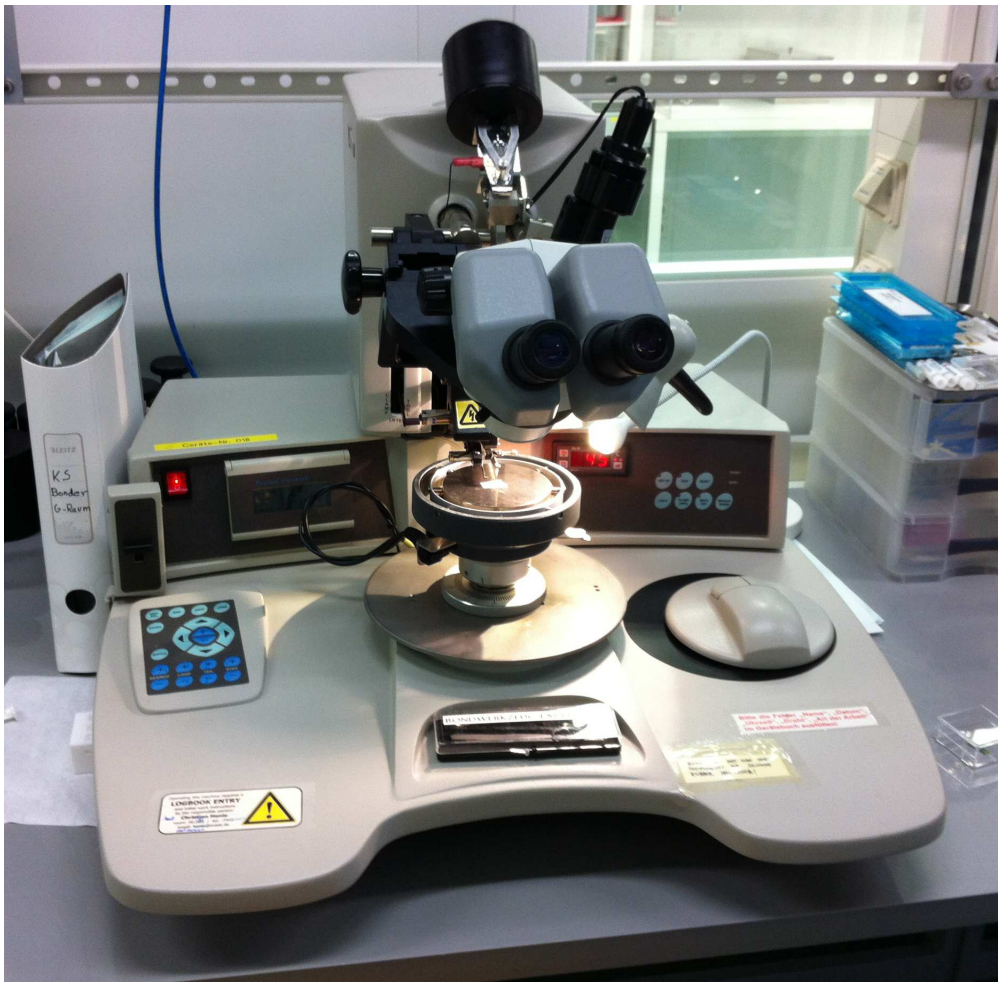
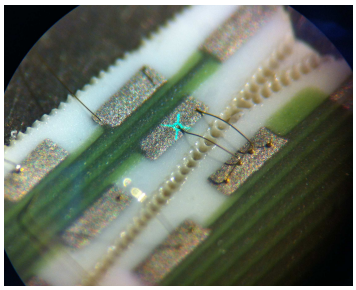


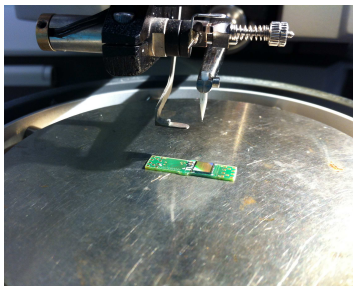
Figure 4.27: Wire bonding machine: *Kulicke and Soffa 4526*.

depicted in Fig. 4.31. It consists of a probe station, with a microscope to contact the pads of the PCB on one side and those of the IC on the other, and a digital multimeter to verify the electrical contact of the bonded wires.

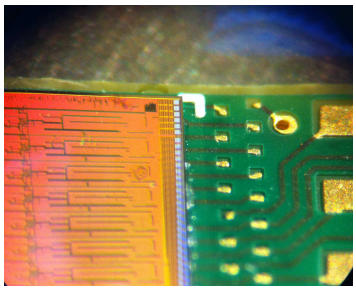
The last step to conclude with the ICs' bonding was to protect the fragile connections with



(a) Bonding test



(b) Bonding tool



(c) Zoom on the recording IC

Figure 4.28: The ICs gluing on the micro PCB

a drop of the same epoxy glue used to fix the ICs on the PCB substrate. The pictures of the

Ball-bonding	
Parameter	**Value**
Search	3.0
Power	4.0
Time	9.0
Force	4.0

(a)

Wire	
Parameter	**Value**
Step back	1.5
Reverse	1.0
Kink height	1.0
Y speed	1.0
Loop	4.0

(b)

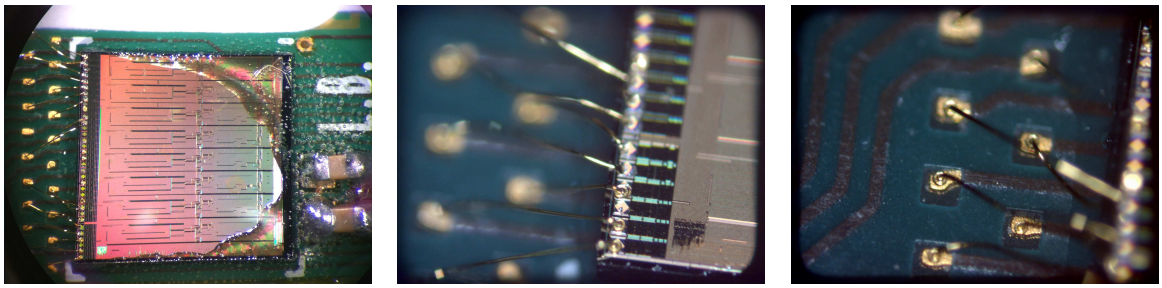
Wedge-bonding	
Parameter	**Value**
Search	3.0
Power	3.0
Time	6.0
Force	4.5
Tail	4.0

(c)

Table 4.3: The used wire-bonding parameters.

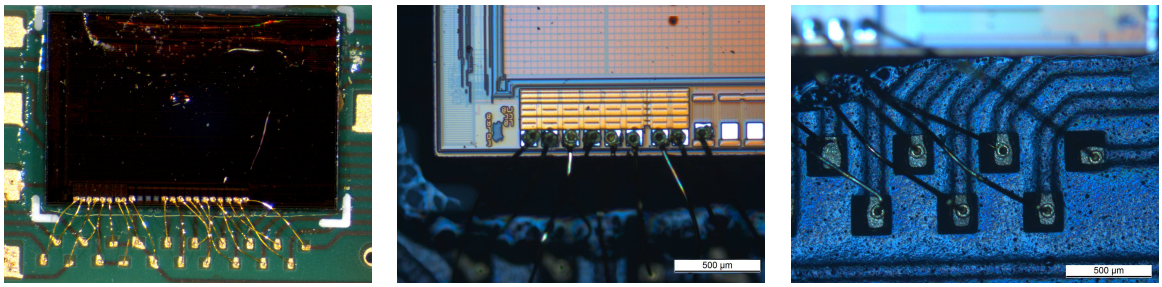
sealed bonded ICs are collected in Fig. 4.32.

The last step to completely assemble the bidirectional neural interface was to solder the



(a) Entire bonded chip (b) Bonded IC's pads (c) Bonded PCB's pads

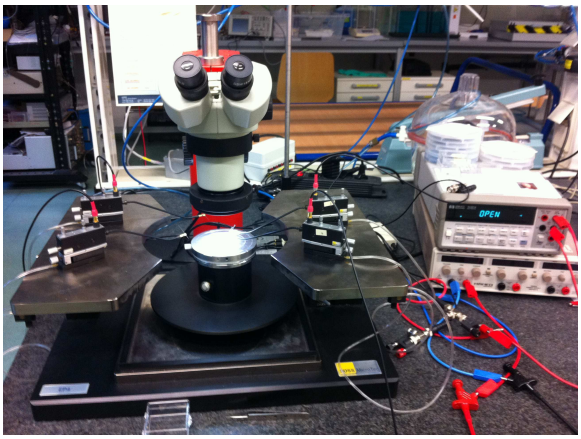
Figure 4.29: Some details of the bonded recording chip.



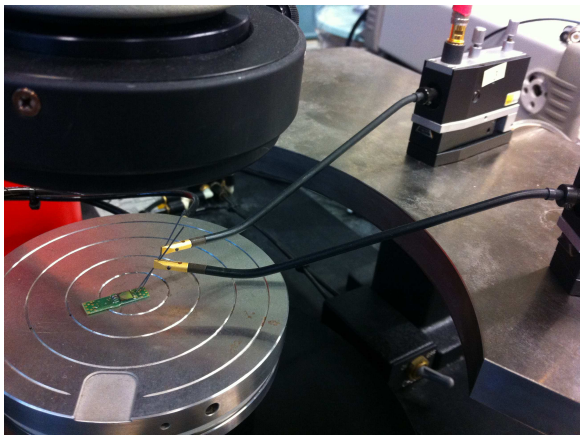
(a) Entire bonded chip (b) Bonded IC's pads (c) Bonded PCB's pads

Figure 4.30: Some details of the bonded stimulation chip.

other electronic components: the bypass and accumulation capacitors and the temperature and humidity sensors. The whole hosted system is depicted in Fig. 4.33.

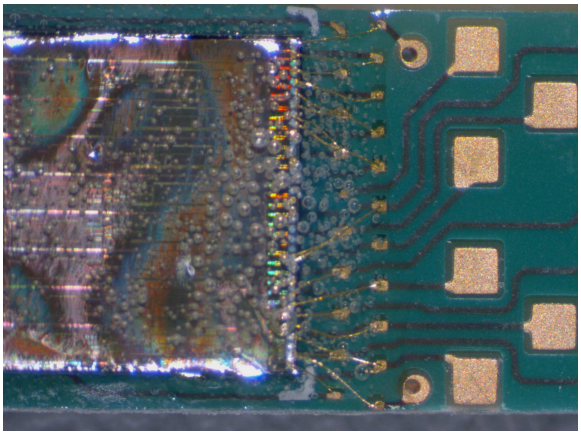


(a) The probe station

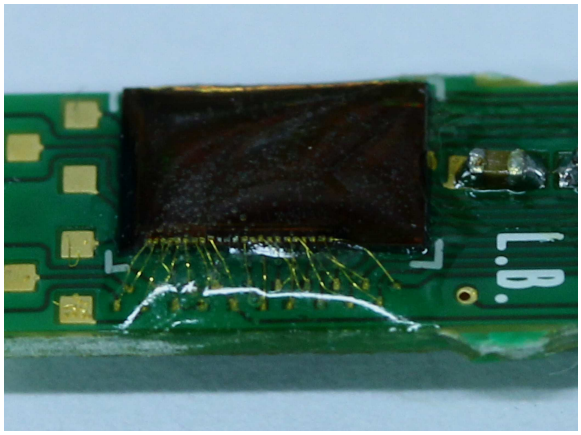


(b) Zoom on the tested board

Figure 4.31: The setup for testing the connections of the wire bonded ICs.

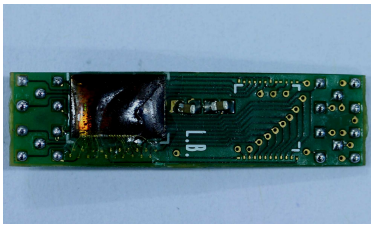


(a) Recording chip

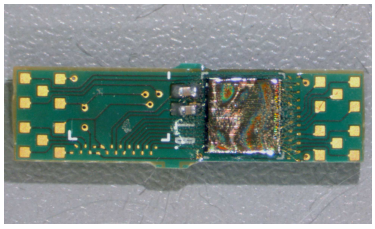


(b) Stimulation chip

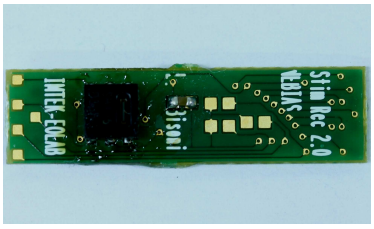
Figure 4.32: The (a) recoding and (b) stimulation ICs with protected wire-bonds.



(a) Top view: stimualtion IC



(b) Top view: recording IC



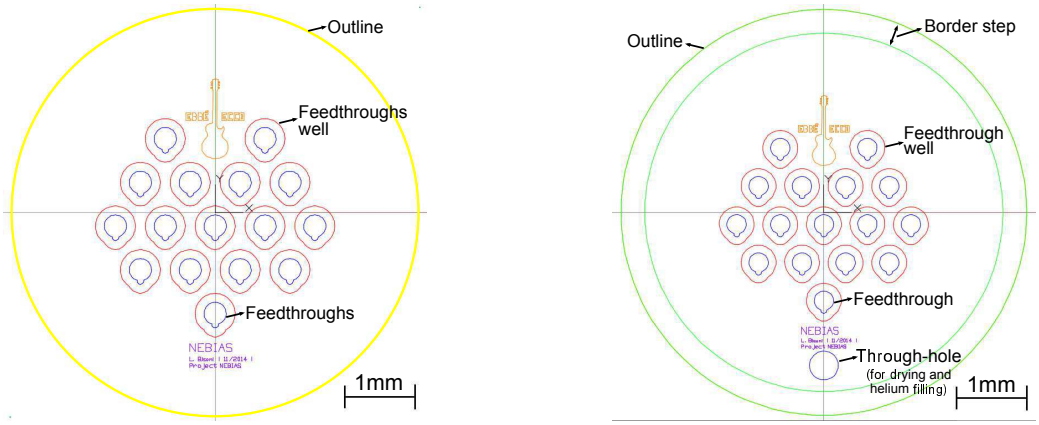
(c) Bottom view

Figure 4.33: The complete bidirectional neural interface: the top view with the (a) stimulation and the (b) recording ICs; the (c) bottom view with the humidity and temperature sensor.

Alumina caps

The ceramic caps, described in Section 4.4.2, to hermetically close the package and to provide a substrate for the hermetic feedthroughs, were completely manufactured in the laboratory. The whole fabrication process is divided in four main phases: the layout design, the

ceramic substrate lasering, the ceramic "cooking" and the caps metallization. In the following the main steps of the different phases are detailed.
The caps' layout, depicted in Fig. 4.34, was designed with the *Autocad* software on the base



(a) Small cap (b) Wide cap

Figure 4.34: The (a) small and the (b) wide cap drawing designed with *Autocad*.

of the 3D models described in Section 4.4.2. It is a two-dimensional (2D) representation that does not contain information on the thickness of the different cap's structures (outline, vias and vias well). These information are directly provided to the software (*Magic Mark V3*), that controls the laser, by setting few parameters such as the laser-beam intensity, and the number of time that the beam goes over the same track. Moreover, before being processed, the real-scale cap designs were enlarged of a 1.2 scale factor due to the ceramic shrinking during the sintering process that will be later discussed. The laser machine used to manufacture the ceramic substrates is the *DPL Genesis Marker* by the *ACI Laser* company, depicted in Fig. 4.35. The laser parameters used to manufacture the different parts of the cap are collected in Table 4.4. The substrate for the cap fabrication, shown in Fig. 4.36a, is composed of four

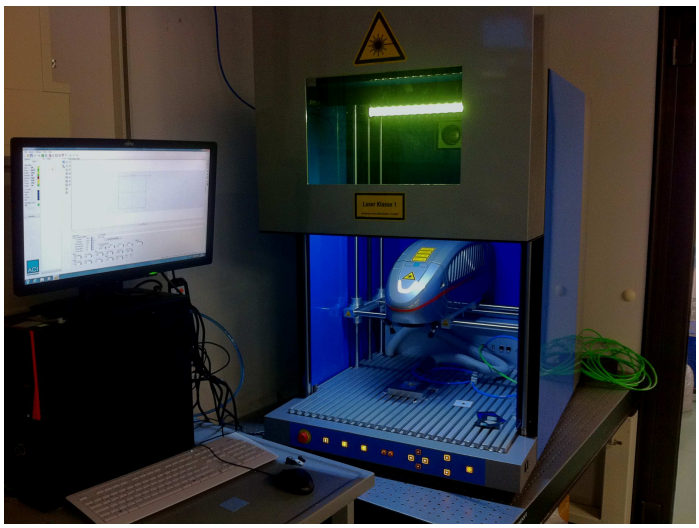


Figure 4.35: Lasering machine: *DPL Genesis Marker* by the *ACI Laser* company.

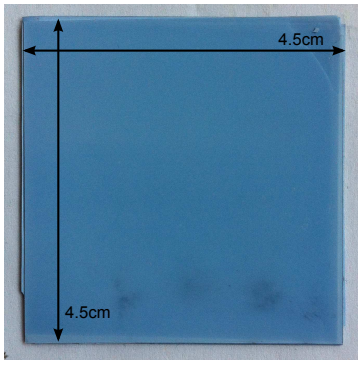
Feedthroughs & Outline	
Parameter	**Value**
Power	75.0
Speed	$15.00 mm/s$
Pulse width	$3\mu s$
Pulse freq.	7Hz
# of passes	16
Start delay	$1\mu s$
End delay	$1\mu s$

(a)

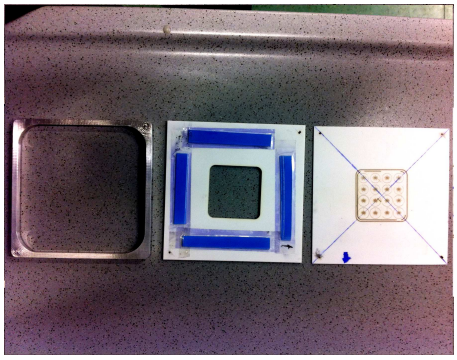
Feedthroughs well	
Parameter	**Value**
Power	35.0
Speed	$10.00 mm/s$
Pulse width	$3\mu s$
Pulse freq.	6Hz
# of passes	4
Start delay	$1\mu s$
End delay	$1\mu s$

(b)

Table 4.4: Laser parameters.



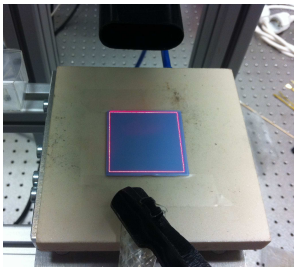
(a) A 4-layer ($0.8mm$) alumina substrate.



(b) Cermaic substrate alignment tool.

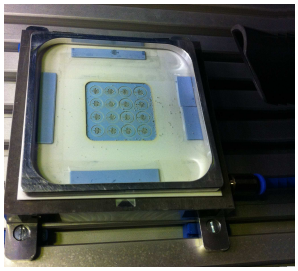
Figure 4.36: The (a) alumina substrate and the (b) related alignment tool.

thin layers with a thickness of $200\mu m$ each one, pressed together in order to get post sintered caps with an overall thickness of about $600\mu m$. Each layer is a special mix of alumina with organic compounds that make it flexible and easily manufacturable. Fig. 4.37 collects different pictures of the cap lasering phase. In particular, a special tool, depicted in Fig. 4.36b, to flip and align the ceramic substrate was developed and used to manufacture the small step along the external border of the wider cap depicted in Fig. 4.34b. The post-lasered caps are depicted in Fig. 4.38. The next phase in the cap fabrication is the ceramic *"cooking"* com-



(a) Substrate alignment

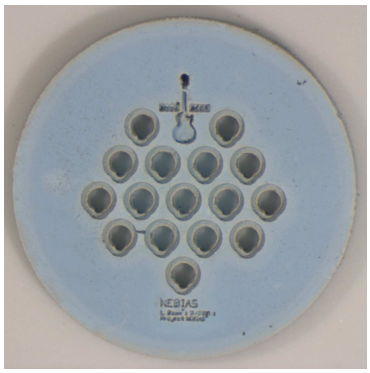
(b) Small cap lasering



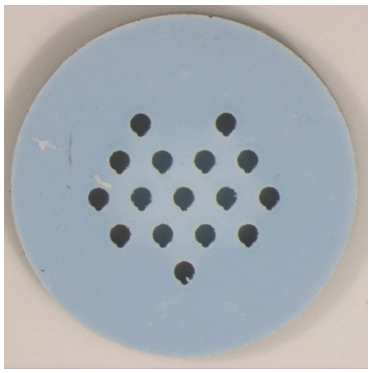
(c) Wide cap lasering

Figure 4.37: The ceramic cap lasering phase.

posed of two sequential steps: the organic burnout (Fig. 4.39) and the sintering (Fig. 4.41).

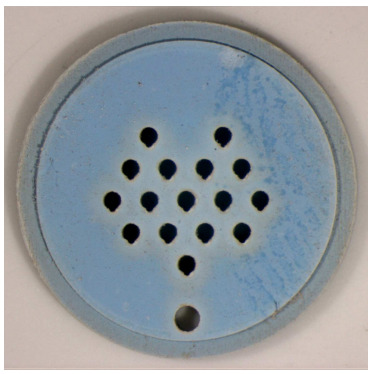


(a) Small cap: inner side



(b) Small cap: outer side

(c) Wide cap: inner side

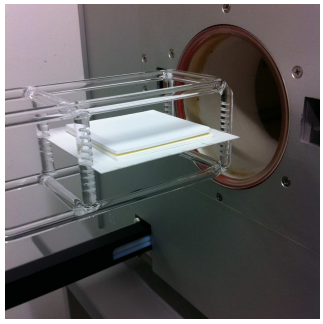


(d) Wide cap: outer side

Figure 4.38: The post-lasered ceramic caps.

The former consists in burning all organic compounds from the ceramic mixture by placing the fresh processed structures in a oven at a variable temperature according to the profile depicted in Fig. 4.40. After the organic burnout, the ceramic parts are very fragile like a mass of powder. For this reason, a sintering phase to make the alumina caps compact and solid is required. During this phase the caps were placed into another oven at higher temperature according to Fig. 4.42. The post sintered caps are depicted in Fig. 4.43.

(a) Oven



(b) Zoom on the samples holder

Figure 4.39: The oven for the organic burnout.

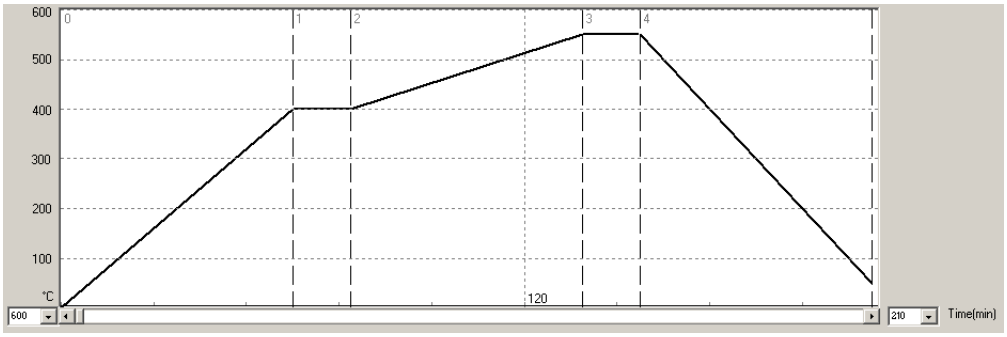


Figure 4.40: Temperature profile for the organic burnout.

(a) Oven

(b) Zoom on the samples holder

Figure 4.41: The oven for the organic burnout.

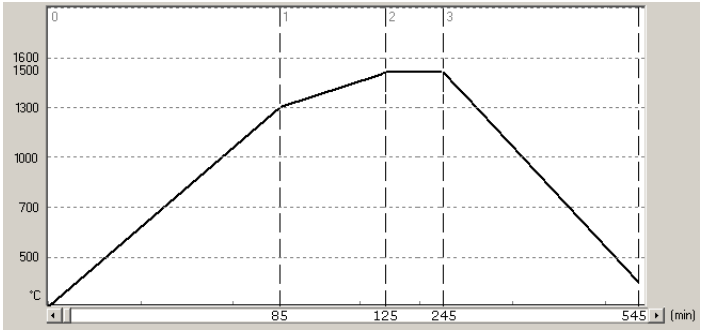
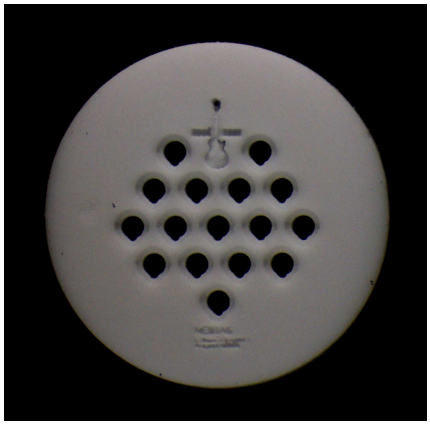
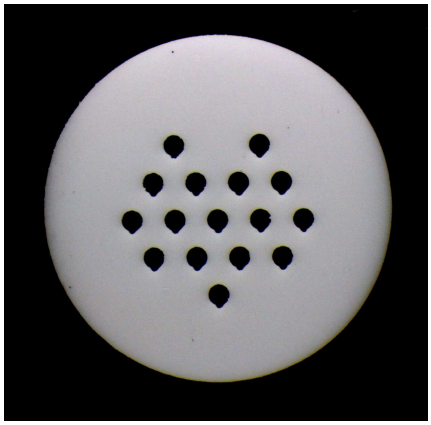


Figure 4.42: Temperature profile for the ceramic cap sintering.

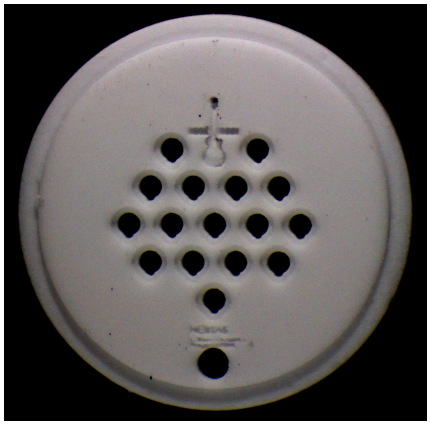
At this point, before being metallized, the caps were accurately cleaned and dried. The cleaning process consists in the sequence of 3 baths, of 5 minutes each one, in the following solvents: Leslie's Soup, Isopropanol and DI-water. After that, in order to dry, they were placed into a oven at 70°C for 3 hours.



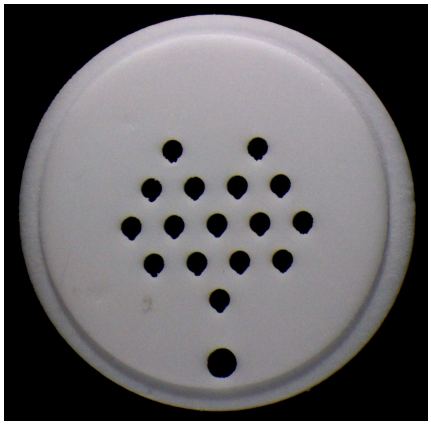
(a) Small cap: inner side



(b) Small cap: outer side



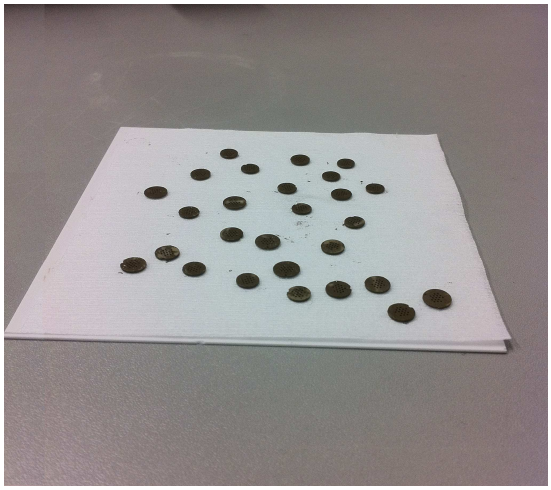
(c) Wide cap: inner side



(d) Wide cap: outer side

Figure 4.43: The post sintered ceramic caps.

(a) Tools



(b) The caps covered by the Pt-Au paste

Figure 4.44: The ceramic caps metallization phase.

The last step in the alumina caps development is the metallization of all the parts that need to be soldered: the external border, to hermetically join the cap to the alumina tube, and the vias and vias-well to crate the hermetic feedthroughs. All structures were covered by a thin

layer of Pt-Au paste, as depicted in Fig. 4.44, and then placed into the oven for 90 minutes with the temperature profile depicted in Fig. 4.45. Fig. 4.46 shows the post processed caps, completely covered by a thin Pt-Au layer. A grinding process was therefore required in order to remove the extra paste from the caps. The resulting metallized caps are depicted in Fig. 4.47.

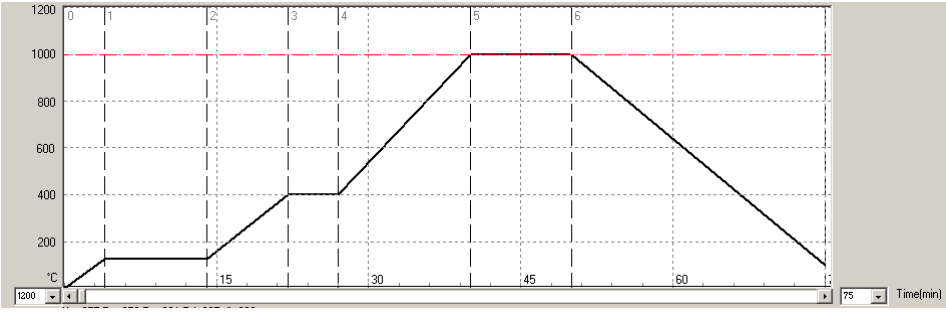


Figure 4.45: Temperature profile for the metallization process.

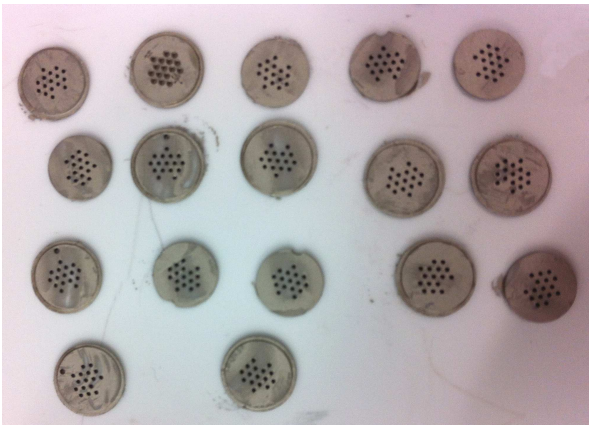


Figure 4.46: The caps after the Pt-Au deposition.

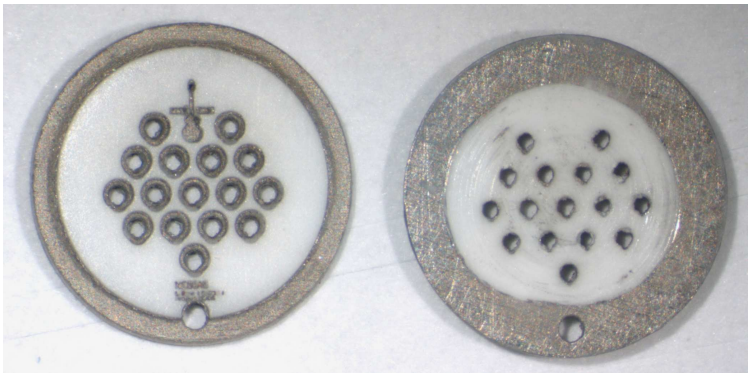


Figure 4.47: The alumina caps at the end of the manufacturing process.

Package assembly

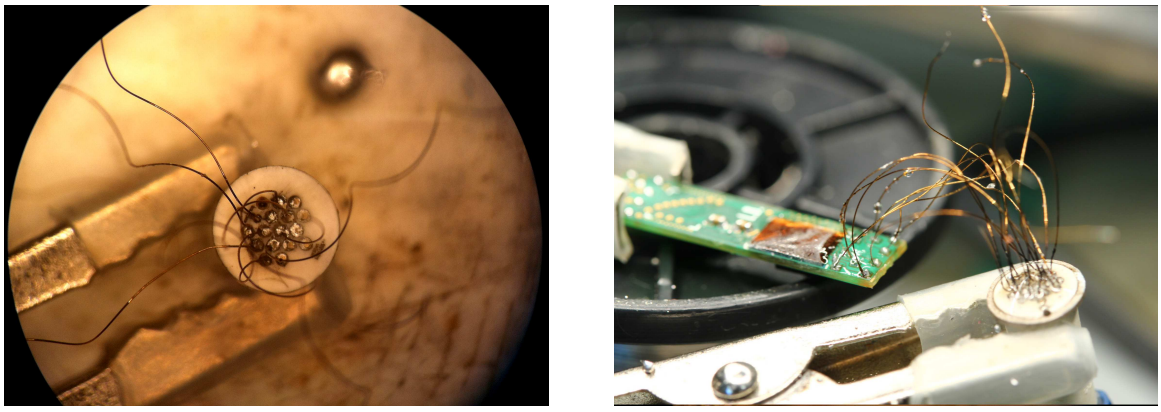
After that all package's parts had been manufactured, they were assembled together using the tools depicted in Fig. 4.48, in order to create the bidirectional neural interface prototype. As depicted in Fig. 4.49, the Omnetics connectors were soldered on the ceramic caps to form the hermetic feedthroughs. After that the *MP35N* wires were first connected to the hermetic feedthroughs and then soldered to the PCB's pads as shown in Fig. 4.50a and Fig. 4.50b, respectively. The completely assembled prototype is depicted in Fig. 4.51.

(a) Microscope (b) Soldering tools

Figure 4.48: The soldering tools used for the package assembly.

(a) (b)

Figure 4.49: The hermetic feedthroughs manufacturing process.



(a) (b)

Figure 4.50: The PCB soldering to the hermetic feedthroughs.

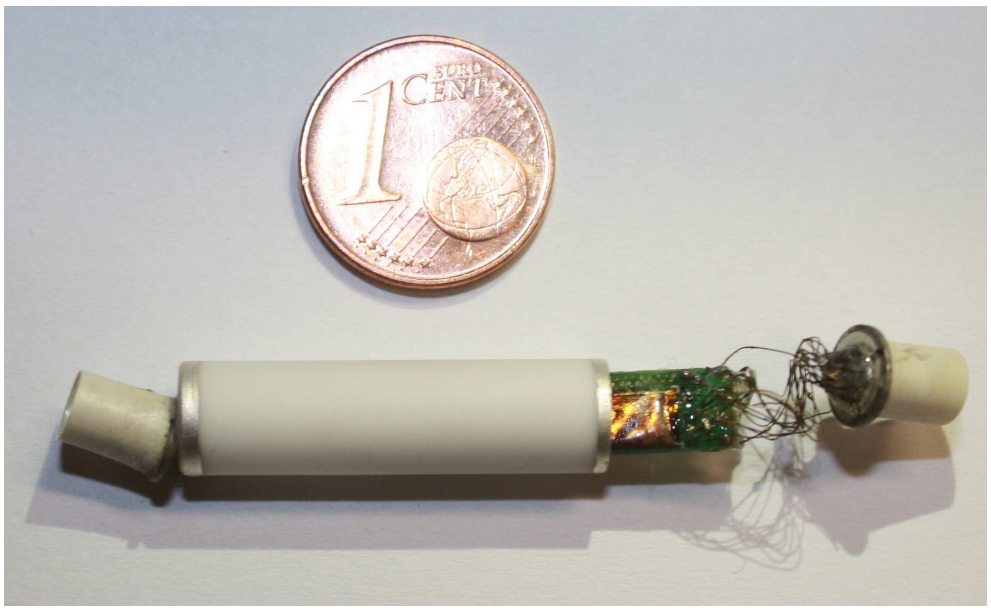


Figure 4.51: The completely assembled prototype.

Chapter 5

A wearable device for high-frequency EEG signal recording

The recording of high-frequency oscillations (HFO) through the skull has been investigated in the last years highlighting interesting new correlations between the EEG signals and common mental diseases. Therefore, since most of the commercially available EEG acquisition systems are focused on the low frequency signals, a wide-band EEG recorder is here presented. In the following, after a brief introduction on the state-of-the-art EEG recorder, the system architecture along with the implementation details are described. Then, a possible remote interface, designed for the EEG recorder testing purpose, is presented. Finally, in the last section, the in-vivo experimental results and the comparison with commercially available EEG recorders are discussed.

5.1 Introduction and state of the art

The electroencephalogram (EEG) is a common technique for detecting symptoms of neurological diseases such as epilepsy, sleep disorders, anxiety and learning disabilities. These pathologies have a great impact on people common life and are quite common. For example anxiety disorders affects approximately 13.6% of the European population [10], and, in 2010, its overall cost in Europe was €74.4 billion [79]. Most of the mentioned mental disorders require long-term EEG monitoring to follow the course of the disease and sometimes to prevent further degradations of the patient condition such as epileptic discharges. In these cases the longer is the EEG measurements period the higher is the probability of a successful event detection. Moreover EEG acquisition during daily life activities is highly recommended to better reveal some pathologies.
Traditional ambulatory EEG systems do not satisfy these requirements. In fact patients can be continuously observed for only a few hours because of the costs and resource overheads. Moreover there are some inconveniences such as forcing people to take time off work and moving them from their natural environment. As a consequence, patients often feel uncomfortable and, depending on their pathology, this can affect the EEG acquisition, introducing

undesired artifacts. As a result of recent technology innovations, new outpatient EEG systems were introduced. Such mobile solutions overcome some of these limitations reducing the overall patient monitoring costs and increasing the effectiveness of the measurements [196]. Despite their benefits such systems are still cumbersome and/or too complex to be used outside hospitals and require expert assistance.
Wearable EEG is aimed to overcome these issues, allowing the recording of a longer temporal window that includes all stages of sleep and wakefulness and increasing the likelihood of recording typical symptoms. Many efforts have been already put on the realization of wearable EEG systems. Some examples are presented in [29] and [34] in which respectively a semi-custom and a completely custom CMOS EEG recorder was realized, whereas a 4-channel BCI-cap based on off-the-shelf components is described in [97]. Other examples are the Epoc [50], the Imec's headset [136] and the Quasar's [142] DSI 10/20. They all use proprietary radio link for data transmission resulting in a reduced power consumption though they require specific hardware to interconnect a remote back-end. Only a few systems have been developed using a standard communication link such as the ThinkGear [128] and the Starfast [7]. Furthermore currently available EEG systems mainly operate with a bandwidth under $100Hz$ that may be enough to cover the most common diagnostic purposes, but a wider bandwidth, up to $600Hz$, is required to investigate some pathologies [116]. As fully discussed in [116], many improvements are still required in order to get a promising solution, easy to use by non-expert users in a completely uncontrolled environment. Some critical aspects that refer to the electrode-skin adherence, the battery life time and the quality of the acquired EEG signals have to be solved.
According to the idea of spreading the use of wearable EEG recorders, the system requires a low impact on people daily life. In other words the device should not imply the use of additional special equipments and it should be very practical. These requirements and the increasing spread of smartphones and tablets among a wide variety of users, from teen to elders [173], suggest these new generation mobiles as the best solution to control the wearable EEG recorders. Furthermore this choice is supported by recent researches on moving the telemedicine toward mobile platforms [156], [37], [107], [49].
The EEG system proposed in this work is based on a custom PCB with off-the-shelf components (COTS) and uses a standard BT link to transmit the acquired signals. As a consequence it exhibits a higher power consumption compared to those solutions, previously presented, that use custom radio link but it has the advantage of being easily interfaced with any BT-based terminal and integrated with such new healthcare systems. In addition, today's technology allows mobile devices with high computational power, huge storage memory and fully programmable. In this way they can store and elaborate the EEG signals allowing a wide-range of applications. Anyway our EEG recorder can also be connected to a traditional desktop PCs for which a simple Microsoft Windows-based application for testing purposes was developed. Being a wearable device, special efforts were made in reducing its power consumption and in device miniaturization. As a result, only the essential components were included in the project: an amplifying/filtering block, an analog to digital converter, a microcontroller, a BT transceiver and a power management module.

5.2 System Architecture and implementation

The designed system, named BlueThought by joining the implemented transmission link (Bluetooth) with the nature of the acquired signals (the human thought), is based on a differential 8 channel recording unit. The EEG signals detected with a standard EEG cap are first amplified and then converted into digital signals by an *ADS1299* component from Texas Instrument. Once acquired, digital signals are transmitted to a remote back-end by means of a *Microchip Bluetooth RN-42* module. Moreover a USB connection was introduced to charge the EEG recorder battery and as additional channel for data transfer. A *Microchip PIC18F46J50* coordinates data exchange between ADC and BT or USB external controller. The system architecture is depicted in Fig.5.1. In addition, a power management unit gen-

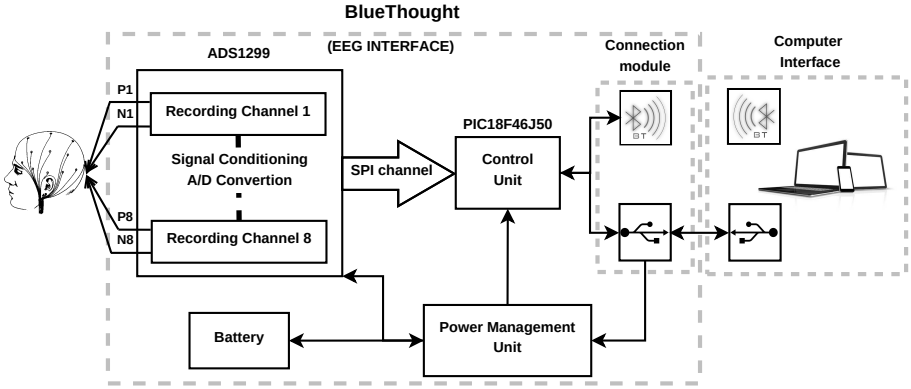


Figure 5.1: BlueThought: System Architecture.

erates all digital and analog voltage supplies for the ADC, the microprocessor and the BT transceiver from a $3.7V-950mAh$ LiPo battery. Even the battery charging circuit was implemented on the board. The EEG recorder was realized on the $5.5cmX3.5cm$ double face board depicted in Fig.5.2. In the following further details on the main modules of the EEG recorder will be described.

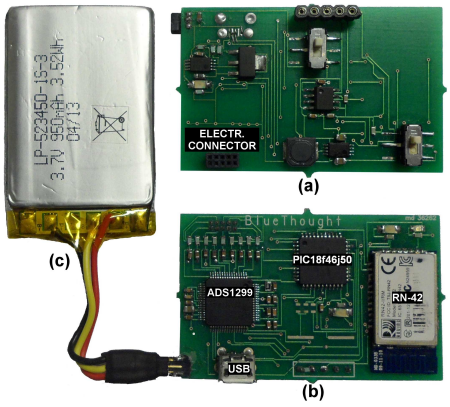


Figure 5.2: EEG Interface prototype: power management circuit on bottom side(a); *ADS1299* (ADC), *PIC18F46J50* (microprocessor), USB and *RN-42* (BT transceiver) on top face(b) and a $3.7V-950mAh$ LiPo battery(c).

5.2.1 Signal conditioning and digital conversion

Before being converted into digital format, the input signals are filtered and amplified. To reduce power consumption and PCB area we selected the *ADS1299* A/D converter which includes the signal conditioning block avoiding the need of any additional component. Moreover, exhibiting a low power consumption of $5mW$ in stand-by mode that is increased up to $40mW$ during signal recording, the *ADS1299* is suitable for our application. This device contains eight independent differential channels allowing simultaneous acquisition. As depicted in Fig. 5.3, an internal multiplexer allows to select the P and N input signals among various sources and depending on the selected signals different recording modes are possible: normal recording, test and impedance monitoring mode. The normal recording mode is the default working set-up in which EEG signals are acquired in both single-ended and differential configuration. In single-ended measurements the N signals are internally shorted to the external reference (typically mid-supply voltage) or to the bias signal generated by the internal bias module on the base of a desired input signal combination. Whereas in differential measurements both P and N signals come from the EEG cap. To reduce the number of interconnections between the EEG recorder and the bonnet all N input lines are shorted together getting only one common reference electrode conveniently placed on the patient body. In test mode, different internally-generated test signals can be selected as input allowing the signal acquisition chain to be tested out. Another important feature provided by the *ADS1299* is the lead-off detection. It consists in a continuous patient electrode impedance monitoring to verify if a suitable connection is present or not.

The first stage of each acquisition channel is a differential low-noise programmable gain

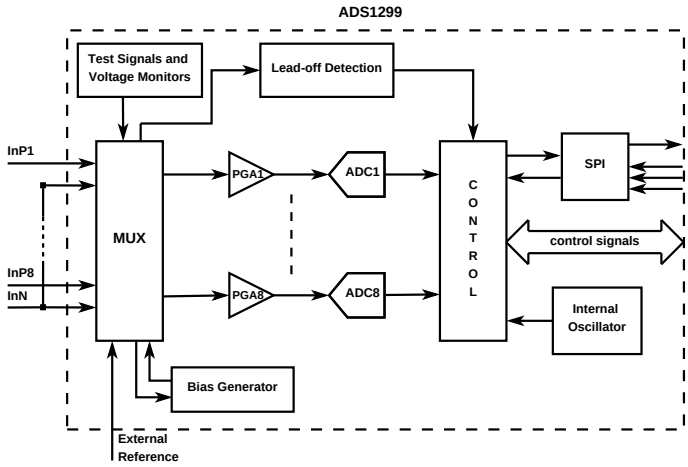


Figure 5.3: *ADS1299* main architecture: Signal conditioning and analog to digital conversion.

amplifier (PGA). It offers seven gain settings (1,2,4,6,8,12, and 24) that can be set-up by writing the channel-setting registers (one per channel) of the *ADS1299*. As mentioned in Section5.1, our EEG recorder can acquire signals with a bandwidth wider then standard EEG monitor. In fact, as reported in Tab.5.1, the system supports different sample rates from $250SPS$ up to $2000SPS$ resulting in a maximum bandwidth of $524Hz$. This makes our device suitable for a wide range of applications even those requiring the analysis of signals out of standard EEG frequency. After being amplified, the signal is digitalized by a $24-bit$ $\Sigma\Delta$ converter. The ADC operates in two different modes: continuous mode (default) and single-shot mode. In the first modality, when a start command is sent, it continuously converts the input

$-3dB$ **Bandwidth [Hz]**	**Sample Frequency [SPS]**	**Output Data Rate [Kbps]**
65	250	6.75
131	500	13.50
262	1000	27.00
524	2000	54.00

Table 5.1: EEG Recorder $-3dB$ bandwidth with the required sample frequency and the correspondent output data rate.

signal. The conversion ends when a stop command is received. Whereas, if the device is in single-shot mode it generates only one sample per received start command. This means that to begin a new conversion, a new start command has to be sent. Regardless of the operating mode, as a single sample conversion ends, a data-ready signal (DRDY) is pulled down to notify the microprocessor that a new sample is ready. After being converted, the eight samples (each per channel) are packed and sent to the micro-controller over a $3MHz$ SPI connection. In the following the control unit is described. It forwards the samples received from the ADC to the BT transceiver or to the USB controller depending if a wireless or a wired connection is being used.

5.2.2 Control unit

The *Microchip PIC18F46J50* is based on a new *nanoWatt XLP (eXtreme Low Power)* technology that hugely reduce its power consumption with respect to other micro-controllers with the same features. The microprocessor is used as control unit to serve two main tasks: system set-up and data exchange. The PIC is powered at $3.3V$ with a CPU clock frequency of $48MHz$ generated by an on-chip oscillator. At system power-up, the PIC is used to setup the EEG interface defining both recording and connection parameters such as acquisition gain and bandwidth, ADC SPI clock frequency, BT data rate and communication protocol parameters. All values are tuned to find a good compromise between the acquired EEG signal quality and the power consumption. Once that the system started to acquire the EEG signals, the control unit coordinates data exchange among the converter and BT or USB remote back-end. The microprocessor provides several internal peripherals that, if not used, can be disabled to save power. In particular we are interested in using the USB and the UART in/out ports to respectively connect the PIC to a remote USB controller or to the BT transceiver.
Although the system communication mode can be on-line modified by the user, if, on power-up, any device is connected to the USB port, the PIC automatically enables the USB controller otherwise the BT transceiver is turned on. Once defined the connection mode, the microprocessor starts a polling cycle waiting for data coming from the remote controller. The received commands are decoded and executed. Such commands, generally are aimed at controlling the ADC or the BT transceiver but they can also be addressed to the same microprocessor for example to setup the USB controller. The main steps of the firmware are described in the flow chart of Fig.5.4. Regardless of the back-end connection mode (via USB or BT) and only in single-shot recording, the same polling cycle is used by the PIC to send the sampled data to the remote controller. Otherwise, in continuous recording, sampled data transmission is handled by an interrupt service routine. The *ADS1299* data-ready signal

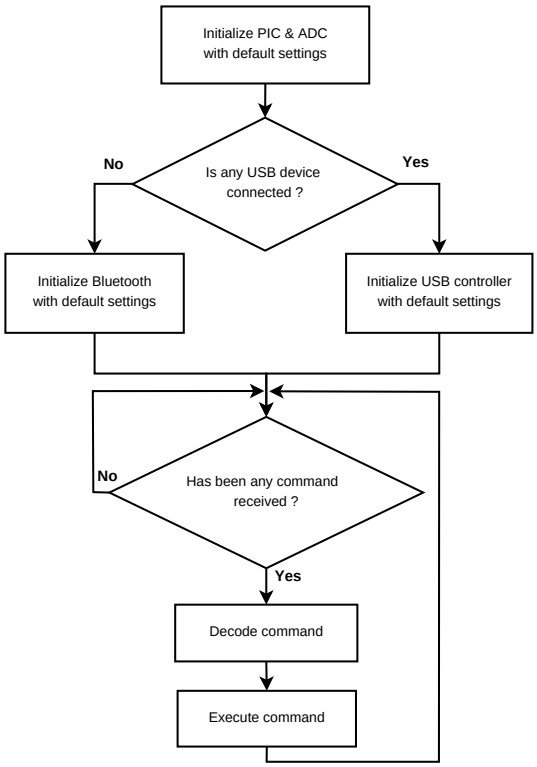


Figure 5.4: Main steps of the control unit firmware.

(DRDY) is connected to an interrupt sensitive pin of the PIC acting as an external interrupt. When DRDY is pulled down (i.e. new samples are available) an exception is raised and the interrupt service routing is executed. The new samples are transferred from the ADC to the microprocessor that forwards data to the remote controller. Some details about the USB and the BT connection are given in the following paragraph.

5.2.3 Data transmission

In normal operation mode, the BT transceiver allows wireless data transmission between the EEG recorder and the remote back-end, whereas the USB controller is used for battery recharging. Nevertheless, in test mode, the wired connection is quite useful for both data transfer and system powering. The communication link specifications are set by the amount

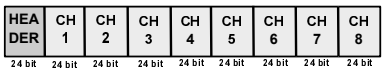


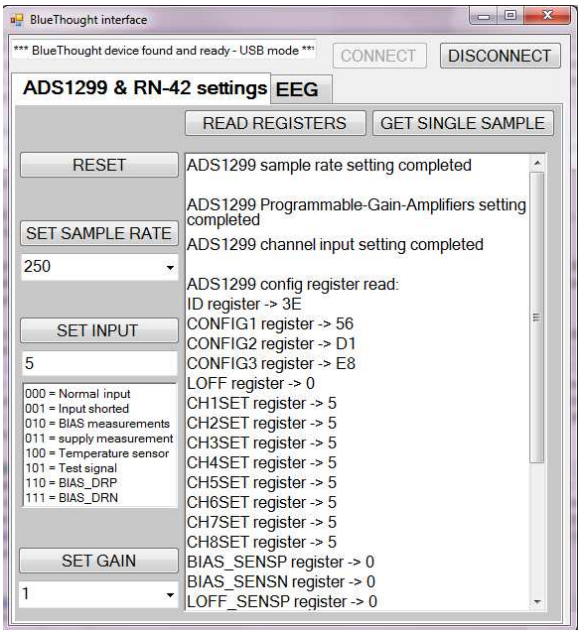
Figure 5.5: Signle data packet transmitted by the ADC.

of data to transfer during the continuous data acquisition mode at the highest frequency allowed by the system. From Table 5.1, in order to enable high frequency EEG recording, a sample frequencies of $2000SPS$ is required. Moreover, considering that the *ADS1299* acquires eight channels per time and that each sample is converted into a $24bit$ word, $192bit$ of payload with an additional header of $24bit$ has to be transferred each $0.5ms$ (Fig. 5.5). As computed in Eq. 5.1, the maximum output data rate (ODR) required in worst conditions is

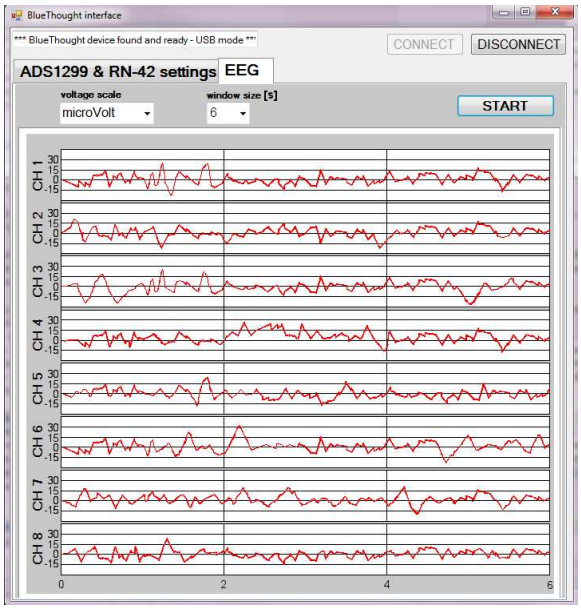
$54Kbyte/sec$ that is a critical parameter to define the data-exchange channel specifications.

$$\begin{aligned} &\text{Single data packet: } 216bit \\ &\text{ODR(@2000SPS): } \frac{2000*216}{8} = 54Kbyte/sec \end{aligned} \tag{5.1}$$

The USB port is directly handled by an on-chip USB controller and can operate in two different modalities: CDC and HID mode. To make the USB suitable for our application, a standard HID protocol was implemented. Working at full speed ($48MHz$) with $64-byte$ data packet size, the data transfer speed is limited to $64KBytes/sec$. In addition, to make the transmission more efficient, two sampled data packets ($2x216bit = 432bit$) are grouped in the same USB frame. As a result, in worst conditions (i.e. with the maximum sample rate, $2000SPS$), the required data transfer rate amounts to $27KByte/sec$ that is below the USB transfer rate limit. In contrast to the USB HID protocol, the BT transceiver does not require fixed size packets, but their length is adapted to the amount of transferred data. The *RN-42* is a small form factor, low power, class 2 BT radio with on-chip antenna. It delivers up to a $3Mbps$ data rate for distances up to 20 meters. It uses an UART port to communicate with the control unit and operates in two modes: data mode (default) and command mode. In data mode, the module works as a data pipe. When the module receives data, it strips the BT headers and forwards the data to the UART port. When data is written to the UART port, the module constructs the BT packet and sends it out over the BT wireless connection. Thus, the entire process of sending/receiving data to the host is transparent to the PIC. The command mode is used to defining the BT operating mode, the UART baud rate and others control flow parameters. Moreover the *RN-42* operates in slave mode so that other BT devices (PC, tablet or smartphone) can discover and connect to the module.



(a) System setup window



(b) On-line plotting window in a μV amplitude scale and with a $6s$ temporal window

Figure 5.6: Visual C++ application for connecting and controlling the developed EEG interface.

5.3 Remote Interface

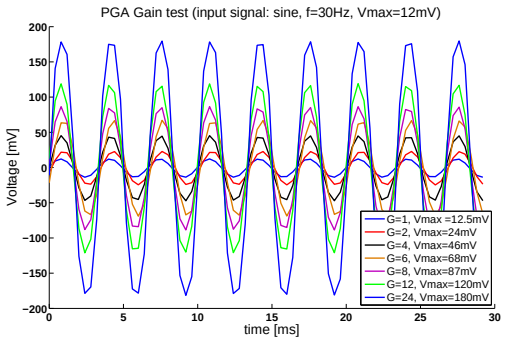
The designed system is a general purpose EEG recorder and depending on the treated pathology a specific software can be developed. At this first stage of the project a Visual C++ application was written, implementing only the essential features for the hardware debugging. The ADC module can be completely configured in terms of PGA gain and sample rate and both continuous and single-shot modes are selectable. The eight recorded signals can be plotted together in the same graph or on separate sub-window for a real-time view and stored in a text file for off-line data computing. Fig.5.6a and Fig.5.6b show the two main window of the developed interface. The first refers to the system settings and the second to the plotting of the eight recorded signals. For all channels is possible to setup the amplitude scale (μV, mV or V) and the temporal window size.

5.4 Experimental Results

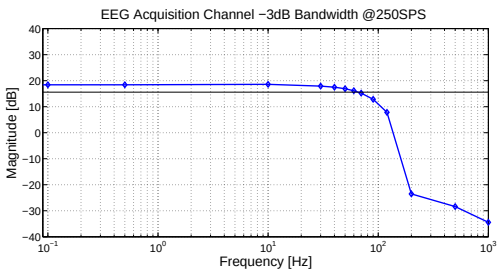
Table 5.2: EEG Recorder Power Consumption in different working conditions.

Power Consumption [mW]	ADC (ON)	ADC (OFF)
Bluetooth (OFF)	119	158
Bluetooth (ON)	230	270

All system features were first characterized and than compared with a standard laboratory equipment. To start with its static electrical characterization, Tab.5.2 collects the EEG interface power consumption in different working conditions. In idle state (only the microprocessor is on) it has a minimum power consumption of about $119mW$ whereas in worst conditions (i.e. all devices are on, sample rate of $2000SPS$ and active BT data transmission) it absorbs a maximum of $270mW$. Under this conditions and with the chosen battery ($3.7V-950mAh$ LiPo) the system can continuously work for about 13 hours. Further ex-



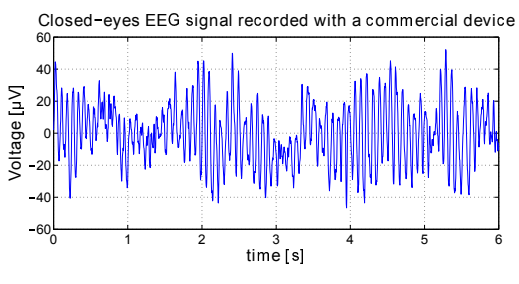
(a) Gain programmability



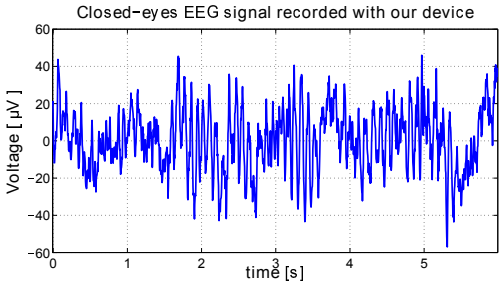
(b) $-3dB$ bandwidth ($63.5Hz$)

Figure 5.7: The EEG interface gain programmability and bandwidth validation by recording a $12mV-30Hz$ sine at $250SPS$.

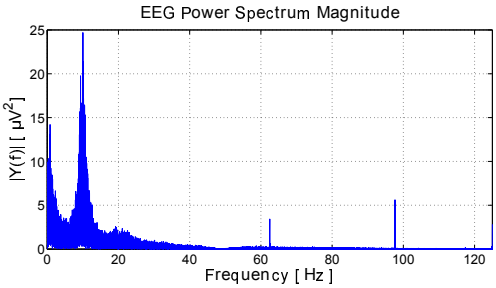
periments were performed to study the dynamic behaviour of the EEG acquisition channel. Its gain programmability from $1V/V$ up to $24V/V$ was confirmed acquiring a $12mV-30Hz$



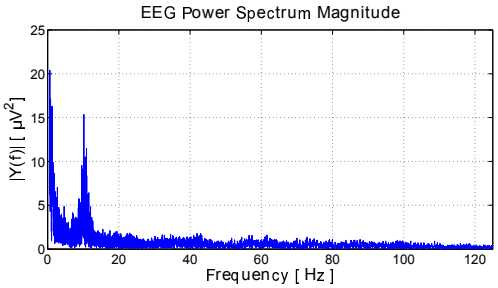
(a) Micromed Brain QUICK: time domain



(b) Our device: time domain



(c) Micromed Brain QUICK: frequency domain



(d) Our device: frequency domain

Figure 5.8: Closed-eyes EEG signal, in time and frequency domain, recorded at 250SPS.

sine as depicted in the above plot of Fig.5.7a. The device showed a 63.5Hz −3dB bandwidth at sample rate of 250SPS and the magnitude bode diagram of the recording channel transfer function is depicted in Fig.5.7b. Moreover both wired (USB) and wireless (BT) connections were tested. Once the system main functions have been proved, some in-vivo EEG measurements, on one human subject, were performed. To evaluate the signal quality of the designed EEG recorder, the system was compared with a commercial device (Brain QUICK,[114]) depicted in Fig.5.9 where the huge difference in terms of dimensions between the two devices is also highlighted. Moreover, the experimental setup, depicted in Fig.5.10, includes a commercial EEG cap (*KIT-CAP-SPEXT61* from Micromed) with 61 electrodes used to acquire the neural signals. To better compare the two devices, they were connected to adjacent electrodes and simultaneous recordings were performed in different patient conditions. During the first test, the human subject was in resting state with closed eyes to avoid any kind of artefact. Fig.5.8 shows the EEG signals acquired by the Brain Quick (Fig. 5.8a and Fig. 5.8c) and by our EEG recorder (Fig. 5.8b and Fig. 5.8d). The signals recorded at 250SPS are quite similar in both time and frequency domains. The system capability to record signals above standard EEG bandwidth was also proved by acquiring some signals at 2000SPS from a patient with closed eyes as depicted in Fig. 5.11. Moreover, in Fig.5.12 it is possible to appreciate the differences between an open-eyes (on the left) and a closed-eyes (on the right) EEG signal perfectly recorded by our device at 250SPS. To further validate our system, some typical EEG artefacts such as the teeth-grinding signal (Fig.5.13) and the eyes-blinking effect (Fig.5.14) were recorded. They respect the typical shapes and amplitudes of such signals. Finally, Table 5.3 collects the main features of some commercially available device compared to the proposed solution.

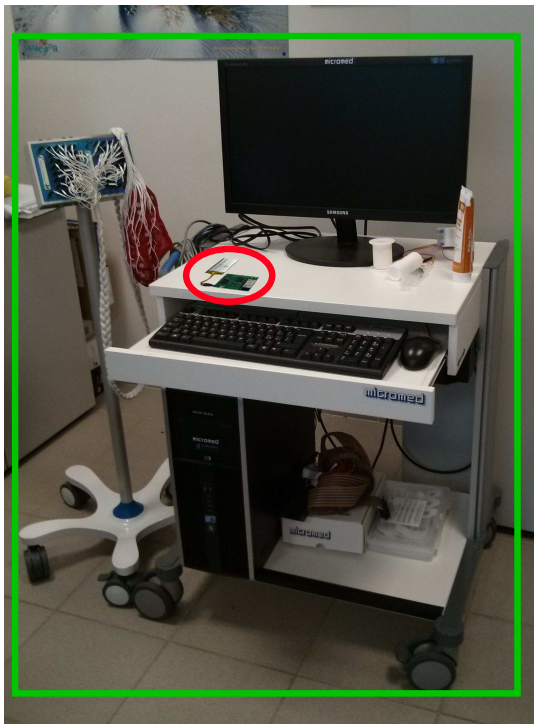


Figure 5.9: Comparison between our wearable EEG interface (red circle) and a cumbersome commercial device (green box).

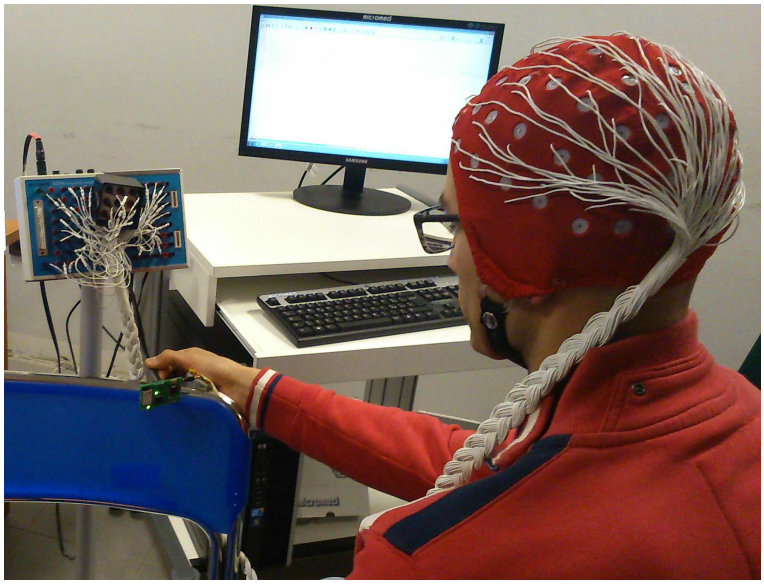


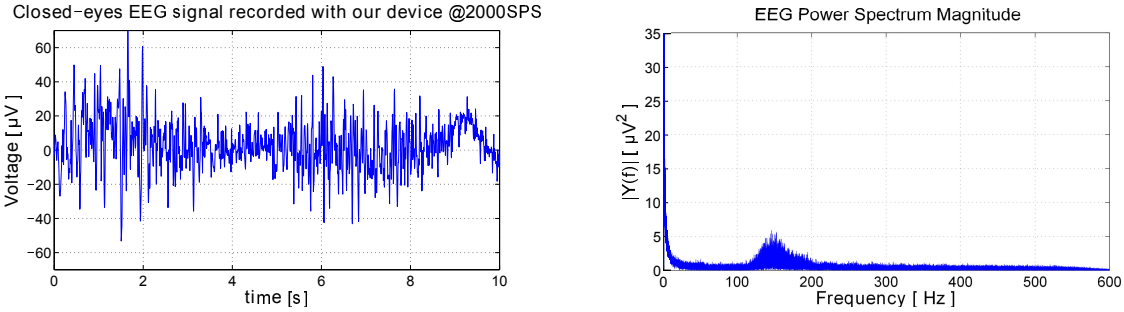
Figure 5.10: Experimental setup for in-vivo EEG measurements.

5.5 Results discussion

The proposed EEG recorder is a wearable system that, thanks to its small dimensions (height: 5.5cm x width: 3.5cm x depth: 1.0cm), can be easily placed on the patient head and integrated with the electrodes framework. The developed device has 8 independent acquisition channels and was designed with the aim of being user-friendly and suitable for all applications in which a long-time EEG monitoring is required. In fully working condition (i.e.

	Our device	Quasar	Imec	Emotiv Epoc	NeuroSky	Brown L.	Enobio
CMRR	$>110dB$	$>120dB$					$115dB$
Input Impedance	$1G\Omega$	$47G\Omega$					
Bandwidth	$0.01-524Hz$	$0.02-120Hz$	$0.3-100Hz$	$0.2-45Hz$	$3-100Hz$	$0.5-375Hz$	$0-250(500)Hz$
Channel number	8	12	12	14	1	8	$8-20(32)$
Noise	$<2\mu$Vpp	3μVpp	4μVpp			1μVpp	$<1\mu$Vrms
Bit number	24	16	12	16		11	24
Wireless protocol	BT	Proprietary	Nordic RF	Proprietary	BT	Proprietary	BT
Power consumption	$270mW$		$42mW$		$130mW$	$12mW$	
Run time	$13h$	$24h$		$12h$	$10h$	$30h$	$16h$
Technology	COTS		ASIC / COTS			ASIC / COTS	

Table 5.3: Comparison between some state-of-the-art EEG Recorders.



(a) Time domain (b) Frequency domain

Figure 5.11: Closed-eyes EEG signal, in time and frequency domain, recorded at $2000SPS$.

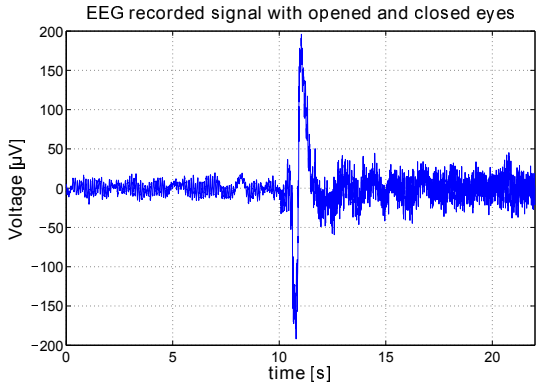


Figure 5.12: EEG recorded signal with opened-eyes (from $0s$ to $10s$) and closed-eyes (from $12s$ to $22s$).

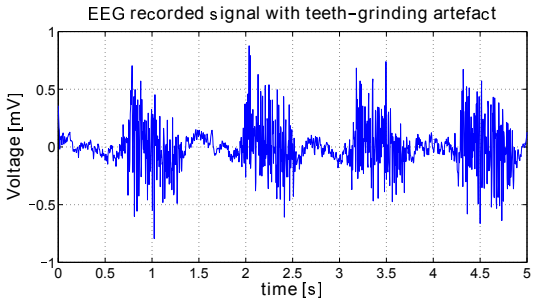


Figure 5.13: EEG recorded signal with teeth-grinding artifacts.

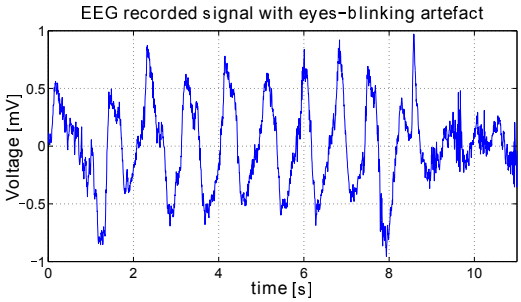


Figure 5.14: EEG recorded signal with eyes-blinking artifacts.

when acquiring and transmitting data) the system exhibits an overall power consumption of $270mW$. Even-though it is higher than of other systems (Tab.5.3), the device allows 13 hours of continuous signal recording that is in line with other wearable devices. The higher power consumption is mainly due to the choice of using a COTS solution and a standard BT link to connect a remote controller. However it gives the device the great advantage to easily connect any BT-based end-terminal in contrast to other systems that, using a proprietary wireless link, require specific hardware. Moreover, compared to others state-of-the-art equipments, our EEG recorder has a wider bandwidth, up to $524Hz$, allowing high-frequency EEG monitoring. This can be very useful to deeper understand and investigate a certain number of pathologies. In addition, a Windows-based Visual C++ software was written for the EEG recorder testing purpose. The system was completed validated by in-vivo measurements on human patient and compared with a commercial laboratory equipment.

Chapter 6

Concluding remarks

The work presented in this thesis is the result of three years of research during which several advancements, in the long way aimed at realizing a fully implantable device for neural recording and PNS stimulation, have been achieved. Four main topics have been dealt with, first an IC for neural signal recording with an embedded low voltage stimulator has been realized and tested, then, due to the insufficient capability of the low voltage stimulator to activate action potentials in the peripheral nervous fibers, an high voltage IC for fully programmable neural stimulation has been developed and tested, moreover, an implantable package to host the two developed ICs has been designed and developed and finally a discrete electronic interface for electroencephalographic signal recording has been realized.
The proposed IC for neural signal recording was designed in a $0.35\mu m$ CMOS technology process from Austriamicrosystems. It embeds both the front-end amplifier and the first stage of the sigma-delta convert on chip, therefore the signal provided to the external is a robust digital signal with high immunity to noise. The proposed approach is to keep the analog part of the system as simple as possible, moving the complexity on the digital side. The analog IC module is composed by a first order analog preamplifier/prefiltering block and by a third order single loop sigma delta modulator. The bandpass high selective filter is provided by the digital part of the system implemented in a Xilinx Virtex 5 LX330 FPGA. The laboratory measurements and the in-vivo tests confirmed the capability of the system to amplify, filter and correctly digitalize, with a 10 bit resolution, the recorded neural signals in the order of magnitude of tens of microvolts. The device exhibits an $IRN = 1.64\mu V_{rms}$ with a $3.4mW$ power consumption (referred to single channel), the total power can be reduced to $2.5mW$ using the device in the lower gain configuration. The chip area occupancy is $0.8mm^2$ for each recording channel. Future developments are aimed, first, at investigating a time continuous analog front-end in order to further reduce the power consumption and, second, at developing an on-chip voltage reference generator and a wireless data transmission module in order to get a completely stand-alone implantable device.
Concerning the stimulation chip, the device was designed on a $0.35\mu m$ CMOS technology process that supports operating voltages up to $50V$. The proposed IC includes a voltage booster to increase the stimulation voltage up to $17V$ from the $3.3V$ power supply. In this way it overcomes the problem of the high impedance at the electrode-tissue interface, delivering relatively high currents to impedances up to $50k\Omega$. Moreover it embeds also a current pulse generator and an output stage. The former is aimed at generating the stimulation

patterns with programmable amplitude (from $10\mu A$ to $300\mu A$), pulse width (from $0.8\mu s$ to $150\mu s$) and frequency (up to $400Hz$). The latter is the module that converts the stimulation current from a low into a high voltage domain and delivers the pulse to the implanted electrode. The developed IC has 8 independent stimulation channels with an overall area of $18.5mm^2$. The power consumption was measured in different working conditions: the static power is $5mW$, while the total power (static and dynamic), measured during a biphasic pulse stimulation of $300\mu A$ in amplitude and a duration of $150\mu s$, is $29mW$. The device had been completely tested by means of laboratory measurements and in-vivo results that highlighted the system capability of selectively activate different neural fibers in the sciatic nerve of a rat with a chronic implant. Even though the IC power consumption is compatible with the performed in-vivo experiments, it is still too much high for a completely implantable solution. Therefore, in future versions of the chip the reduction of the power consumption is one of the main goals that might be achieved by optimizing the design choices and the technology process selection.
Both ICs test results prove the system capability to be used as a compact, efficient and complete device for neural recording and stimulation in laboratory trials with small animals and opens very interesting perspectives on future developments aimed at making the device fully implantable for long-term experiments on humans.
In order to enable the future implantation of the developed bidirectional neural interface, first in animals and later in humans, an implantable package is proposed. It consists in a small alumina tube with an inner volume of $0.64cm^3$ able to host both developed ICs with the minimal electronics required for the ICs proper operation and for the package testing purpose. The package is hermetically sealed at both extremities with custom fabricated alumina caps that contains the hermetic feedthroughs to enable the electronic interconnection between the hosted system and the implanted electrodes on one side and the external digital controller with the power management module on the other side. Finally, the whole package is covered by a silicon rubber layer in order to improve its biocompatibility by better matching the tissue Young's Modulus and, therefore, reducing the risk of tissue damages. For what concern the interconnections, due to lack of real implantable connectors and since it was not the main focus of this work, a standard, non-implantable, connector was selected. However, in order to enable the first, future, in-vivo tests, a package for the connectors was designed too. The package for the neural interface has been completely designed and developed but not tested yet. Therefore, a future plan is to perform all the hermeticity and life-time estimation tests required to validate the proposed solution and to highlight possible system improvements.
The last project developed in this thesis has been the design of a COTS based EEG interface. It is a wearable system that, thanks to its small dimensions (height: $5.5cm$ x width: $3.5cm$ x depth: $1.0cm$), can be easily integrated with the electrodes framework. The device has 8 recording channels and uses a BT link to transfer the acquired data to the remote back-end. In fully working condition (i.e. when acquiring and transmitting data) the system exhibits an overall power consumption of $270mW$ enabling a continuous EEG recording up to 13 hours with the selected $3.7V-950mAh$ LiPo battery. The device was completed validated by in-vivo measurements on humans and compared with a commercial laboratory equipment. Moving towards a device that can become part of everyday life improving the people living conditions, from both health and entertainment points of view, is our main goal. Therefore, being a wearable device, next developments are the reduction of the power consumption and the developing of smartphone-based application to respectively increase the battery life

and to make the system completely portable. In particular, some future improvements include the use of a new generation BT called Bluetooth 4.0 Low Energy (BTLE) that drastically reduce the power transmission and a review of the control unit strategy turning off, time by time, all on-board unused devices. Moreover the possibility to optionally expand the number of input channels by plugging in an additional acquisition module and the introducing of on-board data storage capabilities might be considered. Finally, the possibility of using a custom chip solution for signal conditioning and converting based on the same architecture of the already developed IC will might be investigated to further reduce both power consumption and system dimensions.

Bibliography

[1] *Design of Analog Integrated Circuits and Systems*. McGraw-Hill Companies, 1994. [cited at p. 34]

[2] *Biological Performance of Materials: Fundamentals of Biocompatibility*. CRC Press, 4 edition, 2005. [cited at p. 26]

[3] *Human Physiology: An Integrated Approach*. Benjamin-Cummings Publishing Company, 4th edition, 2007. [cited at p. 11]

[4] *Implantable Neural Prostheses 2*, chapter Technology Advances and Challenges in Hermetic Packaging for Implantable Medical Devices, pages 27–61. Springer New York, 2010. [cited at p. 26, 28]

[5] *Implantable Neural Prostheses 2*. Springer-Verlag New York, 2010. [cited at p. 131]

[6] *Analog integrated circuit design*. 2011. [cited at p. 34]

[7] I. Cester G. Ruffini A. Riera, S. Dunne. Starfast: a wireless wearable eeg/ecg biometric system based on the enobio sensor. *Proceedings of the International Workshop on Wearable Micro and Nanosystems for Personalised Health (pHealthâĂŹ08)*, May 2008. [cited at p. 156]

[8] K. Abdelhalim, H.M. Jafari, L. Kokarovtseva, J.L. Perez Velazquez, and R. Genov. 64-channel UWB wireless neural vector analyzer soc with a closed-loop phase synchrony-triggered neurostimulator. *IEEE Journal of Solid-State Circuits*, 48(10):2494–2510, 2013. [cited at p. 32]

[9] T. Akin, K. Najafi, and R.M. Bradley. A wireless implantable multichannel digital neural recording system for a micromachined sieve electrode. *IEEE Journal of Solid-State Circuits*, 33(1):109–118, 1998. [cited at p. 78, 79]

[10] Bernert S. et al. Alonso J., Angermeyer MC. Prevalence of mental disorders in europe: results from the european study of the epidemiology of mental disorders (esemed) project. *Acta Psychiatrica Scandinavica*, 109:21–27, June 2004. [cited at p. 155]

[11] Soon Kwan An, Se-Ik Park, Sang Beom Jun, Choong Jae Lee, Kyung Min Byun, Jung Hyun Sung, B.S. Wilson, S.J. Rebscher, Seung Ha Oh, and Sung June Kim. Design for a simplified cochlear implant system. *IEEE Transactions on Biomedical Engineering*, 54(6):973–982, 2007. [cited at p. 86]

[12] K. Arabi and M.A. Sawan. Electronic design of a multichannel programmable implant for neuromuscular electrical stimulation. *IEEE Transactions on Rehabilitation Engineering*, 7(2):204–214, 1999. [cited at p. 87]

[13] S.K. Arfin and R. Sarpeshkar. An energy-efficient, adiabatic electrode stimulator with inductive energy recycling and feedback current regulation. *Biomedical Circuits and Systems, IEEE Transactions on*, 6(1):1–14, 2012. [cited at p. 82]

[14] S. Ayers, K.D. Gillis, M. Lindau, and B.A. Minch. Design of a cmos potentiostat circuit for electrochemical detector arrays. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 54(4):736–744, 2007. [cited at p. 39]

[15] J.N.Y. Aziz, R. Genov, B.L. Bardakjian, M. Derchansky, and P.L. Carlen. Brain-silicon interface for high-resolution in vitro neural recording. *IEEE Transactions on Biomedical Circuits and Systems*, 1(1):56–62, 2007. [cited at p. 33, 37]

[16] J. Badia, T. Boretius, D. Andreu, C. Azevedo-Coste, T. Stieglitz, and X. Navarro. Comparative analysis of transverse intrafascicular multichannel, longitudinal intrafascicular and multipolar cuff electrodes for the selective stimulation of nerve fascicles. 8(3), 2011. [cited at p. 19]

[17] A. Bandyopadhyay, G. Mulliken, G. Cauwenberghs, and Nitish Thakor. Vlsi potentiostat array for distributed electrochemical neural recording. In *IEEE International Symposium on Circuits and Systems, 2002. ISCAS 2002*, volume 2, pages 740–743, 2002. [cited at p. 39]

[18] K. Bazaka and M.V. Jacob. Implantable devices: Issues and challenges. *Electronics*, 2(1):1–34, 2013. [cited at p. 26]

[19] M. Bennati, F. Thei, M. Rossi, M. Crescentini, G. D'Avino, A. Baschirotto, and M. Tartagni. A sub-pa $\sigma\delta$ current amplifier for single-molecule nanosensors. In *IEEE International Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009*, pages 348–349, 2009. [cited at p. 39]

[20] S. Bhunia, S. Majerus, and M. Sawan. *Implantable Biomedical Microsystems: Design Principles and Applications*. William Andrew, 1 edition, 2015. [cited at p. 28]

[21] M. Bloch, C. Lauterbauch, and W. Weber. High efficiency charge pump circuit for negative high voltage generation at 2 v supply voltage. In *Proceedings of the 24th European Solid-State Circuits Conference, 1998. ESSCIRC 1998*, pages 100–103, 1998. [cited at p. 84]

[22] G. Bontorin, J. Tomas, and S. Renaud. Low noise and low cost neural amplifiers. In *14th IEEE International Conference on Electronics, Circuits and Systems, 2007. ICECS 2007*, pages 1324–1327, 2007. [cited at p. 33]

[23] T. Boretius, K. Yoshida, J. Badia, K. Harreby, A. Kundu, X. Navarro, W. Jensen, and T. Stieglitz. A transverse intrafascicular multichannel electrode (time) to treat phantom limb pain - towards human clinical trials. In *2012 4th IEEE RAS EMBS International Conference on Biomedical Robotics and Biomechatronics (BioRob)*, pages 282–287, 2012. [cited at p. 19, 25, 122]

[24] T. Borghi, A. Bonfanti, G. Zambra, R. Gusmeroli, A.S. Spinelli, and G. Baranauskas. A compact multichannel system for acquisition and processing of neural signals. In *29th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2007. EMBS 2007*, pages 441–444, 2007. [cited at p. 35, 38]

[25] S. Bossi, S. Micera, A. Menciassi, L. Beccai, K.-P. Hoffmann, K.-P. Koch, and P. Dario. On the actuation of thin film longitudinal intrafascicular electrodes. In *The First IEEE/RAS-EMBS International Conference on Biomedical Robotics and Biomechatronics, 2006. BioRob 2006.*, pages 383–388, 2006. [cited at p. 19]

[26] Boundless. Boundless anatomy and physiology: Structure of a nerve, 2015. [cited at p. vii, 11]

[27] S. Boyer, M. Sawan, M. Abdel-Gawad, S. Robin, and M.M. Elhilali. Implantable selective stimulator to improve bladder voiding: design and chronic experiments in dogs. *IEEE Transactions on Rehabilitation Engineering*, 8(4):464–470, 2000. [cited at p. 87]

[28] A. Branner and R.A. Normann. A multielectrode array for intrafascicular recording and stimulation in sciatic nerve of cats. *Brain Research Bulletin*, 51(4):293–306, 2000. [cited at p. 20]

[29] Yazicioglu R.F. Torfs T. et al Brown L., Van de Molengraft J. A low-power, wireless, 8-channel eeg monitoring headset. *Engineering in Medicine and Biology Society (EMBC)*, 32nd Annual International Conference of the IEEE EMBS:4197–4200, August-September 2010. [cited at p. 156]

[30] Tim M. Bruns, Narendra Bhadra, and K.J. Gustafson. Variable patterned pudendal nerve stimuli improves reflex bladder activation. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 16(2):140–148, 2008. [cited at p. 87]

[31] M. Bugbee, N. Donaldson, A. Lickel, N.J.M Rijkhoff, and J. Taylor. An implant for chronic selective stimulation of nerves. *Medical Engineering & Physics*, 23(1):29–36, 2001. [cited at p. 91]

[32] K.J. Bundy. Corrosion and other electrochemical aspects of biomaterials. *Critical Review in Biomedical Engineering*, 22(3-4):139–251, 1994. [cited at p. 26]

[33] D.R. Cantrell and J.B. Troy. A time domain finite element model of extracellular neural stimulation predicts that non-rectangular stimulus waveforms may offer safety benefits. In *30th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2008. EMBS 2008*, pages 2768–2771, 2008. [cited at p. 25]

[34] Silva H.R. Mendes P.M. et al Carmo J.P., Dias N.S. A 2.4-ghz low-power/low-voltage wireless plug-and-play module for eeg applications. *Sensors Journal*, 7:1524–1531, November 2007. [cited at p. 156]

[35] J. Carpaneto, A. Cutrone, S. Bossi, P. Sergi, L. Citi, J. Rigosa, P.M. Rossini, and S. Micera. Activities on pns neural interfaces for the control of hand prostheses. In *2011 Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBC*, pages 4637–4640, 2011. [cited at p. 24]

[36] C.H. Chan, J. Wills, J. LaCoss, J.J. Granacki, and J. Choma. A micro-power low-noise autozeroing cmos amplifier for cortical neural prostheses. In *IEEE Biomedical Circuits and Systems Conference, 2006. BioCAS 2006*, pages 214–217, 2006. [cited at p. 33, 36, 38]

[37] Hinton L. Chan S.R., Torous J. and Yellowlees P. Mobile tele-mental health: Increasing applications and a move to hybrid models of care. *Healthcare*, 2(2):220–233, May 2014. [cited at p. 156]

[38] R. Chebli and M. Sawan. Fully integrated high-voltage front-end interface for ultrasonic sensing applications. *IEEE Transactions on Circuits and Systems I*, 54(1):179–190, 2007. [cited at p. 84]

[39] C.-H. Chen, D.-J. Yao, S.-H. Tseng, S.-W. Lu, C.-C. Chiao, and S.-R. Yeh. Micro-multi-probe electrode array to measure neural signals. *Biosensors and Bioelectronics*, 24(7):1911–1917, 2009. [cited at p. 25, 82]

[40] Kuanfu Chen, Zhi Yang, Linh Hoang, J. Weiland, M. Humayun, and Wentai Liu. An integrated 256-channel epiretinal prosthesis. *IEEE Journal of Solid-State Circuits*, 45(9):1946–1956, 2010. [cited at p. 89, 93]

[41] H. Chun, Y. Yang, and T. Lehmann. Required matching accuracy of biphasic current pulse in multi-channel current mode bipolar stimulation for safety. In *2012 Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 3025–3028, 2012. [cited at p. 25]

[42] Hosung Chun, Yuanyuan Yang, and T. Lehmann. Required matching accuracy of biphasic current pulse in multi-channel current mode bipolar stimulation for safety. In *2012 Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 3025–3028, 2012. [cited at p. 91]

[43] I.P. Clements, V.J. Mukhatyar, A. Srinivasan, J.T. Bentley, D.S. Andreasen, and R.V. Bellamkonda. Regenerative scaffold electrodes for peripheral nerve interfacing. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 21(4):554–566, July 2013. [cited at p. 21]

[44] S. Cogan. Neural stimulation and recording electrodes. *Annual Review of Biomedical Engineering*, 10:275–309, 2008. [cited at p. 25]

[45] S.C. DeMarco, Wentai Liu, P.R. Singh, G. Lazzi, M.S. Humayun, and J.D. Weiland. An arbitrary waveform stimulus circuit for visual prostheses using a low-area multibias dac. *IEEE Journal of Solid-State Circuits*, 38(10):1679–1690, 2003. [cited at p. 87, 92, 93]

[46] A. Demosthenous, I. Pachnis, Dai Jiang, and N. Donaldson. An integrated amplifier with passive neutralization of myoelectric interference from neural recording tripoles. *IEEE Sensors Journal*, 13(9):3236–3248, 2013. [cited at p. 32, 78, 79]

[47] J.F. Dickson. On-chip high-voltage generation in mnos integrated circuits using an improved voltage multiplier technique. *IEEE Journal of Solid-State Circuits*, 11(3):374–378, 1976. [cited at p. 82, 101]

[48] E.G. Duffin. Implantable defibrillator. *The Biomed Eng handbook*, 2006. [cited at p. 128]

[49] M.A El Khaddar, H. Harroud, M. Boulmalf, M. ElKoutbi, and A Habbani. Emerging wireless technologies in e-health trends, challenges, and framework design issues. *Multimedia Computing and Systems (ICMCS), 2012 International Conference on*, pages 440–445, May 2012. [cited at p. 156]

[50] Emotiv. *http://emotiv.com*, December 2013. [cited at p. 156]

[51] M. Forde and P. Ridgely. Implantable cardiac pacemakers. *The Biomed Eng handbook*, 2006. [cited at p. 128]

[52] T. Foutz and C. McIntyre. Evaluation of novel stimulus waveforms for deep brain stimulation. *Journal of neural engineering*, 7(6), 2010. [cited at p. 87]

[53] W. Franks, I. Schenker, P. Schmutz, and A. Hierlemann. Impedance characterization and modeling of electrodes for biomedical applications. *IEEE Transactions on Biomedical Engineering*, 52(7):1295–1302, 2005. [cited at p. 25]

[54] H. Gao, R.M. Walker, P. Nuyujukian, K.A.A. Makinwa, K.V. Shenoy, B. Murmann, and T.H. Meng. Hermese: A 96-channel full data rate direct neural interface in 0.13μ m CMOS. *IEEE Journal of Solid-State Circuits*, 47(4):1043–1055, 2012. [cited at p. 32, 37]

[55] R. Genov, Milutin Stanacevic, Mihir Naware, G. Cauwenberghs, and N.V. Thakor. 16-channel integrated potentiostat for distributed neurochemical sensing. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 53(11):2371–2376, 2006. [cited at p. 39]

[56] J. Georgiou and C. Toumazou. A 126μw cochlear chip for a totally implantable system. *IEEE Journal of Solid-State Circuits*, 40(2):430–443, 2005. [cited at p. 92]

[57] W. Germanovix and C. Toumazou. Design of a micropower current-mode log-domain analog cochlear implant. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 47(10):1023–1046, 2000. [cited at p. 92]

[58] G. Giudetti, J. del Valle Macia, X. Navarro Acebes, and S. Micera. Ngf-loaded plga microparticles for advanced multifunctional regenerative electrodes. In *2014 36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 1993–1995, 2014. [cited at p. 21]

[59] C.-S.A. Gong, Kai-Wen Yao, Jyun-Yue Hong, and Muh-Tian Shiue. On investigation into a cmos-process-based high-voltage driver applied to implantable microsystem. In *VLSI Design, Automation, and Test (VLSI-DAT), 2012 International Symposium on*, pages 1–4, 2012. [cited at p. 86]

[60] A. Gore, S. Chakrabartty, S. Pal, and E.C. Alocilja. A multichannel femtoampere-sensitivity potentiostat array for biosensing applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 53(11):2357–2363, 2006. [cited at p. 36, 39]

[61] B. Gosselin, V. Simard, and M. Sawan. Low-power implantable microsystem intended to multichannel cortical recording. In *Proceedings of the 2004 International Symposium on Circuits and Systems, 2004. ISCAS 2004*, volume 4, pages 5–8, 2004. [cited at p. 35, 38]

[62] J.A. Gregory, A. Borna, S. Roy, X. Wang, B. Lewandowski, M. Schmidt, and K. Najafi. Low-cost wireless neural recording system and software. In *Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2009. EMBC 2009*, pages 3833–3836, 2009. [cited at p. 32]

[63] W.M. Grill and J.T. Mortimer. Stimulus waveforms for selective neural stimulation. *IEEE Engineering in Medicine and Biology Magazine*, 14(4):375–385, 1995. [cited at p. 87]

[64] R. Gusmeroli, A. Bonfanti, T. Borghi, A.S. Spinelli, and G. Baranauskas. A switched-capacitor neural preamplifier with an adjustable pass-band for fast recovery following stimulation. In *28th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2006. EMBS 2006*, pages 652–655, 2006. [cited at p. 35, 38]

[65] M.E. Halpern and J. Fallon. Current waveforms for neural stimulation-charge delivery with reduced maximum electrode voltage. *IEEE Transactions on Biomedical Engineering*, 57(9):2304–2312, 2010. [cited at p. 25, 87]

[66] O.P. Hamill, A. Marty, E. Neher, B. Sakmann, and F.J. Sigworth. Improved patch-clamp techniques for high-resolution current recording from cells and cell-free membrane patches. *Pflugers Archiv*, 391(2):85–100, 1981. [cited at p. 39]

[67] D. Han, Yuanjin Zheng, R. Rajkumar, G.S. Dawe, and Minkyu Je. A 0.45 V 100-channel neural-recording ic with sub-μ W/channel consumption in 0.18μm CMOS. *IEEE Transactions on Biomedical Circuits and Systems*, 7(6):735–746, 2013. [cited at p. 32, 33, 34, 37]

[68] T.J. Harpster, S.A. Nikles, Mehmet R. Dokmeci, and K. Najafi. Long-term hermeticity and biological performance of anodically bonded glass-silicon implantable packages. *IEEE Transactions on Device and Materials Reliability*, 5(3):458–466, 2005. [cited at p. 28]

[69] R.R. Harrison. A versatile integrated circuit for the acquisition of biopotentials. In *Custom Integrated Circuits Conference, 2007. CICC '07. IEEE*, pages 115–122, 2007. [cited at p. 23]

[70] R.R. Harrison and C. Charles. A low-power low-noise cmos amplifier for neural recording applications. *Solid-State Circuits, IEEE Journal of*, 38(6):958–965, 2003. [cited at p. 23, 24, 32, 34, 37, 44]

[71] R.R. Harrison, R.J. Kier, C.A. Chestek, V. Gilja, P. Nuyujukian, S. Ryu, B. Greger, F. Solzbacher, and K.V. Shenoy. Wireless neural recording with single low-power integrated circuit. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 17(4):322–329, 2009. [cited at p. 32, 37]

[72] C. Hassler, R.P. von Metzen, P. Ruther, and T. Stieglitz. Characterization of parylene c as an encapsulation material for implanted neural prostheses. *Journal of Biomedical Materials Research Part B: Applied Biomaterials*, 93B(1):266–274, 2010. [cited at p. 28]

[73] J. Holleman and B. Otis. A sub-microwatt low-noise amplifier for neural recording. In *29th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2007. EMBS 2007*, pages 3930–3933, 2007. [cited at p. 33]

[74] M. R. Hoque, T. Ahmad, T. R. McNutt, H. A. Mantooth, and M. M. Mojarradi. A technique to increase the efficiency of high-voltage charge pumps. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 53(5):364–368, 2006. [cited at p. 126]

[75] T. Horiuchi, T. Swindell, D. Sander, and P. Abshier. A low-power cmos neural amplifier with amplitude measurements for spike sorting. In *Proceedings of the 2004 International Symposium on Circuits and Systems, 2004. ISCAS 2004*, volume 4, pages 29–32, 2004. [cited at p. 33, 36, 38]

[76] ChristieQ. Huang, PaulM. Carter, and RobertK. Shepherd. Stimulus induced ph changes in cochlear implants: An in vitro and in vivo study. *Annals of Biomedical Engineering*, 29(9):791–802, 2001. [cited at p. 95]

[77] Wen Chang Huang, Jin Chang Cheng, and Po Chin Liou. A charge pump circuit — cascading high-voltage clock generator. In *4th IEEE International Symposium on Electronic Design, Test and Applications, 2008. DELTA 2008*, pages 332–337, 2008. [cited at p. viii, 84, 85]

[78] Ya-Chun Huang, Ming-Dou Ker, and Chun-Yu Lin. Design of negative high voltage generator for biphasic stimulator with soc integration consideration. In *Biomedical Circuits and Systems Conference (BioCAS), 2012 IEEE*, pages 29–32, Nov 2012. [cited at p. 25, 82, 93]

[79] M. Svensson H.-U. Wittchen et al J. Olesen, A. Gustavsson. The economic cost of brain disorders in europe. *European Journal of Neurology*, 19:155–162, January 2012. [cited at p. 155]

[80] N. Jackson, S. Anand, M. Okandan, and J. Muthuswamy. Nonhermetic encapsulation materials for mems-based movable microelectrodes for long-term implantation in the brain. *Journal of Microelectromechanical Systems*, 18(6):1234–1245, 2009. [cited at p. 28]

[81] Dai Jiang, D. Cirmirakis, and A. Demosthenous. A vestibular prosthesis with highly-isolated parallel multichannel stimulation. *IEEE Transactions on Biomedical Circuits and Systems*, 9(1):124–137, 2015. [cited at p. 24]

[82] F. Jin, X. Liu, P.K. Chu, G. Xu, L. Shen, and H. Tong. Bioactivity and corrosion behavior of magnesium alloys treated by plasma electrolytic oxidation. pages 334–334, 2006. [cited at p. 26]

[83] T. Jochum, T. Denison, and P. Wolf. Integrated circuit amplifiers for multi-electrode intracortical recording. *Journal of Neural Engineering*, 6(1), 2009. [cited at p. 32]

[84] S. Julien, T. Peters, F. Ziemssen, B. Arango-Gonzalez, S. Beck, H. Thielecke, H. BÃijth, S. Van Vlierberghe, M. Sirova, P. Rossmann, B. Rihova, E. Schacht, P. Dubruel, E. Zrenner, and U. Schraermeyer. Implantation of ultrathin, biofunctionalized polyimide membranes into the subretinal space of rats. *Biomaterials*, 32(16):3890–3898, 2011. [cited at p. 28]

[85] M.J. Kane, P.P. Breen, F. Quondamatteo, and G. OLaighin. Bion microstimulators: A case study in the engineering of an electronic implantable medical device. *Medical Engineering & Physics*, 33(1):7–16, 2011. [cited at p. 28, 128]

[86] A. Kiourti and K.S. Nikita. A review of implantable patch antennas for biomedical telemetry: Challenges and solutions [wireless corner]. *IEEE Antennas and Propagation Magazine*, 54(3):210–228, 2012. [cited at p. 128]

[87] F. Kohler, M.A. Ulloa, J.S. Ordonez, T. Stieglitz, and M. Schuettler. Reliability investigations and improvements of interconnection technologies for the wireless brain-machine interface - 'braincon'. In *2013 6th International IEEE/EMBS Conference on Neural Engineering (NER)*, pages 1013–1016, 2013. [cited at p. 29]

[88] A. Kundu, K.R. Harreby, K. Yoshida, T. Boretius, T. Stieglitz, and W. Jensen. Stimulation selectivity of the "thin-film longitudinal intrafascicular electrode" (tflife) and the "transverse intrafascicular multi-channel electrode" (time) in the large nerve animal model. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 22(2):400–410, 2014. [cited at p. 19]

[89] N. Lago, E. Udina, and X. Navarro. Regenerative electrodes for interfacing injured peripheral nerves: neurobiological assessment. In *The First IEEE/RAS-EMBS International Conference on Biomedical Robotics and Biomechatronics, 2006. BioRob 2006.*, pages 1149–1153, 2006. [cited at p. 21]

[90] P.J. Langlois, A. Demosthenous, I. Pachnis, and N. Donaldson. High-power integrated stimulator output stages with floating discharge over a wide voltage range for nerve stimulation. *IEEE Transactions on Biomedical Circuits and Systems*, 4(1):39–48, 2010. [cited at p. 86, 87, 93]

[91] J. Lee, H.-G. Rhew, D.R. Kipke, and M.P. Flynn. A 64 channel programmable closed-loop neurostimulator with 8 channel neural amplifier and logarithmic adc. *IEEE Journal of Solid-State Circuits*, 45(9):1935–1945, 2010. [cited at p. 32, 37]

[92] S.Y. Lee and S.C. Lee. An implantable wireless bidirectional communication microstimulator for neuromuscular stimulation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 52(12):2526–2538, 2005. [cited at p. 32, 33, 34, 35, 36, 37]

[93] Xing Li, Yan Lu, Chi-Ying Tsui, and Wing-Hung Ki. An adaptive wireless powering and data telemetry system for optic nerve stimulation. In *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1404–1407, 2014. [cited at p. 24]

[94] K. Limnuson, D.J. Tyler, and P. Mohseni. Integrated electronics for peripheral nerve recording and signal processing. In *Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2009. EMBC 2009*, pages 1639–1642, 2009. [cited at p. 32, 37]

[95] C.-M. Lin, Y.-T. Lee, S.-R. Yeh, and W. Fang. Flexible carbon nanotubes electrode for neural recording. *Biosensors and Bioelectronics*, 24(9):2791–2797, 2009. [cited at p. 20]

[96] Chi-Hung Lin and K. Bult. A 10-b, 500-msample/s cmos dac in $0.6mm^2$. *IEEE Journal of Solid-State Circuits*, 33(12):1948–1958, 1998. [cited at p. 92]

[97] Chin-Teng Lin, Li-Wei Ko, Jin-Chern Chiou, Jeng-Ren Duann, Ruey-Song Huang, Sheng-Fu Liang, Tzai-Wen Chiu, and Tzyy-Ping Jung. Noninvasive neural prostheses using mobile and wireless eeg. *Proceedings of the IEEE*, 96(7):1167–1183, July 2008. [cited at p. 156]

[98] C.C. Liu. A 70db gain low-power band-pass amplifier for bio-signals sensing applications. In *IEEE International Symposium on Circuits and Systems, 2007. ISCAS 2007*, pages 577–580, 2007. [cited at p. 33, 38, 86]

[99] X. Liu, A. Demosthenous, and N. Donaldson. An integrated stimulator with dc-isolation and fine current control for implanted nerve tripoles. *IEEE Journal of Solid-State Circuits*, 46(7):1701–1714, 2011. [cited at p. 87, 93]

[100] X. Liu, B. Subei, M. Zhang, A.G. Richardson, T.H. Lucas, and J. Van der Spiegel. The pennbmbi: A general purpose wireless brain-machine-brain interface system for unrestrained animals. In *2014 IEEE International Symposium on Circuits and Systems (ISCAS),*, pages 650–653, 2014. [cited at p. 32]

[101] Xiao Liu, A. Demosthenous, and N. Donaldson. An integrated implantable stimulator that is fail-safe without off-chip blocking-capacitors. *IEEE Transactions on Biomedical Circuits and Systems*, 2(3):231–244, 2008. [cited at p. 87, 91, 93, 95]

[102] Xiao Liu, A. Demosthenous, Dai Jiang, and N. Donaldson. Design of an implantable stimulator asic with self-adapting supply. In *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1881–1884, 2013. [cited at p. 82, 87]

[103] Xiao Liu, A. Demosthenous, A. Vanhoestenberghe, Dai Jiang, and N. Donaldson. Active books: The design of an implantable stimulator that minimizes cable count using integrated circuits very close to electrodes. *IEEE Transactions on Biomedical Circuits and Systems*, 6(3):216–227, 2012. [cited at p. 87, 93]

[104] G.E. Loeb, R.A. Peck, J. Singh, Y.-H. Kim, S. Deshpande, L.L. Baker, and J.T. Bryant. Mechanical loading of rigid intramuscular implants. *Biomedical Microdevices*, 9(6):901–910, 2007. [cited at p. 28]

[105] D. Loi, C. Carboni, G. Angius, G.N. Angotzi, M. Barbaro, L. Raffo, S. Raspopovic, and X. Navarro. Peripheral neural activity recording and stimulation system. *IEEE Transactions on Biomedical Circuits and Systems*, 5(4):368–379, 2011. [cited at p. 32, 40, 94]

[106] C.M. Lopez, A. Andrei, S. Mitra, M. Welkenhuysen, W. Eberle, C. Bartic, R. Puers, R.F. Yazicioglu, and G.G.E. Gielen. An implantable 455-active-electrode 52-channel CMOS neural probe. *IEEE Journal of Solid-State Circuits*, 49(1):248–261, 2014. [cited at p. 32, 37]

[107] C. Lupu and M. Cosmin-Constantin. Actual portable devices as base for telemedicine and e-health: Research and case study application. *E-Health and Bioengineering Conference (EHB), 2013*, pages 1–4, Nov 2013. [cited at p. 156]

[108] O. Macherey, A. Van Wieringen, R.P. Carlyon, J.M. Deeks, and J. Wouters. Asymmetric pulses in cochlear implants: Effects of pulse shape, polarity, and rate. *Journal of the Association for Research in Otolaryngology*, 7(3):253–266, 2006. [cited at p. 87]

[109] O. Macherey, A. Van Wieringen, R.P. Carlyon, I. Dhooge, and J. Wouters. Forward-masking patterns produced by symmetric and asymmetric pulse shapes in electric hearing. *The Journal of the Acoustical Society of America*, 127(1):326–338, 2010. [cited at p. 87]

[110] E.M. Maynard, C.T. Nordhausen, and R.A. Normann. The utah intracortical electrode array: A recording structure for potential brain-computer interfaces. *Electroencephalography and Clinical Neurophysiology*, 102(3):228–239, 1997. [cited at p. 20]

[111] D.R. Merrill, J. Bikson, and J.G.R. Jefferys. Electrical stimulation of excitable tissue: design of efficacious and safe protocols. *Journal of Neuroscience Methods*, 141(2):171–198, 2005. [cited at p. 25, 87]

[112] C.S. Mestais, G. Charvet, F. Sauter-Starace, M. Foerster, D. Ratel, and A.L. Benabid. Wimagine: Wireless 64-channel ecog recording implant for long term clinical applications. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 23(1):10–21, 2015. [cited at p. 28, 32, 37, 128]

[113] S. Micera, A. Benvenuto, J. Carpaneto, C.D. Cipriani, L. Citi, P. Dario, L. Denaro, G. Dipino, F. Ferreri, E. Guglielmelli, K.-P. Hoffmann, S. Raspopovic, J. Rigosa, L. Rossini, P. Rossini, M. Tombini, and G. Cavallo. Double nerve intraneural interface implant on a human amputee for robotic hand control. *Clinical Neurophysiology*, 121(5):777–783, 2010. [cited at p. 19]

[114] Micromed. Brain quick. *http://www.micromed.eu*, 2014. [cited at p. 163]

[115] M. Miguez and A. Arnaud. A low noise gm-c chopper for eng signal amplification. In *Proceedings of the XIII Workshop de Iberchip*, 2007. [cited at p. 33, 35, 38]

[116] V. Mihajlovic, B. Grundlehner, R. Vullers, and J. Penders. Wearable, wireless eeg solutions in daily life applications: What are we missing? *Biomedical and Health Informatics, IEEE Journal of*, PP(99):1–1, 2014. [cited at p. 156]

[117] I.R. Minev, D.J. Chew, E. Delivopoulos, J.W. Fawcett, and S.P. Lacour. High sensitivity recording of afferent nerve activity using ultra-compliant microchannel electrodes: an acute in vivo validation. *Journal of Neural Engineering*, 9(2), 2012. [cited at p. 21]

[118] W. Mokwa. Ophthalmic implants. In *2003 Proceedings of IEEE Sensors*, volume 2, pages 980–986, 2003. [cited at p. 89]

[119] J. Mouine, K.A. Ammar, and Z. Chtourou. A completely programmable and very flexible implantable pain controller. In *Proceedings of the 22nd Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2000*, volume 2, pages 1104–1107, 2000. [cited at p. 87]

[120] M. Mueller, F. Kohler, J.S. Ordonez, T. Stieglitz, and M. Schuettler. Fabrication of flat electrodes utilizing picosecond laser manufacturing technology: Preliminary study for fabrication of a novel transverse intrafascicular multichannel electrode. In *2014 IEEE 19th International Functional Electrical Stimulation Society Annual Conference (IFESS)*, pages 1–4, Sept 2014. [cited at p. 28]

[121] K. Murari, Nitish Thakor, Milutin Stanacevic, and G. Cauwenberghs. Wide-range, picoampere-sensitivity multichannel vlsi potentiostat for neurotransmitter sensing. In *26th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2004. IEMBS 2004*, volume 2, pages 4063–4066, 2004. [cited at p. 39]

[122] P. Nadeau and M. Sawan. A flexible high voltage biphasic current-controlled stimulator. In *Biomedical Circuits and Systems Conference, 2006. BioCAS 2006. IEEE*, pages 206–209, 2006. [cited at p. 25, 83, 87]

[123] S. Nag, D. Sharma, and N.V. Thakor. A 24 vpp compliant biphasic stimulator for inductively powered animal behavior studies. In *2013 35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 3242–3245, 2013. [cited at p. 82]

[124] S. Nag, D. Sharma, and N.V. Thakor. Ultra-low power neural stimulator for electrode interfaces. In *2014 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pages 488–491, 2014. [cited at p. 82, 87, 93]

[125] G. Naples, J. Mortimer, A. Scheiner, and J. Sweeney. A spiral nerve cuff electrode for peripheral nerve stimulation. *IEEE transaction on biomedical engineering*, 35:905–916, 1988. [cited at p. 18]

[126] X. Navarro, T.B. Krueger, N. Lago, S. Micera, T. Stieglitz, and P. Dario. A critical review of interfaces with the peripheral nervous system for the control of neuroprostheses and hybrid bionic systems. *Journal of the Peripheral Nervous System*, 10(3):229–258, 2005. [cited at p. 21]

[127] M.H. Nazari and R. Genov. A fully differential cmos potentiostat. In *IEEE International Symposium on Circuits and Systems, 2009. ISCAS 2009*, pages 2177–2180, 2009. [cited at p. 39]

[128] NeuroSky. *http://neurosky.com*, 2009. [cited at p. 156]

[129] H.P. Neves. *1 - Materials for implantable systems*, pages 3–38. Woodhead Publishing, 2013. [cited at p. 26]

[130] C. O. Oluigbo, A. Salma, and A. R. Rezai. Deep brain stimulation for neurological disorders. *IEEE Reviews in Biomedical Engineering*, 5:88–99, 2012. [cited at p. 81]

[131] J. Ordonez, P. Dautel, M. Schuettler, and T. Stieglitz. Hermetic glass soldered micro-packages for a vision prosthesis. In *2012 Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 2784–2787, 2012. [cited at p. 28, 128]

[132] M. Ortmanns, A. Rocke, M. Gehrke, and H.-J. Tiedtke. A 232-channel epiretinal stimulator asic. *IEEE Journal of Solid-State Circuits*, 42(12):2946–2959, 2007. [cited at p. 87]

[133] G. Palumbo and D. Pappalardo. Charge pump circuits: An overview on design strategies and topologies. *Circuits and Systems Magazine, IEEE*, 10(1):31–45, 2010. [cited at p. 101, 103]

[134] H. Park and D.M. Durand. Motion control of the rabbit ankle joint using a flat interface nerve electrode. In *Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2009. EMBC 2009.*, pages 6789–6792, 2009. [cited at p. 18]

[135] Jin-Young Park and Yeonbae Chung. A low-voltage charge pump circuit with high pumping efficiency in standard cmos logic process. In *IEEE Conference on Electron Devices and Solid-State Circuits, 2007. EDSSC 2007*, pages 317–320, 2007. [cited at p. 83]

[136] S. Patki, B. Grundlehner, A Verwegen, S. Mitra, J. Xu, A Matsumoto, R.F. Yazicioglu, and J. Penders. Wireless eeg system with real time impedance monitoring and active electrodes. *Biomedical Circuits and Systems Conference (BioCAS), 2012 IEEE*, pages 108–111, Nov 2012. [cited at p. 156]

[137] R. Pelliconi, D. Iezzi, A. Baroni, M. Pasotti, and P.L. Rolandi. Power efficient charge pump in deep submicron standard cmos technology. *IEEE Journal of Solid-State Circuits*, 38(6):1068–1071, 2003. [cited at p. viii, 83, 84]

[138] Vadim S. Polikov, Patrick A. Tresco, and William M. Reichert. Response of brain tissue to chronically implanted neural electrodes. *Journal of Neuroscience Methods*, 148(1):1–18, 2005. [cited at p. 86]

[139] A. Prasad and J.C. Sanchez. Quantifying long-term microelectrode array functionality using chronic in vivo impedance testing. *Journal of Neural Engineering*, 9(2), 2012. [cited at p. 20, 28]

[140] L. Pylarinos. Charge pumps: An overview. In *In Proceedings of the IEEE International Symposium on Circuits and Systems*, 2003. [cited at p. 83]

[141] C. Qian, J. Parramon, and E. Sanchez-Sinencio. A micropower low-noise neural recording front-end circuit for epileptic seizure detection. *IEEE Journal of Solid-State Circuits*, 46(6):1392–1405, 2011. [cited at p. 34, 38]

[142] Quasar. *http://www.quasarusa.com*, December 2013. [cited at p. 156]

[143] S. Raspopovic, M. Capogrosso, J. Badia, X. Navarro, and S. Micera. Experimental validation of a hybrid computational model for selective stimulation using transverse intrafascicular multichannel electrodes. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 20(3):395–404, 2012. [cited at p. 124]

[144] Stanisa Raspopovic, Marco Capogrosso, Francesco Maria Petrini, Marco Bonizzato, Jacopo Rigosa, Giovanni Di Pino, Jacopo Carpaneto, Marco Controzzi, Tim Boretius, Eduardo Fernandez, Giuseppe Granata, Calogero Maria Oddo, Luca Citi, Anna Lisa Ciancio, Christian Cipriani, Maria Chiara Carrozza, Winnie Jensen, Eugenio Guglielmelli, Thomas Stieglitz, Paolo Maria Rossini, and Silvestro Micera. Restoring natural sensory feedback in real-time bidirectional hand prostheses. *Science Translational Medicine*, 6(222):222ra19, 2014. [cited at p. 94, 95, 124]

[145] B. Razavi. *Design of analog cmos integrated circuits*. 2001. [cited at p. 23, 44]

[146] H.-G. Rhew, J. Jeong, J.A. Fredenburg, S. Dodani, P.G. Patil, and M.P. Flynn. A fully self-contained logarithmic closed-loop deep brain stimulation soc with wireless telemetry and wireless power management. *IEEE Journal of Solid-State Circuits*, 49(10):2213–2227, 2014. [cited at p. 32, 37]

[147] Hyo-Gyuem Rhew, Jaehun Jeong, J.A. Fredenburg, S. Dodani, P.G. Patil, and M.P. Flynn. A fully self-contained logarithmic closed-loop deep brain stimulation soc with wireless telemetry and wireless power management. *IEEE Journal ofSolid-State Circuits*, 49(10):2213–2227, 2014. [cited at p. 82, 86, 87, 93]

[148] R. Rieger, M. Schuettler, D. Pal, C. Clarke, P. Langlois, J. Taylor, and N. Donaldson. Very low-noise eng amplifier system using CMOS technology. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 14(4):427–437, 2006. [cited at p. 32, 37, 78, 79]

[149] R. Rieger and J. Taylor. Design strategies for multi-channel low-noise recording systems. *Analog Integrated Circuits and Signal Processing*, 58(2):123–133, 2009. [cited at p. 43]

[150] R. Rieger, J. Taylor, A. Demosthenous, N. Donaldson, and P.J. Langlois. Design of a low-noise preamplifier for nerve cuff electrode recording. *IEEE Journal of Solid-State Circuits*, 38(8):1373–1379, 2003. [cited at p. 23, 32]

[151] L. Robblee and T. Rose. Electrochemical guidelines for selection of protocols and electrode materials for neural stimulation. *Agnew WF, McCreery DB (Eds.). Neural prostheses: fundamental studies. Prentice Hall, NJ: Englewood Cliffs*, pages 25–66, 1990. [cited at p. 25]

[152] C. Robillard, J. Coulombe, P. Nadeau, and M. Sawan. Neural stimulation safety and energy efficiency: Waveform analysis and validation. page 019, 2006. [cited at p. 25]

[153] J. SacristÃąn-Riquelme and M.T. OsÃl's. Implantable stimulator and recording device for artificial prosthesis control. *Microelectronics Journal*, 38(12):1135–1149, 2007. [cited at p. 34, 36, 38, 78, 79]

[154] M. Sahin and Y. Tie. Non-rectangular waveforms for neural stimulation with practical electrodes. *Journal of Neural Engineering*, 4(3), 2007. [cited at p. 25]

[155] A. Saiz-Vela, F. Mounaim, P. Miribel-Catala, M. Sawan, and J. Samitier. Miniaturized sip supply board based on tpvd charge pump ics for high-voltage biomedical applications. In *2011 IEEE 9th International New Circuits and Systems Conference (NEWCAS)*, pages 514–517, 2011. [cited at p. viii, 84, 85]

[156] Robert S.H. Istepanian Sapal Tachakra, X.H. Wang and Y.H. Song. Mobile e-health: The unwired evolution of telemedicine. *Telemedicine Journal and e-Health*, 9(3):247–257, September 2003. [cited at p. 156]

[157] M. Sawan. Wireless smart implants dedicated to multichannel monitoring and microstimulation. In *IEEE/ACS International Conference on Pervasive Services, 2004. ICPS 2004*, pages 21–26, 2004. [cited at p. 35]

[158] M. Sawan, Yamu Hu, and J. Coulombe. Wireless smart implants dedicated to multichannel monitoring and microstimulation. *IEEE Circuits and Systems Magazine*, 5(1):21–39, 2005. [cited at p. 36]

[159] E. Scheme and K. Englehart. Electromyogram pattern recognition for control of powered upper-limb prostheses: State of the art and challenges for clinical use. *Journal of Rehabilitation Research & Development*, 48(6):643–660, 2011. [cited at p. 1]

[160] M.A. Schiefer, M. Freeberg, G.J.C. Pinault, J. Anderson, H. Hoyen, D.J. Tyler, and R.J. Triolo. Selective activation of the human tibial and common peroneal nerves with a flat interface nerve electrode. *Journal of Neural Engineering*, 10(5), 2013. [cited at p. 18]

[161] M.A. Schiefer, K.H. Polasek, R.J. Triolo, G.C. Pinault, and D.J. Tyler. Selective stimulation of the human femoral nerve with a flat interface nerve electrode. *Journal of Neural Engineering*, 7(2), 2010. [cited at p. 18]

[162] M. Schuettler. Electrochemical properties of platinum electrodes in vitro: Comparison of six different surface qualities. In *29th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2007. EMBS 2007*, pages 186–189, 2007. [cited at p. 28]

[163] M. Schuettler, F. Kohler, J.S. Ordonez, and T. Stieglitz. Hermetic electronic packaging of an implantable brain-machine-interface with transcutaneous optical data communication. In *2012 Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 3886–3889, 2012. [cited at p. 28, 128]

[164] M. Schuettler, J.S. Ordonez, T.S. Santisteban, A. Schatz, J. Wilde, and T. Stieglitz. Fabrication and test of a hermetic miniature implant package with 360 electrical feedthroughs. In *2010 Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 1585–1588, 2010. [cited at p. 26]

[165] M. Schuettler, V. Seetohul, N.J.M. Rijkhoff, F.V. Moeller, N. Donaldson, and J. Taylor. Fibre-selective recording from peripheral nerves using a multiple-contact cuff: Report on pilot pig experiments. In *2011 Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBC*, pages 3103–3106, 2011. [cited at p. 32]

[166] R.N. Scott and P.A. Parker. Electromyogram pattern recognition for control of powered upper-limb prostheses: State of the art and challenges for clinical use. *Journal of Medical Engineering & Technology*, 12(4):143–151, 1988. [cited at p. 1]

[167] J. Shin, In-Young Chung, Young June Park, and Hong Shick Min. A new charge pump without degradation in threshold voltage due to body effect [memory applications]. *IEEE Journal of Solid-State Circuits*, 35(8):1227–1230, 2000. [cited at p. viii, 83, 84]

[168] M. Shoaran, M.H. Kamal, C. Pollo, P. Vandergheynst, and A. Schmid. Compact low-power cortical recording architecture for compressive multichannel data acquisition. *IEEE Transactions on Biomedical Circuits and Systems*, 8(6):857–870, 2014. [cited at p. 32]

[169] R. Shulyzki, K. Abdelhalim, A. Bagheri, M.T. Salam, C.M. Florez, J.L. Perez Velazquez, P.L. Carlen, and R. Genov. 320-channel active probe for high-resolution neuromonitoring and responsive neurostimulation. *IEEE Transactions on Biomedical Circuits and Systems*, 9(1):34–49, Feb 2015. [cited at p. 32]

[170] F.J. Sigworth and K.G. Klemic. Microchip technology in ion-channel research. *IEEE Transactions on NanoBioscience*, 4(1):121–127, 2005. [cited at p. 39]

[171] T. Sinkjaer and D. Popovic. Peripheral nerve stimulation in neurological rehabilitation. In *First International IEEE EMBS Conference on Neural Engineering, 2003*, pages 474–476, 2003. [cited at p. 24]

[172] M. Sivaprakasam, Wentai Liu, M.S. Humayun, and J.D. Weiland. A variable range bi-phasic current stimulus driver circuitry for an implantable retinal prosthetic device. *IEEE Journal of Solid-State Circuits*, 40(3):763–771, 2005. [cited at p. 89, 92, 93]

[173] Aaron Smith. Smartphone ownership 2013. *Pew Research Center, http://www.pewinternet.org /2013/06/05/smartphone-ownership-2013/*, June 2013. [cited at p. 156]

[174] A. Srinivasan, M. Tahilramani, J.T. Bentley, R.K. Gore, D.C. Millard, V.J. Mukhatyar, A. Joseph, A.S. Haque, G.B. Stanley, A.W. English, and R.V. Bellamkonda. Microchannel-based regenerative scaffold for chronic peripheral nerve interfacing in amputees. *Biomaterials*, 41(0):151–165, 2015. [cited at p. 21]

[175] R. St-Amand, Y. Savaria, and M. Sawan. Design optimization of a current source for microstimulator applications. In *Proceedings of the 37th Midwest Symposium on Circuits and Systems, 1994*, volume 1, pages 129–132, 1994. [cited at p. 92]

[176] M. Stanacevic, K. Murari, A. Rege, G. Cauwenberghs, and N.V. Thakor. Vlsi potentiostat array with oversampling gain modulation for wide-range neurotransmitter sensing. *IEEE Transactions on Biomedical Circuits and Systems*, 1(1):63–72, 2007. [cited at p. 39]

[177] M.S.J. Steyaert and W.M.C. Sansen. A micropower low-noise monolithic instrumentation amplifier for medical purposes. *Solid-State Circuits, IEEE Journal of*, 22(6):1163–1168, 1987. [cited at p. 24]

[178] T. Stieglitz and M. Schuettler. *2 - Material-tissue interfaces in implantable systems*, pages 39–67. Woodhead Publishing Series in Biomaterials. Woodhead Publishing, 2013. [cited at p. xii, 29]

[179] P. Strojnik and P.H. Peckham. Implantable stimulators for neuromuscular control. *The Biomed Eng handbook*, 2006. [cited at p. 128]

[180] Austria Micro System. http://asic.ams.com/. [cited at p. 52, 109]

[181] B. Tahayori and S. Dokos. Optimal stimulus profiles for neuroprosthetic devices: Monophasic versus biphasic stimulation. In *2013 35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 5978–5981, 2013. [cited at p. 87]

[182] M.D. Tarler and J.T. Mortimer. Selective and independent activation of four motor fascicles using a four contact nerve-cuff electrode. *IEEE transaction on nerual systems and rehabilitation engineering*, 12(2):251âĂŞ257, 2004. [cited at p. 18]

[183] T. Tateno and J. Nishikawa. A cmos ic-based multisite measuring system for stimulation and recording in neural preparations in vitro. *Frontiers in Neuroengineering*, 7(39), 2014. [cited at p. 32]

[184] J.D. Techer, S. Bernard, Y. Bertrand, G. Cathebras, and D. Guiraud. New implantable stimulator for the fes of paralyzed muscles. In *Proceeding of the 30th European Solid-State Circuits Conference, 2004. ESSCIRC 2004*, pages 455–458, 2004. [cited at p. 91]

[185] F. Thei, M. Rossi, M. Bennati, M. Crescentini, F. Lodesani, F. Morgan, and M. Tartagni. Parallel recording of single ion channels: A heterogeneous system approach. *IEEE Transactions on Nanotechnolog*, 9(3):295–302, 2010. [cited at p. 39]

[186] A.K. Thota, S. Kuntaegowdanahalli, J. Orbay, A.K. Starosciak, J.J. Abbas, K.W. Horch, and Ranu Jung. A multi-lead multi-electrode system for neural-interface enabled advanced prostheses. In *Biomedical Engineering Conference (SBEC), 2013 29th Southern*, pages 109–110, 2013. [cited at p. 24]

[187] D.J. Tyler and D.M. Durand. Functionally selective peripheral nerve stimulation with a flat interface nerve electrode. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 10(4):294–303, 2002. [cited at p. 18]

[188] A. Uranga, X. Navarro, and N. Barniol. Integrated cmos amplifier for eng signal recording. *IEEE Transactions on Biomedical Engineering*, 51(12):2188–2194, 2004. [cited at p. 33, 34, 35, 38]

[189] S. Venkatraman, K. Elkabany, J.D. Long, Yimin Yao, and J.M. Carmena. A system for neural recording and closed-loop intracortical microstimulation in awake rodents. *IEEE Transactions on Biomedical Engineering*, 56(1):15–22, 2009. [cited at p. 32]

[190] C. Veraart, W.M. Grill, and J.T. Mortimer. [cited at p. 123]

[191] P. Verma and N. A. Melosh. Gigaohm resistance membrane seals with stealth probe electrodes. *Applied Physics Letters*, 97(3), 2010. [cited at p. 39]

[192] D.A. Wagenaar, J. Pine, and S. M. Potter. Effective parameters for stimulation of dissociated cultures using multi-electrode arrays. *Journal of Neuroscience Methods*, 138(1-2):27–37, 2004. [cited at p. 25]

[193] L. Wallman, Y. Zhang, T. Laurell, and N. Danielsen. The geometric design of micromachined silicon sieve electrodes influences functional nerve regeneration. *Biomaterials*, 22:1187–1193, 2001. [cited at p. 21]

[194] Y. Wang, Zhigong Wang, Xiaoying LuĬĹ, and Huiling Wang. Fully integrated and low power cmos amplifier for neural signal recording. In *27th Annual International Conference of the Engineering in Medicine and Biology Society, 2005. IEEE-EMBS 2005*, pages 5250–5253, 2005. [cited at p. 32, 33, 34]

[195] K. Warwick, M. Gasson, and B. et al Hutt. The application of implant technology for cybernetic systems. *Archives of Neurology*, 60(10):1369–1373, 2003. [cited at p. 20]

[196] E. Waterhouse. New horizons in ambulatory electroencephalography. *Engineering in Medicine and Biology Magazine*, 22:74–80, May-June 2003. [cited at p. 156]

[197] P.T. Watkins, R.J. Kier, R.O. Lovejoy, D.J. Black, and R.R. Harrison. Signal amplification, detection and transmission in a wireless 100-electrode neural recording system. In *Proceedings of 2006 IEEE International Symposium on Circuits and Systems, 2006. ISCAS 2006*, pages 2192–2196, 2006. [cited at p. 36, 38]

[198] W. Wattanapanitch, M. Fee, and R. Sarpeshkar. An energy-efficient micropower neural recording amplifier. *IEEE Transactions on Biomedical Circuits and Systems*, 1(2):136–147, 2007. [cited at p. 24, 33, 34, 37, 79]

[199] W. Wattanapanitch and R. Sarpeshkar. A low-power 32-channel digitally programmable neural recording integrated circuit. *IEEE Transactions on Biomedical Circuits and Systems*, 5(6):592–602, 2011. [cited at p. 32]

[200] P. Weerakoon, K. Klemic, F.J. Sigworth, and E. Culurciello. An integrated patch-clamp amplifier for high-density whole-cell recordings. In *IEEE International Symposium on Circuits and Systems, 2007. ISCAS 2007*, pages 1205–1208, 2007. [cited at p. 39]

[201] I. Williams and T.G. Constandinou. An energy-efficient, dynamic voltage scaling neural stimulator for a proprioceptive prosthesis. *IEEE Transactions on Biomedical Circuits and Systems*, 7(2):129–139, 2013. [cited at p. 82, 93]

[202] K.D. Wise and K. Najafi. Fully-implantable auditory prostheses: restoring hearing to the profoundly deaf. In *International Electron Devices Meeting, 2002. IEDM 2002*, pages 499–502, 2002. [cited at p. 128]

[203] D.S. Won, I. Obeid, J.C. Morizio, M.A.L. Nicolelis, and P.D. Wolf. A multichannel cmos analog front end ic for neural recordings. In *Proceedings of the Second Joint Engineering in Medicine and Biology, 2002. 24th Annual Conference and the Annual Fall Meeting of the Biomedical Engineering Society EMBS/BMES Conference, 2002*, volume 3, pages 2070–2071, 2002. [cited at p. 35, 38]

[204] J. Wu, W.-F. Feng, and W.C. Tang. A multi-channel low-power circuit for implantable auditory neural recording microsystems. In *Proceedings of the 12th International Conference of Biomedical Engineering*, 2005. [cited at p. 20, 32, 36, 37]

[205] J.-T. Wu and K.L. Chang. Mos charge pumps for low-voltage operation. *IEEE Journal of Solid-State Circuits*, 33(4):592–597, 1998. [cited at p. viii, 83]

[206] Q. Xu, D. Hu, B. Duan, and J. He. A fully implantable stimulator with wireless power and data transmission for experimental investigation of epidural spinal cord stimulation. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, PP(99):1–1, 2015. [cited at p. 82, 87, 93]

[207] T. Yamazoe, H. Ishida, and Y. Nihongi. A charge pump that generates positive and negative high voltages with low power-supply voltage and low power consumption for non-volatile memories. In *Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on*, pages 988–991, 2009. [cited at p. 84, 102]

[208] L. Yao, J. Zhao, P. Li, R.-F. Xue, Y.P. Xu, and M. Je. A 20v-compliance implantable neural stimulator ic with closed-loop power control, active charge balancing, and electrode impedance check. In *Solid-State Circuits Conference (A-SSCC), 2014 IEEE Asian*, pages 201–204, 2014. [cited at p. 25]

[209] R. Yazicioglu, C. van Hoof, and R. Puers. *Biopotential readout circuits for portable acquisition systems*. 2008. [cited at p. 24]

[210] Paul B. Yoo and D.M. Durand. Selective recording of the canine hypoglossal nerve using a multicontact flat interface nerve electrode. *IEEE Transactions on Biomedical Engineering*, 52(8):1461–1469, 2005. [cited at p. 18]

[211] K. Yoshida, K. Jovanovic, and R.B. Stein. Intrafascicular electrodes for stimulations and recording from mudpuppy spinal roots. *Journal of Neuroscience Methods*, 96(1):47–55, 2000. [cited at p. 19, 25]

[212] K. Yoshida, M. Kurstjens, L. Citi, K.P. Koch, and S. Micera. Recording experience with the thin-film longitudinal intra-fascicular electrode, a multichannel peripheral nerve interface. In *IEEE 10th International Conference on Rehabilitation Robotics, 2007. ICORR 2007*, pages 862–867, 2007. [cited at p. 19]

[213] K. Yoshida, D. Pellinen, D. Pivin, P. Rousche, and D. Kipke. Development of the thin-film longitudinal intra-fascicular electrode. page 089, 2000. [cited at p. 25]

[214] K. Yoshida and R.B. Stein. Characterization of signals and noise rejection with bipolar longitudinal intrafascicular electrodes. *IEEE Transactions on Biomedical Engineering*, 46(2):226–234, 1999. [cited at p. 23]

[215] A. Zabihian and A.M. Sodagar. A new architecture for multi-channel neural recording microsystems based on delta-sigma modulation. In *Biomedical Circuits and Systems Conference, 2009. BioCAS 2009. IEEE*, pages 81–84, 2009. [cited at p. 36]

[216] Y. Zhao, S. Inayat, D.A. Dikin, J.H. Singer, R.S. Ruoff, and J.B. Troy. Patch clamp technique: Review of the current state of the art and potential contributions from nanoengineering. *Proceedings of the Institution of Mechanical Engineers, Part N: Journal of Nanoengineering and Nanosystems*, 222(1):1–11, 2008. [cited at p. 39]

[217] C.M. Zierhofer, I.J. Hochmair-Desoyer, and Erwin S. Hochmair. Electronic design of a cochlear implant for multichannel high-rate pulsatile stimulation strategies. *Rehabilitation Engineering, IEEE Transactions on*, 3(1):112–116, 1995. [cited at p. 91, 92]

[218] X. Zou, Lei Liu, Jia Hao Cheong, Lei Yao, Peng Li, Ming-Yuan Cheng, Wang Ling Goh, R. Rajkumar, G.S. Dawe, Kuang-Wei Cheng, and Minkyu Je. A 100-channel $1-mW$ implantable neural recording IC. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 60(10):2584–2596, 2013. [cited at p. 32, 33, 34, 37]

List of Publications Related to the Thesis

Published papers

Journal papers

- L. Bisoni, C. Carboni, L. Raffo, N. Carta, M. Barbaro, *A HV-CMOS integrated circuit for neural stimulation in prosthetic applications*, IEEE Transactions on Circuits and Systems–II: Express Briefs, vol. 62, no. 2, pp. 1-5, 2015

Conference papers

- L. Bisoni, E. Mastinu, M. Barbaro, *A wide-band and user-friendly EEG recording system for wearable applications*, to appear in *Proc. of the 8th International Conference on Biomedical Electronics and Devices (BIODEVICES 2015)*, pp. 29-36, 2015

- C. Carboni , L. Bisoni, N. Carta, M. Barbaro, *Compact, multi-channel, electronic interface for PNS recording and stimulation*, to appear in *Proc. of the 11th Iasted International Conference on Biomedical Engineering (BioMed 2014)*, pp. 65-71, 2014