Ultraflexible all-organic complementary transistors and inverters based on printed polymers

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Organic electronics has been steadily evolving, with improving performances, including unrivaled mechanical properties. One of the main technological trends aims at thinner and lighter form factors, toward the realization of ultraflexible and conformable large-area electronic devices, capable of withstanding harsh mechanical stresses and therefore finding applications where rigid or brittle technologies would fail. Pursuing this objective, a critical role is known to be played by the substrate, whose thickness needs to be reduced as much as possible while maintaining processability. Ultrathin substrates, and the neutral plane strategy have therefore been exploited to realize ultrathin organic devices, while ultraflexible complementary circuits based on printed organic semiconductors, realized by means of high-throughput and large-area techniques, have not been achieved so far. In this work, all-polymer organic field effect transistors and complementary inverters have been printed onto a micrometer-thin parylene substrate, subsequently also used as a top isolation in order to place the active components in the neutral plane of stresses. These devices show proper low voltage operation, with supply voltages as low as 2 V, and retain stable and uniform performances upon the application of harsh mechanical stresses, such as rolling and crumpling. These results represent the first demonstration of semi-transparent and fully organic crumpable printed electronics, and pave the way toward the realization of more complex complementary logic circuits, laying the foundation for their widespread and cost-effective integration into consumer products.

Introduction

Electronics is continuously evolving, advancing from its heavy and bulky beginnings towards extreme downscaling and, in an alternative applications scenario, towards the realization of large-area flexible and stretchable devices. In the latter case, organic electronics is one of the main players, able to overcome some of the limitations of other candidates for large-area technologies, such as the lack of flexibility and optical semitransparency. Indeed, organic semiconductors present some unique features such as biocompatibility, lightweight, flexibility, low environmental impact, and easy tailoring of the materials properties. Moreover, they allow a high-throughput, large-area, cost-effective solution-based manufacturing of ultrathin and transparent semiconducting films, compatible with low-cost plastic substrates, which is crucial when aiming at mass production and diffusion in the consumer market.[1-4]

Flexible and mechanically robust opto-electronic components are the building blocks and enablers of applications such as rollable displays (and their backplanes), flexible imagers and other applications with unconventional form factors. A lot of research has been done in such direction,[5] however, most of the works reported in literature have been carried out employing bending radii of few millimetres. While this is often acceptable, there is a wide variety of applications for which very small bending radii are needed. At these extreme conditions, strain-induced damage of the active parts comes into play, [6] especially for electronic devices that need to be rolled, twisted, wrinkled, bent with sharp edges or repeatedly crumpled.[7] These applications include conformable large-area sensors and electronic skin, where the devices are intimately laminated onto the skin. The latter can be used for health monitoring, medical treatments or implants, restoring functions and biological studies,[8-12] but also information technology-related elements such as human-machine interfaces, soft robotics and augmented reality.[13, 14] These devices thus need to be placed in direct contact with curved and moving systems such as the skin or the external surface of soft robots, and should not hinder their mobility or cause discomfort of any kind.[6, 15-17] For this reason, they should not only be flexible, but also grant conformability in three dimensions. Therefore, the flexibility, lightness and conformability of these opto-electronic devices need to be increased even further, entering the field of epidermal or imperceptible electronics. When a system is bent with a bending radius equal to R_B, the applied strain is equal to [18]

$$\epsilon = h_S/R_B \quad (1)$$

where h_s is the thickness of the device, whose main contribution comes from the substrate. A thinner substrate allows sustaining smaller bending radii, and thus leads to a reduced stiffness and an increased flexibility of the device. Imperceptible, ultrathin and lightweight solar cells,[19, 20] Organic Light Emitting Diodes (OLEDs),[21-23] displays,[24, 25] sensors,[ADD REFS 26,27, 28] and memories [26] have been realized. For what concerns microelectronic circuits, ultraflexible [6, 15, 17, 20, 23, 27-31] or substrate-free devices[32-37] have been demonstrated. Nevertheless, these works rely on fabrication techniques involving opaque metallic electrodes, either gold or silver. Additionally, with some exceptions related to silver-based inkjet printed devices,[17] most of these works require lithographic and/or vacuum-based processes, which show limited compatibility with some organic substrates. In particular, this fabrication approach lacks of transparency, which is a crucial property to facilitate the integration on the target surface, while the employment of an all polymer configuration allows to easily reach this goal.

In this work, we present fully polymeric organic field-effect transistors (OFETs) and complementary inverters printed onto a 2 μm thick parylene substrate and subsequently encapsulated with a second parylene layer of identical thickness to locate the printed active layers into the neutral plane of mechanical stresses. These devices are able to operate at voltages as low as 2 V, and their performances are comparable with those of transistors and circuits realized on common, much thicker plastic foils, demonstrating the compatibility of the adopted process with microns thick substrates. Thanks to the reduced thickness of the overall structure, excellent robustness to harsh mechanical stresses such as rolling and crumpling has been obtained, with only limited loss in performances. In this way, ultraflexible, printed, semi-transparent and all-polymer complementary OFETs and inverters operating at low voltage have been demonstrated, a first step toward the implementation of high-throughput manufacturing of imperceptible electronic circuitry for its widespread and ubiquitous integration.

Experimental

Materials. The PEDOT:PSS Clevios PJ700 formulation was purchased from Heraeus. A silver nanoparticles based ink, Silverjet DGP-40LT-15C, was purchased from Advanced Nano Products (ANP). Ethylene glycol, polyethyleneimine (branched, average $M_W \approx 10000$), polymethylmetacrylate ($M_W \approx 120000$), and polystyrene were purchased from Sigma Aldrich. For what concerns the semiconductors, P(NDI2OD-T2), also known as ActivInk N2200, was purchased from Flexterra Corporation, while DPPT-TT ($M_W \approx 50000$-100000, PS Standard Polydispersity (PDI) = 2.5) was purchased form 1-Material. Parylene-C dimer was purchased from Specialty Coating Systems (SCS).

Device fabrication and characterization. The parylene substrates have been realized by depositing a 2 μm thick layer of parylene onto microscope glass slides with a SCS Labcoater 2 – PDS2010 system. The parylene substrates have been used as deposited, and a bottom-contact/top-gate (BCTG) architecture has been employed for the

realization of printed OFETs. PEDOT:PSS source and drain electrodes have been inkjet printed, using a Fujifilm Dimatix DMP2831, realizing channels with width of ~ 1000 µm and lengths of ~ 65 µm. Silver inkjet printed pads have been realized on the electrodes where electrical connections are created during the characterization. These pads are not necessary for the operation of the transistors and circuits, but they are necessary to simplify the electrical characterization. For the n-type transistors, a PEI based injection layer has been inkjet printed on top of the electrodes to decrease their workfunction.[38] Next, semiconductor areas have been inkjet printed: P(NDI2OD-T2) has been dissolved in mesitylene, with a concentration of 7 mg/ml, while DPPT-TT has been dissolved in 1,2-dichlorobenzene with a concentration of 2.5 mg/ml and blended in a 1:1 volume ratio with a polystyrene solution at the same concentration and solvent. P(NDI2OD-T2) has been printed first to realize n-type OFETs, and annealed for 1 hour at 120 °C in nitrogen atmosphere, while DPPT-TT has been printed to realize the p-type OFETs right after the annealing of the n-type semiconductor and then underwent a thermal treatment, in nitrogen atmosphere, at 110 °C for 10 minutes. Both layers thickness is in the range of tens of nm. After the deposition and thermal annealing of the semiconductors, the dielectric stack has been realized. First, an ultrathin PMMA layer, around 20 nm thick, has been deposited by spin coating from an n-butyl acetate solution with a concentration of 10 mg/ml. Then, a parylene film with a thickness of around 160 nm (C_{diel} = 15nF cm^{-2}) has been deposited with the same technique and instrument used for the deposition of the substrate. PEDOT:PSS gate electrodes have been realized via inkjet printing. The encapsulation layer has been realized with another parylene film, about 2 µm thick, deposited with the same method presented above right after printing the gate electrodes. Holes have been laser drilled in correspondence of the contacts and subsequently filled with inkjet printed PEDOT:PSS to facilitate the electrical measurements. The encapsulated devices have been detached from the carrier in order to assess their mechanical stability. First, with the help of a scalpel, the edges of the printed pattern have been cut, defining the final shape of the ultraflexible system, and then, with the help of tweezers, the system has been detached, creating a self-standing device. The characterization of both the as-fabricated and the self-standing devices has been performed in nitrogen atmosphere using an Agilent B1500A Semiconductor Parameter Analyser. The reported thickness values have been obtained using a KLA-Tencor Alpha Step IQ stylus profilometer.

Results and discussion

When bending a flexible film, one of the surfaces is in tension while the other one is in compression, and there exists a surface inside the bent layer where no strain is applied; this surface is known as neutral-strain or neutral-plane position.[39] In order to increase the stability of ultraflexible devices integrated into such film, a well-known strategy is to place the active layer in the neutral-plane position, thus reducing the applied strain and increasing the durability. This can be

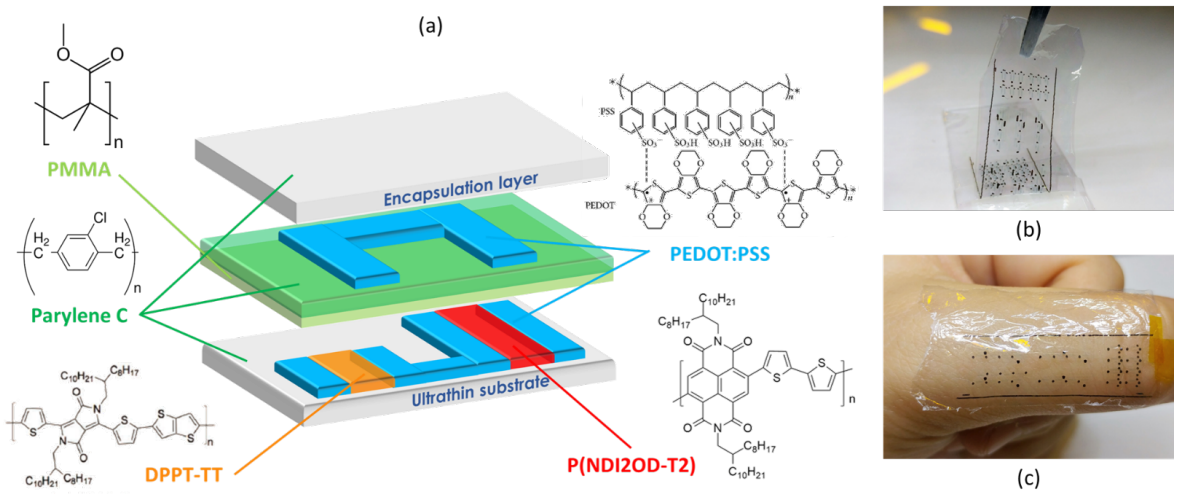

Figure 1 (a) Schematic representation of the structure of the printed inverter and chemical formula of the polymers employed. Photographs of the final device during the detachment (b) and applied on skin (c).

achieved upon coating the circuits with an encapsulation layer having same thickness and Young modulus as the substrate where they are patterned on, in agreement with

$$Y_S d_S = Y_E d_E \quad (2)$$

where *Y* is the Young modulus, *d* is the thickness, and the subscripts *S* and *E* refer to the substrate and the encapsulation layer, respectively. As previously proposed by Sekitani et al.,[31] here we adopted the same material, parylene, for both the substrate and encapsulation, with two layers with identical thicknesses, 2 µm. The first ultra-thin parylene layer, serving as substrate, has been deposited onto a glass carrier to facilitate the handling of the sample during fabrication. After the fabrication of the OFETs and inverters, the second parylene layer has been deposited on top, playing a dual role: besides allowing to place the active layer in the neutral plane of the stresses, it acts as a protective layer, creating a barrier between the devices and the environment.[40, 41].

Poly(3,4-ethylenedioxithiophene):polystyrene sulphonate (PEDOT:PSS) has been selected as the conducting material for source and drain electrodes, because of its printability, high optical transparency and low temperature processing.[42] Before fabricating complete electronic devices, PEDOT:PSS lines with different lengths and widths have been inkjet printed on the 2 µm thick parylene substrate, in order to optimize the printability and investigate the lines resistance. The latter has been extracted from the slope of the current-voltage characteristics (*I-V*), reported in **Errore. L'origine riferimento non è stata trovata.**.

The resistance can be expressed with the standard formula $R = \rho L/A$, from which the resistivity value is calculated as $\rho = RA/L$. The lines have a thickness of 40 nm, and the average resistivity amounts to (3.41 ± 0.45)*10^5 Ωm, hence no major differences are found when a thin parylene substrate is used instead of more common plastic foils, such as PEN: in the latter case we measure $\rho =$2.95*10^5 Ωm.

A bottom-contact/top-gate (BCTG) architecture has been used for the realization of printed OFETs and additive processes only have been employed, granting in principle an easier scaling-up of the fabrication flow. First, PEDOT:PSS source and drain electrodes and contact pads have been inkjet printed onto the parylene substrate, defining channels with average length (*L*) and width (*W*) equal to ~ 65 and ~ 1000 µm respectively. In order to improve the charge injection for the n-type devices, a polyethylenimine (PEI)-based injection layer has been printed on top of the electrodes, enhancing the injection of electrons thanks to a reduced electrode work function.[38] Then, the semiconducting areas have been patterned on top of the source and drain electrodes via inkjet printing. Poly([N,N'-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bitthiophene)) (P(NDI2OD-T2)) has been chosen as semiconductor for the n-type devices, while 3,6-diketopyrrolopyrrole-alt-5,5-(2,5-di(thien-2-yl)thieno [3,2-b]thiophene) (DPPT-TT), blended with polystyrene (PS), is the semiconductor of choice for the p-type ones. The use of multicomponent systems is an approach that has been developed in order to expand the functionalities and features of organic electronics. In particular, blending semiconducting polymers with insulating counterparts improves their mechanical characteristics, making them more stable and flexible, and it widens the reachable range of viscosities, thus expanding the count of fabrication techniques that can be employed. Moreover, an improved environmental stability with respect to the neat semiconductor, thanks to a partial self-encapsulation has been reported.[43] The DPPT-TT semiconductor employed in this work presents a high viscosity, which limits its printability and reduces the quality of the printed areas. DPPT-TT has thus been blended with PS in a weight ratio of 1:1 to tune its viscosity in solution and facilitate inkjet-printing, with an improved ease of droplet jetting.

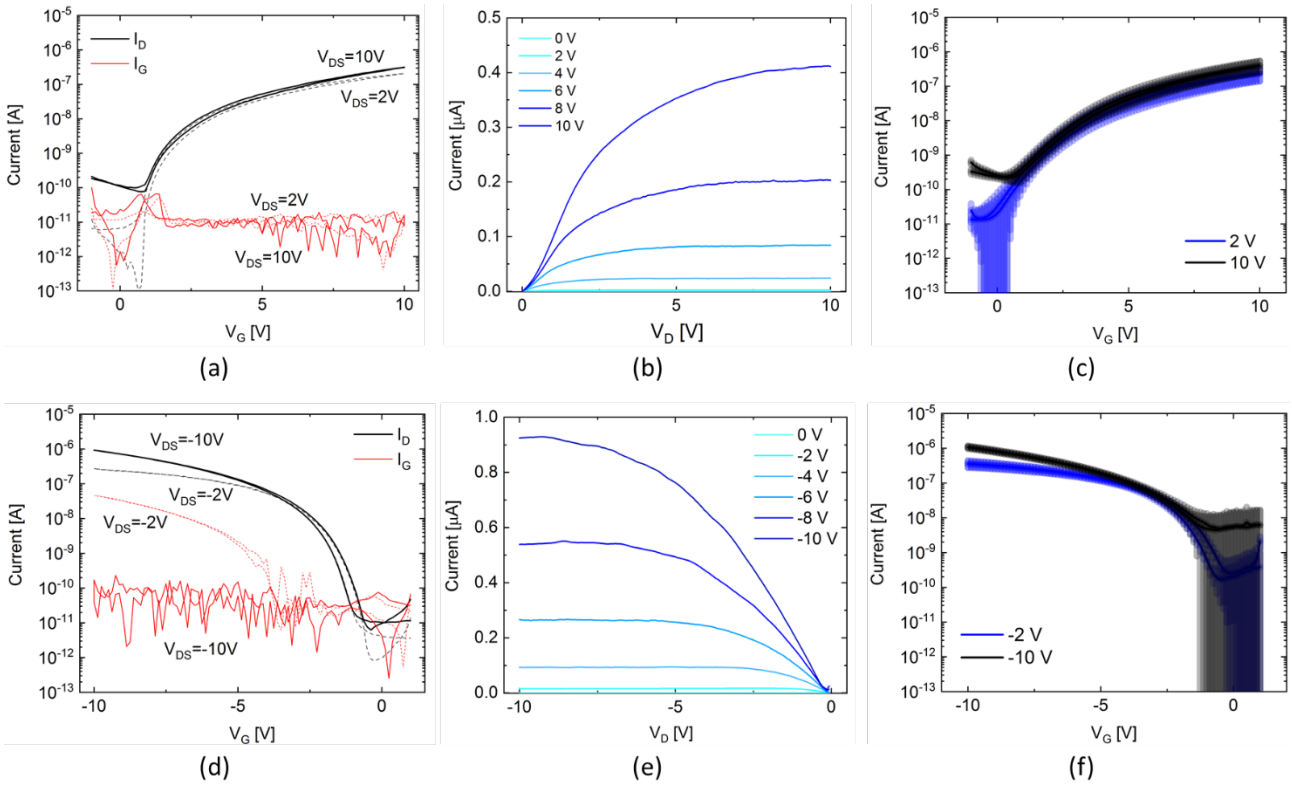

Figure 2 Electrical characterization of complementary printed OFETs on a parylene substrate. Transfer characteristics for (a) n-type and (d) p-type devices, output curves for (b) n-type and (e) p-type transistors, and average transfer characteristics, measured over 10 devices, with their standard deviation, for (c) n-type and (f) p-type OFETs.

Aiming at low-voltage operation, a double layer, composed of an ultrathin spin-coated PMMA film, 20 nm thick, and a parylene-C film, with a thickness of around 160 nm, has been employed.[42] Parylene, commercial name of poly(chloro-p-

xylylene), is a low-k, semicrystalline and thermoplastic polymer. Its solution-free, chemical vapour deposition technique allows to grow flexible, chemically inert, conformal, and, most importantly, pinhole-free films, thus allowing to strongly reduce the thickness of the dielectric layer, and increasing its capacitance, without creating short circuits. The ultrathin PMMA film at the interface is needed in order to avoid direct contact between parylene-C, and specifically its chlorine atoms, and the n-type semiconductor. In fact, it has been reported that during parylene-C deposition, Cl non-bonding electrons can reduce the strong electron withdrawing property in the imide unit of P(NDI2OD-T2), leading to a worsening of FET performances.[44] A comparison between devices made with and without the PMMA interlayer is reported in Figure S2 in the Supporting Information (SI). By introducing the interlayer, the excellent dielectric properties of parylene and the optimal electrical interface of PMMA with a variety of semiconductors are combined,[45] granting optimal operation for devices of both polarities.[42] PEDOT:PSS has been inkjet printed on top of the dielectric layer to realize gate electrodes.
In Figure 1 photographs of typical final samples, with single transistors and inverters are shown, both during the detachment from the carrier and after application on the skin.
The electrical characterization of two sets of 10 n- and p-type printed OFETs, while still attached on the glass carrier, is reported in Figure 2.

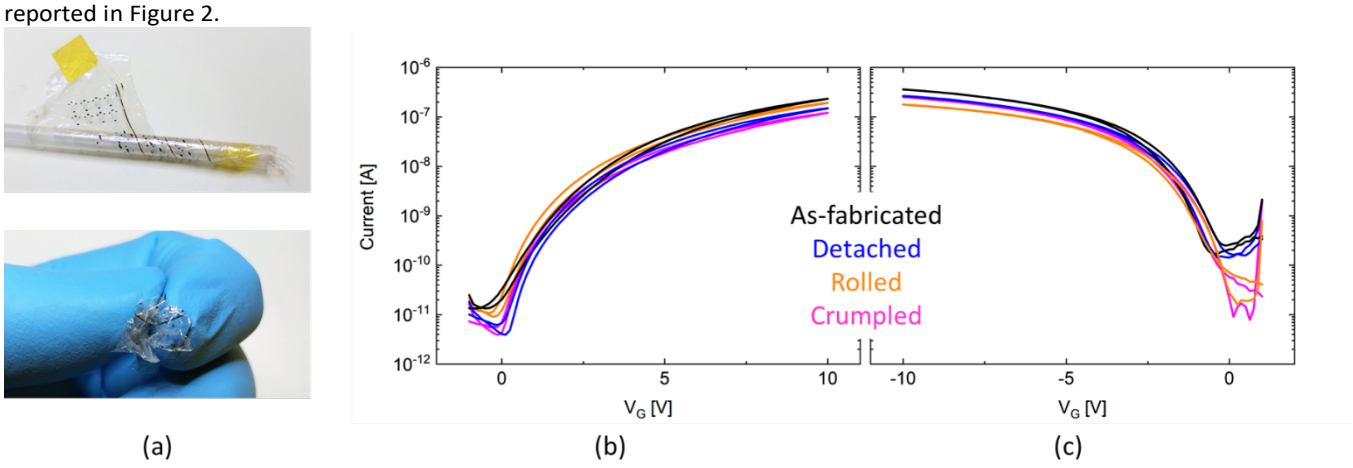

Figure 3 (a) Photographs of the samples undergoing mechanical tests, rolling (top) and crumpling (bottom). Average transfer characteristics after each mechanical test, in linear (±2V) regime for (b) n-type and (c) p-type OFETs. The black curve refers to the as-fabricated devices, the blue curve for the detachment case, orange curve for rolling and pink for crumpling.

Both p-type and n-type OFETs operate at low voltage, as it can be seen from their characteristic curves, with clear field-effect modulation at 2 V. P-type devices show almost ideal output and transfer curves, while n-type OFETs have more obvious small non-idealities related to the injection of electrons from the contacts, evidenced by the slight S-shape of the output curve. Nevertheless, transistors of both polarities are successfully operating with high reproducibility, as it can be seen from the average transfer characteristics, shown in Figure 2c,f. The average maximum drain currents extracted in saturation at ±10 V, are 0.46 ± 0.18 µA for the n-type OFETs and 1.07 ± 0.09 µA for the p-type ones. The average mobilities have also been extracted, according to the gradual channel approximation.[46] The linear and saturation mobility for the p-type printed transistors are equal to 0.09 and 0.11 $cm^2 V^{-1} s^{-1}$ respectively, while n-type devices show an average linear mobility equal to 0.10 $cm^2 V^{-1} s^{-1}$ and a saturation mobility of 0.09 $cm^2 V^{-1} s^{-1}$ (Figure S3). Devices of both polarities have a small hysteresis; p-type OFETs shift toward more positive voltages, while n-type ones have a slight shift toward negative voltages. This effect can be ascribed to the filling, during the forward sweep, of shallow traps at the interface between the dielectric and the semiconducting layer, which remain filled during the backward scan. Overall, the performances of these devices are in line with the ones of analogous printed transistors on standard organic electronics substrates, such as PEN. In particular, the DPPT-TT mobility here reported is just a factor of 2 lower with respect to literature for similar fabrication techniques,[47] while in the case of the P(NDI2OD-T2) FETs, the mobilities are very close to the typical values reported for similar devices printed on PEN.[42]
Having established that the printed OFETs show good electronic properties as fabricated on the carrier, they have then been detached from it and have undergone tests of robustness to strong mechanical stress, which consisted of rolling and crumpling. In the former case, the sample has been rolled around a thin plastic cylinder, with a diameter of about 1 mm, while in the latter the sample has been manually crumpled, as presented in **Errore. L'origine riferimento non è stata trovata.**. In both cases, the transistors characteristics have been measured in flat configuration, both before and after mechanical stress.

During the mechanical characterization, ten devices for each polarity have been characterized at every step, and the average transfer curves with their standard deviations are shown in Figure S4. A comparison of the average transfer curves only for the printed ultraflexible OFETs during all the characterization steps are shown in **Errore. L'origine riferimento non è stata trovata.** and Figure S5, for devices of both polarities, in linear and saturation regimes. The main extracted transistor parameters are reported in **Errore. L'origine riferimento non è stata trovata.**, while a graphical comparison of the mobility values is presented in Figure S6.

100 % of the devices were correctly operating after undergoing the mechanical stresses, demonstrating the robustness of the printed OFETs. All maximum drain currents recorded belong to the same order of magnitude, with a reduction of a factor 2 in the worst cases. The standard deviation of the average transfer curves remains small, as it can be seen in Figure S4 and from the values in **Errore. L'origine riferimento non è stata trovata.**. Similar trends are reported for the mobility values of both types of devices, in linear and saturation regimes, while for the subthreshold swing and the on-off ratio no significant variations are detectable. We note that most of the change in device characteristics occurs with the detachment, which subjects the device to the first mechanical stress.

Table 1 Average parameters for n- and p-type OFETs evaluated for the as-fabricated devices and after each mechanical characterization step.

n-type OFETs	Encapsulated	Detached	Rolled	Crumpled
Linear mobility [$cm^2\ V^{-1}\ s^{-1}$]	0.10	0.06	0.08	0.05
Saturation mobility [$cm^2\ V^{-1}\ s^{-1}$]	0.09	0.05	0.07	0.03
Maximum drain current [µA]	0.46 ± 0.18	0.26 ± 0.11	0.55 ± 0.37	0.19 ± 0.05
Subthreshold swing [mV dec^{-1}]	732 ± 186	658 ± 89	813 ± 266	535 ± 59
Turn-on voltage [V]	0.12	0.28	0.07	0.08
On-off ratio	9×10^4	8×10^4	1×10^5	6×10^4

p-type OFETs	Encapsulated	Detached	Rolled	Crumpled
Linear mobility [$cm^2\ V^{-1}\ s^{-1}$]	0.09	0.06	0.04	0.06
Saturation mobility [$cm^2\ V^{-1}\ s^{-1}$]	0.11	0.08	0.05	0.07
Maximum drain current [µA]	1.07 ± 0.09	0.80 ± 0.26	0.52 ± 0.19	0.67 ± 0.21
Subthreshold swing [mV dec^{-1}]	439 ± 213	360 ± 246	269 ± 76	166 ± 26
Turn-on voltage [V]	-0.35	-0.34	-0.32	-0.15
On-off ratio	2×10^6	6×10^5	2×10^5	4×10^5

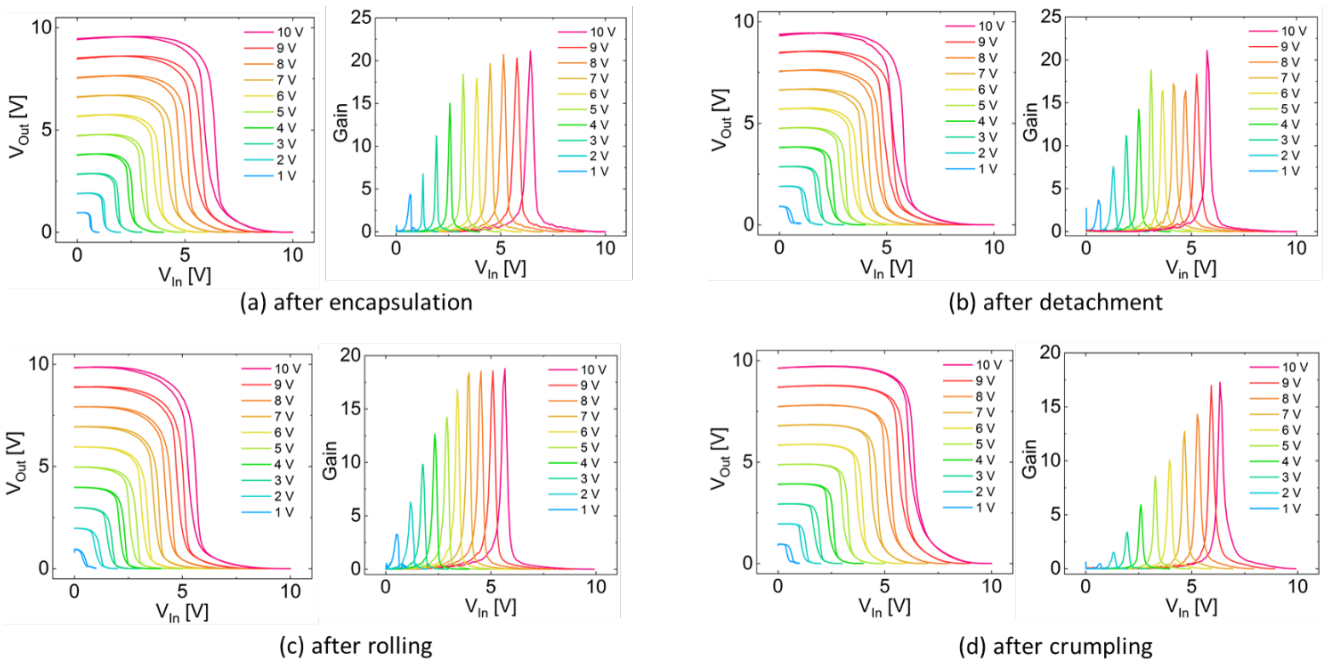

Figure 4 Voltage transfer characteristic and gain curves for the printed complementary inverters, after encapsulation (a), after detachment (b), after rolling (c) and after crumpling (d).

The small reduction in mobility and drain current can be explained considering the pivotal role of the semiconductor-dielectric interface for the proper operation of the OFETs. When a strain is applied to a device, it leads to surface rearrangements, with modifications of the polymer structure and changes in the surface heterogeneity and energy, which in turn alter the interface between the two above-mentioned layers, and thus modify the transistor behaviour. Polymer dielectrics that allow for a larger degree of reorganization lead to lower heterogeneities when strains are applied, and thus more robust mechanical performances. For what concerns the dielectric constant, low-k dielectrics show generally better response to mechanical stress compared to high-k ones, since they have less dipoles at the interface and subsequently less surface rearrangements that might disrupt the semiconductor operation. Additionally, the application of a stress to interfaces between materials with different Young moduli might lead to surface modification. In our devices we have adopted low-k dielectrics, so the surface dipoles rearrangements are minimized and their contribution to the performances loss is minimum. All the materials used for the devices presented here are flexible, but they present quite different Young moduli, ranging from tens MPa to GPa. We therefore propose that this mismatch, both between the electrodes and the semiconductor and between the semiconductor and dielectric, is the leading cause for the slight loss in performances reported above.

Overall, we have demonstrated that the printed OFETs can survive the mechanical tests, while seeing their characteristics non severely modified. P-type devices after stress are still more performing than n-type ones, maintaining the difference in the maximum drain currents highlighted before the mechanical stresses.

One of the features of our devices is the transparency. The transmittance of an array of OFETs has been evaluated using UV-vis spectroscopy in the visible region, and the average transparency is higher than 90%. In Figure S7 the UV-vis spectrum and the measurement spot are shown.

The p- and n-type transistors presented have been fabricated with the same fabrication techniques, on the same substrate, and employing identical electrodes and dielectric materials. This largely simplifies the integration of these devices into complementary logic circuits. To exemplify the fabrication of circuits and test also their mechanical robustness, we opted for one of the simplest logic gates, the logic inverter.[48] The complementary organic inverter is composed of one p-type and one n-type transistor, with shared drain electrode and a common gate, acting as input and output nodes, and it is fabricated with the same techniques presented for the realization of the printed OFETs. The two transistors forming the complementary inverter have been designed with identical channel lengths, $L_P = L_N \approx 65$ µm, while the channel width for p-type devices (W_P) is designed to be half of that of n-type OFETs (W_N), with $W_P = 500$ µm and $W_N = 1000$ µm, to better balance the OFETs currents.

The voltage transfer curves (VTC) of the inverters have been measured and the gain values have been extracted as the first derivative of the VTC with respect to the applied voltage. The obtained results, measured before the detachment from the glass slide, are shown in Figure 4a and a proper inverting behaviour for the printed inverters is reported for voltages as low as 1 V, highlighting the low-voltage operation granted by the employed dielectric layer. The average gain value is around 15, with the maximum gain equal to 21 recorded for a supply voltage V_{DD} of 10 V, while the noise margins,

calculated with the maximum equal criteria, lay in the range between 45% and 55% of $V_{DD}/2$, and the average deviation of the inverting threshold from $V_{DD}/2$ is equal to 26%.
As it can be seen from Figure 4, the complementary inverters are properly working even after the application of harsh mechanical stresses, as expected given the reliability of the single transistors. In all the cases, the inverters show proper inverting behaviour, switch at a voltage that is close to the middle of the voltage interval applied, and present a small hysteresis, which can be related with that of the single transistors addressed above. For what concerns the inverting threshold, the detached devices have an average deviation from $V_{DD}/2$ that is equal to 22%, while for the rolled and crumpled ones is equal to 16% and 30% respectively.
Focusing on the gain, the detached devices show values close to those of the as-fabricated devices, with an average gain equal to 14.5, a maximum gain obtained for V_{DD} = 10 V and equal to 21, and gains higher than 10 obtained for supply voltages as low as 3 V. During both mechanical tests, a slight deterioration takes place, with average gain values equal to 11.7 and 9.1 respectively. The maximum gain value for rolled devices is equal to 19, reported for V_{DD} = 10 V, while for crumpled inverters is 17.5 at V_{DD} = 10 V. This slight loss in gain values can be related with a loss in output impedance of the OFETs, which are not as ideal as in the as-fabricated devices. The minimum voltage for which a gain equal or higher than 10 is obtained increases, up to 4 and 6 V for rolling and crumpling respectively. These voltage values, despite not being as ideal as in the as-fabricated devices, are still low enough to be compatible for example with powering supplied by thin film batteries or harvesters such as plastic solar cells.

Conclusions

We have demonstrated ultraflexible and all-polymer complementary OFETs and inverters, operating at low voltage, and able to withstand rolling and crumpling. These devices have been realized onto an ultrathin parylene film, and an equally thick parylene layer has been used as encapsulation. PEDOT:PSS has been used as electrode material, P(NDI2OD-T2) and DPPT-TT as semiconductors, and the dielectric bilayer is composed of PMMA and parylene. The fabrication of these devices has been performed by inkjet printing all materials requiring patterning, and by coating of a thin, bi-layer dielectric. Two mechanical tests have been performed, in order to assess the mechanical robustness of these devices, namely rolling and crumpling. The printed OFETs are demonstrated to be very robust to such harsh tests: all of tested devices survive both tests, maintaining uniformity of performances. The currents, and the corresponding mobility, show only a moderate reduction upon detachment of the samples from the rigid carrier adopted for fabrication, while mostly retaining their performances with the following tests. This is, at the best of the authors' knowledge, the first demonstration of ultraflexible, semi-transparent all-organic printed complementary OFETs and logic gates operating in the sub-10 V regime.
Our results demonstrate the compatibility of the proposed fabrication process, based on a combination of printing and large-area coatings, and device architectures for the development of mass-produced, cost-effective, lightweight, and ultraflexible organic devices aiming at imperceptible, wearable and epidermal electronics applications.

Conflicts of interest

There are no conflicts to declare.

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