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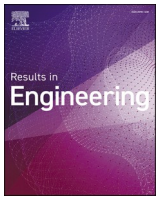

Research paper

Aggressively scaled T-Gated GaN-on-silicon RF power HEMT featuring step graded SRL-AlGaN buffer for next generation broad band power amplifiers

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ABSTRACT

GaN HEMT has gained much interest recently because of its widespread uses, which range from high voltage systems used in power electronic devices to RF power amplifiers. The industry is currently focusing on developing GaN HEMT on Silicon-substrate in order to lower costs and integrate GaN technology with Si-based components. In this work, the RF power performance of T-gate with novel step graded strain relief layered GaN—HEMT analyzed on Si (Silicon) wafer by Silvaco simulation TCAD tool. The effect of gate length (L_G), gate recess (G_R), work function, gate-to-source (L_{GS}) length scaling, and gate-to-drain (L_{GD}) length scaling was studied. The G_M (transconductance) observed maximum value in this work is 936.40 mS/mm, and the maximum drain current (I_D) reached 1.96 A/mm for HEMT with L_G= 40 nm. The cut-off frequency (f_T) observed with the minimum L_{GS} of 150 nm is 442.59 GHz. Decreasing the gate length resulted in higher transconductance, drain current, and cut-off frequency (f_T), with no alteration in the threshold voltage. In addition, the results of L_G scaling on G_M & other capacitance parameters have been analysed, which prefer a best way for boosting DC & RF performances of GaN—HEMTs. Reducing the L_{GS} and L_{GD} distances in this HEMT minimizes the channel length, allowing for faster carrier transport and increasing both the transconductance (GM) and drain current. This adjustment enhances current flow without altering the threshold voltage, as the gate control over the channel remains unaffected.

1. Introduction

GaN material shows promise for high-voltage, high-frequency, and high power-density applications attributable to 3.4 eV wide E_G (Energy bandgap), more critical electric field, and high velocity of saturation. Analysis of the DC, radiofrequency (RF) functionality of GaN—HEMTs and AG (AlGaN/GaN) heterojunctions has garnered a lot of attention as research has progressed. Currently, AG-HEMTs on silicon substrates have been profit-oriented approaches for high-efficiency conversion (power) systems with compact sizes [1–5]. Several techniques have been explored to enhance transistor functionality, including the implementation of gradient channel layers and the incorporation of field-plate structures. Trapping effects at the surface & inside GaN buffer frequently limit the performance of HEMTs. These consequences lead to drop of output current, breakdown voltage, and, eventually, the RF power output of the device [6–9]. However, by adding boron to GaN binary compounds, this degradation can be considerably reduced. Alloys based on boron nitride have intriguing physical characteristics that may be able to address these issues [10–13].

The strain relief layer (SRL) in Silicon based HEMTs consists of principal layers: a nucleation-layer (AlN), AlGaN transition layers, and a thick gallium-nitride layers above. These buffer layers are carefully designed so that the aluminum composition gradually decreases as the distance from the silicon wafer increases. The step-graded layer essentially shows a low Ga-concentration near the Si interface, and a high concentration in the thick gallium-nitride layer. Lowering the Ga-content in the AlGaN transition layers has been found to align the thermal expansion coefficient of the SRL structure more closely with that of silicon. The function of strain relief layers is vital in reducing the impact of strain and lattice mismatch on various levels of the device's construction [14–16]. On the contrary, elevating the Ga-percentage in the AlGaN layers aligns thermal expansion coefficient of the layer with

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that of the gallium-nitride layer. Here SRL, integrated into this silicon based structure, facilitates the production of gallium-nitride HEMTs with efficient strain relief in the active region, enhancing functionality and reliability [17–21].

To clearly articulate the novelty and emphasize specific contributions of this work are unique architecture, scaling optimization, cost effective, and fabrication feasibility, these points distinguish our design from the state-of-the-art devices. The proposed GaN HEMT incorporates step-graded strain relief layers (SRLs) on a silicon substrate. This design effectively reduces dislocation density while improving 2DEG confinement. Unlike existing approaches such as *Sc*-doped GaN or AlN-substrate HEMTs.This work, systematically investigates the effects of scaling L_{GS} and drain-to-gate (L_{GD}) lengths, as well as gate recess (G_R) and work function. With this structure achieving G_M of 963.4 mS/mm, which exceeds many state-of-the-art designs with comparable gate lengths. Demonstrating a f_T of 442.59 GHz, a competitive value in comparison to *Sc*-doped GaN and InAlN/GaN devices used for high-frequency applications. Unlike expensive sapphire or SiC substrates, the silicon platform in this work significantly reduces production costs while achieving high power density and frequency performance. This makes the design practical for commercial integration in RF and power electronic devices the T-gate HEMT structure with a recess of 2 nm ensures manufacturability using current lithographic techniques, addressing the scalability challenges often seen in ultra-thin AlN or *Sc*-doped designs.

A design mitigates short-channel effects and enhances performance metrics, making it suitable for high-RF power applications [22]. This study presents innovative designs for increasing the RF & DC analysis of GaN-based HEMTs through a dual-channel N-polar structure. The optimized NPDC—HEMT achieved a 45.91 % enhancement in current density and 126.3 % improvement in Ft, reaching 52.6 GHz in its T-gate variant. A gate-length of 90 nm, InAlN/GaN HEMTs on silicon, focusing on electrical and RF performance. Key achievements include a record-low DIBL of 43 mV/V, a peak intrinsic G_M of 553 mS/mm, and a current gain cutoff frequency of 175 GHz. The outcomes underscore the potential of this device for cost-effective, high-frequency microwave applications [23]. The GaN HEMT designs incorporating a recessed gate and novel dielectric configurations. Key findings include a high transconductance of over 500 mS/mm and low on-resistance values, enabling high efficiency and linearity for millimeter-wave applications. These innovations reduce trap effects and optimize RF performance, highlighting the design's potential for next-generation wireless technologies [24].

InAlN/GaN HEMTs are widely regarded for their high 2DEG density due to the strong polarization mismatch between InAlN and GaN. However, the recent advancements have addressed inherent issues with in segregation and barrier stability of the HEMT. A study comparing AlN and InAlN as sub-barriers showed that while InAlN improves carrier mobility, it suffers from reduced breakdown voltage and reliability due to in segregation. AlN-based HEMTs demonstrated superior breakdown voltage of 294 V, and output power density of 11.3 W/mm compared to InAlN (121 V and 8.69 W/mm) [25]. *Sc*-doped GaN has emerged as a best alternative due to its ferroelectric properties and ultra-wide bandgap: ScAlN/GaN HEMTs offer enhanced polarization-induced charge density, improving cut-off frequency and output power. For instance, a recent study reported fT values exceeding 400 GHz, positioning these devices for millimeter Wave applications like 5G and radar. Challenges include the complexity of doping processes and high production costs, making scalability a concern despite their superior performance [26]. Double-channel devices using GaN/AlN/GaN configurations improve linearity and output current density. These structures allow carrier distribution across two channels, widening gate voltage swing while maintaining good gate control. A recent comparison [27] demonstrated that double-channel devices outperformed single-channel HEMTs in terms of linearity and breakdown voltage, capable them for high-linearity RF applications.

In this work, a comprehensive investigation of strain relief layered HEMT is examined by Silvao TCAD simulation. The manuscript introduces a novel combination of step-graded strain relief layers (SRL) and T-gate design for GaN HEMT on a silicon substrate, with specific scaling optimizations for L_{GS}, L_{GD}, and L_G. These optimizations achieved remarkable RF/DC performance metrics, such as a G_M of 936.4 mS/mm and a cut-off frequency (f_T) of 442.59 GHz, without altering the threshold voltage. Unlike prior studies, this work systematically correlates the gate length and scaling dimensions to performance enhancement while maintaining device stability. The impact of gate length, gate-recess, gate work function (depends on gate metal), source-to-gate length scaling, and drain-to-gate length scaling on T-gate HEMT are comprehensively investigated. The DC/RF performance parameters G_M, drain current (I_D), cut-off frequency, output current, and capacitances of gate to source and drain to gate are improved and compared systematically.

2. Device structure

The T-gate GaN transistor structure with the SRL on a silicon substrate is illustrated in the 2-D Figure. The structure begins with a 250nm AlN nucleation layer to mitigate dislocations, succeeded by a series of three SRLs of AlGaN with thicknesses of 200nm, 500nm, and 400nm, respectively, with varying Al compositions as depicted in the 2-D Fig. 1. On top of these layers, a 1500 nm gallium-nitride buffer layer is positioned to enhance 2DEG confinement & reduce I_L (leakage currents). In this structure, the thickness of gallium-nitride channel layer is 200nm, succeeded by a 6nm $Al_{(0.1)}Ga_{(0.9)}N$ barrier layer. A 3nm passivation (SiN) layer is placed between source and drain to prevent current collapse. The L_{GS} is set at 300nm, while the L_{GS} is kept at 800nm. The T-gate, recessed at 2nm, has a width of 100nm as potrayed in Fig. 1(a&b). Studies suggest that the layered HEMT construction with strain relief can improve other electrical properties, such as 2DEG density. The development of GaN HEMT devices featuring strain relief layers fabricated using all-clean techniques is still in its nascent stages. Controlling material electrical contact and attaining lattice matching across several barrier layers present a unique challenge. To deal with these challenges, we, therefore, suggest a novel strain relief layered HEMT construction with adjustable device performance parameters.

The performance metrics by changing the source to gate & gate to drain distance are analysed in this work. Reducing L_{GS} and L_{GD} minimizes parasitic capacitances, enhancing carrier transport and transconductance without altering the threshold voltage. The step-graded SRL reduces dislocations and improves 2DEG density, contributing to higher drain current and cut-off frequency. Increasing the gate recess enhances gate control, leading to higher transconductance and threshold voltage.

The proposed HEMT structure is highly manufacturable due to its silicon substrate, which reduces costs and integrates seamlessly with CMOS processes. Key trade-offs are reliability, cost, power consumption, and scalability. The Step-graded SRLs reduce dislocation density, enhancing long-term performance. Silicon substrates are cheaper than sapphire or SiC, improving economic viability. Optimized scaling improves energy efficiency. The proposed parameters (e.g., $L_{GS} = 150$ nm, $L_G = 40$ nm) are achievable with state-of-the-art fabrication techniques, ensuring compatibility with mass production requirements

3. Results and discussion

This work objectives are, to analyze the RF and DC analysis of T-gate based HEMTs with a novel step-graded strain relief layer (SRL) on silicon substrates using Silvaco TCAD simulations. To explore the effect of gate scaling parameters, including gate length (L_G), gate recess (G_R), and source-to-gate (L_{GS}) and drain-to-gate (L_{GD}) lengths, on key metrics like transconductance (G_M), drain current (I_D), and cut-off frequency (f_T). To evaluate how gate metal work functions affect threshold voltage and overall performance. To propose practical design optimizations for

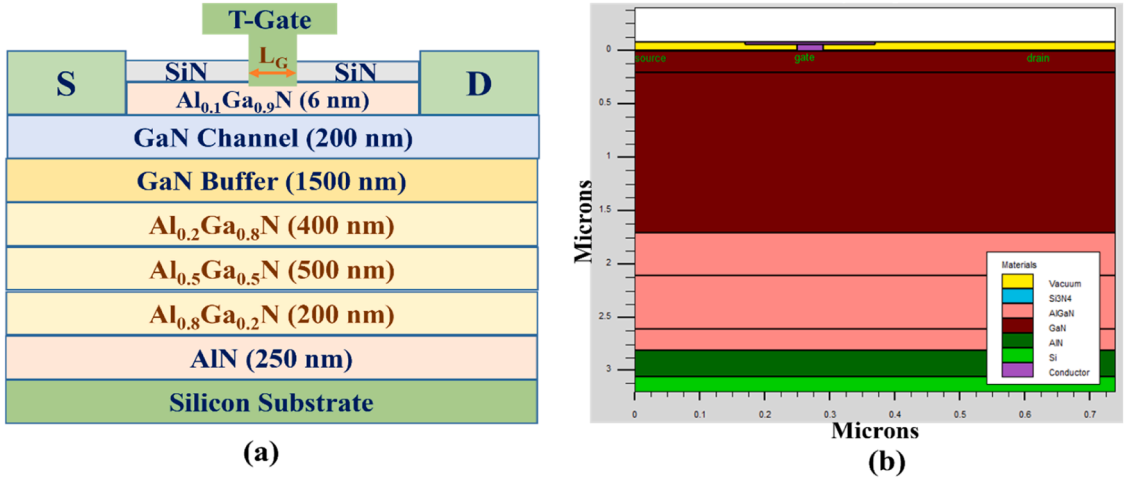

Fig. 1. Illustration of (a) Silicon based HEMT structure (2-D view), (b) HEMT structure from TCAD simulation.

better manufacturability, scalability, and device stability.

Field-dependent and constant mobility models for electrons and hole, are incorporated in the device simulation. For carrier generation & recombination, the shockley–Read–Hall recombination design is utilized. The drift-diffusion design transportation formulas are solved in a self-consistent way in parallel with Poisson's and continuity equations for electrons & holes. Fig. 1(b) shows the proposed structure from TCAD tool. The TCAD validation of the suggested transistor is shown in Fig. 2, along with the measured outcomes from the device used in Reference [28]. The validation of TCAD simulation is supported by experimental data from [Sanae Boulay et al.]. The simulated V_{GS}-I_D curve aligns with experimental data, showing consistent trends in threshold voltage (V_{th}), G_M, and I_D. Threshold Voltage (V_{th}) point of view, the Simulated V_{th} is 1.1 V, and Experimental V_{th} is around 1.15 V. here deviation is approximately 4.3 %. Coming to transconductance, the Simulated G_M is 936.4 mS/mm, and Experimental G_M is 900 mS/mm. here deviation is approximately 4 %. the drain current value, in the simulated is 1.96 A/mm, and experimental is approximately 2 A/mm. here, the deviation is approximately 2 %. This close agreement validates the model's accuracy, providing confidence in the simulation results.

The device functionality behaviors are dependent on the device structure geometry. This HEMT structure performance analyzed first at four various gate lengths such as 100nm, 80nm, 60nm, and 40nm. The

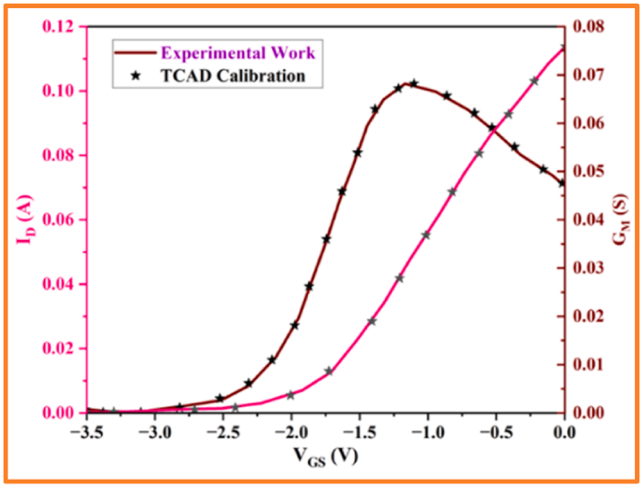

Fig. 2. V_{GS} vs. I_D and transconductance plots are used to calibrate the TCAD simulation tool against experimental results, as demonstrated by Sanae Boulay et al. [28].

impact of L_G is based on the below equation [29]

$$I_D = \frac{Q_G\ Vsat\ \eta}{L_G} \quad (1)$$

Where Q_G= charge under the gate electrode, Vsat=saturation velocity, η=modulation efficiency

We know that, the max oscillation frequency and the cutoff frequency (f_T) are connected. The recognized expression shown below is used to calculate the f_T. The f_T is directly related to G_M, and inversely correlated with the capacitance in the junctional areas [30].

$$f_T = \frac{G_M}{2\pi(C_{GS} + C_{GD})} \quad (2)$$

In this HEMT device, only a small portion of the charge carriers reach the saturation velocity and enter the quantum well. With the exception of perfect transistors, where it is assumed that all carriers flow through the channel at a saturation velocity, modulation efficiency is therefore less than unity. Therefore, gate length should be reduced to maximize drain current while avoiding needlessly raising off current. This report presents simulations of the device with varying gate lengths from 100 to 40 nm. Fig. 3 illustrates the impact of L_G scaling on device behaviour with a $Al_{(0.1)}Ga_{(0.9)}$ N barrier layer in the structure. At L_G = 40 nm, device demonstrates a peak G_M of 569.29 mS/mm, marking a 31.45 %, 20.78 %, and 10.24 % enhancement over the peak G_M observed at L_G = 100, 80, & 60 nm, respectively. Moreover, with a highest I_D of 1.96 A/mm, the HEMT at L_G = 40 nm exhibits an 73.45 %, 47.36 % and 22.5 % improvement in peak drain current compared to L_G = 100 , 80, & 60 nm, respectively. The drain currents for the transistor plotted versus the V_{ds} at each of the four L_G's under gate voltages of 0 V, and −2 V are revealed in Fig. 3(d). Analysis of the results reveals that the transistor with L_G = 40 nm achieves a peak I_D of 2.01 A/mm @ V_{GS} = 0 V. This marks a 35.81 %, 24.07 %, and 12.29 % increase over the maximum I_D noted for L_G = 100, 80, & 60 nm, respectively. Additionally, the L_G = 40 nm device demonstrates a peak f_T of 434.43 GHz, showcasing a substantial improvement of 139.3 %, 89.13 %, and 42.71 % compared to the cut-off frequency values recorded for L_G = 100, 80, & 60 nm HEMTs, respectively.

Fig. 4 represents the characteristic analysis of the transistor at various gate-recess values, (G_R=Gate Recess), with range from 2 nm to 4 nm. Surface electric fields become significant as the gate-recess increases, resulting in a reduction of n_s (2DEG density) & subsequent loss in carrier mobility as the barrier thickness beneath the gate decreases. Additionally, a positive V_{th} (threshold voltage) shift is caused by this phenomenon [31]. The device exhibits notably high transconductance at G_R = 4nm, which can be attributed to proximity effects' ability to

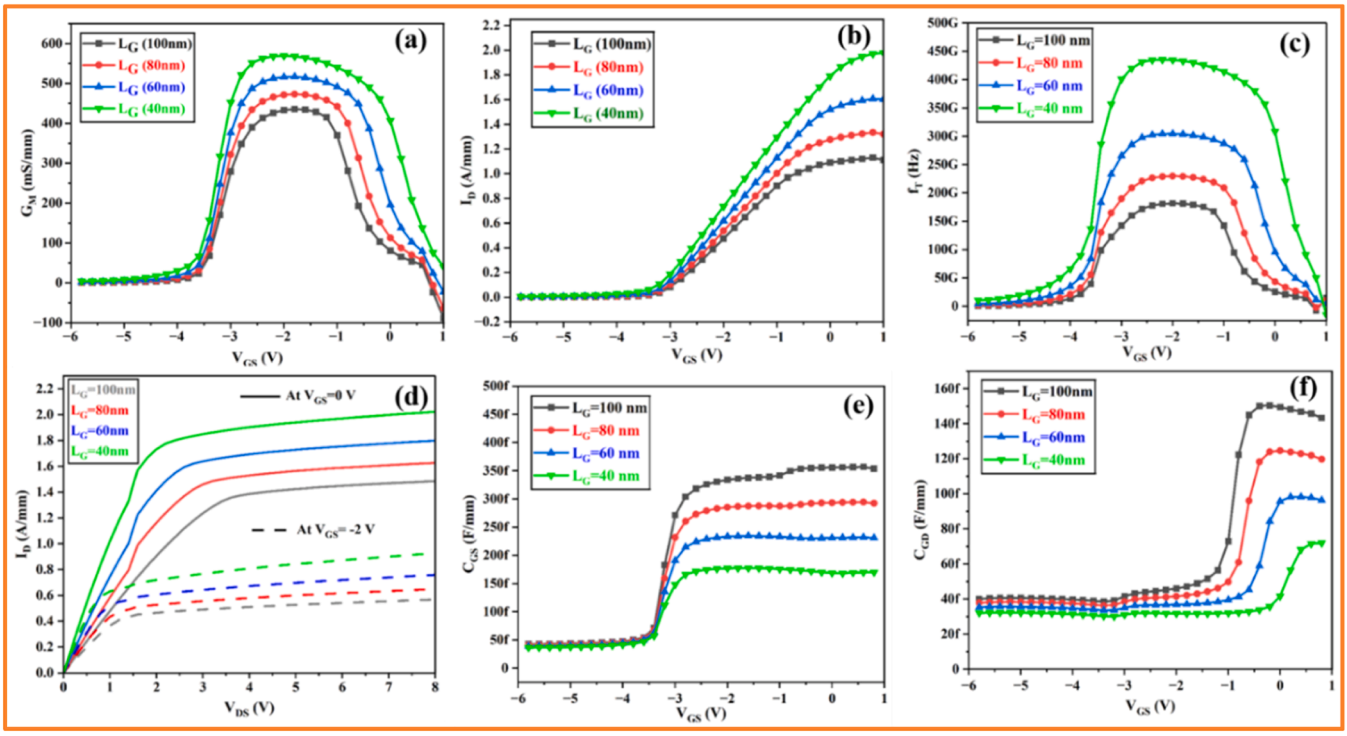

Fig. 3. The results of gate length (L_G) scaling on (a) Transconductance (G_M), (b) Transfer characteristics, (c) f_T vs $V_{GS,}$ and (c) Output curves, (e) C_{GS} (source-to-gate capacitance), (f) C_{GD} (drain-to-gate capacitance).

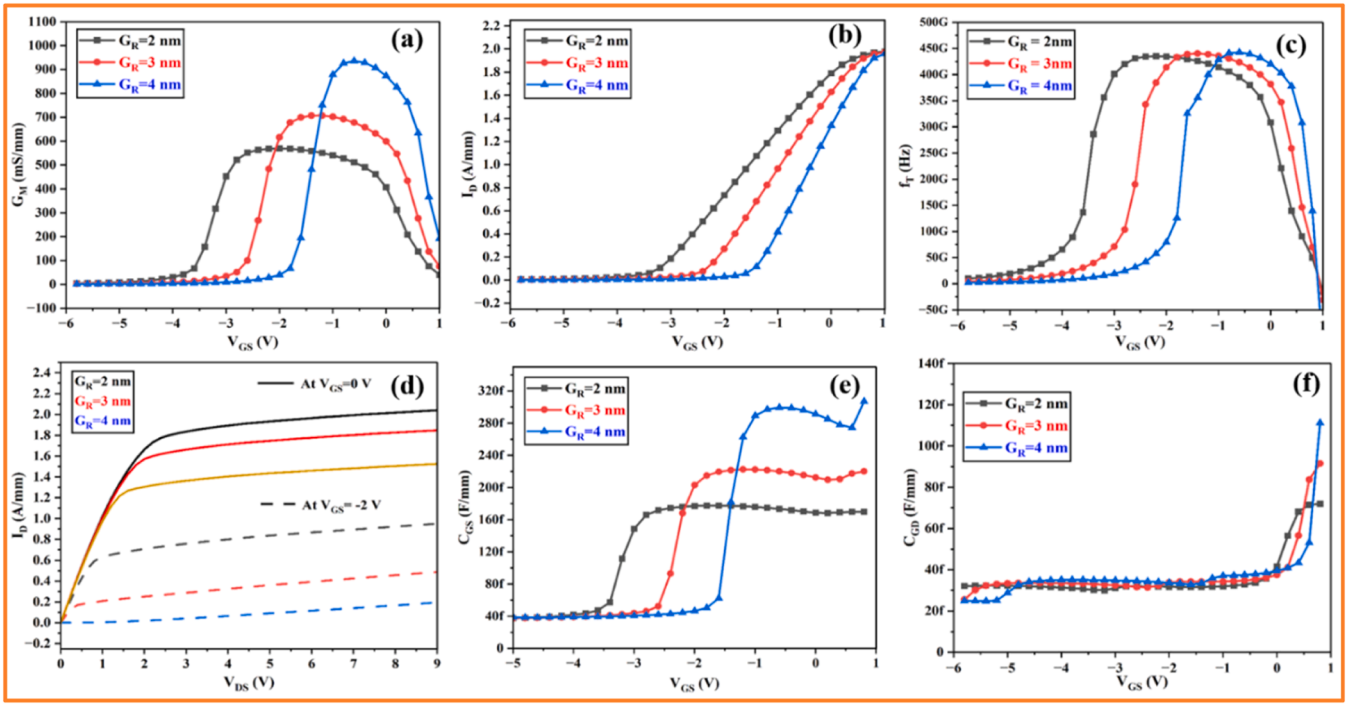

Fig. 4. The results of G_R on (a) G_M, (b) Drain current (I_D), (c) f_T vs $V_{GS,}$ (c) Output curves, (e) $C_{GS,}$ and (f) C_{GD}.

effectively control sheet charge density. From Fig. 4, the device reaches its maximum transconductance value of 936.40 mS/mm at G_R = 4 nm. varying gate recess depth result in varying drain current (I_D) density values. In particular, the I_D density values are 1.92, 1.91, & 1.90 A/mm, respectively, at G_R values of 2nm, 3nm, and 4nm. The drain characteristics exhibit a comparable pattern, as illustrated in Fig. 4(d). The decline in 2DEG density and carrier mobility is mostly responsible for the I_D degradation as recess depth increases. At G_R = 2nm, the device reaches f_T of 435.12 GHz.

Controlling the threshold voltage precisely is necessary to guarantee the proper functioning for power electronic applications. The following technique can be used to examine the threshold voltage (V_{th}) of HEMT based on gallium nitride using a polarization-dependent model [32].

$$V_{th}(x) = \varphi_m(x) - \Delta E_C \frac{qN_D d}{2\varepsilon(x)} - \frac{\sigma(x)}{\varepsilon(x)} d$$

In this context, x, φm(x), and ΔEc(x) denotes the Al material of AlGaN, the SB (Schottky barrier) height, & the conduction band offset between GaN & AlxGa1-xN, respectively. Moreover, ε(x), d, and ND indicate the thickness, doping amount, and dielectric permittivity of the AlxGa1-xN barrier. σ(x) represents the charge density of the induced polarization sheet.

In this work, we studied DC & RF performance of the HEMT incorporating an $Al_{(0.1)}Ga_{(0.9)}$ N barrier layer and used gate metal optimization to produce a positive V_{th} movement. The impact of gate-metal on transistor performance is seen in Fig. 5& 6. The maximum values of G_M, I_D, output current, and f_T that were noted are 935.83 mS/mm, 1.95 A/mm,1.44 A/mm and 442.74 GHz, respectively. Simulated energy band diagrams reveal the impact of gate metals on device threshold voltage. As the metal work function, ϕm (x), of the gate increases, the threshold voltage shifts positively. This positive shift occurs because a higher gate work function raises the energy barrier, requiring a greater gate voltage to invert the channel. This positive side shift in V_{th}, observed with increasing work function, can be elucidated by analyzing EB graphs observed through simulations, shedding light on how gate metals affect the V_{th} of the proposed transistor structure.

The band diagrams analysis for this HEMT device with various gate metals shown in Fig. 5. The primary reason for the change in performance is the elevation of the edge of the CB, this shift is directly related to the increasing work function values corresponding to different schottky barrier heights. According to Fig. 5, as work function values increase, there is a modest decrease in the carrier density of the AG-epitaxial sheet, which accounts for the observed rise in V_{th}. The structure's recessed gate technique contributes to the rise in V_{th} as well. This technique results in a small drop in the amount of sheet carriers by lowering the effective barrier thickness below the gate. It is notable that the aluminium gate metal attained the maximum saturation I_D in the Fig. 6, showing 1.43 A/mm at a V_{GS} of 0 V. The phenomenon wherein the amount of carriers at the AlGaN/GaN junction declines as gate work function parameters increase is explained by the device's peak I_D occurring at the lowest gate metal value [33].

Fig. 7 illustrates the results of varied length for source to gate functionality at a L_{GD} of 350 nm. The results, including G_M, transfer characteristics, output curves, cutoff frequency, C_{GS}, & C_{GD}, are compared. In Fig. 6(a), with a source to gate length of 150 nm, the HEMT shown a maximum transconductance of 936.40 mS/mm. Concurrently, Fig. 7(b) shows a highest drain current of 1.95 A/mm. Notably, the highest I_D of 1.05 A/mm is achieved at $V_{GS} = -0.5$ V, and this increases to 1.51 A/mm at $V_{GS} = 0$V for $L_{GS} = 350$ nm, as shown in the output characteristics

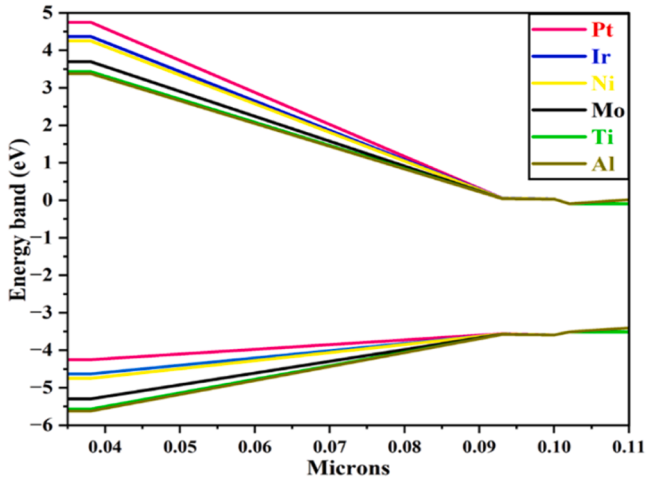

Fig. 5. Band diagram with various Gate metals.

in Fig. 6(c). The f_T vs V_{GS} graphs depicted in Fig. 6(d) demonstrate that at $L_{GS} = 150$ nm, the device achieves a highest f_T of 442.59 GHz. As L_{GS} decreases, parasitic capacitance will also decrease, as displayed in Fig. 6. The C_{GS} and C_{GD} variations with L_{GS} scaling follow the trend of the transistors RF functionality. The gate-metal work function influences the Schottky barrier height, directly affecting threshold voltage. Metals with higher work functions, such as Pt, reduce V_{th}, enabling better gate control and minimizing leakage. Conversely, lower work function metals, like Ti, may increase V_{th} but are more cost-effective. The manuscript uses a balanced approach, selecting a gate metal that optimizes performance while maintaining manufacturability. Compared to literature, the selected metal demonstrates similar V_{th} trends, aligning well with both performance and practical constraints.

The findings indicate that if L_{GS} is more, RF and DC characteristics of the transistor will degrade. Fig. 6 highlight that the device with $L_{GS} = 150$ nm exhibits better performance. The influence of the electrical characteristics on L_{SD} becomes apparent first in the E_F (along the channel) component in gallium-nitride device. Reducing the gap between source and gate expands the field below the gate, increasing electron speed and enhancing channel current, thereby improving DC&RF characteristics [34,35]. This emphasizes the importance of restricting the gate to source length to escalate the RF & DC characteristics of the device. To evaluate the effect of L_{GD} scaling, an investigation was performed using a lowest source-to-gate length of 150 nm. Scaling L_{GS} and L_{GD} improves performance but raises challenges like lithography limits and thermal management. For example, achieving 150 nm L_{GS} and 350 nm L_{GD} requires advanced lithographic techniques (e.g., e-beam lithography), which are feasible but costly. The focus of this work is on theoretical optimization to guide experimental design. In Future studies, we will address manufacturability by integrating realistic process constraints and thermal modelling.

The results of L_{GD} scaling on transistor functionality is depicted in Fig. 8 at a fixed gate to source distance of 150 nm. The acquired results for the C_{GS} and C_{GD}, output curves, f_T, transfer characteristics, and transconductance are analysed. This HEMT structure shown a maximum G_M of 936.40 mS/mm, and a highest drain current of 1.92 A/mm, when the gate to drain length was set at 350 nm as shown in Fig. 8 (a&b). The drain characteristics of Fig. 7(c) show that the greatest saturation drain current was 1.48 A/mm when V_{GS} was set at 0V and increased to 1.89 A/mm at V_{GS}=0.5V for L_{GD}=350nm. The f_T vs V_{GS} graphs in Fig. 7(d) demonstrate that a highest f_T of 442.59 GHz is reached at L_{GD}=350 nm. Fig. 8(e-f) illustrates how parasitic capacitance drops when L_{GD} shrinks in size. The results indicates that the enhanced DC and RF functionality can be ascribed to the rise in electric field that follows the decrease in L_{GD} [36]. Finally, the device's conductance-band distribution and electron density in the quantum well are displayed in Fig. 9.

The threshold voltage (V_{th}) is highly sensitive to the work function of the gate metal. A higher work function increases the Schottky barrier height, requiring a greater gate-to-source voltage to form a conductive channel. Conversely, lower work function materials reduce V_{th}, which can lead to enhanced leakage but improve gate modulation efficiency. In this work, the selected gate metal balances this trade-off, ensuring stable V_{th} while maintaining high G_M. This is crucial for high-frequency applications where tight control over V_{th} reduces noise and improves reliability. Shortening L_{GS} increases the electric field under the gate, leading to more efficient channel control. This trend stabilizes V_{th} as the gate retains strong modulation over the channel. Stable V_{th} across a wide operating range indicates that the device is less susceptible to temperature-induced carrier fluctuations, a common challenge in wide-bandgap semiconductors A predictable V_{th} minimizes gate-drive power, enhancing efficiency in RF power amplifiers where precise modulation is critical for linearity and low distortion. The observed V_{th} stability suggests reduced hysteresis and trapping effects, increasing device reliability during high-frequency switching or in radiation-prone environments such as space applications. Table 1

GaN based HEMTs have shown significant promise for high-

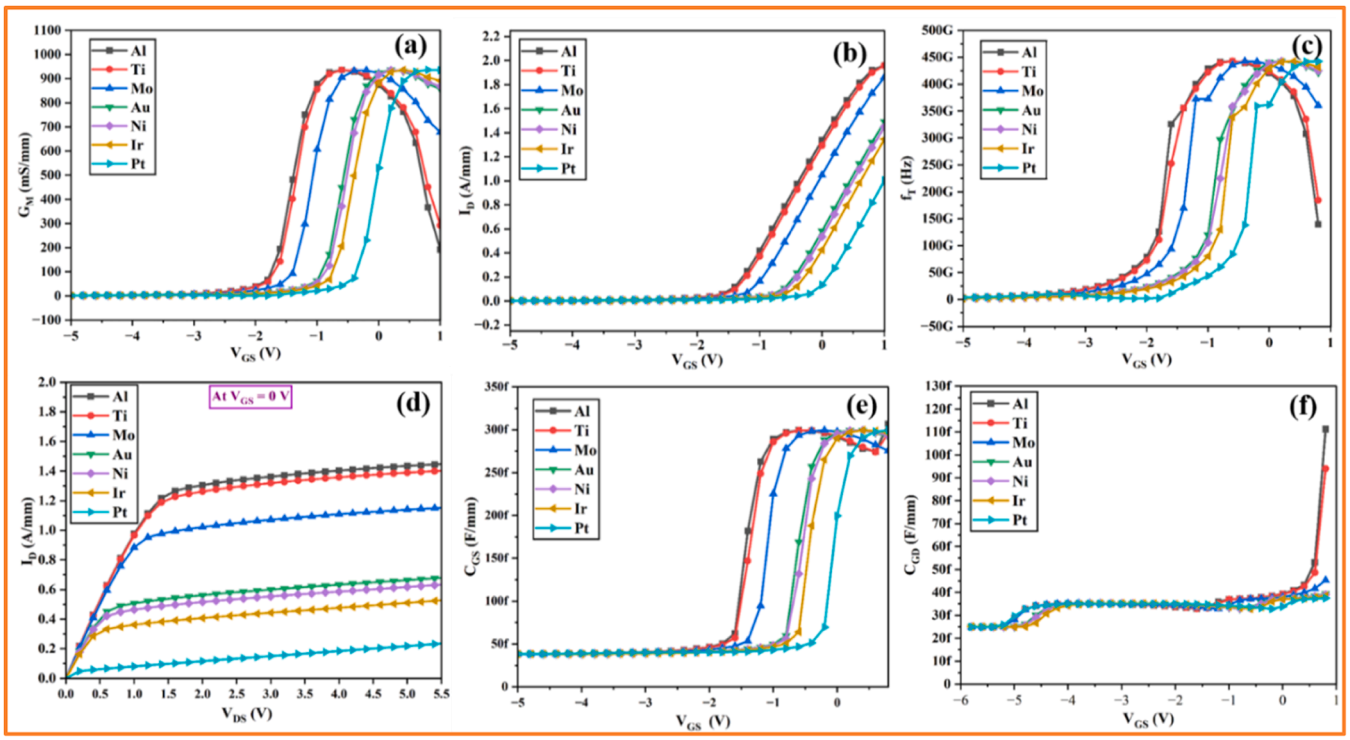

Fig. 6. The performance of work function analysis on (a) transconductance(G_M), (b) Transfer characteristics, (c) f_T vs $V_{GS,}$ (c) Output curves, (e) $C_{GS,}$ and (f) $C_{GD.}$

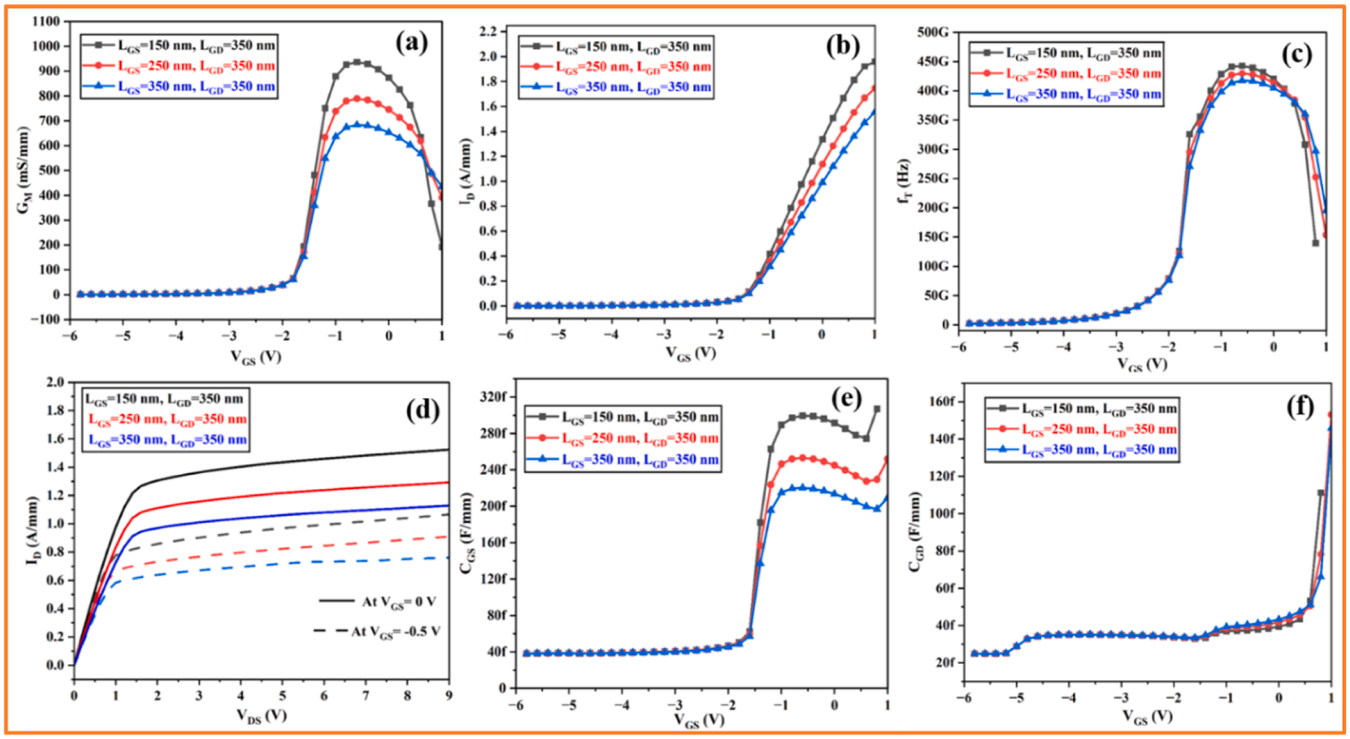

Fig. 7. The results of gate-to-source length scaling on (a) G_M, (b) Transfer characteristics, (c) f_T vs $V_{GS,}$ (c) Output curves, (e) $C_{GS,}$ and (f) $C_{GD.}$

frequency and high-power applications. Competing technologies include InAlN/GaN and *Sc*-doped GaN HEMTs, which offer specific benefits. InAlN/GaN HEMTs achieve a natural lattice match with GaN, reducing dislocations and enhancing 2DEG density. However, their stability during fabrication is limited due to oxidation susceptibility, making long-term reliability a challenge. *Sc*-doped GaN HEMTs improve thermal management and electron mobility through localized states in the conduction band, but the doping process is complex and costly. In contrast, the step-graded SRL approach studied here offers a cost-effective solution with silicon substrates, effectively managing dislocations while enhancing RF/DC performance. By optimizing scaling parameters and using advanced T-gate designs, this work provides

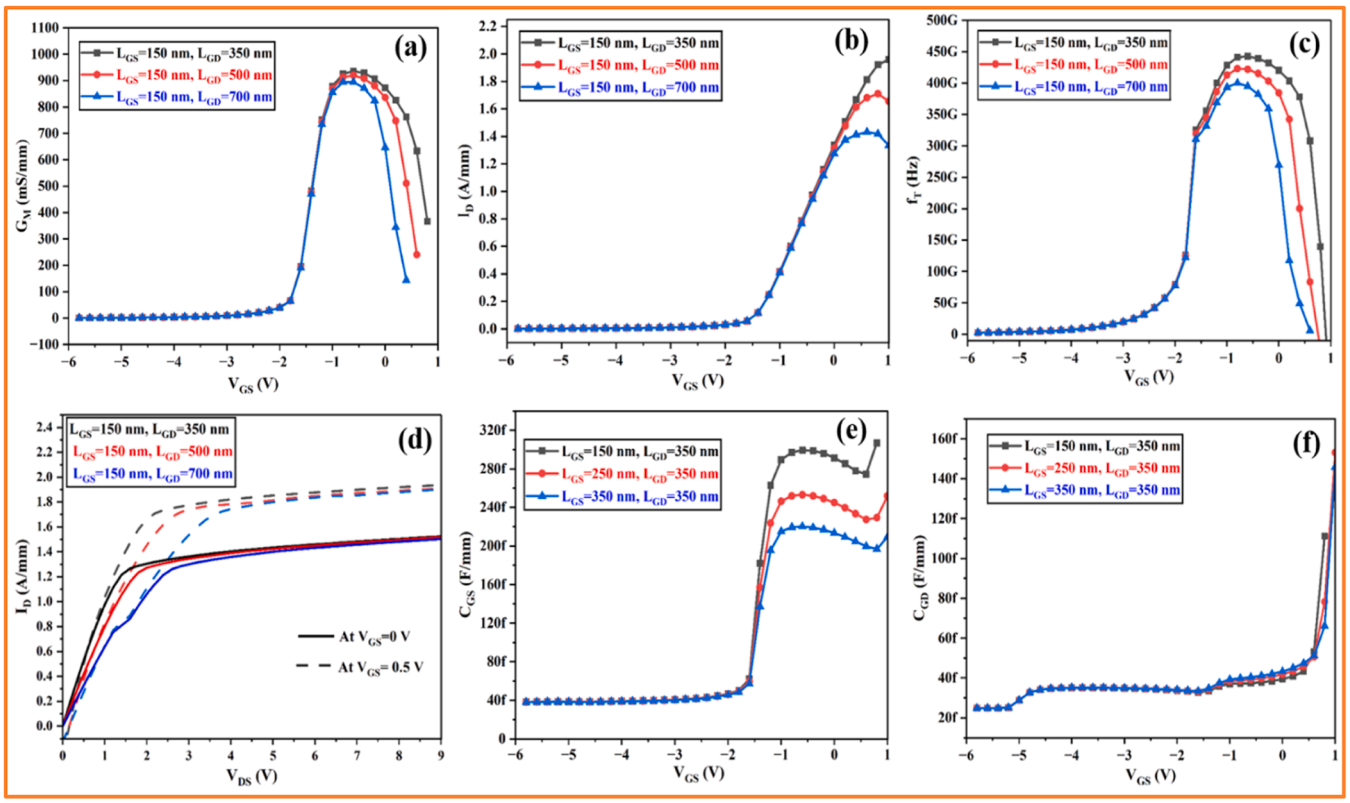

Fig. 8. The results of drain to gate length scaling on (a) G_M, (b) Transfer characteristics, (c) f_T vs $V_{GS,}$ (c) Output curves, (e) $C_{GS,}$ and (f) C_{GD}.

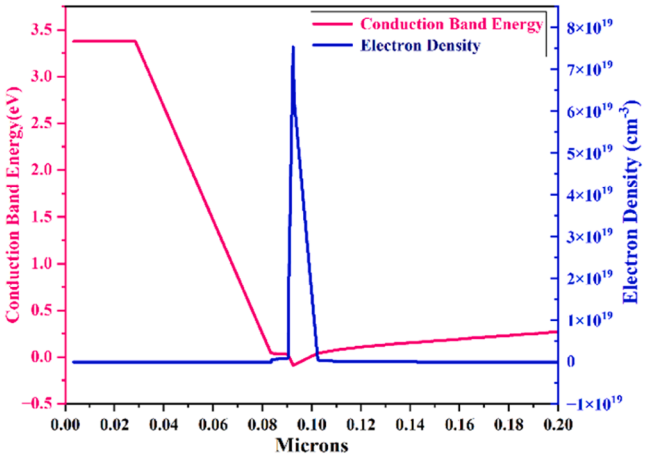

Fig. 9. Conduction Energy-band & Electron density distribution of SRL –HEMT at L_G=40nm.

practical performance improvements without the trade-offs seen in competing designs.

This design is highly relevant for space electronics and RF power amplification. In space applications, reliability under radiation and extreme conditions is critical; the SRL improves structural stability and reduces dislocation effects. For RF amplifiers, achieving a high cut-off frequency (442.59 GHz) and transconductance (963.4 mS/mm) enables higher power density, vital for 5G technology and radar systems. The use of silicon wafer not only reduces costs but also facilitates integration with existing silicon-based systems, making the design suitable for mass production. The comprehensive comparison table is given below.

While scaling parameters significantly enhance performance,

Table 1
: comprehensive comparison of the results.

Analysis	Variation	G_M (mS/mm)	Drian current (A/mm)	Output current at V_{GS}=0V (A/mm)	f_T (GHz)
Gate length	100nm	433.28	1.13	1.48	181.44
	80nm	471.31	1.33	1.62	229.63
	60nm	516.27	1.60	1.79	304.45
	40nm	569.29	1.96	2.01	434.43
Gate recess	2nm	936.40	1.92	1.6	435.12
	3nm	935.83	1.91	1.84	441
	4nm	936.40	1.90	2.04	444.1
Gate-to-source length scaling	L_{GS} = 150 nm, L_{GD}=350nm	936.40	1.95	1.51	442.59
	L_{GS} = 150 nm, L_{GD}=350nm	835.21	1.45	1.21	350.75
	L_{GS} = 150 nm, L_{GD}=350nm	732.18	1.02	0.89	287.12
Gate-to-drain length scaling	L_{GS} = 150 nm, L_{GD}=350nm	912.32	1.84	1.77	425.33
	L_{GS} = 150 nm, L_{GD}=350nm	923.47	1.89	1.83	433.12
	L_{GS} = 150 nm, L_{GD}=350nm	936.40	1.92	1.89	442.59

challenges such as increased parasitic effects and thermal issues arise. This study aims to establish theoretical benchmarks to guide practical designs of HEMT. Although fabrication challenges exist, the insights provided here lay the foundation for optimizing trade-offs between performance, cost, and reliability.

4. Conclusion

In summary, we have investigated a high-performance 40nm gate length and gate to source length of 150nm with 350nm gate to drain distance transistor on silicon substrate. Here, highest transconductance (G_M) of 963.40 mS/mm, f_T of 442.59GHz and a drain current per unit gate width of 1.96 A/mm. Reducing the gate length led to an increase in transconductance, I_D, and cut-off frequency, while no change was observed in the threshold voltage. Expanding the gate recess enhances the transconductance and threshold voltage, although there is minimal variation in the I_D, and f_T. Reducing the distance between gate-to-source and gate-to-drain leads to higher G_M and drain current, with no impact on the threshold voltage. This optimization enables the attainment of remarkable power density and DC & Rf performance, rendering it highly applicable for various applications including high-power space electronics and Cutting-edge RF power amplification technology.

Compliance with Ethical Standards

The authors have not conducted studies involving human participants or animals for this article.

CRediT authorship contribution statement

A Akshaykranth: Writing – original draft, Formal analysis, Data curation. **J Ajayan:** Writing – original draft, Visualization, Validation, Data curation, Conceptualization. **Sandip Bhattacharya:** Visualization, Validation, Formal analysis. **D Nirmal:** Visualization, Validation. **Santhosh Paramasivam:** Writing – review & editing, Visualization, Validation, Resources, Conceptualization. **Gianluca Gatto:** Writing – review & editing, Validation, Supervision, Project administration, Funding acquisition, Conceptualization. **Amit Kumar:** Writing – review & editing, Visualization, Validation, Resources.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

The authors do not have permission to share data.

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