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Development and Characterization of Flexible Double-Gate Organic
Transistors for Sensing Applications

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Abstract

Since the first tools were realized, curiosity and necessity have always led humanity to search for better solutions to improve daily life. Although progress is something that accompanied the growth of humanity as a civilization, it is undeniable that inventions and discoveries increased exponentially in the last 200 years. It is also true that one invention or discovery calls for another one and so on. Of course, once something is invented, it can always be perfected and when someone discovers something, knowledge can always be expanded, as there might be obscure aspects that cannot be unravelled without new inventions and technologies. Sometimes inventions are accidental, other times they come from research addressed to invent something else that led to unexpected results. Transistor invention is a consequence of the will of various researchers to develop a device, based on a semiconductor, that could amplify signals. This invention opened the doors for a whole new generation of devices, from the simplest radios to more complex devices like computers. Today we have these objects in most houses, because over the years the technology was perfected, industrialized and made affordable for almost anyone. And new branches of research developed over the years, to further improve, differentiate and exploit new technologies and materials that were developed or needed testing. Organic electronics is a technology that seems relatively new to the audience, since the first market available device was presented less than two decades ago, but research on that field dates way back. But if you look at all human history, progresses since organic materials first approach have been a multitude and today is widespread, especially in monitors. Organic electronics is the starting point of a new kind of technology that's gained a lot of interest in the latest decades of the 20th century and continues now in the 21st century. The possibility to realize flexible devices in a large area gives this field of research a particular interest, since it opens the doors to a multitude of new possible applications. Particular interest has been given to the possible biological and biomedical aspects of such technology, thanks to the possibility to realize flexible devices that could fit inside clothes and adhere to the body, to acquire data with more precision. Conformable devices, realized using ultra-thin substrates, have been employed for artificial skin, a logical consequence of the flexibility properties of such materials. Effects of deformation are discussed and analysed, since integrity of devices is paramount to the effectiveness of this technology. Since its invention, a multitude of transistor architecture have been proposed and explored, to always find new or better solutions to problems and, with the discovery of conduction properties, flexibility, as well as durability and reliability, gained importance when designing a new device. One architecture in particular garnered

attention in the scientific scope and is explored and studied in a lot of different configurations, possibilities of use, and advantages that offers. The double-gate architecture, both in inorganic and organic electronics, is vastly used and studied, as it presents itself as a platform for the realization of versatile devices, from circuitry to sensing. As a matter of fact, as will also be presented in this thesis, this architecture has multiple advantages, such as the possibility to tune the threshold voltage, allowing to design circuits realized with a number of devices that all have the same working point. Moreover, the top gate of these structures can be used as a sensing platform, effectively realizing a sensor for mechanical quantities such as temperature and force; ideally, therefore, when properly tuned and characterized, they could be employed for the realization of artificial skin, granting fundamental capabilities to those who lost them. Alternatively, it can be properly functionalized for the recognition of biological species, effectively becoming a biosensor. Of course, when considering these, biocompatibility of materials is a primary property that material must have. The main target of this PhD research activities is to report a thorough study on the aforementioned architecture, with a focus on its multiple beneficial aspects, and investigate the mechanical properties of organic semiconductors. One of the benefits of using such architecture is to tackle a problem that afflicts organic electronics, the degradation of the active layer, that thanks to its self-encapsulating nature, double-gates effectively counter.

After a brief introduction about flexible electronics in chapter 1, a state of the art on organic electronics specifically regarding the double gate architecture is presented in chapter 2. Materials and methods, as well as the instrument used, are described in the relative section of chapter 3. Chapter 4 delves into the description of the fabrication and optimization process followed to realize the double gate structure. The mechanical characterization of the devices as temperature and force sensors, both separately and in multimodal mode is reported in chapter 5. Finally, effects of mechanical deformation on different semiconductor are reported in chapter 6, as well as a preliminary characterization of strain sensors. In conclusion, a summary of the results obtained is reported.

List of Publications

1. Pecunia, V., Petti, L., Andrews, J., Ollearo, R., Gelinck, G. H., Nasrollahi, B., ... & Leong, W. L. (2024). Roadmap on printable electronic materials for next-generation sensors. *Nano Futures*.
2. Concas, M., Mascia, A., Lai, S., Bonfiglio, A., & Cosseddu, P. (2024). Fabrication of Flexible Double-Gate Organic Thin Film Transistor for Tactile Applications. *Advanced Materials Technologies*, 9(22), 2400534.
3. Mascia, A., Concas, M., Podda, E., Casula, G., Lai, S., & Cosseddu, P. (2024). Mechanical Deformation Effects on Flexible Thin Film Transistors: A Comparison Between 6, 13-Bis (Triisopropylsilylethynyl) Pentacene and N, N'-Bis-(2-Ethylhexyl)-1, 7-Dicyanoperylene-3, 4: 9, 10-bis (Dicarboximide) Derivatives. *Advanced Materials Interfaces*, 2400783.

Conference Presentations

- 17th International Symposium on Flexible Organic Electronics (ISFOE), 1 – 4 July 2024, Thessaloniki, Greece

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1. Chapter I: Introduction to flexible electronics

Nowadays, silicon-based technology has reached a very high level of optimization and miniaturization, and most devices used every day are realized with such technology. The last 50 years saw a rapid increase in the market related to electronic devices^[1–3]. Think about how today, devices like smartphones, TVs or computers are widely diffused, as well as solar cells, and it's an ever-evolving sector, with companies that fight to have the latest and more advanced model in their portfolio. In **Figure 1**, the market share for different flexible devices is reported.

Global Flexible Electronics Market Share, By Application, 2023

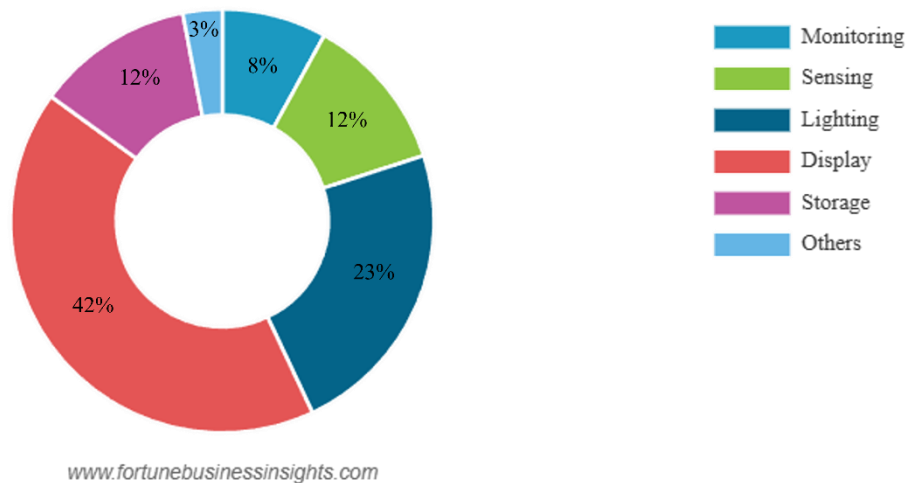


Figure 1: Flexible electronics market report performed by Fortune Business Insight^[4].

However, this seems to be not enough, as humanity strives to research always better solutions, and more efficient devices, to improve daily life. A leading research sector for the development of always more efficient flexible electronic devices is artificial skin. For instance, robots designed for household and entertainment tasks will require advanced skin sensitivity to interact safely and effectively with humans. The challenge lies in creating a vast network of pressure sensors that can be seamlessly integrated into a flexible, cost-effective material. Traditional silicon-based electronics, while powerful, lack the flexibility and scalability necessary for such a system. Metal-oxide-semiconductor field-effect transistors (MOSFETs) are not suitable for such applications, due to the way they are built.

Organic thin-film transistors (OTFTs) offer a promising solution. These devices, built from organic materials, are inherently flexible and can be produced at low cost using large-area

printing techniques. However, the family of organic devices is a quite large one, since the only requirement to be included here is that the semiconductor used is organic and the other components can be inorganic. There are in fact different metals that, with the right thickness, can be considered flexible and some inorganic semiconductors are being studied^[5]. Moreover, TFTs are born of inorganic materials, thanks to the employment of amorphous silicon (aSi)^[6], and flexible inorganic transistors are proposed using Zinc Oxide (ZnO) as semiconductor^[7]. Therefore, it is worth noting that flexible devices can be realized using only inorganic materials, although such family of devices will not be discussed here.

There are of course differences also inside the family of organic devices, since employed semiconductors can be n-type or p-type. Different from MOSFETs, that work in depletion mode, OFETs work in accumulation mode and the charge carriers are not intrinsic to the semiconducting material but are injected by the source and drain electrodes. P-type organic devices are more common, since development of n-type semiconductors is more challenging.

By combining OFETs with rubber-based pressure sensors, researchers aim to develop a practical artificial skin that can accurately perceive pressure and enable robots to interact with their environment in a human-like manner. A first approach to such a problem was proposed by Someya et al.^[8], since, at the time, artificial skin progress was falling behind with respect to vision and speech recognition. When we consider flexible devices, we think of all of those devices that can adapt to non-planar surfaces to optimize their performances meanwhile offering the best solution to overcome some limitation. Apart from the already mentioned artificial skin, there's a multitude of applications that would benefit from being realized using flexible devices. For instance, flexible solar cells could be applied to backpacks, bags or directly on clothes, without hindering the users' comfort, but supplying them with the possibility to charge their phone or some other small device^[9,10].

Sensing also plays a vital role in the development of flexible technology, due to its intrinsic properties of adaptation to irregular surfaces, especially with conformable devices such as electrodes or transistors^[11,12]. Flexibility, stretchability, and conformability are all properties fundamental in the development of devices that could, potentially, enhance the quality of life of people. Athletes could benefit from having devices directly attached to their skin, to monitor their performances in real-time, without having to wear annoying and cumbersome equipment. This also applies to healthcare environments, where having devices that can be worn without any physical or psychological distress meanwhile monitoring vital parameters

of the patient, would be a notable step ahead toward the integration of technology into our daily lives. This, of course, is strictly connected to the era we are living in, the Internet of Things (IoT) era.

Regarding sensing, an ulterior step related to thin-film transistors concerns the employment of dual-gate structures that can enhance sensitivity, thanks to the better control over the electric properties of the device. They are very versatile, due to the variety of materials and architectures that can be employed and are of course flexible. Robustness is also an important characteristic, enabling them to be used without damaging the active layer. Moreover, the presence of the second gate, makes them tunable and, if realized with the proper material, also able to detect various analytes thanks to the possibility to functionalize its surface. Last but not least, stability over time ensures a reliable and repeatable response to stimuli.

For these reasons, flexible technology study is of the utmost importance nowadays, and having reliable, efficient, and lasting devices is fundamental, also to reduce the impact that humanity is having on the welfare of its own planet. Finding solutions that would use materials in a more efficient way, with low consumption of energy for its production, that are cheaper and easier to produce with respect to what we are now doing, is an objective to strive for.

1.1 Thesis objective

Among the various flexible devices presented, always more focus is given to the transistors that can be used as sensor, joining the properties of a transistor, namely its intrinsic amplification properties, to those of materials and architectures that can transform such transistors in sensing devices for biological or mechanical quantities. Specifically, the aim for this category of devices is to be completely adaptive to the end user, allowing for a passive or active use, so that it could improve the overall quality of life. Of course, one of the main targets of this family of devices is to aid whoever uses them, without causing any discomfort, being lightweight, thin and unintrusive, with perfect integration with the daily life. With this in mind, flexible electronics is in constant growth and is strictly connected to the development of wearable devices but not only.

The aim of this thesis is to develop and optimize a robust and reliable transistor, realized with relatively cheap, fast, and large area techniques, that can be employed as a sensor for mechanical quantities. At present day, even though dual-gate thin-film transistor architecture is widely employed and recognized for its goodness, very few employed such kind of structure to realize force sensors and even less when considering temperature sensing. For this reason, the proposition is to fill the gap in the literature and present a device capable to respond to different stimuli, both separately and contemporarily.

Thus, in recent decades, organic electronics have been extensively studied as a technology platform for creating devices with biocompatible materials that can be deposited and processed on flexible and even ultra-flexible substrates, leading to easier production processes. With the birth of the IoT era, smart functionalities are required to be added to commonly used objects, but also to devices used in healthcare environment, allowing them to intercommunicate; moreover, the need of cost efficient, light weighted, and also flexible electronic systems is highly required. For such reasons, in recent years, many different technologies have been investigated and developed. Among them, organic electronics have gained a constantly increasing interest. Significant progress has been made in the development of flexible organic semiconductor devices, offering the potential to transform various technological sectors. Key advancements in organic light-emitting diodes, photovoltaics, thin-film transistors, integrated circuits, sensors, and memories have propelled this field forward. This thesis provides a comprehensive overview of critical challenges, including material optimization, device design, mechanical robustness, strain

effects, and fabrication methods. Additionally, we highlight successful applications and discuss future directions for this promising technology.

2. Chapter II: State of the art

Transistors are a fundamental component of most modern technological device. Developed in the second half of the 1940s, when the first transistor was demonstrated by J. Bardeen and W. Brattain at Bell Labs^[13], they are unanimously considered one of the most important inventions of the 20th century^[14–16]. Being so pervasive in modern technology, research has led to many discoveries in the field that are today used every day.

Silicon-based technology has undeniably revolutionized modern life, powering countless devices from smartphones to supercomputers. However, the relentless pursuit of smaller, faster, more energy-efficient, and more versatile electronics has pushed traditional silicon transistors to their physical limits, due to the lack of some properties needed for determined applications. As a result, researchers and engineers have turned their attention to alternative materials and device architectures, and their attention was captured by organic materials, that owned different interesting properties. This started a new branch of research, Organic Electronics.

Organic electronics is the branch of electronics that employs organic, carbon-based, molecules for the development and realization of electronic devices and systems. Dating back to 1986, when the first Organic Field Effect Transistor (OFET) was presented by Mitsubishi Electric researchers^[17], it now has almost 40 years of history and scientific discoveries, constantly updating. New polymers and small molecules are continuously developed to realize conductive and semiconductive materials that can fit the cause to achieve devices that can be manufactured using large area and cheap approaches^[18–20] such as coating^[21,22], inkjet printing^[23] or screen printing^[24].

Among the many advantages of the employment of polymeric materials, one of the most important properties is related to the possibility of fabricating flexible electronic devices and systems which has indeed opened a wide range of possible applications that were not suitable by employing rigid inorganic materials as silicon. Nowadays, a huge progress has been achieved in various flexible electronic devices, such as organic light-emitting diodes (OLEDs)^[25,26], organic field-effect transistors (OFETs)^[27–31], organic photovoltaics (OPVs)^[32,33], organic sensors, and memories^[34–37].

Without any doubt, among the many reported devices, organic transistors, OFETs, represent the building blocks for the development of whatever kind of flexible electronic systems and

have been intensively studied for many applications such as displays, smart tags, and sensors etc^[38–40].

OFETs can be used for logic circuits^[41–43], and, moreover, Someya's group developed an ultra-thin complementary organic transistor showing the amplifying capability^[44]. Amplification, a core characteristic of transistors, has been tested through the years, for different applications such as biosignals amplification systems compatible with innovative electrodes^[45], recording of electrocardiac signals through differential organic amplifiers^[46], or the monitoring of low level electroencephalographic signals^[47]. Also, one can design the transistor to operate at low voltages and high frequencies, for example for integration with lithium batteries, as demonstrated by Klauk's group^[48,49]. A summary of all the possible applications can be found in **Figure 2**.

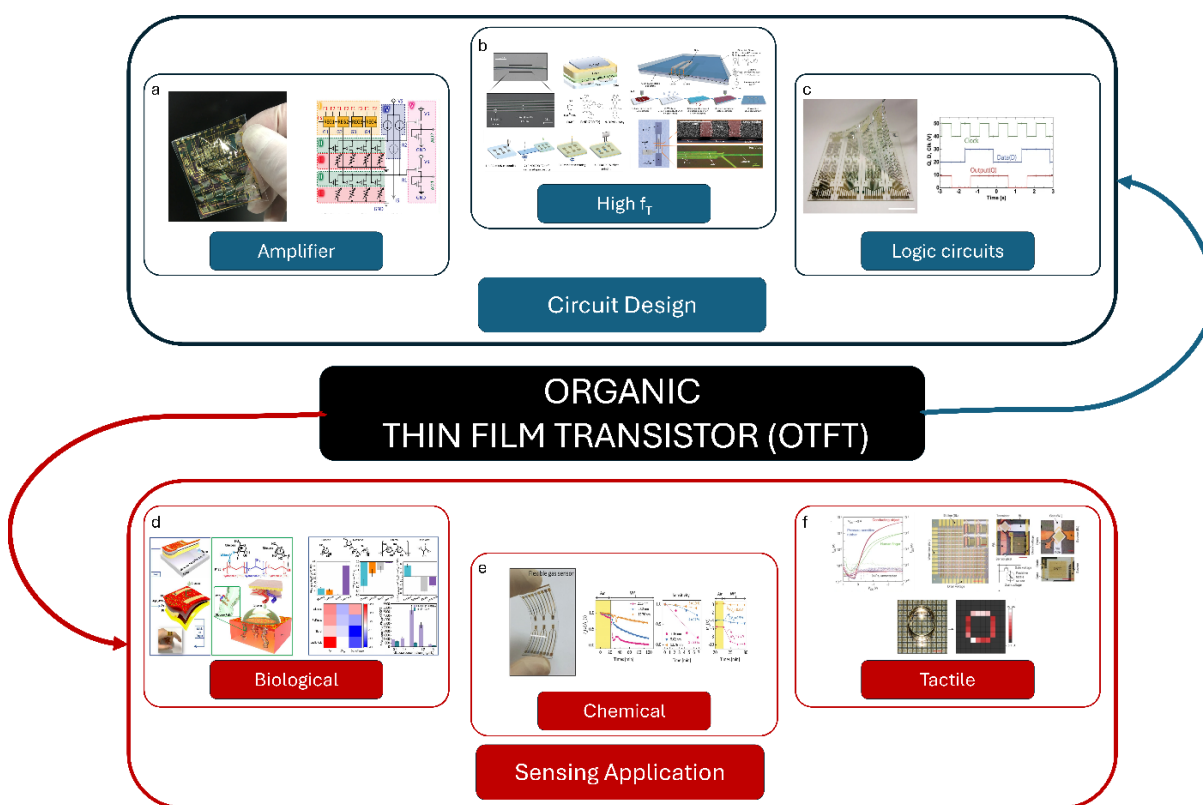


Figure 2: OTFT can be employed for a wide variety of applications, from design of circuits, such as (a) amplifier, (b) high frequency transistors, and (c) logic circuits to sensing applications for (d) biological, (e) chemical, and (f) tactile. Adapted and reproduced with permission from ref.^[50–56]. Copyright (a) American Association for the Advancement of Science 2020, (b) Wiley 2023 and Wiley 2021, (c) Springer Nature 2016, (d) Elsevier 2022, (e), Wiley 2016, (f) Springer Nature 2013.

Despite their many advantages, OFETs are not yet fully optimized in view of practical applications. As a matter of fact, one of the most annoying elements that

one has to deal with when working with organic materials is the degradation of the active layer given by environmental interaction, especially with water and oxygen (**Figure 3**)^[57,58]. Specifically, water creates a polar film, increasing density traps near the semiconductor and conductivity between source and drain respectively reducing mobility and increasing OFF current; oxygen instead, being electronegative, attracts electrons increasing holes in the channel and thus increasing OFF current and shifting threshold voltage but, most importantly, it oxidizes the semiconductor molecule, increasing hopping barrier and reducing the mobility. Another element that can cause degradation in device performances is light; it can cause oxidation, and generate trapping states that reduce mobility^[59]. Stability of this kind of devices is constantly under investigation, obviously because they can be interesting but if they are not reliable, there's no point in trying to use them for real world applications^[60–63]. The problem of degradation affects all organic technologies, not only OFETs, but also, for example, solar cells^[64–66].

While notable progress has been achieved in electrical performance and durability of organic thin-film transistors, reliability and reproducibility represent a fundamental characteristic that still has open issues which severely hindered the industrial development of organic electronic products^[28,67–69].

For these reasons a lot of work have been made on the development not only of novel and more reliable materials, but also on the design and fabrication of different devices architectures that could partially limit the before mentioned drawbacks, possibly adding new functionalities to the final devices.

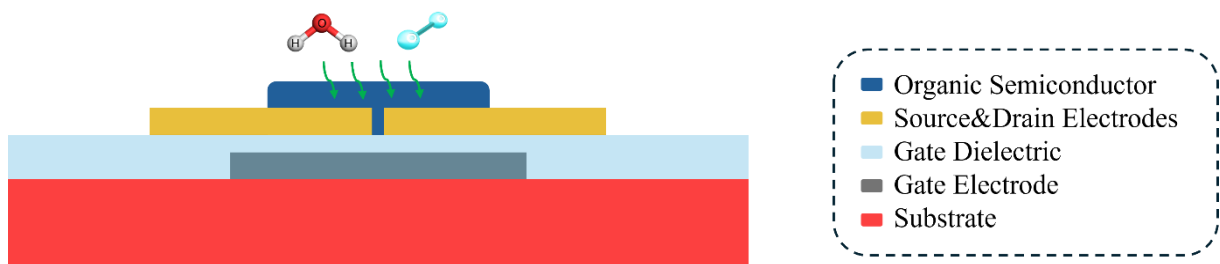


Figure 3: Bottom Gate Bottom Contact (BGBC) architectures are one of the most employed structures for developing Organic Thin Film Transistors (OTFTs). Such devices suffer from organic active layer degradation and water and oxygen are two of the main reasons of that.

One particularly promising research argument is the development of Organic Thin-Film Transistors (OTFTs). These devices, composed of organic semiconductor materials, offer several advantages over their inorganic counterparts, including flexibility, low-cost fabrication, and compatibility with large-area printing techniques.

Among them, we can find Field-Effect Transistors (FETs) that employ a Double-Gate (DG) configuration have gained wide interest over the years due to the advantages they offer. First of all, using such configuration, it is possible to modulate the flux of current within the channel through two different gate electrodes, offering a better control over the transistor working point. In fact, Double-Gate configurations have been already employed to improve Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), as they have better performances at low voltage and low power consumption and have enhanced features in various applications^[70,71]. The dual-gate structure, moreover, offers the capability to tune the threshold voltage (V_{th}) of the device, thus modifying the transistor properties^[72–74].

Among the various OTFT architectures, Dual-Gate (DG) OTFTs have emerged as a compelling option for a wide range of applications. This unique device configuration, featuring two independent gate electrodes, provides enhanced control over carrier transport and device performance. DG OTFTs offer superior electrical characteristics, such as higher mobility, lower threshold voltage, and steeper subthreshold slope, compared to single-gate devices. The dual-gate structure can effectively shield the channel region from external disturbances, leading to improved device reliability and longevity. The independent control of the two gates enables the design of flexible and reconfigurable circuits, opening to new possibilities for wearable and implantable electronics. DG OTFTs can be employed as highly sensitive sensors for various physical and chemical parameters, including strain, pressure, temperature, and gas.

The potential applications of DG OTFTs are vast and far-reaching. Some of the most promising areas include wearable electronics (flexible and stretchable displays, smart textiles, and health monitoring devices), Internet of Things (IoT) applications (low-power, energy-efficient sensors and actuators), flexible and printable electronics (large-area, roll-to-roll production of electronic devices), and biomedical devices (implantable medical devices and biosensors). As research and development in this field continue to advance, we can expect to see even more innovative and groundbreaking applications of DG OTFTs. Employing a Double-Gate configuration in thin film transistors architectures, as depicted in **Figure 4**, leads to an intrinsic passivation of the transistor active channel, thus leading to a dramatic reduction of its degradation due to environment contamination. Moreover, the employment of a Double-Gate architecture could be exploited for the development of different kind of sensing devices. In fact, by properly functionalizing the second gate electrode, its interaction with an external medium can lead to a charge

displacement that, in turns, leads to a modulation of the carrier concentration in the transistor channel, or in other words, to a shift of the threshold voltage. There are, indeed, several recent reports where such an approach has been efficiently employed for the fabrication of high performing charge sensing devices.

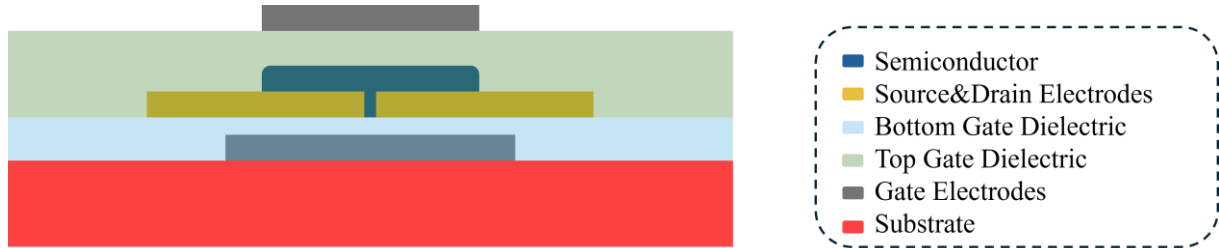


Figure 4: Standard Double-Gate structure in bottom contact configuration.

As of today, Dual-Gate Transistors (DGTs) have a long story, being the 1981 the first year in which this kind of structure was reported^[75] and have a large diffusion over the field of radio frequency (RF). However, before 2003 this kind of structure was not applied to the organic electronics^[76]; and one of the first applications came in 2007 as an inverter^[77].

For these reasons, this thesis is focused on those transistors that fall in the organic category and, specifically, on those devices that employ a Double-Gate configuration for their operation, a four-terminal device in which a secondary gate can be employed to tune the device characteristics. First of all, a panoramic of all the various Double-Gate architectures is presented, with different approaches and design strategies to overcome common issues related to organic materials. In particular, the focus is on the fabrication methods and design and material optimization of these four different Double-Gate organic transistors architectures, namely organic thin-film transistors (OTFTs), organic charge modulated field-effect transistors (OCMFETs), electrolyte-gated organic field-effect transistors (EGOFETs), and organic electrochemical transistors (OECTs). Moreover, this thesis aims to describe all the possible applications, in which the Double-Gate architecture offers advantages and outstanding solutions for the realization of several types of devices for sensing and circuits. As is discussed in the conclusions, the addition of a fourth terminal gives more degrees of freedom in the realization of the device itself.

2.1 Dual-gate transistor architectures

Since it was first proposed, different device architectures have been proposed for the fabrication of Double-Gate Organic Transistors (DGOTs), in order to exploit the benefits that having two gates granted to the device. In **Figure 5** are summarized the most common DG architectures. This structure involves several types of devices, ranging from the standard Organic Field Effect Transistor (OFET) architecture to the Organic Charge Modulated FET (OCMFET), the Electrolyte-Gate Field Effect Transistor (EGOFET), and even the Organic Electrochemical transistor (OECT).

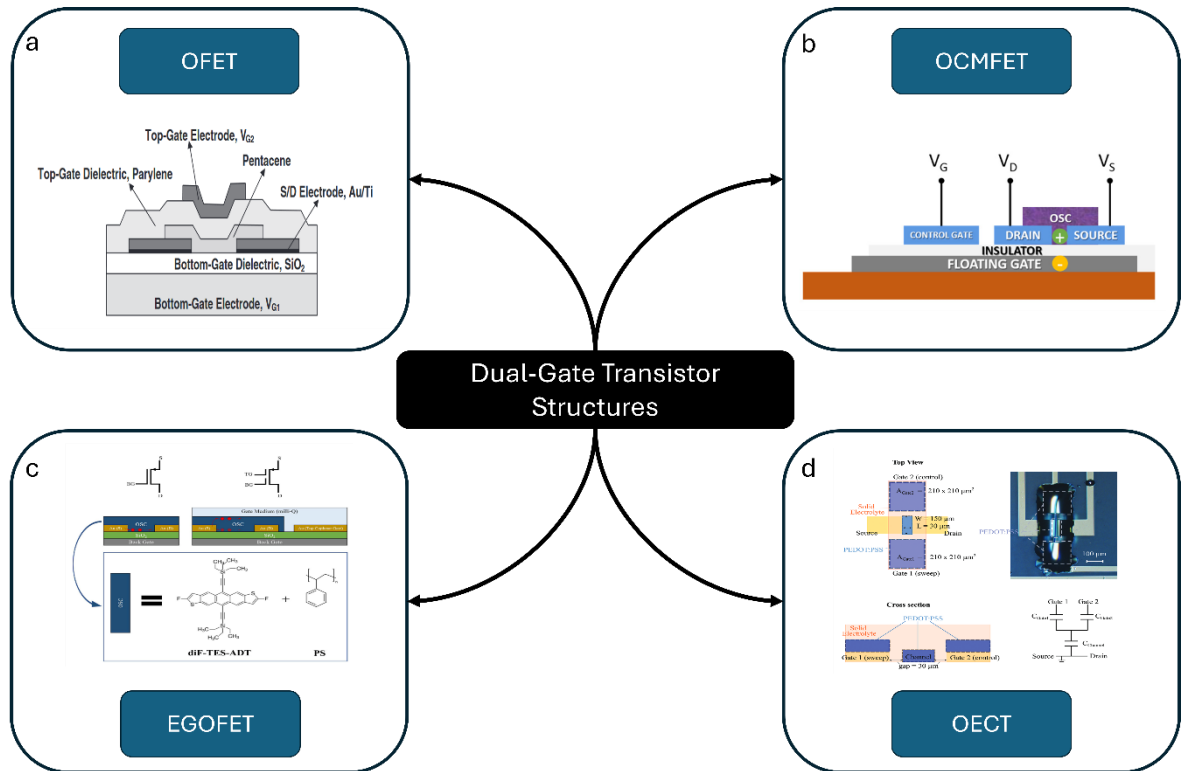


Figure 5: Different architectures for transistor with a Dual-Gate configuration: a) Dual-Gate (DG) Organic Field Effect Transistor (DG OFET), b) Organic Charge Modulated Field Effect Transistor (OCMFET), c) DG Electrolyte Gate Organic Field Effect Transistor (DG EGOFET), and d) DG Organic Electrochemical Transistor (DG OEFCT). Adapted and reproduced with permission from ref.^[78], ref.^[79], ref.^[80] and ref.^[74], respectively. Copyright (a) IOP Publishing 2007, (b) MDPI, Basel, Switzerland 2018, (c) Elsevier 2022, (d) Wiley 2022.

2.1.1 Dual-gate organic field effect transistor (DG OFET)

A common Dual-Gate architecture involves a Thin Film Transistor (TFT) with both a bottom and a top gate. In this configuration, two gates, one on the bottom and one on the top, control the flow of electrical current through a shared active layer. The top gate is typically added after the bottom gate and two dielectric layers are deposited to separate the two gates from

the active layer and from each-other. This dual-gate setup allows for more precise control over the device's electrical characteristics, since charge accumulation inside the channel can be controlled in a finer way.

Cui et al.^[76] reported the first example of a Dual-Gate Organic Field Effect Transistor (DG OFET). The device was characterized by a bottom gate-bottom contact configuration, surmounted by a second dielectric layer and a second gate on top of it. The result is a stack of materials with a total thickness of approximately 1 – 2 μm (excluding the substrate). The proposed device employs Pentacene as organic semiconductor, focused on the efficiency of the gate dielectric layer. A comparison between a thermal oxide and a self-assembled SiO_2 layer is reported with the latter that shows better results, both in an OFET configuration and employed as a top dielectric for the double-gate OFET, with 10 layers of SiO_2 . Following the same line of thought, two years later, Cui and Liang proposed a Dual-Gate device based on Pentacene semiconductor, in which the top dielectric layer was composed by a SiO_2 nanoparticle thin film^[81], which production was thoroughly described, extending the previous work on the subject. The device can be operated at relatively low voltages, with V_{DS} ranging from 0 to -10 volts and V_{GS} between 0 and -15 volts. Devices characterization shows good control from both gates, also thanks to the thin top dielectric layer. A comparison between the device in single gate configuration and its Double-Gate counterpart showed how the latter has overall better performances. The mobility is evaluated to be $0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for the device operated only from the bottom gate, $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ when characterized from both. Critically, this device architecture establishes two independent conduction channels, each controlled by its respective gate. This dual-channel configuration significantly improves the precision with which the drain current can be regulated. An investigation focused on better understanding some properties of DG OFETs was led by Iba et al^[72]. Here, they addressed directly the control of the threshold voltage of a device, using a second (top) gate. This parameter is very important, as it determines circuit functionality and yield. Although these Pentacene-based devices do not operate at extremely low voltages, they offer a wide range of operating conditions. Additionally, the threshold voltage can be adjusted over a considerable range by biasing the bottom gate and correspondingly adjusting the top gate voltage. Researchers have explored techniques to directly manipulate the threshold voltage by modifying the interface between the active layer and the dielectric. This is often done by exposing the device to UV-ozone or oxygen plasma, which introduces traps at the interface. This approach allows for precise tuning of the threshold voltage during the manufacturing process, providing designers with a starting point for circuit design. However, this method

sacrifices the dynamic tunability offered by a second gate. Once the threshold voltage is set during fabrication, it becomes fixed^[82]. Following the line of works that exploit this kind of structure, using pentacene as semiconductor^[83], Gelinck et al. suggested that the improved performance was linked to the variable threshold voltage. However, they emphasized that the formation of a top channel had a minimal impact on the mobility, due to the increased thickness of the top channel, that resulted in a field-effect mobility that was four orders of magnitude lower than the primary channel. More recent work addressed the matter, investigating the charge distribution inside the channel; what happens is that the formation of two channels occurs when the thickness of the semiconductor is higher than the accumulation width, whether, for semiconducting monolayers or very thin layers, a single channel is formed, and different effects take place in these two different situations. The study, however, further confirms that the top channel mobility is way lower, probably because of the roughness of the interface between the top part of the semiconductor and the dielectric on top of it^[84]. Despite this limitation, charge carrier distribution and control over it is more efficient in this kind of structure with respect to the single gate OTFT, and this applies also to OTFTs that employ a different organic semiconductor as active layer, as claimed by Shiwaku et al.^[85] For example, one of the first proposed organic devices with this kind of architecture, employed [9,9]-dioctylfluorene-*co*-bithiophene (F8T2), an organic copolymer, as semiconductor^[86], showcasing an increased On/Off ratio thanks to its properties, and further validate the possibility to modulate the threshold voltage. A common trait of these works is that the top conductive channel experiences degradation because of the excessive roughness of the semiconductor/dielectric interface. A solution that may resolve this aspect, comes from the fabrication of a single crystal DG OFET; a rubrene crystal grown in the channel area, tackles the roughness aspect, and has a high carrier concentration diffused in the bulk^[87]. There are also different simulative works, conducted on two different layouts, that showed that a thick semiconductor layer in a dual-gate OFET behaved better than a thin one in single gate OFET, thanks to the control that the presence of the second gate enabled over the channel^[88]. It was also demonstrated that a Self-Assembled Monolayer (SAM) of chloro 11-5-ethyl-2,2',5',2'',5'',2'',5'',2''-quinquethien-5-yl undecyl dimethylsilane can be used as organic semiconductor^[89] and further validates the fact that thickness of the active layer determines the formation of one or two channels. Double-gate transistors in a sandwiched configuration face challenges due to the semiconductor layer's thickness and the interface with the top dielectric. As the semiconductor layer thickens, the two charge transport channels become separated, requiring careful tuning. Additionally, the quality of

the dielectric material and its interface with the semiconductor significantly impact device performance. Therefore, selecting the most suitable dielectric material is crucial for optimizing device functionality^[90]. Of course, other aspects play a fundamental role in the efficiency of the device, like the contact resistance that could hinder charge transport, severely worsen device's performances^[91]. Testing two different configurations double-gate, bottom contact (BC) and top contact (TC), the result was that the BC configuration offered a better control over threshold voltage, mobility, and contact resistance and, regarding this last parameter, in TC configuration, the reduction was achieved only for negative top gate/small bottom gate voltage values, whereas in the BC the reduction was seen for all bias values. A modelling of a device based on the PDPP-TNT (small molecule OSC) compared with experimental data^[92] on that device showed that of the three possible configurations, double-gate, bottom gate and top gate, the DG mode is better than the SG and bottom control is better than top one. This behaviour was further confirmed in later, more recent works^[85,93], showing also how various conductors and semiconductors can be used for the DG OFET fabrication. Overall, this structure can be regarded as reliable and robust, also because the top dielectric and electrode, protect the active layer from fast degradation.

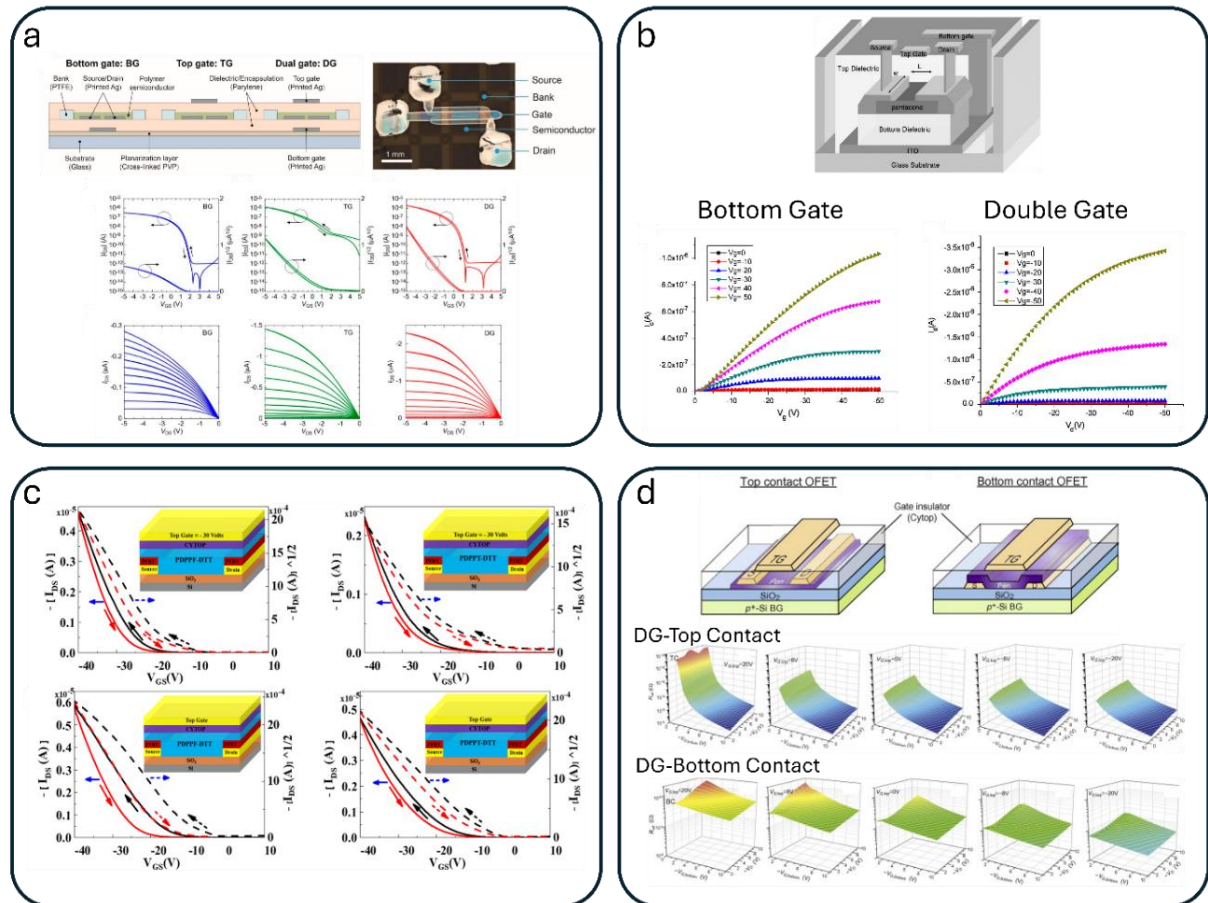


Figure 6: Dual-Gate Organic Field Effect Transistors (DG-OFETs) have been studied for tuning and optimization of the devices performances; a) R. Shiwaku developed and simulated (based on finite element method (FEM)) the Dual-Gate organic transistor behaviour, indicating that such device produces a dual-channel (due to the dual gate configuration) and thus exhibit excellent control of charge carrier density in the organic semiconducting layer leading to a better switching characteristics than the single-gate devices. Reproduced and adapted with permission from ref.^[85] Copyright MDPI, Basel, Switzerland 2018; b) Dual-Gate organic transistor showed comparable and even better performances, with respect the Single-Gate counterpart. Adapted with permission from ref.^[90]. Copyright Elsevier 2010; c) Dual-Gate architectures can be employed to enhance the organic transistor performances and stability over time by a properly device optimization. Reproduced with permission from ref.^[93]. Copyright IOP Publishing 2021; d) Dual-Gate structure can be employed to tune the contact resistance in Pentacene-based organic transistors in both Top contact and Bottom contact transistor architectures. Reproduced with permission from ref.^[91]. Copyright Elsevier 2012.

2.1.2 Organic charge modulated field effect transistor (OCMFET)

In the second half of the first decade of the 2000s, University of Cagliari proposed the Charge-Modulated Field-Effect Transistor (CMFET)^[94], a device based on a floating gate transistor in which the bias is given through the control gate while the sensing part is an exposed portion of the floating gate. Following this, a few years later the first organic CMFET was used as DNA detector^[95]. An advantage of this kind of structure is given by the possibility to keep the sensor area away from the transistor area, thus decoupling the sensing

part from the active layer. The device acts as a charge sensor; in fact, the sensing area is able to detect charge or charge distribution variation that, by varying the charge in the floating gate and thus affecting the carrier distribution inside the channel. As a result, the output current of the transistor varies according to the modulation of the threshold voltage (V_{th}), which can be summarized as follow: $\Delta V_{th} = -Q_S/C_{tot}$ where Q_S is the amount of charges coupled with the sensing area and C_{tot} represent the total capacitances of the structure (the control capacitor C_{CF} and the parasitic components due to the superposition between floating gate and the metal contacts lying on the opposite side of the dielectric layer, C_{SF} and C_{DF}).

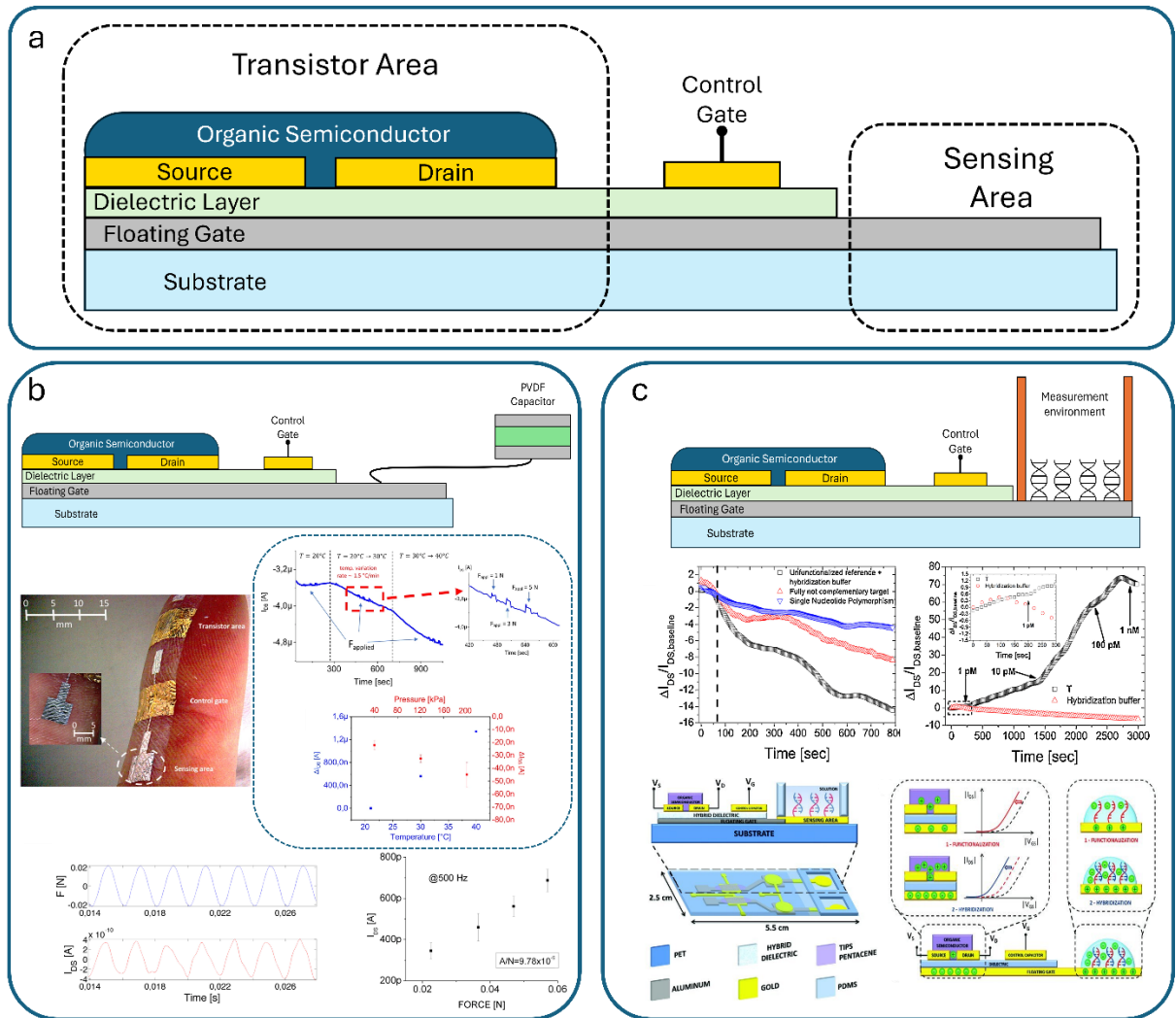


Figure 7: The Organic Charge Modulated Field Effect Transistor (OCMFET), developed at the University of Cagliari, has been employed for several sensing application; a) cross-section schematic representation of the OCMFET, with transistor and sensing areas highlighted; b) OCMFET for tactile (force/pressure and temperature sensing) applications. Adapted and reproduced with permission from ref.^[96,97]. Copyright Elsevier 2016 and Springer Nature 2018; c) OCMFET employed as DNA sensor Adapted and reproduced with permission from ref.^[98,99]. Copyright Elsevier 2016 and Wiley 2012.

The OCMFET, whose schematic representation is shown in **Figure 7**, has been originally conceived for biochemical applications^[95,100], as it allows detecting those biochemical reactions related to charge/charge distribution variations, genetic, enzymatic, immunologic activity, and pH variation, with the great advantages to be reference-less. In the last years, it has been also successfully applied as cellular interface *in vitro* for electrically-active cells^[101,102], and as a sensor for physical variables, as pressure and temperature^[96,97].

An alternative layout with the aim to enhance the device sensitivity and simultaneously decrease the overall sensor dimension was recently proposed and characterized as a multimodal tactile sensor, able to detect both temperature and force variations^[103]. Vertical organic channel field-effect transistors (OCMFETs) with a top floating gate and a bottom gate offer several advantages. They enable short-channel devices and self-encapsulate the organic semiconductor, making them suitable for low-cost production on flexible substrates. By coupling a piezoelectric and pyroelectric Polyvinylidene Fluoride (PVDF) capacitor to the vertical OCMFET, the device can function as both a pressure and temperature sensor^[103,104]. Moreover, since the vertical-OCMFET has the sensing area exposed, the PVDF capacitor can be deposited directly on top of it. Table 1 shows the main characteristics of some of these devices. In **Table 1** are reported the main parameters of the considered devices.

Table 1: In this table are reported the main results achieved for various dual-gate devices, fabricated with different techniques and materials, as well as different purposes. All works reported in this table refer to organic devices.

Paper	Mobility [cm ² V ⁻¹ s ⁻¹]	Threshold Voltage [V]	I _{ON} /I _{OFF}	Notes
[76]	0,1	-2,2	3,8 10 ³	
[77]	0,03	-2,8	5 10 ⁵	Bottom Swipe
	0,005	11,6	2,3 10 ⁴	Top Swipe
[82]	0,26	-17	//	Control
	0,39	+116		Plasma O ₂
[85]	0,05	0,42	//	
[86]	0,08	//	5 10 ⁴	
[87]	43	3		Single-Crystal Device
[90]	0,52	//	8 10 ³	
[91]	0,2	//	//	
[92]	0,98	0,2	6,2 10 ⁷	
[93]	0,098	Hysteresis not negligible	//	PDPPF-DTT
	0,031			PDPPT-DTT
[96]	0,028	2,4	5 10 ²	
[104]	//	13	//	

2.1.3 Dual-gate electrolyte-gated organic field effect transistor

Among the different transistor architectures that have been developed in the last decades, the Electrolyte-gate OFET (EGOFET) represents an interesting device widely studied in the organic electronic field, especially for biosensing applications^[105,106]. In **Figure 9a** is reported the possible solution proposed for the realization of a Double-Gate EGOFET, where the device is characterized by a standard bottom gate-bottom contact thin-film transistor architecture and a top gate immersed into an electrolytic solution, which is directly in contact with the organic semiconductor.

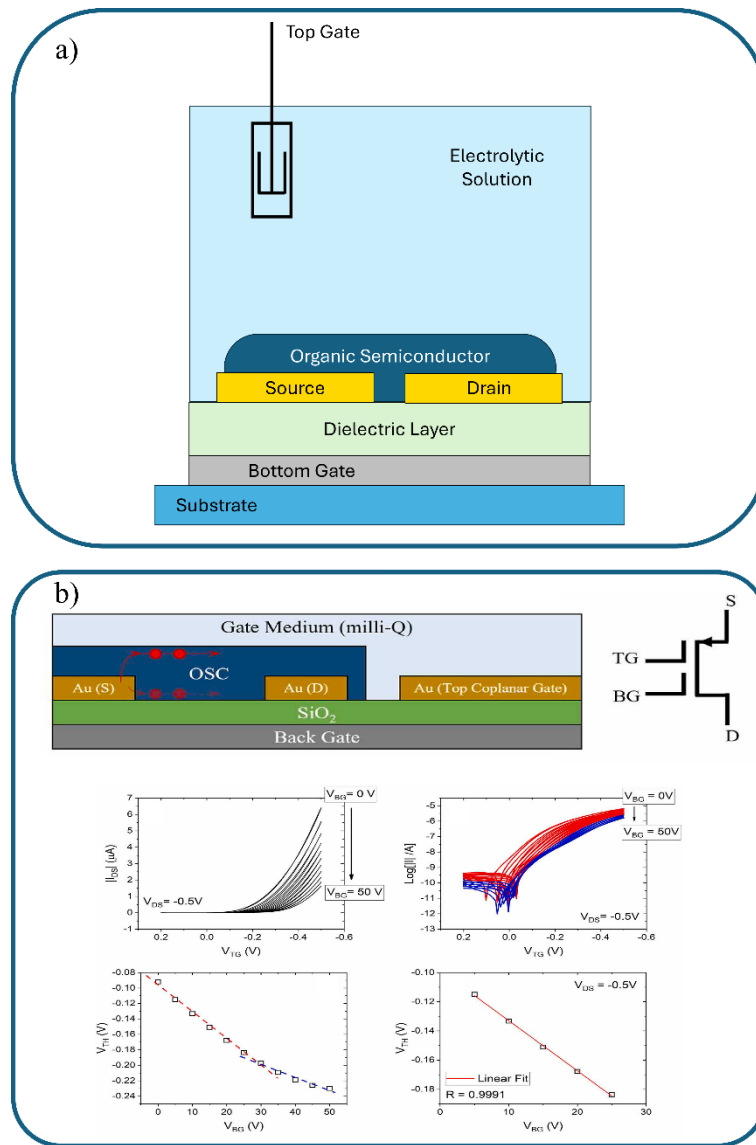


Figure 8: Schematic representation of possible architectures for the Dual-Gate Electrolyte-gated Organic Field Effect Transistor (DG-EGOFET). The addition of a second gate creates a standard bottom gate bottom contact thin film transistor architecture. Figures and graph adapted and reproduced with permission from ref.^[80]. Copyright Elsevier 2022.

Another approach in the modification of the standard EGOFET architecture, reported in **Figure 8b**, can be found in Lago et al. work^[80]. The suggested structure employs a second gate coplanar to source and drain electrodes and is completely immersed in the medium, which is directly in contact with the dielectric layer. By incorporating a second gate into an EGOFET, the ability to precisely control the threshold voltage is gained, as previously discussed for other transistor species. This is advantageous as it allows to set a specific operating point, independent of the solution's properties. This, in turn, leads to stable output signals during measurements and prevents fluctuations in the device's sensing capabilities due to varying switch-on conditions. Importantly, the dual-gate configuration doesn't necessitate a sandwich-like structure around the active area, reducing the risk of short circuits.

A few years prior to Lago et al. work, the same dual-gate configuration design was developed by Zhang et al.^[107]. The authors investigated a dual-gate configuration for both EGOFETs and OECTs, creating a hybrid liquid-solid device. By incorporating a second gate at the base, since the top one is intrinsic in the structure, they aimed to precisely control the threshold voltage and enhance device performance. This approach also expanded the material compatibility for such applications. Both structures can be effectively modelled using existing dual-gate transistor models.

2.1.4 Dual-gate organic electrochemical transistor

Within the realm of field-effect devices, Organic Electrochemical Transistors (OECTs) emerge as a compelling solution for developing organic devices specifically designed for sensing and biosensing applications. Although their electrical behaviour resembles that of conventional organic transistors, OECTs operate on a distinct principle. The flow of current in OECTs is governed by the exchange of ions between an electrolyte and the organic conductor channel. Therefore, the device output current is controlled by the doping level of a conducting polymer using an electrolyte solution^[108,109]. Among the possible OECT device configurations, the Dual-Gate architecture represents an interesting solution for tuning the device properties. Also in this case, by adding a fourth terminal it is possible to finely tune the transistor characteristics.

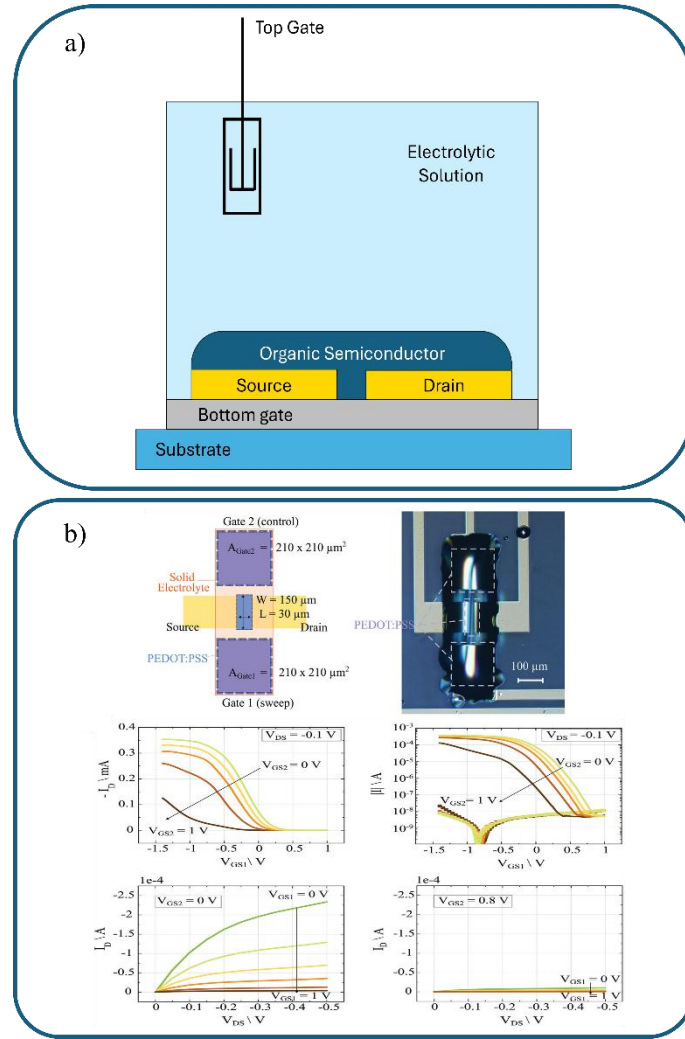


Figure 9: Schematic representation of a possible architecture for the Dual-Gate Organic Electrochemical Transistor (DG-OECT). The addition of a second gate creates a standard bottom gate bottom contact thin film transistor architecture. Figures and graphs adapted and reproduced with permission from ref.^[74]. Copyright Wiley 2022.

With this intent, J. Ji et al.^[110] developed a dual-liquid-gated OECT with the aim to optimize the transistor electrical characteristics after the device fabrication. The authors developed a planar dual-gate device, which allows an easier fabrication process with respect the standard OECT architecture, and, moreover, developed a mathematical model to demonstrate the device functioning system. The Dual-Gate OECT architecture can be employed even for sensing applications. Y. Song et al.^[111] compared the performances between a single and dual gate OECT as a bio-sensing device, showing that the DG-OECT can erase the drifts of the current along the experiment, and also it is able to increase the accuracy of antibody-antigen interaction detection, and further decrease or eliminate the effect of ions in the buffer solution. Similarly, J. Harris and co-authors implemented a floating gate OECT architecture as a platform for yeast sensing for several filed of applications^[112]. The proposed device has a dual-gate architecture, where one gate is used as a control gate to set the biasing of the

device, whereas the other floating (and functionalized) gate is used as sensing element of the transistor for bio-impedance-based measurements. S-E Wu et al. presented another DG-OECT architecture^[113] as a sensing device for monitoring seawater's dissolved oxygen concentration. Particularly, the authors demonstrated that the dual-gate configuration is able to extend the sensor operating voltage window and improves device stability, while simultaneously improving the device robustness even in harsh environments and scenarios such as the seawater.

Bio-hybrid artificial synapses for human-machine applications represent an interesting research field that has recently gained attention. Among the different type of devices that can be used in such a field, OECTs represents an interesting solution for such a problem and the Dual-Gate configuration can be implemented to improve the device performances. Q. Xu and co-authors implemented a fully printed OECT as an artificial synapse. The device showed not only good reproducibility and stability over time, but also the capability to have a short-term plasticity dominated by sodium ionic dynamic and also a dopamine-mediated long-term plasticity. Moreover, thanks to the DG configuration, the device was able to mimic multiple presynaptic dopamine stimulations, which is important since a postsynaptic membrane is usually affected by multiple presynaptic stimulations^[114].

2.2 Dual-gate transistors application

The dual-gate transistor architecture presents a versatile platform for the design of digital, analogic, and sensor circuits, with particular relevance to wearable electronics. Initially, this architecture was intensively investigated and developed for digital circuit design, specifically as a fundamental building block for logic gates, thanks to its robustness and versatility. The additional gate terminal offers precise control over the device's threshold voltage, enabling enhanced performance, reduced power consumption, and improved circuit density.

More recently, dual-gate transistors, including Organic Field-Effect Transistors (OFETs), Electrolyte-Gated Organic Field-Effect Transistors (EGOFETs), and Organic Electrochemical Transistors (OECTs), have been increasingly utilized for various sensing applications. The dual-gate configuration allows for independent tuning of the device's electrical characteristics, enabling enhanced sensitivity, selectivity, and dynamic range. This flexibility has led to the development of a wide range of sensors, including chemical sensors, biosensors, and environmental sensors.

2.2.1 Logic and inverter

Logic operations are the base of circuitry. Since its first proposition, double-gate devices were employed in this regard^[115]; this work presented the typical DG structure with polymers to obtain smoother surfaces and avoid degradation of top conduction channel. One of the first application of the double-gate organic transistor came in 2007 by Koo et al.^[77] What was proposed here, as shown in **Figure 10a**, was a new type of inverter in which the double gate was employed to compensate the chemical degradation of the organic transistor.

The researchers fabricated two inverter configurations for comparison: one with both driver and load transistors as single-gate devices, and another with only the driver transistor as a dual-gate device. While acknowledging the increased complexity of dual-gate fabrication, they highlight the significant improvement in controllability it offers. They suggest that a device with both driver and load transistors as dual-gate devices would be the ideal solution for achieving full control over the system. Additionally, they emphasize the role of the top dielectric and electrode layers in enhancing the device's overall durability^[78]. A fundamental factor to consider when evaluating the goodness of an inverter is the noise margin; this parameter, as noted by Spijkman et al., can be optimized using the top gate to tune the

threshold voltage as needed^[116]. Results of this experiment, led to enhancements in the noise margin from 1 V to about 5 V. Speaking about logic, analog-to-digital converters (ADC) have also been investigated, with improvement in gain and input capacitance owed to the DG structure^[117]. The efficiency of DG applied to inverter technology was further confirmed by Kumar et al.; comparing SG versus DG transistor-based inverter circuits, they showed better performances in terms of mobility, I_{ON}/I_{OFF} and subthreshold slope as well as an increase in both noise margin and gain that varies respectively by 8% to 19% and 18% to 26%, depending on the inverter configuration used^[118]. Other logic operations have been explored, employing the DG structure, such as NAND and NOR, with the comparison between diode-load logic (DLL) and zero- V_{gs} -load logic^[119]. To improve the gain, a good amplifier is needed, and DG proved to be efficient in this, thanks to its versatility and ease of control^[120]. Over the years, many groups investigated the possibility to use organic DG transistors for the realization of inverters or logic circuits addressing their research to logic operations^{[121],[122]}, or trying to fabricate an inverter through inkjet printing^{[123],[124]}. In **Figure 10b** and **Figure 10c** are reported some recent examples of double gate organic transistor employed for the design of logic circuit.

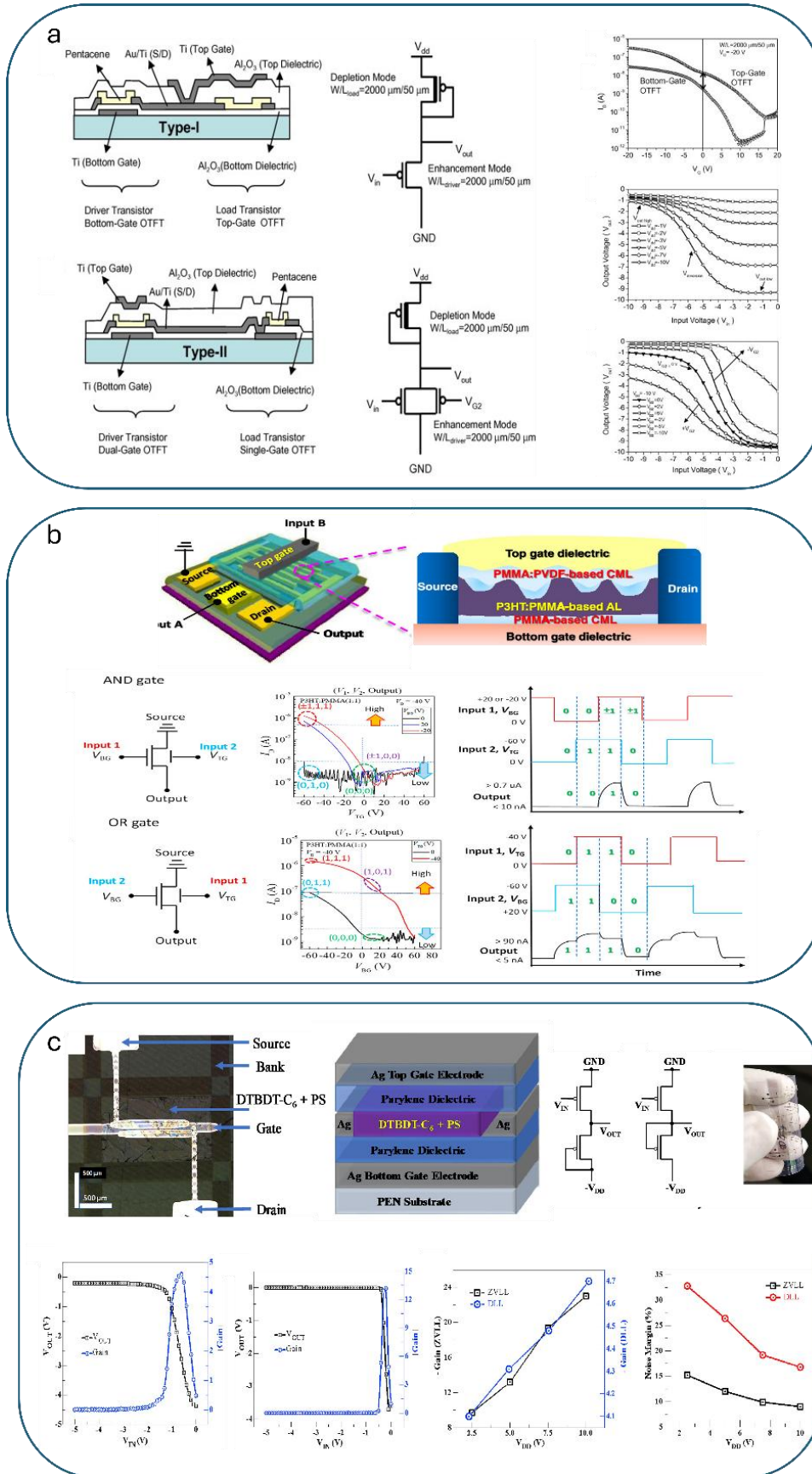


Figure 10: Dual-Gate organic transistors have been employed, as first example of such device applications, for the development of logic circuits. A) The schematic cross-sectional structures, bias configuration and output characteristics reported with permission from ref.^[77]. Copyright 2007

Elsevier; B) Schematic representation and cross-section structure of the Dual Gate Organic transistor developed by B-R Lin et al. using a semiconducting/insulating polyblend-based active layer with asymmetric top and bottom charge modulation layers (atb-CMLs). AND gate and OR gate characteristics are presented as well. Reported with permission from ref.^[121]. Copyright 2020 American Chemical Society. C) Printed Dual-Gate Organic transistor for PMOS inverters developed by S. Singh et al. with the aim to enhance the inverter characteristic by controlling the device threshold voltage. Reported with permission from ref.^[123]. Copyright 2020 Elsevier.

2.2.2 Radio-frequency identification (RFID)

Radio-Frequency Identification (**RFID**) is a technology widely and daily used. **SIM** (*Subscriber Identity Module*) cards and credit cards, for example, can be found in almost every pocket, making this technology pervasive. Its diffusion is thanks to its consolidated fabrication processes in inorganic field^[125], and having a wide range of applications, it is only natural that research is now moving toward technologies that allow a cost/area efficient manufacturing process. Organic electronic, in principle, has many advantages that suite well the production of these devices, and some exploited it for the fabrication of such devices. Good results were obtained in the fabrication of a 64-bit RFID tag^[126] in a single gate configuration, replicated later in a configuration in which both load and drive transistors are built as more robust double-gate^[127,128]. Recently, insights on the application of DG to RFID investigated two configurations of the inverter and simulated a possible RFID system, with the important conclusion that post fabrication tunability can allow to optimize various characteristics of the device^[129]. In **Table 2** are summarized the results obtained for various applications of the double-gate structure in this field of research.

Table 2: Here are reported the main results obtained for various devices employed for the realization of circuits, inverters and logic.

Paper	Mobility [cm ² V ⁻¹ s ⁻¹]	Threshold Voltage [V]	I _{ON} /I _{OFF}	Notes
[115]	5 10 ⁻⁴	//	//	
[78]	0,01 0,03	0,6 1,1	2,3 10 ⁴ 3,9 10 ⁴	Bottom Gate Top Gate
[116]	1,9 10 ⁻³	-2,6	//	
[118]	0,1	-2,2	3,8 10 ³	Inverter in DLL and ZVLL
[120]	0,1	-0,069 to -2,58	//	Low voltage inverter, max gain 29,3 dB
[122]	(h) 4,6 ± 2,1 10 ⁻² (e) 1,3 ± 0,7 10 ⁻¹	-3,1 ± 0,4 4,2 ± 0,9	//	AntiAmbipolar Transistor

[123]	0,37 ± 0,02	0,23	~10 ⁷	PMOS inverter, max gain 23 dB
[124]	0,43	0,25	~10 ⁸	DLL PMOS inverter
[127]	0,15	//	//	

2.2.3 Dual-gate transistor for biosensing applications

A transistor-based biosensor is a device in which the sensing activity is done by biological components in the sensitive layer. Organic transistors are widely used in the field of sensing, from EGOFETs to OECTs, thanks to the wide variety of materials, large area production and flexibility. History of biosensors starts at the beginning of the 1960s when scientist Leland C. Clark developed the enzyme electrode^[130,131], and starting that moment, research in this field received a boost. In 1970 was developed the first ISFET (Ion-sensitive Field-Effect Transistor), presented by P. Bergveld^[132] but the frontier of using double gated devices for these applications is only recently gaining interest. Taking an ISFET as a reference, in 2010 Spijkman et al. proposed a DG transducer that could help in overcoming some critical issues linked to organic electronics in aqueous environment^[133]. The primary limitations of this approach are Faradaic leakage and hysteresis, which can compromise the stability and reproducibility necessary for reliable sensing. To mitigate these issues, careful adjustments must be made. Direct contact between the electrode, semiconductor, and water must be avoided to prevent electrolysis. The detection mechanism relies on the shift in threshold voltage, which is influenced by the ratio of dielectric capacitances and the top gate dielectric surface potential. By adjusting this capacitance ratio, the sensitivity of the device can be tuned. However, the small Debye length in physiological solutions poses a significant challenge. To address the degradation of the active layer in aqueous environments, an alternative approach involves relocating the sensing area by extending the top gate. This configuration can potentially improve the device's stability and long-term performance^[134]. Given their versatility and the constant need of reliable biosensors, DGs have been tested also as Ph sensors^{[135],[136]}. A different approach proposed recently by Jouharchi et al. and then by S. K. Jain and A. M. Joshi starts from the usual DGOTFT with a little tweak in the structure; both dielectric layers are mixed, that is a part of the dielectric is an air gap in which biomolecules get trapped^{[137],[138]}. When a molecule is captured by the sensor, its recognition is typically based on one or two parameters: dielectric constant for neutral molecules, and dielectric constant and charge density for charged molecules. The variation in drain current serves as a measure of the device's sensitivity, which is maximized when the entire sensing

area is filled with the target molecule. This label-free sensing configuration offers increased sensitivity and could serve as a foundation for developing flexible and biocompatible biosensors. Theoretically, any transistor architecture can be adapted to a dual-gate configuration. For example, as previously reported, an electrolyte-gated organic field-effect transistor (EGOFET) can be modified by adding a second gate to fine-tune the operating point and optimize sensitivity^[139]. Given the increasing interest in wearable biosensors, the development of flexible and easily producible device configurations is crucial. Printing techniques are considered a promising approach to achieve these goals. Recently, Baek et al. demonstrated a fully printed dual-gate device with functionalized gates, representing a significant step towards practical wearable biosensors.^[140]

Figure 11a shows how, using a functionalized gate coupled with a DG TFT, operating in the subthreshold voltage can help obtain a higher sensitivity at lower power consumption. One advantage of this kind of device is the possibility to realize it with a quick and scalable process like inkjet printing. This technique, as all printing techniques, is very suitable for the realization of large area, flexible devices. In **Figure 11b** is reported a Dual-gate architecture in which the sensing signal is transduced and amplified by the capacitive coupling between a low- k bottom dielectric and a high- k ionic elastomer top dielectric that is in contact with an analyte solution. This design, as reported in the graphs, exhibits a high signal amplification, high stability under bias stress in various aqueous environments, and a low signal drift, which is a fundamental characteristic for biosensing applications. In **Table 3** is presented a summary of different works that applied the dual-gate structure with relevant results.

Table 3: Reported here are works with interesting results obtained for the biosensing using dual-gate transistors.

Paper	Mobility [cm ² V ⁻¹ s ⁻¹]	Threshold Voltage [V]	I _{ON} /I _{OFF}	Sensitivity	Notes
[133]	10 ⁻³	//	//	$\Delta V_{th} =$ (C _{top} /C _{bottom}) · 58 mV per pH unit	pH Sensor
[134]	//	//	//	0÷10 µg/mL	Immunosensor
[135]	2,2 ± 0,4 10 ⁻²	4,0 ± 1,6	//	-41 ± 7 mV per pH unit	pH Sensor
[138]	//	//	//	15,61	Label-free biosensor
[139]	1				Dual-gate EGOFET
[140]	//	-0,32	//	0,77 a 10 nW	

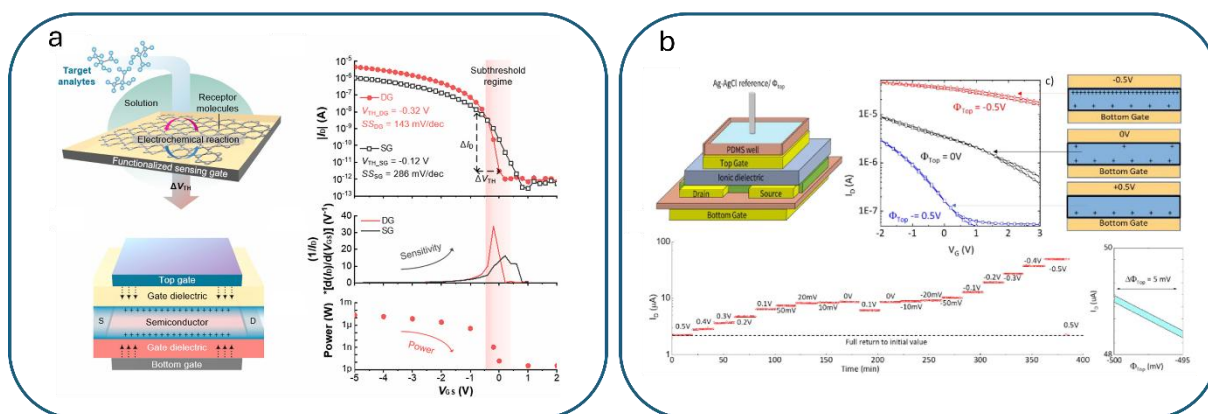


Figure 11: Dual-Gate organic transistors for biosensing applications. (a) Schematic diagram of the sensing gate functionalized with various receptor molecules, transfer characteristics, and relative current change under V_{GS} variation ($1/I_D[d(I_D)/d(V_{GS})]$ extracted from the transfer curves as a function of V_{GS} . Moreover, the measured power consumption as a function of V_{GS} is reported. Reported with permission from ref.^[140]. Copyright 2022 Elsevier. (b) Schematic representation of the architecture and operation of a dual-gate transistor with ionic top dielectric; transfer characteristics of the bottom channel for different top gate voltages, extended stability test of the dual-gate transistor's response to a potential applied at the top interface and limit of resolution of such structure. Reported with permission from ref.^[139]. Copyright 2020 American Chemical Society.

2.2.4 Dual-gate transistor for tactile application

Tactile sensing is one of the most interesting arguments of research in the recent years. Strictly connected to the artificial skin for biomedical and robotic applications, the aim of this branch of research is to mimic, as well as possible, the properties of human skin. The sense of touch, both in the hands but also in the rest of the body, is one of the main instruments with which we experience the world that surrounds us and thus is very important in every aspect of life, from the simpler tasks to the more complicated ones. Tactile sensors based on transistors started to arise in the late '80s/early '90s, with arrays of MOSFET paired with piezoelectric materials^{[141],[142]}. Over a decade later, the first flexible pressure sensor integrated with an OFET was presented by Someya^[143]; starting from this ground-breaking work and thanks to the characteristics of the organic materials employed, tactile devices based on organic transistor structures become to mimic not only skin functionalities but also mechanical properties, such as flexibility and stretchability. Double gate structure has only recently been explored to be used as a pressure sensor with a piezoelectric material as dielectric layer between active layer and top gate^[144]. In this case, transistor and capacitor are fabricated separately and then integrated in a single device in which both gates can control a part of it. The same structure, with different materials and fabrication process was

then used and verified as an effective pressure sensor, in which, during operation, the transfer curve shifted whenever pressure was applied^[145]. **Figure 12a** shows the device structure and the characteristics as a function of the top gate voltage variations. Moreover, the device response can be tuned depending on the applied top gate voltage. As stated before, the OCMFET can be used as a tactile sensor, by coupling one of the two gate (i.e. the floating) with a pyro/piezoelectric materials able to detect temperature and force variations^[103].

Concas et al. employed, for the same objective, the Double-Gate OTFT configuration, with good result also on the stability and reliability side, effectively demonstrating how the top gate acts as a charge sensor^[146]. Here the authors developed a DG organic transistor where the top gate, together with the top dielectric layer, made in Parylene C, act as auto-encapsulating structure, thus improving the device stability and robustness over time. Specifically, such an approach allows to create a barrier able to limit the diffusion of oxidizing species (particularly oxygen and water due to their strong presence in the environment) that could penetrate the semiconductor, causing its degradation. Moreover, by coupling the device with a pyro/piezoelectric material (namely PVDF), the authors demonstrated the possibility of employing the DG structure for multimodal temperature and force sensing detection. The plot in **Figure 12b** is direct evidence of this; through a PVDF capacitor, properly connected to the sensing area, the device can sense the induced charge directly related to the applied stimuli. The higher the force, the higher the variation of current inside the channel. The device was also tested as a temperature sensor, with a similar approach, obtaining good results. **Table 4** reports various results from different works that used the double-gate transistor approach for sensing.

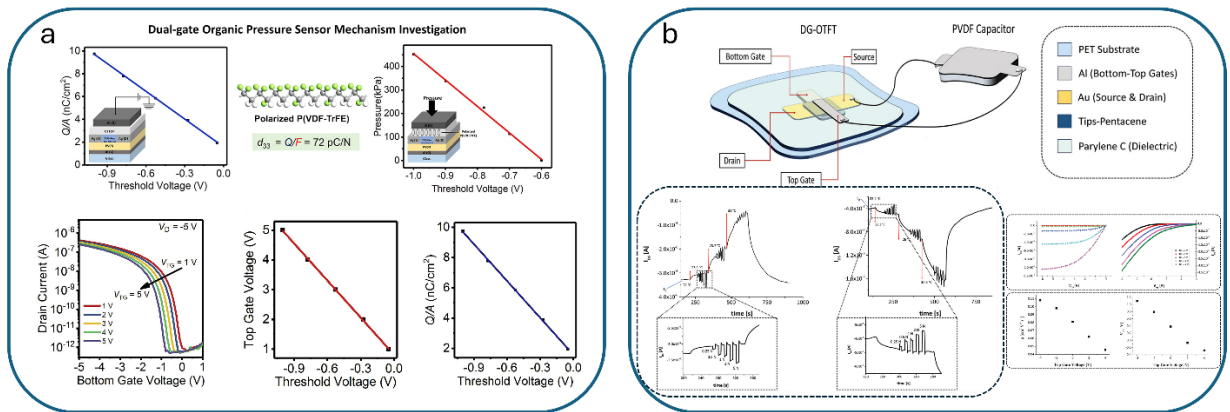


Figure 12: Dual-Gate Organic transistors for tactile applications. a) Piezoresistive-based Dual-Gate Organic Transistor for pressure sensing; The employment of the Top Gate can enhance the device sensitivity and response. Reproduced with permission from ref.^[145]. Copyright 2019 Elsevier. b) Dual-Gate Organic Transistor coupled with a PVDF capacitor capable to sense simultaneously both temperature and force stimuli. Reproduced with permission from ref.^[146]. Copyright 2024 Wiley.

Table 4: In this table are reported the results obtained in various work in which the dual-gate structure was employed for the sensing of mechanical quantities.

Paper	Mobility [cm ² V ⁻¹ s ⁻¹]	Threshold Voltage [V]	I _{ON} /I _{OFF}	Sensitivity	Notes
[103]	//	//	//	Max: 990 nA °C ⁻¹ Max: 194 nA N ⁻¹	Temperature and pressure sensor
[143]	0,2	//	10 ⁵	//	Pressure sensor
[144]	0,27	-0,8	5,1 10 ⁴	ΔI/I = 155 for 300 kPa	Pressure sensor
[145]	0,8	0,18	1,1 10 ⁶	//	Pressure sensor
[146]	2,3 ± 0,5 10 ⁻¹	7,5 ± 3,2 10 ⁻¹	//	Max: 442 nA °C ⁻¹ Max: 241 nA N ⁻¹	Temperature and pressure sensor

2.2.5 Dual-gate light related devices

Light emitting diodes are a fundamental part of modern technology. From simple lights to complex displays, LEDs can be found almost anywhere. The first device of such kind was proposed in 1928 by O. V. Lossev^[147]. However, the device suffered from low efficiency due to the limited photon emission rate of the semiconductor material used. Decades later, at the beginning of the '60s, the first LED in the visible spectrum was reported^[148] and, in the span of a decade, LED were commercially available and affordable. Light emitting properties of organic materials were effectively demonstrated at the beginning of the 1950s and, in time, various groups made discoveries and inventions related to it^[149,150]. By the end of the 1980s, the first usable organic light-emitting diode (OLED) was developed^[151] and, in 2003, the organic light-emitting transistor (OLET) was presented by two separated groups using two different configurations^{[152][153]}. Several limitations must be addressed when developing such a device. To enable light emission, a p-n junction is required to facilitate recombination. This necessitates biasing the semiconductor to accumulate different charge carriers within a specific recombination region. A possible solution to the problem comes with the addition of a second gate to the transistor structure, although, as stated by Roelofs et al.^[154], one has to find a trade-off between the thickness of the semiconductor and the biasing of the device.

An attempt in the realization of a double gate organic light emitting transistor is the one reported previously^[155] and shown in **Figure 13**, in which each gate controls a portion of the active layer, through an electrolyte serving as a dielectric, effectively forming a p-n junction; the issue to be resolved here is posed by the fabrication process as well as stability, with the emission intensity greatly decreased in two hours. As well as emitting light, semiconductors can also absorb it to generate carriers (e^- - h) and thus, a transistor can be used as a photosensor. Transistors offer an advantage over diodes by eliminating the need for external circuitry to amplify the received signal, since a transistor is intrinsically an amplifier. A double-gate structure further improves performances by reducing noise, as previously reported, and enhancing photosensitivity through top-gate voltage tuning. Additionally, the superior performance of double-gate transistors enables their integration with OLEDs for both light generation and detection^[156].

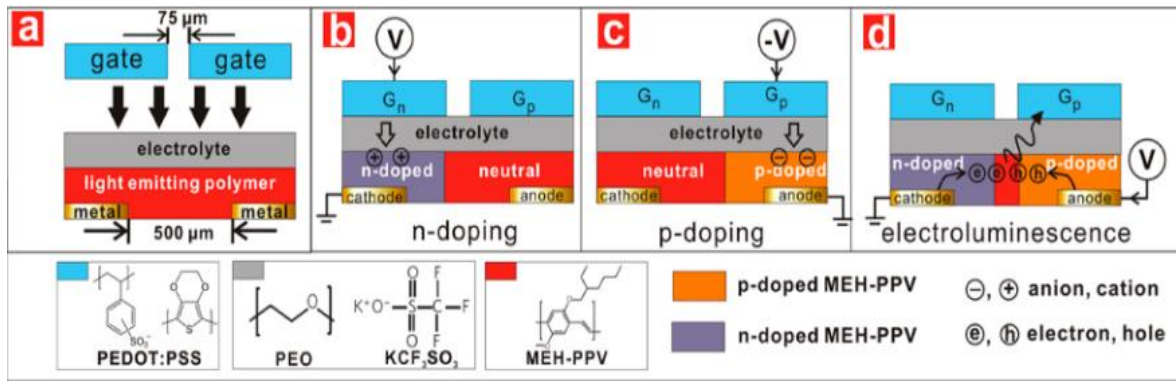


Figure 13: Materials, structure, and operation modes for Double Gate Light-Emitting Electrochemical Transistor (DG-LECT): a) Device structure; b) n-Doping mode; c) p-Doping mode; d) EL mode.

3. Chapter III: Materials and methods

During this thesis work, different materials and methods were employed for the fabrication of the devices. Materials are both organic and inorganic: gold (Au) and aluminium (Al) are used for the electrodes while carbon-based molecules compose the semiconductors, the active layer of the devices. Methods used are thermal evaporation, chemical vapor deposition, inkjet printing, photolithography, drop-casting, and spin-coating. Combining these materials and methods, a large number of devices could be produced in a relatively short period of time.

3.1 Materials

The only requirement for a device to be considered as part of the organic electronics family is that the active layer must be realized with an organic material. This means that every other component of the device can be a metal, or a plastic or any kind of inorganic material that fits the need for the designed architecture. On the other hand, partially or fully organic devices are also possible, from the electrodes^[157] to the dielectric layer^[158]. Organic conducting materials, such for example PEDOT:PSS^[159], are widely used for the realization of printed devices. This is due to the fact that most of the organic materials are solution processable, meaning that they can be used in liquid phase and then the solvent is left to evaporate at room temperature or with heat on hot plates or ovens. In this section are described the materials used in the fabrication of the devices employed in the thesis, with the semiconductor as the only organic material used, at least at the moment.

3.1.1 Aluminium

Aluminium (Al) is a metal of the 13th group with a great affinity with Oxygen (O), characteristic that allows it to form a layer of oxide, therefore a natural dielectric layer. This layer can be advantageous when using this material for the gate electrode of a transistor because it permits to have a thinner dielectric deposited on top of it, enhancing the field effect efficiency. It can be used for flexible devices because, for thicknesses in the range of a few tens of nanometres, it can be bent without cracking it.

3.1.2 Gold

Gold (Au) is a metal of the 11th group and one of the least reactive elements. Thanks to its Fermi level, it is one of the most commonly employed materials for the fabrication of source and drain electrodes in organic electronics. This is because HOMO or LUMO of the organic

semiconductors are very close to the Fermi level of Gold. Moreover, Gold does not oxidize, meaning that it is very stable in air and contact resistance does not vary due to modification to the interface structure between Source/Drain electrodes and semiconductor.

3.1.3 Parylene C

Parylene C, which dimer form is shown in **Figure 14**, is a parylene derivative in which one hydrogen atom is replaced by chlorine inside the aryl ring. It is considered a green polymer as it does not require any initiator for its polymerization process. It is widely used due to the low cost of its precursor, and it offers good properties as a dielectric and as a barrier from external agents such as water or oxygen. Being very easy to deposit, the only downside for many applications is its insolubility in any solvent at room temperature, making it impossible to remove and redo the layer in case of a bad deposition. It has insulating properties, and, in this thesis, it is used as dielectric to separate the electrodes that compose the devices^[160].

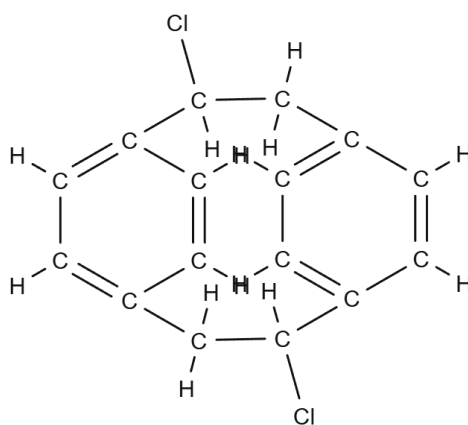


Figure 14: Molecular structure of Parylene C; a chlorine atom (Cl) is substituted to a hydrogen one (H) in the aromatic ring.

3.1.4 TIPS-Pentacene

6,13-bis(triisopropylsilyl)ethynylpentacene, also known as TIPS-Pentacene^[161] is a polymeric organic p-type semiconductor with mobility up to $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Widely used in OFET applications, it is a solution processable material, which makes it interesting for low-cost and large area fabrication processes. Stable in air and ambient conditions, it can be deposited through drop casting technique as it requires low temperatures for proper drying and crystal formation. **Figure 15** shows its molecular structure.

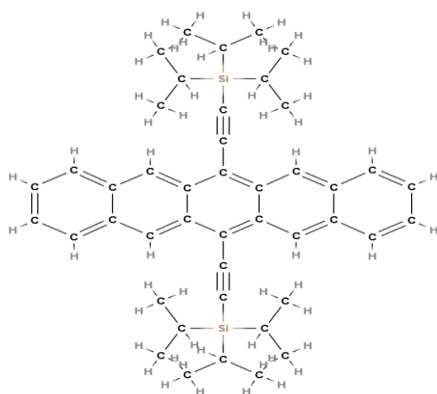


Figure 15: Molecular structure of TIPS-Pentacene, a conductive polymer widely used in semiconductor applications.

3.1.5 N1400

N,N'-bis-(2-ethylhexyl)-1,7-dicyanoperylene-3,4:9,10-bis(dicarboximide) derivative (N1400^[34]) is an n-type semiconductor. It is one of the few solution processable n-type organic molecules that has demonstrated air stability. Deposited through spin-coating technique, it is positioned off-centred with respect to the rotating plate to give the crystal growth a preferential direction. It needs temperatures close to 90 °C for proper drying and crystal formation.

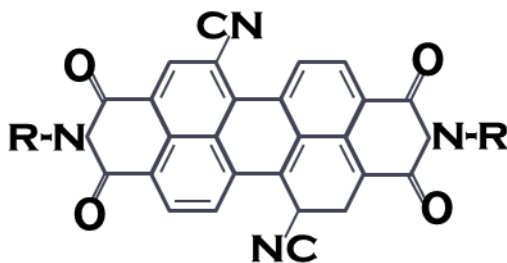


Figure 16: Molecular structure of N1400. A small molecule, solution processable semiconductor with good mobilities and thermal stability.

3.1.6 DPP-DTT

Poly[2,5-(2-octyldodecyl)-3,6-diketopyrrolopyrrole-alt-5,5'-(2,5-di(thien-2-yl)thieno [3,2-b]thiophene)], also known as DPP-DTT^[162] or PDPP2T-TT-OD, which molecular structure is shown in **Figure 17**, is a high mobility p-type semiconductive polymer, suitable for OFETs and sensing. Solution processable, can be deposited both via drop-casting and spin-coating, yielding different results in terms of mobility and thickness. Curing temperature is around 80 – 90 °C, but it can withstand higher temperatures without risk of degrading its properties. Both spin-coating and drop-casting are suitable techniques for its deposition.

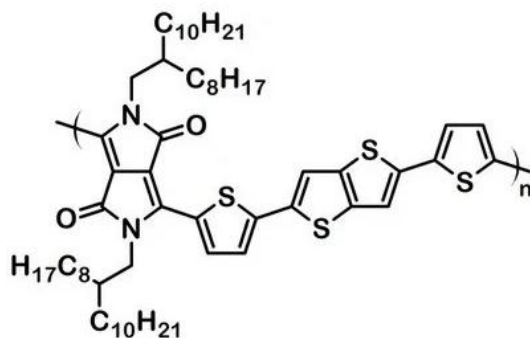


Figure 17: Molecular structure of DPP-DTT. It is a p-type polymer with high mobilities.

3.1.7 PVDF

Polyvinylidene difluoride, known as PVDF^[163], is produced by the polymerization of vinylidene difluoride. It is a highly non-reactive thermoplastic, with chemical formula $(C_2H_2F_2)_n$. It is a material that possesses both piezoelectric and pyroelectric properties, making it very useful for a variety of applications, like sensing or power supply. Its electric properties are obtained by mechanically stretching the material and poling it under tension. PVDF used in this thesis was a commercially available one, from Measurement Specialties Inc.-MEAS, and it was used for the fabrication of capacitors.

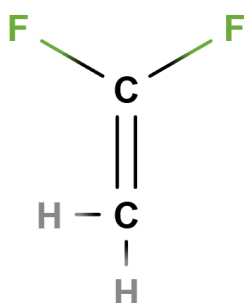


Figure 18: Molecular structure of PVDF, a thermoplastic fluoropolymer, useful for applications like sensors or batteries.

3.1.8 PDMS

Polydimethylsiloxane (PDMS), is a silicone polymer, used in various fields. Its chemical formula is $CH_3[Si(CH_3)_2O]_nSi(CH_3)_3$ with $[Si(CH_3)_2O]_n$ as repeating monomer unit. It is realized by combining two precursors in different quantities, a base and a curing agent. Depending on the hardness required for a determined application, proportion of the two varies. However, over a certain proportion of curing part, the material loses its elastic properties and becomes brittle. It is optically clear, making suitable for various applications, like lenses. In this thesis, it was prepared in a proportion of 1/10 curing/base, and used in the

setup for mechanical force characterization, as it will be better explained in the relative chapter^[164].

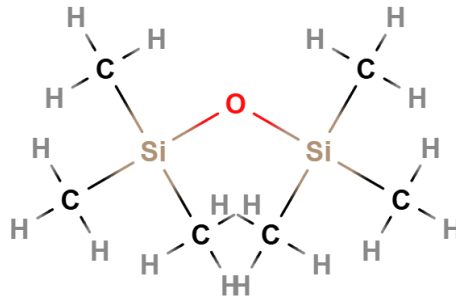


Figure 19: Molecular structure of PDMS. It is employed in various applications, like contact lenses, lubricant or food additive.

3.1.9 Photoresist

Photoresist is a material sensitive to light used in photolithography. During this thesis, photoresist used was a positive tone one, the AZ1518 from Merck. Positive photoresist means that UV light weakens the material, making it soluble in its developer. This is useful for patterning, as masks with the desired pattern, can be employed to transfer such pattern on a substrate, with a high-definition process as unexposed parts remain insoluble in the developer.

3.2 Methods

Methods employed depend on the kind of material chosen for a determined part of the device. If the material is solid, then thermal evaporation or chemical vapor deposition are needed, while if the material is already liquid or can be solubilized, then inkjet printing, spin-coating or drop-casting can be exploited for the fabrication.

3.2.1 Thermal evaporation

Thermal evaporation is a process that substantially relies on two phenomena: Joule effect and high vacuum. A crucible, made of material with a high melting point, is attached to electrodes; a potential is applied to them, current will flow, and the crucible will heat. Tungsten (W) with its melting point at 3422 °C, is a standard material for crucibles, since its melting point is higher than the vaporization points of many common metals used in electronic devices, such as Aluminium (boiling point at 2470 °C) or Gold (boiling point at 2970 °C). In the process, heat is transferred to the source material that, with a lower melting point and evaporation point, will vaporize. The material particles will then travel toward the substrate, and we'll have a film growth of the desired material. The whole process has to be conducted in a high vacuum condition, for two reasons, both related to the presence of particles inside the chamber. Collisions with particles are undesirable because thermal evaporation is a highly directional deposition technique. When in pressure conditions as low as $10^{-5} - 10^{-6}$ Torr, equivalent to $10^{-8} - 10^{-8}$ bar, average travel length or mean free path of the material particles is, usually, bigger than the chamber dimensions. This means that such particles travel in a straight line from the crucible to the substrate. This means that any collision that happens inside the chamber, modifies the travel direction, reducing the quantity of particles that arrive to the substrate, to participate in the film growth. Moreover, if there is a high presence of particles different from the source material, there could be impurities and thus contamination of the deposited film, leading to a lower overall quality. Oxygen and moisture are particularly obnoxious, especially with reactive materials like aluminium or silver. A schematic of what happens inside the vacuum chamber of a thermal evaporator is presented in **Figure 20**.

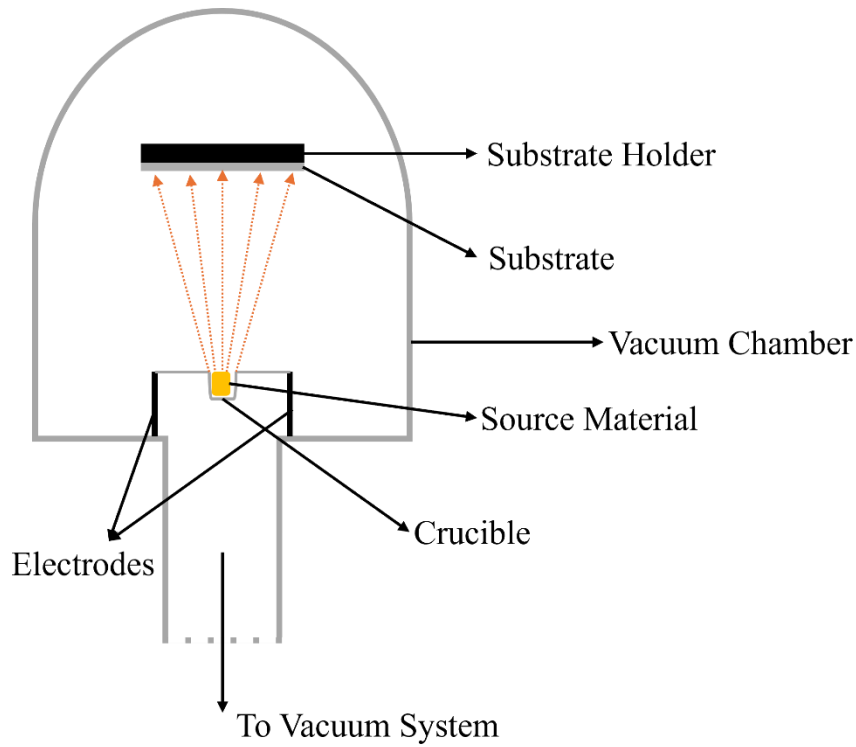


Figure 20: Schematic of a thermal evaporation chamber, with all its elements, during an evaporation process.

3.2.2 Chemical vapor deposition (CVD)

Chemical Vapor Deposition (CVD) is a vacuum deposition technique through which it is possible to realize thin films, usually with sub-micrometres thicknesses, of high quality and high performances. This technique is used to fabricate the dielectric layer of the devices that are the core of this thesis. Specifically, an instrument called SCS PDS 2010 Labocoter 3 (**Figure 21a**) is used to deposit the Parylene C through a low-pressure chemical vapor deposition conducted at room temperature. The process starts inserting a granular raw material, called dimer, inside the furnace. The quantity of raw material inserted is proportional to the effective desired thickness of the deposited layer. Once the process starts, the gas is then heated and vaporized under vacuum environment into a dimeric gas. The gas then undergoes the process of pyrolysis, splitting the dimer into its monomeric form. Now composed by monomer, the gas deposit onto all surfaces forming a multi-layer, polymeric film that covers and encapsulates. A brief and simple schematization of such process is presented in **Figure 21b**. Such process allows to have a uniform and conformal coating, with the ulterior advantage of being transparent. Dielectric thickness used is in the range of hundreds of nanometres.

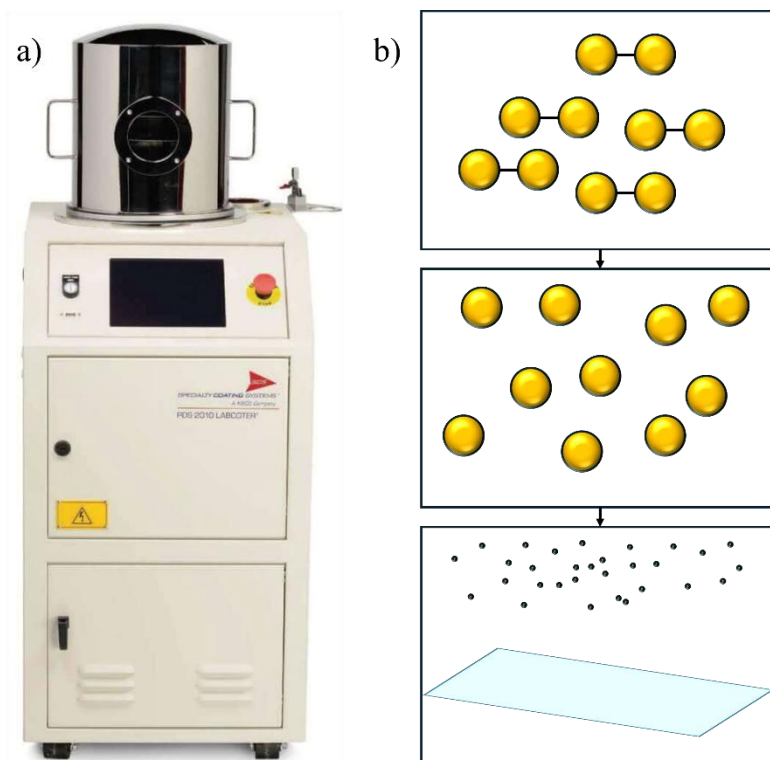


Figure 21: a) Typical Parylene Coater instrumentation; this is the latest model available on the market. b) Simplified schematization of the deposition process of Parylene C.

3.2.3 Spin-coating

Spin-coating is a deposition technique through which thin layers of a liquid material can be deposited and then dried at room temperature or at higher temperature using an oven or a hot-plate. One of the main advantages of this technique is its simplicity, since it only requires a bit of dexterity and care for the dispensation of the material on top of the substrate. To avoid having bubbles that could determine a bad and non-uniform film, deposition must be performed in the correct way with respect to the material used. For most liquid, a Pasteur pipet or a Eppendorf micropipet is suitable, however some materials tend to form huge bubbles when deposited in this way, like Polyvinyl Alcohol (PVA) whether some are way too viscous and require the use of a spatula. Using then the correct spinning recipe, that includes acceleration, rotation speed and spin duration, a layer of the desired thickness can be obtained. It is also a low-cost technique, since it does not require expensive equipment or high temperature treatment of the used materials. However, a lot of material is wasted, since most of it is flung off on the sides due to the high rotation speed. During rotation, most of the solvent evaporates due to the airflow. The sample is then left to rest at room temperature or at a higher temperature inside an oven or on a hot plate. This depends on the solvent used and

how the material needs to dry to obtain the desired results. For example, organic semiconductors need to dry in a correct way to properly form the crystals. The thickness of a film depends on the solution concentration and solvent evaporation rate, which in turn depend on the solvent viscosity, vapour pressure, temperature and local humidity. The more viscous the material, the higher needs to be the spin speed to obtain a thin and uniform layer. Spin thickness curves are usually determined empirically. Other quantities that determine the final film thickness are the initial thickness of the fluid and its density. Although it's an easy technique, it obviously needs to be properly executed to avoid defects on the deposited film. Wettability of the substrate is a very important parameter for a good deposition. **Figure 22** shows a summary of the main passages for the process.

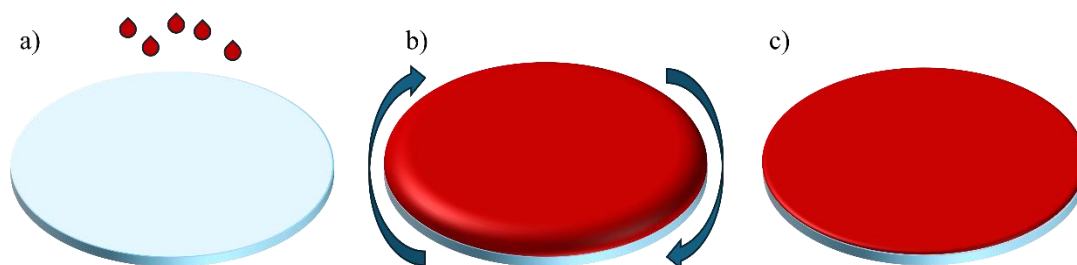


Figure 22: a) The material is deposited, manually or through an automated instrument; b) once the substrate is fully covered, rotation can be started; c) after a set amount of time, rotation automatically stops, and a uniform film is obtained.

3.2.4 Drop-casting

Drop-Casting is a technique mainly used for the deposition of very small quantities of material on top of a surface. Usually, one or a few droplets of material are deposited on a surface and left to dry at room temperature or at a higher temperature, on a hot plate or inside an oven. It is a fast deposition technique, that requires virtually no expertise for a good execution. A valid alternative for polymeric semiconductors, it is not considered, however, a reproducible technique, since the droplet dispersion and the drying conditions are not controllable; the former depends on the electrostatic interaction between the droplet and the surface, the latter is dependent from the solvent employed and the surrounding environment. Moreover, the coating is not uniform, as the film will be thicker at the centre and thinner on the edges, with a particular effect called “*coffee ring effect*” that arises during the drying process. This happens because of the capillary flow induced by the evaporation of the solvent.

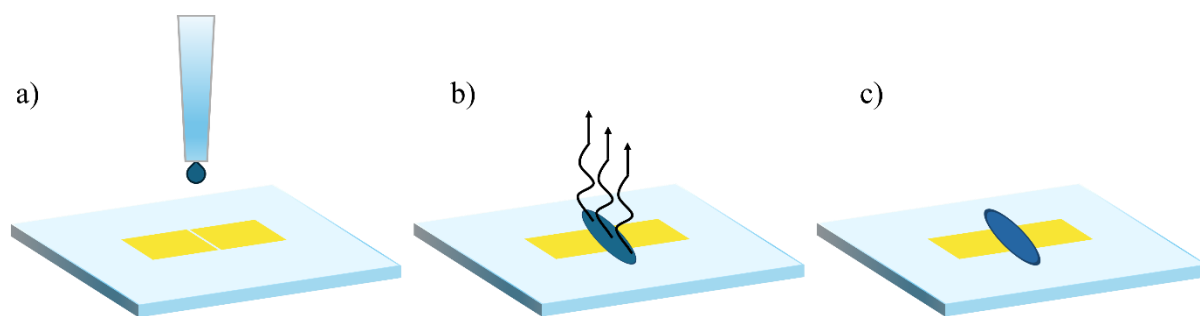


Figure 23: a) Material is deposited on the desired part of the substrate through an Eppendorf micropipet; b) solvent is left to evaporate at room temperature or slightly higher; c) solvent is fully evaporated and the material is dry and ready.

3.3 Instrumentation

Different instruments were used for characterization of the devices.

3.3.1 Keithley 2612 System SourceMeter

The SourceMeter was used to electrically characterize the OFETs, as it allows for fast readings. The instrument was used to apply a voltage difference between the devices terminals and read the output current. Due to how it is built, it only allows for three terminals measurements. In **Figure 24** is presented the instrument.



Figure 24: Photo of the instrument used for part of the electrical characterization of the devices.

3.3.2 Keysight B1500A

The Keysight B1500A semiconductor parameter analyser is a complete device characterization analyser designed for comprehensive semiconductor testing. The instrument supports various measurement techniques and was used for IV characteristics. The built-in structure allows the characterization of devices with more than three terminals, which is needed for double gate devices, since they possess four terminals. The instrument is presented in **Figure 25**.

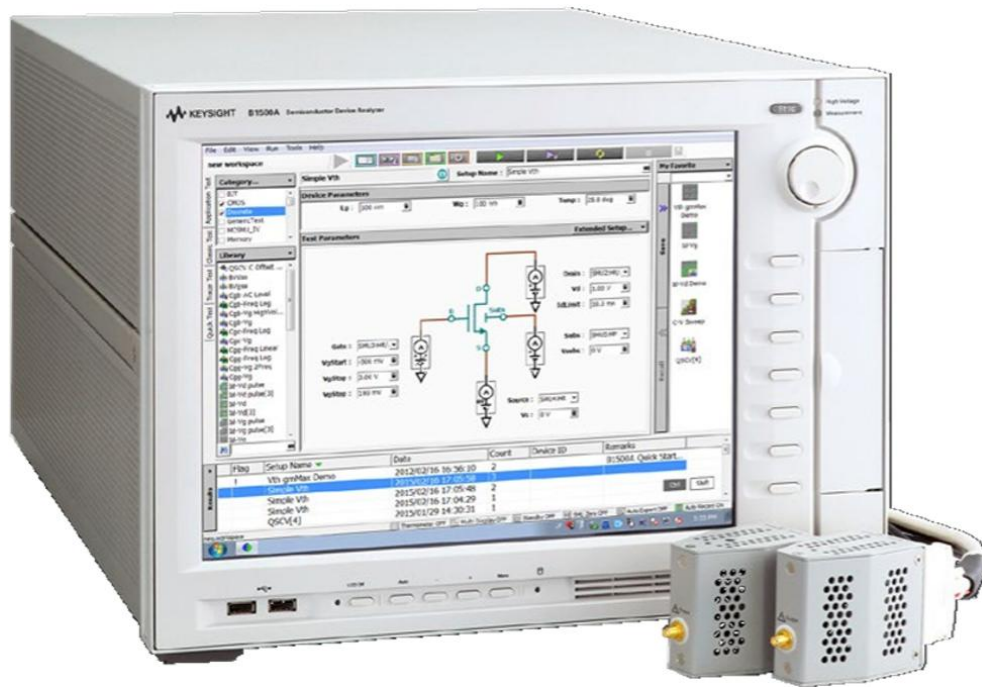


Figure 25: Photo of the Keysight B1500A semiconductor analyser.

3.3.3 Optical PyroCouple Calex PC21MT-1

The optical pyrocouple Calex PC21MT-1 is an infrared instrument, capable of reading a wide range of temperatures. Used to monitor the temperature of the Peltier Cell during the devices' characterization, its output was read through a second keihtley sourcemeter implemented in the setup. It has a fast response time, allowing for efficient monitoring and correlation of the device's response.



Figure 26: The optical pyrocouple used during characterization is a four-terminal device; two of the terminals are for power supply, the other two are for readings and are connected to a sourcemeter that converts optical readings into electric signals.

3.3.4 IMADA Force Measurement System

To characterize the devices as a mechanical force sensor, it was used a dynamometer system that allowed for a precise characterization, thanks to its resolution of 0.001 N. Using the indenter and a small piece of PDMS, forces were applied only in the needed region. To avoid user interferences, the instrument is controlled via its computer program, that allows to dynamically control the applied force.



Figure 27: The IMADA Force measurement system used in our laboratory. It is composed by two main parts, the motorized test stand and the digital dynamometer equipped with an indenter.

4. Chapter IV: Fabrication and characterization of flexible double-gate organic field effect transistors for tactile applications

In the previous chapter, several examples and approaches for the fabrication of Double-Gate transistors have been presented. Among the different structures, the OFET one is the chosen architecture to study and develop a device that answers to most of the requirements for modern organic technologies: flexible, low-cost, large area and stable over time. The approach employed during this thesis work led to the publication of an article^[146] which proposes a sensing device stable over time, tunable meanwhile offering a solution for one of the main issues of organic electronic, the degradation of the active layer.

4.1 Organic field effect transistors fabrication process

The process of fabrication of the OFETs involves the employment of different techniques. The substrate is properly cleaned with Acetone, Ethanol or Isopropanol, and Bidistilled Water and then air dried. The chosen substrate can be Polyethylene Terephthalate (PET) or Polyethylene Naphthalate (PEN), both 125 μm thick, both flexible. Three different architectures were fabricated, to compare the different behaviour and relative advantages or disadvantages. The three different architectures are bottom gate-bottom contact (BG-BC), top gate-bottom contact (TG-BC) and double gate (DG-BC); the latter substantially merges the two other structures, ideally taking advantages from both. Therefore, for what concerns the BG-BC and DG-BC architectures, the first electrode of the device, the bottom-gate is made of aluminium. At the beginning, every electrode was fabricated through a photolithographic process. However, for both bottom and top gate electrodes, in the optimization process, it was decided to realize them through thermal evaporation with a shadow mask, **Figure 28a**, since these electrodes do not require a high resolution. This has two main advantages: the gate can have any desired form, allowing to optimize the space on the substrate and, thanks to this, a photolithography passage can be avoided. This speeds up the fabrication process, meanwhile reducing the use of dangerous solvents such as Hydrofluoric Acid (HF), needed for the etching of aluminium; other acids can be used for the etching of aluminium, but since the resolution needed for the gate fabrication is very low, such approach has been discarded in favour of a more direct one. Once the batch of gates is ready, **Figure 28b**, the samples are positioned inside the Parylene Coater for the deposition of the dielectric layer. A 180 nm thick layer of Parylene C is deposited, **Figure 28c**.

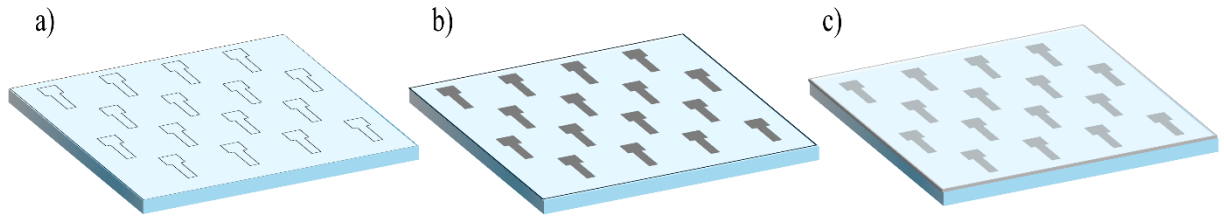


Figure 28: Fabrication process of the Bottom Gate electrode. a) A shadow mask with the desired pattern is positioned onto the substrate; b) gate electrodes are realized through a thermal evaporation; c) Parylene C dielectric layer is realized using the Parylene Coater.

Since the configuration of the devices is a bottom contact one, the next step is to realize source and drain electrodes. This step is also the same one from which the fabrication of TG-BC devices starts. They are realized in gold, so they are fabricated with a thermal evaporation, but this time, since a higher resolution is needed, once the deposition is done, the electrodes will be patterned via photolithographic process. A positive photoresist is deposited, inside a chemical fume hood, onto the golden substrate through spin coating and left to dry inside the oven for 30 minutes at 40 °C. Since photoresist is sensible to UV light, this part of the fabrication needs to be conducted avoiding, as much as possible, exposition of the samples to natural light and any other source of UV. A photolithographic mask with the desired pattern is then positioned so that the gap between the two electrodes is aligned to the centre of the gate electrode. This gap is what will define the channel of the transistor, with dimensions of 4 mm in width (W) and 40 μm in length (L), giving a W/L ratio of 100. After exposition to UV light inside a contact copier, samples are then dipped in development solution, rinsed with water and dried. Next step is a chemical etching that will remove the excess gold, leaving only the patterned electrode. The etcher for gold is Potassium Iodide (KI) and samples are dipped upside down in this liquid for the removal of the unneeded gold. At this point, samples are washed once again with acetone, to remove the remaining photoresist, alcohol and water for proper cleaning. **Figure 29** shows the necessary passages made to realize the source and drain electrodes.

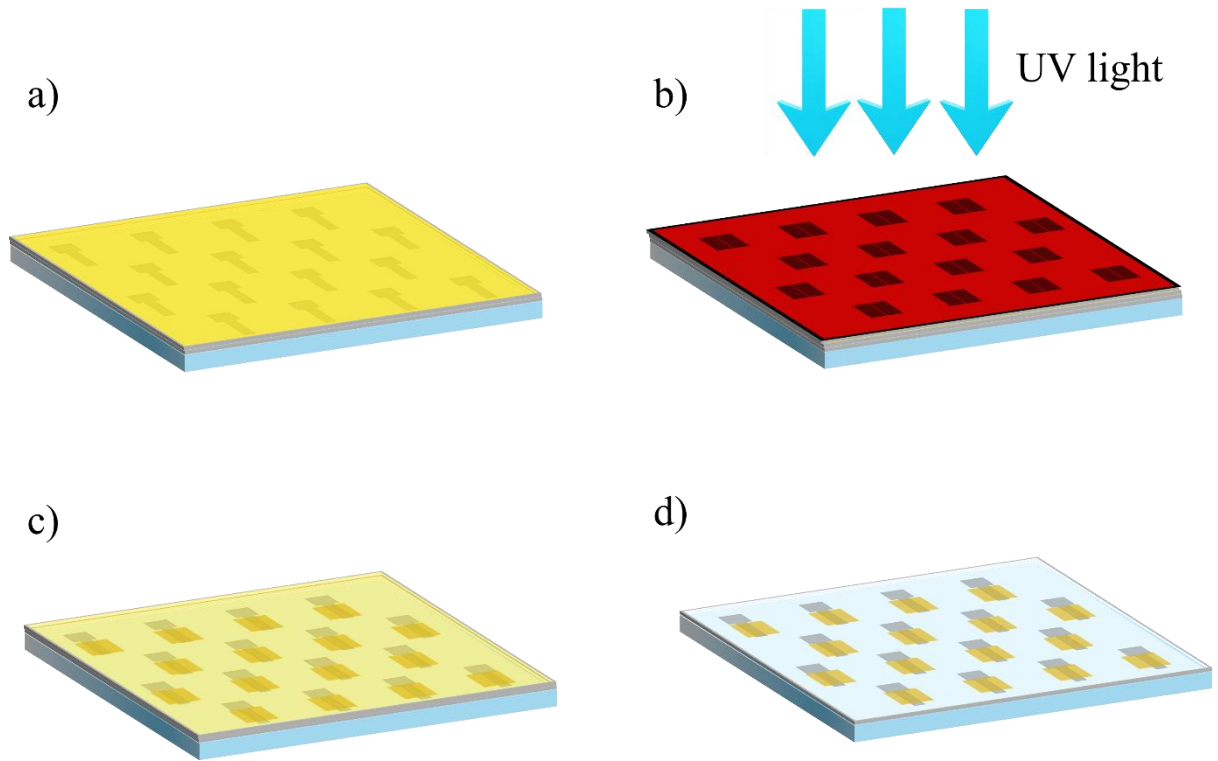


Figure 29: Fabrication process of the Source and Drain electrodes. a) Gold is deposited onto the Parylene C layer; b) positive photoresist is deposited and left to dry. Once ready, a photolithographic mask is positioned and UV light is shone to impress the pattern; c) the substrate is dipped in developer solution, removing the photoresist everywhere except on the covered parts; d) unneeded gold is etched using KI and then washed with acetone to remove the remaining photoresist.

Once ready, the semiconductor can be deposited, taking care of doing so in the chemical fume hood. Depending on which one is chosen, drop casting or spin coating is employed. Semiconductor is then dried and at this point a device can be considered finished (**Figure 30a**). However, since the target of the thesis is to work on double-gate device, to complete the fabrication, a second deposition of Parylene C is made (**Figure 30b**). The parylene film for the second dielectric layer is around 380 nm thick, to avoid short circuits between the semiconductor and the top gate. This can happen due to the roughness of the semiconductor surface. Smaller thicknesses of this dielectric layer have been tested, however this resulted sometimes in faulty devices, reducing the throughput of the fabrication process. The top gate of the device is then deposited in the same way as the bottom gate was, this time though, to reduce as much as possible the capacitive coupling between the two gates, it is a bit narrower in the channel area (**Figure 30c**).

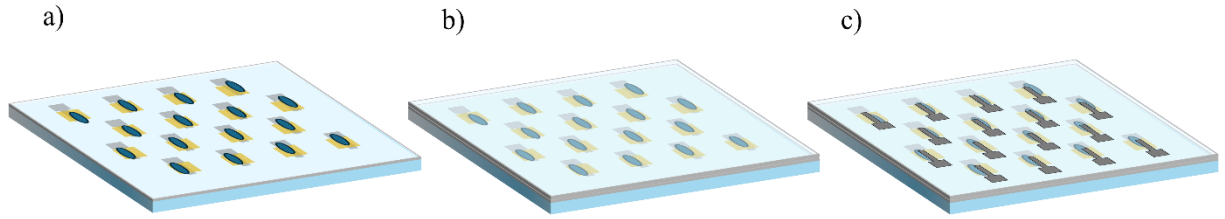


Figure 30: Fabrication process of the Top Gate electrode. a) Semiconductor is deposited in the channel area; b) a second dielectric layer is deposited; c) the top gate is then realized in the same way as the bottom gate.

Both the second Parylene C layer and second gate have an intrinsic effect; in fact, they not only serve as dielectric layer and gate electrode, but they also provide protection to the most fragile part of the device, the active layer. It is a self-encapsulating structure, in which the encapsulation has an active role in the working functionalities of the device. Once that the fabrication process is optimized, if any modification to the structure needs to be conducted, to optimize performance or speed up some part of the process, one parameter at a time will be modified. For instance, a change in the dielectric properties, like thickness or material, would be made leaving everything else unchanged, using the materials of which we have the best knowledge. A cross section with all the component elements of all the proposed architectures are presented in **Figure 31**, **Figure 32**, and **Figure 33**.

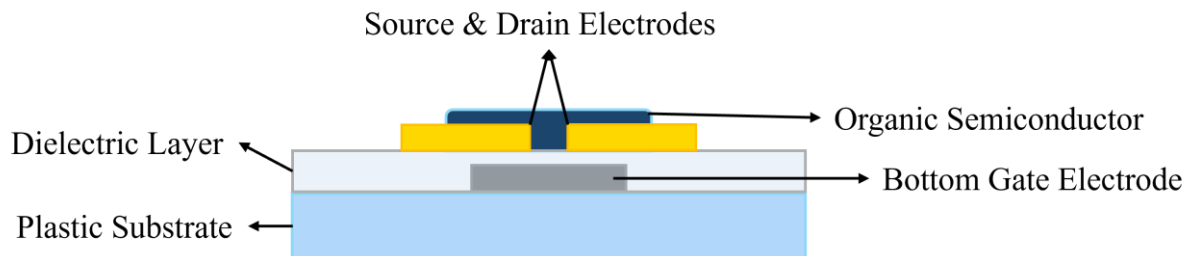


Figure 31: Cross section of the bottom gate-bottom contact device. The channel size is emphasized to show the interface between semiconductor and dielectric. In this configuration, the semiconductor is exposed to all environmental agents and easier to damage by mistake.

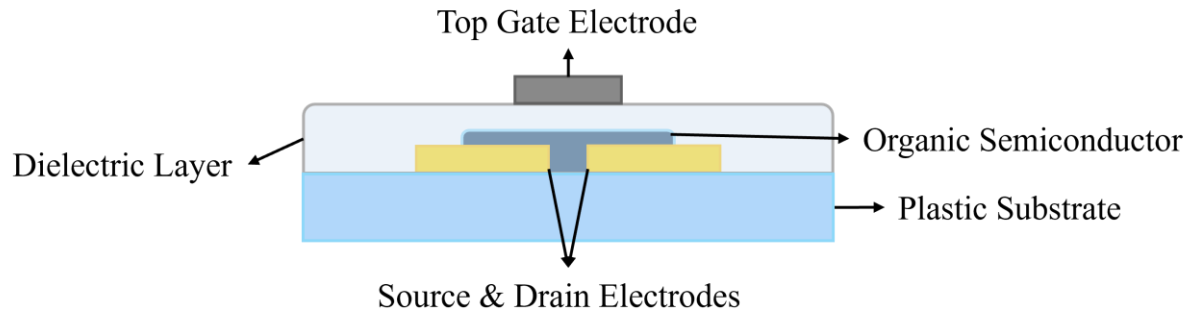


Figure 32: Cross section of the top gate-bottom contact device. The active layer of the device is self-encapsulated due to the dielectric layer and gate electrode. However, due to the higher thickness of the dielectric layer, control over the channel is weaker.

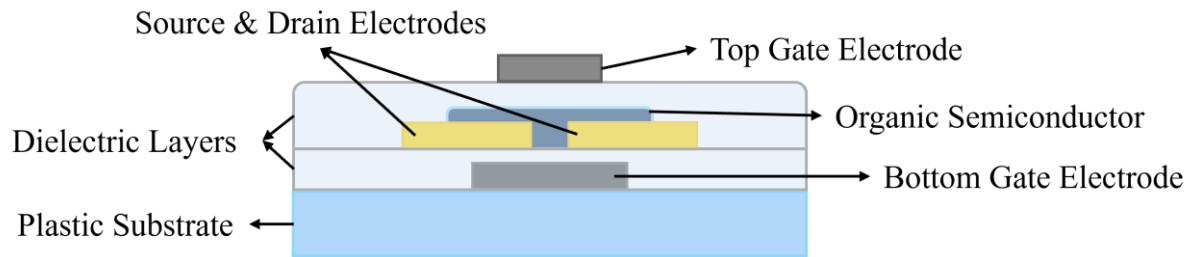


Figure 33: Cross section of the Double Gate device. The channel size is emphasized to show the interface between semiconductor and dielectric. Also, from this is clearer the difference in dimensions of the two gate and the reduced overlapping area of the different electrodes.

4.2 Organic field effect transistors characterization

After development, devices must be characterized to know their behaviour, in which condition they work and how they evolve over time. Before delving into the description of the double gate characteristics, it is useful to introduce the basic functioning of an organic field effect transistor (OFET). Closely related to the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), their ideal output characteristic is quite similar, even though the charge transport is totally different. In fact, while MOSFETs typically work in inversion mode, OFETs work in accumulation mode. The difference between these two working modes is that, for the former there's a shifting from insulating to conductive in the behaviour of the channel, while for the latter, there is an accumulation of charges at the interface between the semiconductor and the gate dielectric. The core of an OFET is a Metal-Insulator-Semiconductor (MIS) structure, which can be considered, in principle, a parallel plate capacitor. The two plates are the gate and the semiconductor, separated by a dielectric, which is a thin insulating film. Source and drain electrodes are patterned in order to contact the organic semiconductor, allowing to probe the conduction across the organic film. They are considered unipolar transistors; this means that current flow is conducted by a carrier of a single type. A typical problem with organic electronics is the stability over time of such devices. Environmental agents like moisture and oxygen are natural enemies of organic materials due to the detrimental effects they have on their durability and performances. Some organic semiconductors are more stable in air than others, with some that cannot possibly be deposited outside of a glovebox^[165]. Air is full of water molecules and the problem with this is that it has a double effect on the semiconductive film: on one hand, water modifies the film morphology, leading to the arising of trap states in the vicinity of the channel, reducing the mobility in the ON state of the device, on the other hand, being water polar, there's an increase in the conductivity between source and drain, leading to an increase in the OFF current and thus a reduction in the ON/OFF ratio of the transistor. Oxygen is vital for humans, but very detrimental for most organic semiconductors' performances. It is highly electronegative; therefore, it attracts electrons from the semiconductor, increasing the OFF current and shifting the threshold voltage of the devices. In some cases, oxygen can be used as a dopant for p-type semiconductors, however, long term exposure to it, can lead to the oxidation of the molecules, increasing the hopping barrier and reducing the mobility. For these reasons, OFETs need a proper encapsulation to avoid the degradation of the active layer. This has to be done using materials and techniques that do not damage the device, particularly the active layer. To have an efficient barrier against degradation, water vapor

transmission rate must be lower than 10^{-6} g/m²/day, oxygen transmission rate lower than 10^{-3} cm³/m²/day. Of course, the barrier needs to be stable over time, meaning that it must not deteriorate during the utilization period. Starting from these assumptions, the first step of the thesis was to fabricate different set of devices with the aforementioned characteristics. One set was composed by typical organic thin film transistors (OTFTs), bottom gate-bottom contact with the exposed semiconductor. One set for the top gate-bottom contact architecture while the other set was composed by double-gate OTFTs, in which the semiconductor was protected by a dielectric layer and a second metal gate. The fabricated devices were measured at day 0 and then every consequent measurement was carried out at increasing time intervals. This procedure was performed for the three different cited semiconductors: TIPS-Pentacene, DPP-DTT, both p-type, and N-1400, n-type. The aim of this study was to highlight the better reliability and ductility of use of double gate architecture, with a control over the working point of each device, allowed by the presence of two gates. In fact, for single-gated structures, once the initial parameters are set, you lose every control over their evolution and, especially with organic electronics, one has to find a mean to protect the active layer from damage and deterioration, meanwhile ensuring to have a device with the best possible performances. Each set of the proposed devices is comprised of 10 devices, with each set realized in a single batch.

4.2.1 Bottom gate-bottom contact architecture

The bottom-gate bottom-contact architecture is the first one analysed. TIPS-Pentacene, is the semiconductor of which we have the best knowledge as it is widely used for the fabrication of OFETs. One thing that has to be noted is that the semiconductor is manually deposited through the use of an EPPENDORF micropipet and the drop casting or spin coating techniques therefore user dependant, and small differences in the behaviour of different devices are to be expected. Although always the same quantity of material is deposited, such differences can be ascribed to the varying interfaces that the semiconductor forms with both source and drain electrodes as it dries. Once the devices are ready, measurement can start. To characterize every device, both characteristics and transfer characteristics are taken. Although the general behaviour of every device is the same, since they are all OFETs, depending on the semiconductor used, results vary notably. All the devices, of every architecture, were kept in the same condition for all the duration of the statistical acquisition, that is in air inside a box, so that no direct light would hit them. This is mostly done to avoid excitation of the semiconductor due to photon absorption. Right after

the deposition and drying of the semiconductor, the first set of measurement has been made. This is considered to be day 0 of the statistic acquisition. **Figure 34** shows the output characteristics and transfer characteristic of a bottom gate-bottom contact device fabricated with TIPS-Pentacene as semiconductor. Threshold voltage (V_{Th}) and carrier mobility (μ) were extracted from the analysis of the transfer characteristic of each device for every semiconductor. After calculating the square root of the absolute value, a linear fit of the saturation region is made to evaluate slope and intercept. From these values, V_{Th} and μ can be calculated using the following formulae:

$$V_{Th} = -\frac{q}{m} \quad (1)$$

$$\mu = \frac{m^2}{\frac{W}{2L}C_{ins}} \quad (2)$$

Elaborating the data leads to a mean value for the two quantities reported in **Table 5**.

Table 5: Mean threshold voltage and carrier mobility values for bottom gate-bottom contact devices with TIPS-Pentacene at day 0 of measurement.

V_{th} [V]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	I_{ON}/I_{OFF}
$7,1 \cdot 10^{-1} \pm 3,7 \cdot 10^{-2}$	$1,9 \cdot 10^{-1} \pm 4,4 \cdot 10^{-2}$	10^3

Although TIPS-Pentacene can reach higher carrier mobility, up to $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ^[166], the values obtained are acceptable for our purposes.

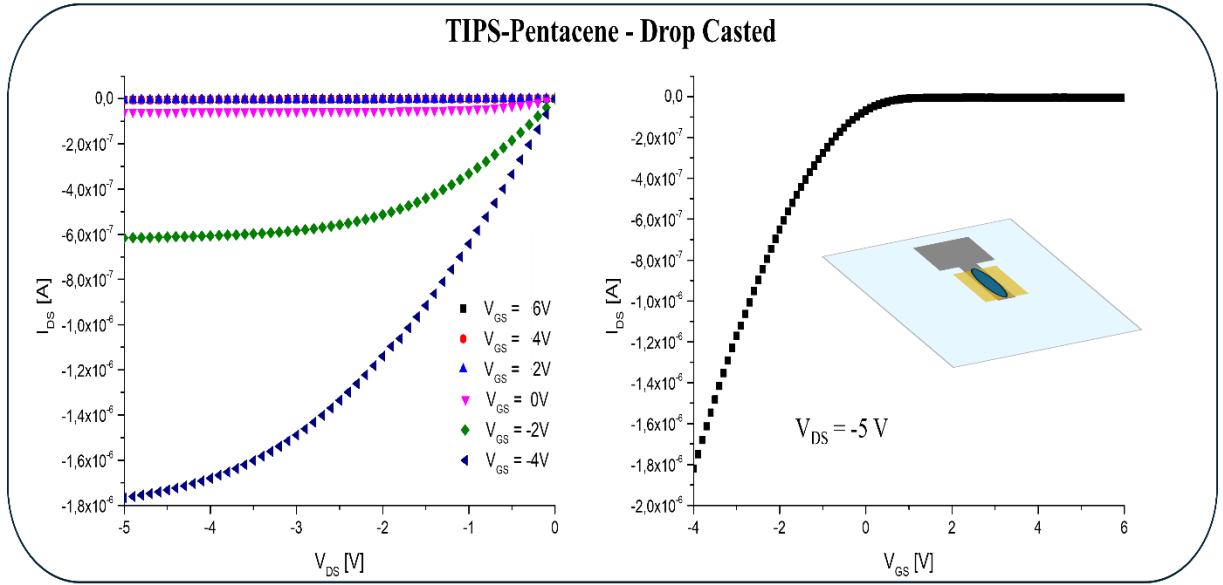


Figure 34: Left, is the characteristic IDVD output of a bottom gate- bottom contact device; right is the transfer characteristic IDVG output of the same device and the schematic of such device. V_{DS} is also indicated for IDVG measurement.

However, since this structure does not contemplate an encapsulation of the active layer, stability over time is far from being assured. In fact, as stated before, oxygen and moisture influenced the properties of the devices, leading to a decrease in carrier mobility. This is clear when considering the evolution of such parameter, as presented in **Figure 35**,

Figure 35: Average mobility evolution over time of TIPS-Pentacene semiconductor bottom gate-bottom contact transistors. The decrease in carrier mobility is sizeable. in terms of percentage variation with respect to the starting value. The decrease in carrier mobility (holes) is consistent and the final mean value of such parameter is around 60% smaller than the starting one. However, even after such a long period of time, devices are still usable, thanks to the stability of TIPS-Pentacene in air. They are not reliable, since parameters vary too much to think they can be used, in this architecture, for a long-term acquisition. Moreover, since also threshold voltage is not stable, as shown in **Figure 36** in terms of percentage variation with respect to day 0 of measurement, the working point of the devices is always different, meaning that the response to determined inputs is not constant. Final values obtained after the end of the acquisition are shown in **Table 6**.

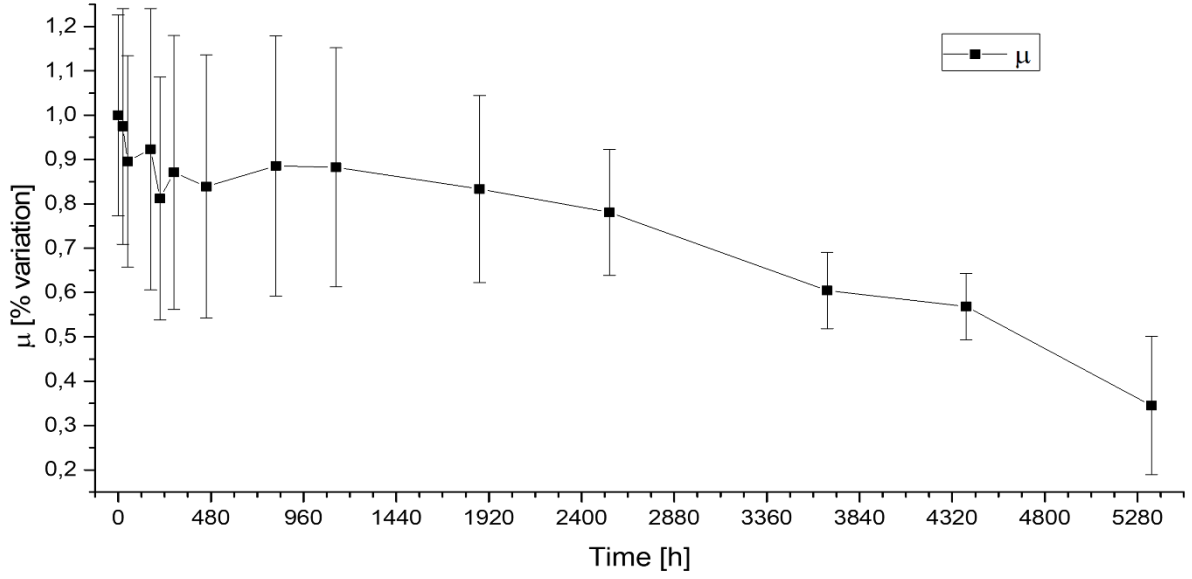


Figure 35: Average mobility evolution over time of TIPS-Pentacene semiconductor bottom gate-bottom contact transistors. The decrease in carrier mobility is sizeable.

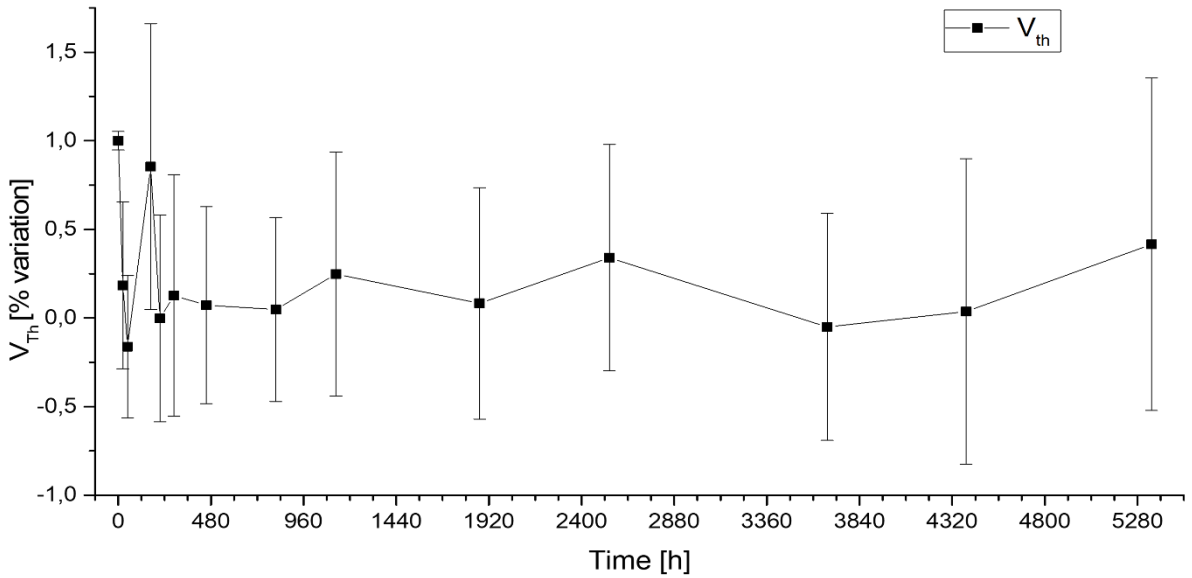


Figure 36: Average threshold voltage evolution over time of TIPS-Pentacene semiconductor bottom gate-bottom contact transistors. This parameter varies too much over time to allow a reliable use in any application that requires stability over time.

Table 6: Mean threshold voltage, carrier mobility values and I_{ON}/I_{OFF} for bottom gate-bottom contact devices with TIPS-Pentacene after over 6 months.

V_{th} [V]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	I_{ON}/I_{OFF}
$2,9 \cdot 10^{-1} \pm 6,6 \cdot 10^{-1}$	$6,8 \cdot 10^{-2} \pm 3 \cdot 10^{-2}$	10^3

These measurements will be the reference for comparison with the other two architectures, and it will be clear which one will be the most efficient in terms of use.

Setting aside this first set of devices, let's consider those prepared with DPP-DTT. This semiconductor can be both drop-casted with longer drying times or spin-coated, which in principle should be the preferred technique, since DPP-DTT requires temperatures higher than room temperature, around 90 °C, and spin coating allows for quicker drying and thinner layers. However, this does not seem to be the case, as evident from the comparison in **Figure 37**.

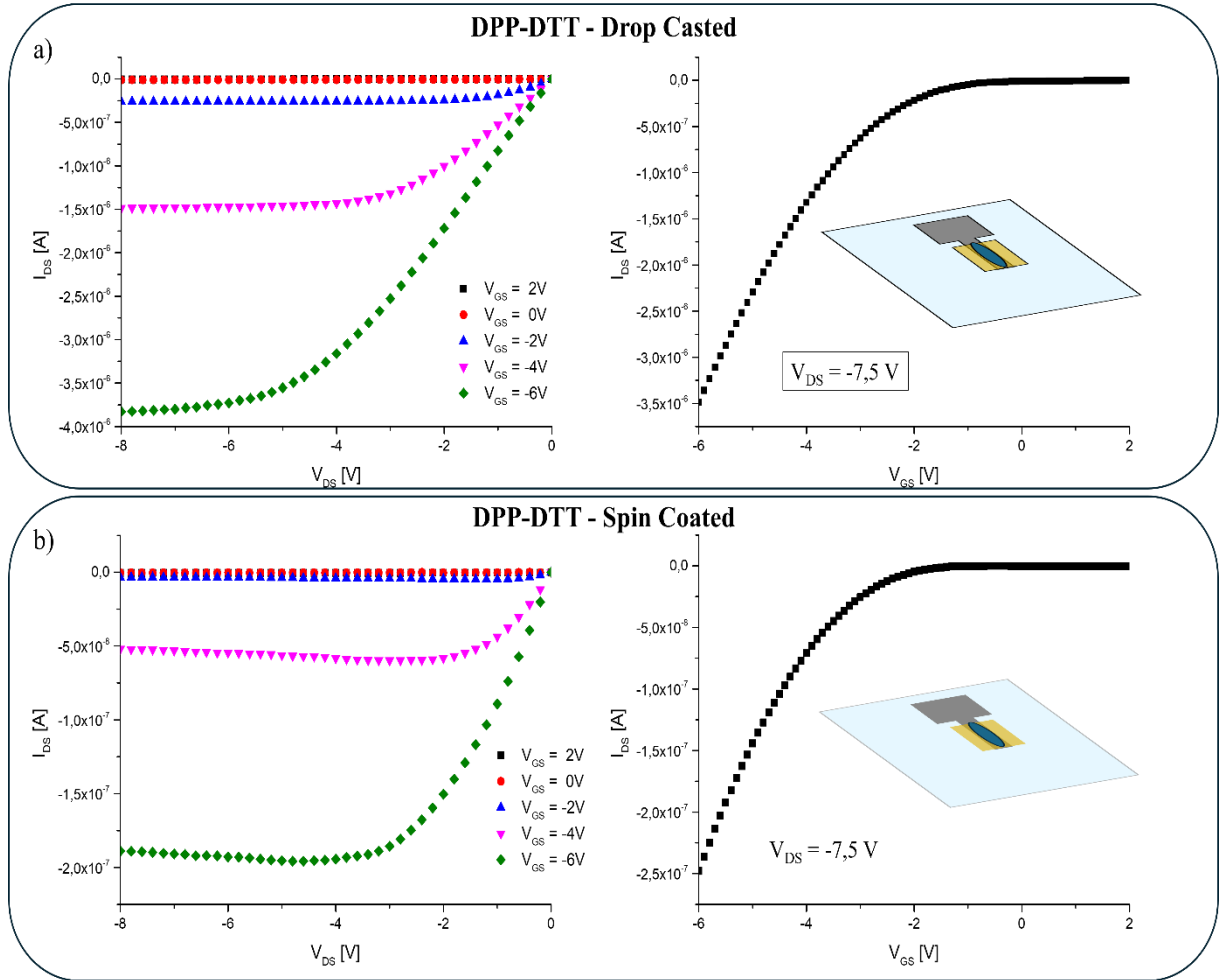


Figure 37: Characteristics and transfer characteristics of two devices realized with the same semiconductor deposited through different techniques. Both sets of devices were tested in the same conditions. a) Semiconductor has been drop-casted. b) Semiconductor has been spin-coated.

What's shown here are the output curves for two device samples, one realized with drop casting, the other with spin coating. As clear from the graphs, the output current of the former is one order of magnitude greater than the latter. Probably, the cause of this is that crystal formation in these devices does not occur in the proper way, and this can be caused by a multitude of factors. Nonetheless, they can be analysed in comparison with the more performing devices, to see if the degradation trend is the same. In **Table 7** are reported the extracted mean values for the two sets of devices. These data, further confirm the fact that

drop-casted samples perform better than spin-coated ones, with a difference of one order of magnitude for what concerns the carrier mobility and a slight difference in terms of threshold voltage, that in both sets of samples has a negative mean value, meaning that they switch on late.

Table 7: Initial threshold voltage, carrier mobility mean values and I_{ON}/I_{OFF} for both drop-casted (top) and spin-coated (bottom) sets of bottom gate-bottom contact devices.

	V_{th} [V]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	I_{ON}/I_{OFF}
Drop-Casted	$-9,2 \cdot 10^{-1} \pm 4,6 \cdot 10^{-1}$	$1 \cdot 10^{-1} \pm 4,8 \cdot 10^{-2}$	10^3
Spin-Coated	$-1,3 \pm 3,7 \cdot 10^{-1}$	$1,4 \cdot 10^{-2} \pm 5,7 \cdot 10^{-3}$	10^2

Following a similar protocol, both sets of samples were measured periodically with increasing distance between each measurement. After a few months, some conclusions can be already taken. For drop-casted devices, mobility had a slight decrease, comparable to that of TIPS-Pentacene samples after the same period. One thing that can be noted from the graph in **Figure 38** is the high error bars, meaning that there is much discrepancy between the parameters of the samples that form the statistical pool. However, this time it was the threshold voltage the most affected, since it became so positive that it was problematic to measure the device keeping a similar range of voltages. In fact, that parameter, endured a shift of around 4 Volts from the beginning to the end, as shown in **Figure 39**. This is not something that can be considered as useful, since the working point of such devices varies too much over a short period of time.

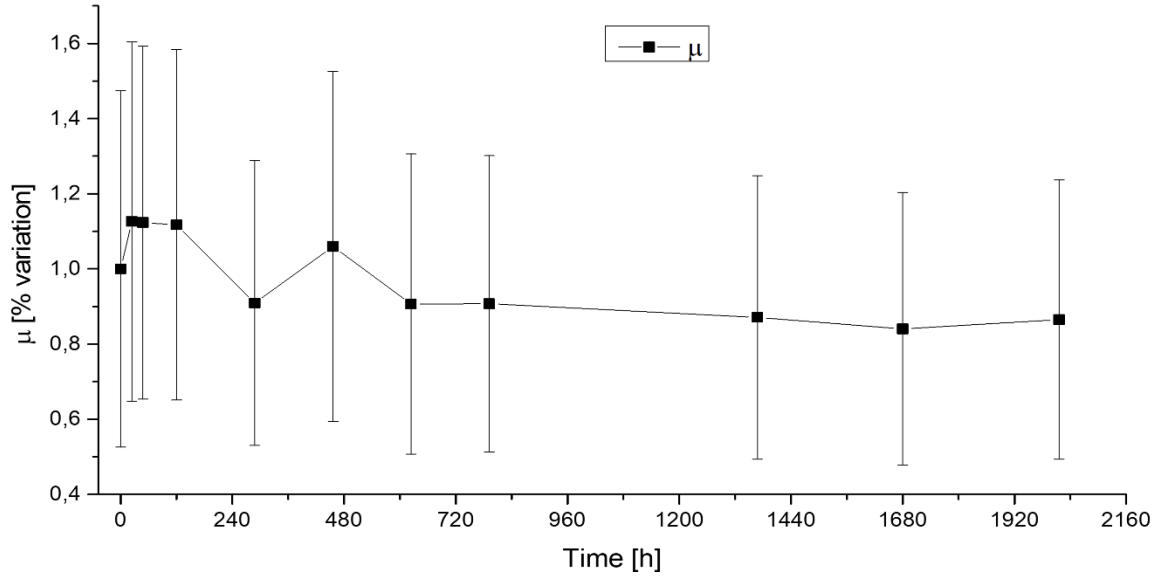


Figure 38: Average mobility evolution over time of drop-casted DPP-DTT semiconductor bottom gate-bottom contact transistors. The decrease in carrier mobility is small but the error bars are very big, meaning that there is a lot of difference between the devices composing the set.

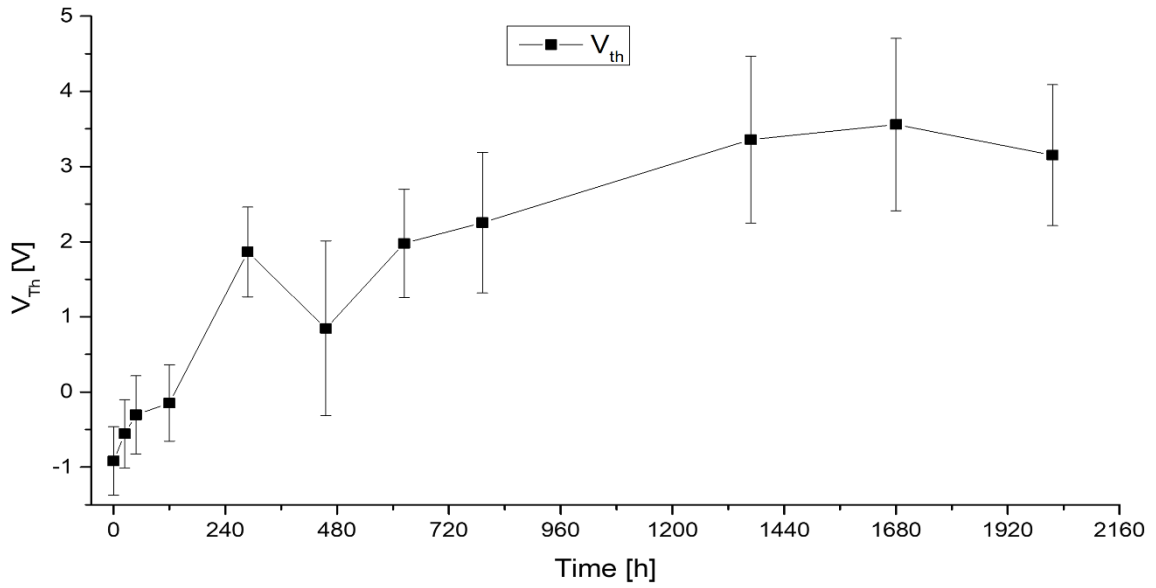


Figure 39: Average threshold voltage evolution over time of drop-casted DPP-DTT semiconductor bottom gate-bottom contact transistors. This parameter varies too much in a short period of time to allow a reliable use in any application that requires stability over time.

For what concerns the samples in which the semiconductor was deposited through spin coating, both mobility and threshold voltage have a different behaviour. Regarding mobility evolution, we have to consider that it started from an already very low value, especially compared to that of the samples realized through drop casting, even though the

semiconductor is the exact same one. Moreover, in just ten days we can see a sizeble decrease in the parameter.

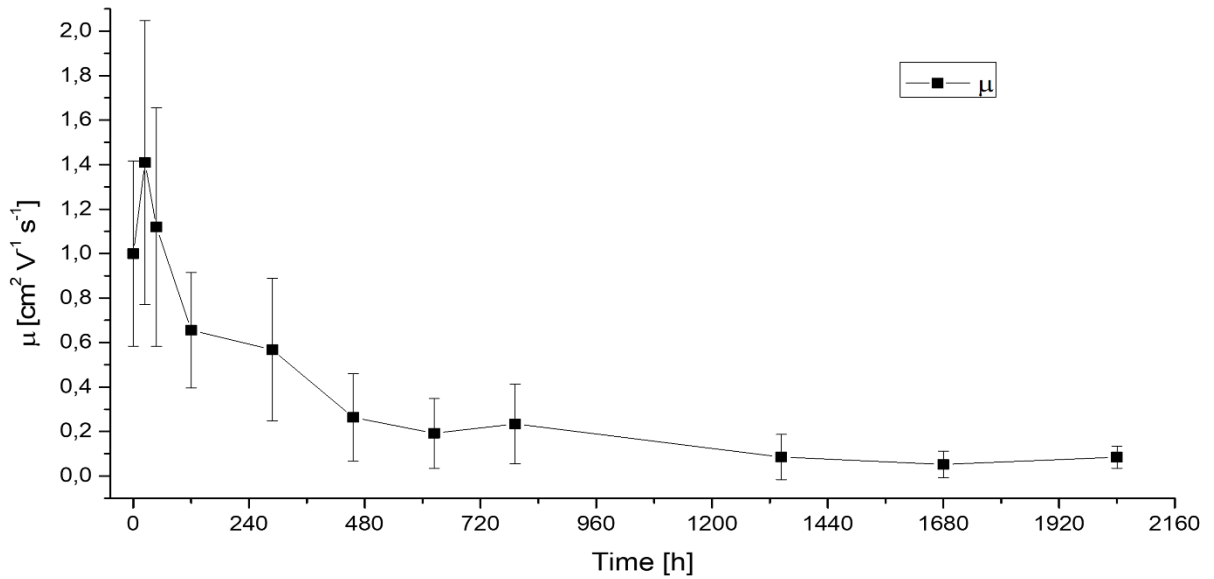


Figure 40: Average mobility evolution over time of spin-coated DPP-DTT semiconductor bottom gate-bottom contact transistors. The decrease in carrier mobility is small but the error bars are very big, meaning that there is a lot of difference between the devices composing the set.

Starting from a very low value, there is then a loss of around 90% of the initial mobility in the timespan of three months. One thing that can be noted is that all the devices in the statistical pool tend to converge toward a value, fact highlighted by the very small error bars. Threshold voltage, just like for the previous set of samples, tends to increase, moving toward

0, however the shift is less substantial. There is, however, a different evolution among the devices, since the error bars tend to become higher as time goes by.

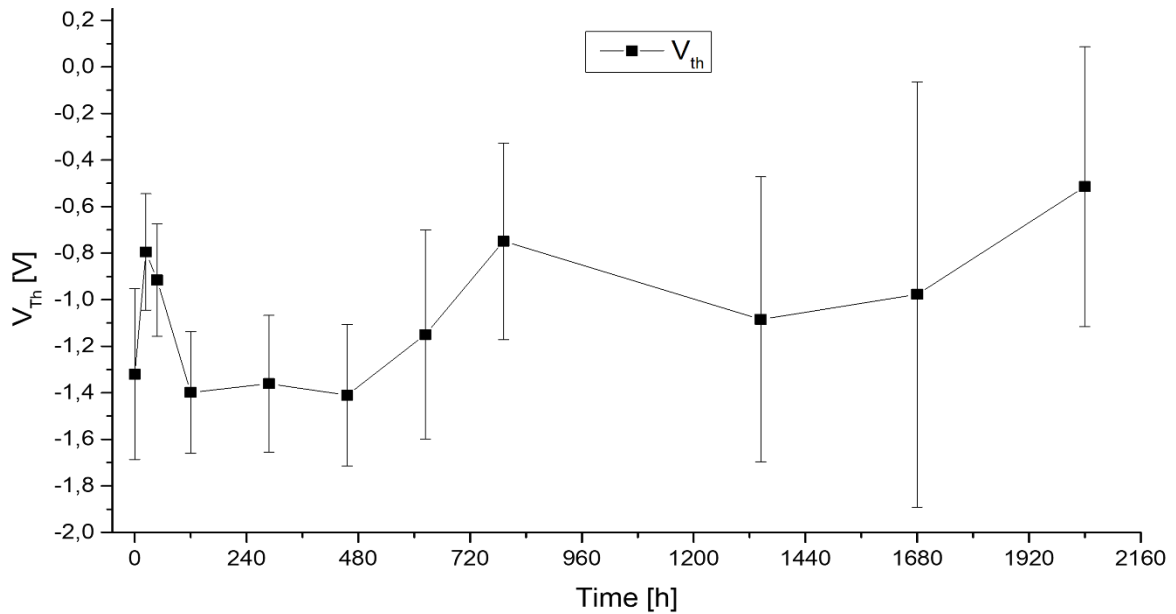


Figure 41: Average threshold voltage evolution over time of spin-coated DPP-DTT semiconductor bottom gate-bottom contact transistors. Starting from a rather negative value, the tendency to go toward less negative ones could in principle be a convenient evolution.

This remarkable difference between the devices of the two sets of samples can be related to the thickness of the active layer. In fact, the first set of samples, deposited with the drop casting technique, present a bulkier surface, with a measured thickness of 600 – 800 nm. This means that oxygen and water take more time to reach the bulk of the material, and thus the degradation process is slower. For the spin coated devices instead, the thickness of the active layer is lower, in the range of 100 – 200 nm; such difference can explain why this set of devices has a very fast degradation process. The difference in the mobility can be related to the different process of formation of the crystals during deposition. In this case, the reasons can be tied to the solvent used and the spin recipe employed for the deposition of the semiconductor. Wrong spin speed or time duration can lead to the formation of short or distant chains, as well as a wrong drying process. In this sense, further investigation is being conducted, with a different solvent, and results seems to be more interesting. The two sets of samples do have something in common, however. In the first days after the deposition of the semiconductor, the mean mobility tends to increase. This is probably related to the oxygen that acts like some sort of dopant, increasing the number of available holes that can

contribute to the mobility. This effect is then suppressed by the detrimental effect that oxygen has on organic materials. The final parameters obtained for the two sets are presented in **Table 8**.

Table 8: Final threshold voltage and carrier mobility mean values for both drop-casted (top) and spin-coated (bottom) sets of bottom gate-bottom contact devices.

	V_{th} [V]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	I_{ON}/I_{OFF}
Drop-Casted	$3,2 \pm 9,4 \cdot 10^{-1}$	$8,7 \cdot 10^{-2} \pm 3,7 \cdot 10^{-2}$	10^2
Spin-Coated	$-5,1 \cdot 10^{-1} \pm 6 \cdot 10^{-1}$	$1,2 \cdot 10^{-3} \pm 6,9 \cdot 10^{-4}$	10

The last semiconductor considered is the type-n. Being electrons the majority carriers, we expect it to work for positive bias. Presented in **Figure 42** are the characteristic and trascharacteristic of a single device. Output current is around $2 \cdot 10^{-7}$ A, meaning that we can expect a low mobility.

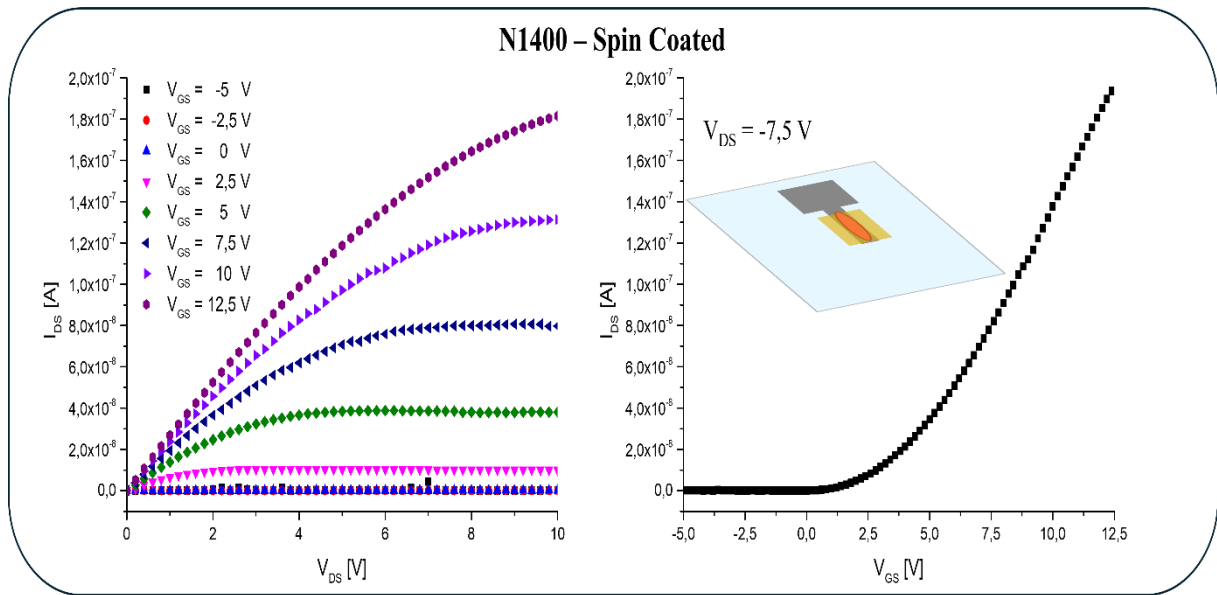


Figure 42: Characteristic (left) and transfer characteristic (right) of a transistor with n-type semiconductor N1400. A sketch of the device is presented on the right.

From the analysis of the samples composing the set, mean parameters of mobility and threshold voltage were extracted. Such parameters are presented in **Table 9**. As expected, mobility is very low, as reported in other works^[167,168]. One thing that is made evident is that mobility is also solvent dependent, with one order of magnitude of variation, depending on which one is used. Following the same protocol as before, periodic measurements were performed to determine the evolution and stability over time of the set of samples realized with the n-type semiconductor N1400.

Table 9: Initial mean values for threshold voltage, mobility and I_{ON}/I_{OFF} for the set of samples realized with n-type semiconductor N1400.

V_{th} [V]	μ [$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$]	I_{ON}/I_{OFF}
$-3 \cdot 10^{-1} \pm 4,2 \cdot 10^{-1}$	$2,5 \cdot 10^{-3} \pm 5 \cdot 10^{-4}$	10^2

All the samples in the set behave in a similar way, showing mobility values close to each other, with relatively small shifts from the mean value. One thing that can be noted immediately is the different trend in the first day of monitoring with respect to the same period in the p-type semiconductor samples. In **Figure 38** and **Figure 40**, in the first days, mobility tends to increase and as stated before, this might be due to the oxygen acting as a dopant, capturing electrons and increasing the available holes for conduction. In **Figure 43**, however, the peak of the degradation is right in the same period. Since, by definition of n-type semiconductor, majority carriers are electrons, the oxygen, being electronegative, captures electrons, reducing the number of carriers available for conduction.

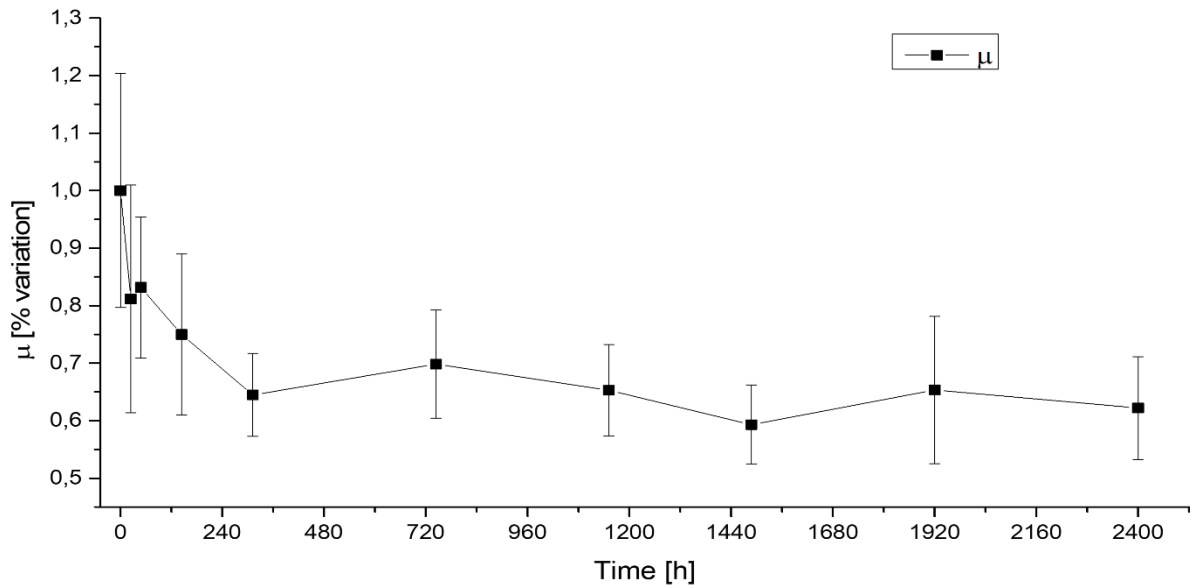


Figure 43: Average mobility evolution over time of N1400 semiconductor bottom gate-bottom contact transistors. The decrease in carrier mobility is sizeable and the effects of degradation on the mobility are evident since from the first days of monitoring.

One aspect that can be considered positive is that variation from the mean among the devices is relatively small for mobility. The same cannot be said for threshold voltage of the same set; mean value has very small shifts over time, however, there is a lot of difference in the working point between each and every device.

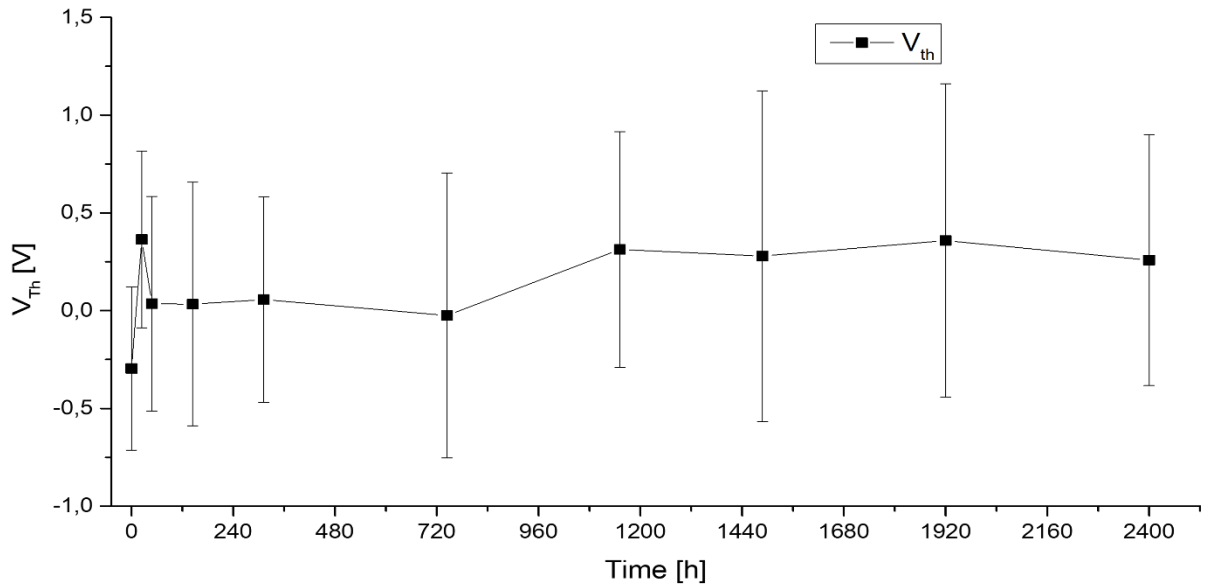


Figure 44: Average threshold voltage evolution over time of N1400 semiconductor bottom gate-bottom contact transistors. The mean value shifts very little over time, however there is much difference among the various devices, with some that switch on much earlier than other.

Concluding this analysis on bottom gate-bottom contact architecture with different semiconductor, a few things can be said. Regarding the mobility of the devices, there is, obviously, evident differences between the different semiconductors considered, but there's also a difference between devices realized with the same one deposited through different means. This is an indication on the importance of the optimal fabrication process, in every step of a device realization. However, as previously mentioned, being all these semiconductors solution processable, the choice of the optimal solvent for the chosen application is of the utmost importance. Being this a structure in which the semiconductor is exposed, it is, sooner or later, inevitably subject to the effect of degradation and is more prone to damage. For long term applications, this is not a favourable situation, due to the fact that shifts in the properties of the device affect its reliability in terms of response. Moreover, these shifts are not under the user control and, as will be discussed later, this is something that cannot be ignored when designing a device that should have some real-world application.

4.2.2 Top Gate-Bottom Contact Architecture

The top gate-bottom contact architecture is somewhat specular to the bottom gate one, with non-negligible differences. It is somewhat trickier to realize this structure, due to the roughness of the semiconductor. If the quality of the dielectric layer is not good enough or the thickness is not sufficient, the deposition of the top gate can lead to short circuits. Therefore, an optimization is needed to reach a good compromise between dielectric thickness and field effect. In fact, due to the same reason, the dielectric layer for a top gate architecture is usually thicker than the bottom gate one. This increase can lead, in some cases, to a less efficient field effect. Only DPP-DTT and N1400 semiconductor were considered in this case, due to a different approach in the study of architectures realized with TIPS-Pentacene. What is expected from this study, is that the evolution of the semiconductor properties, especially the mobility, will be very different, due to the self-encapsulation of the active layer intrinsic in the device architecture. As for the bottom gate-bottom contact architecture, DPP-DTT was deposited both through drop casting and spin coating, but this time the results were different, as shown in **Figure 45**. Due to the roughness of the semiconductor, the deposited dielectric layer for the drop-casted devices was around 420 nm thick, while for the spin-coated, the thickness was around 400 nm. Lower thickness systematically led to short circuits or resistive paths, and this leads to a very high gate current leakage.

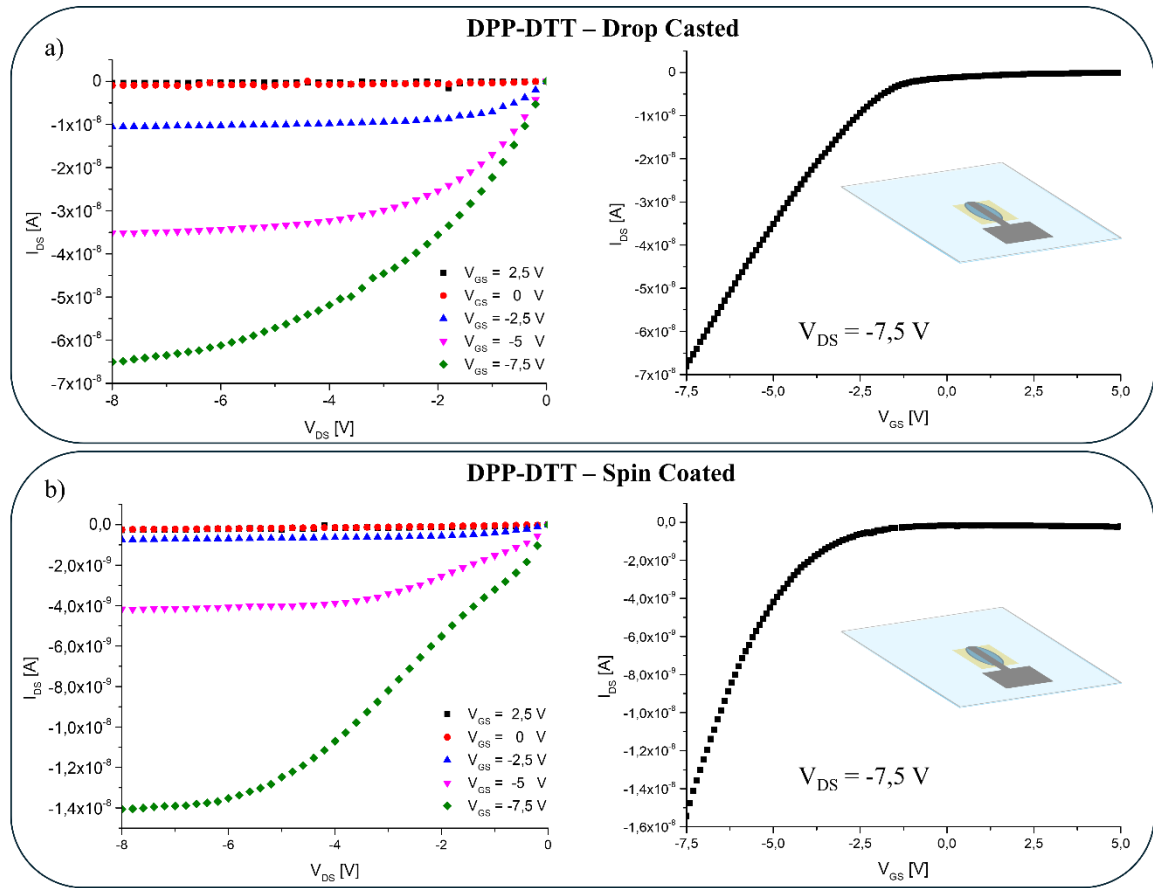


Figure 45: Characteristics and transfer characteristics of two example devices realized with the same semiconductor deposited through different techniques. Both sets of devices were tested in the same conditions. a) Semiconductor has been drop-casted. b) Semiconductor has been spin-coated.

The output current is very low for both specimen of devices, with a drastic reduction in performances, especially for what concerns the drop-casted devices. Moreover, from the IDVG curve of **Figure 45a**, a non-negligible off current is present, and this trait is common to all the devices composing the set. In **Table 10** are presented the mean values of the two different sets extracted from day 0 measurement. If we compare them to those relative to the bottom gated counterpart presented in **Table 7**, we can see that threshold voltage is quite similar, however, mobility is remarkably lower in both sets.

Table 10: Initial mean values for the main parameters of the considered set of samples for both drop-casted (top) and spin-coated (bottom). Mobility is very low, as well as I_{ON}/I_{OFF} ratio.

	V_{th} [V]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	I_{ON}/I_{OFF}
Drop-Casted	$1,3 \pm 9,9 \cdot 10^{-1}$	$1,9 \cdot 10^{-3} \pm 1,2 \cdot 10^{-3}$	10^2
Spin-Coated	$-1,9 \cdot 10^{-1} \pm 5,5 \cdot 10^{-1}$	$6,7 \cdot 10^{-4} \pm 3 \cdot 10^{-4}$	10

Since the semiconductor is protected from external agents that could cause a degradation, the expected result from an ageing analysis is that the mobility would vary very little over

time. This, however, is not what happened, as can be seen from **Figure 46** and **Figure 47**, respectively the evolution of mobility for drop-casted and spin-coated devices.

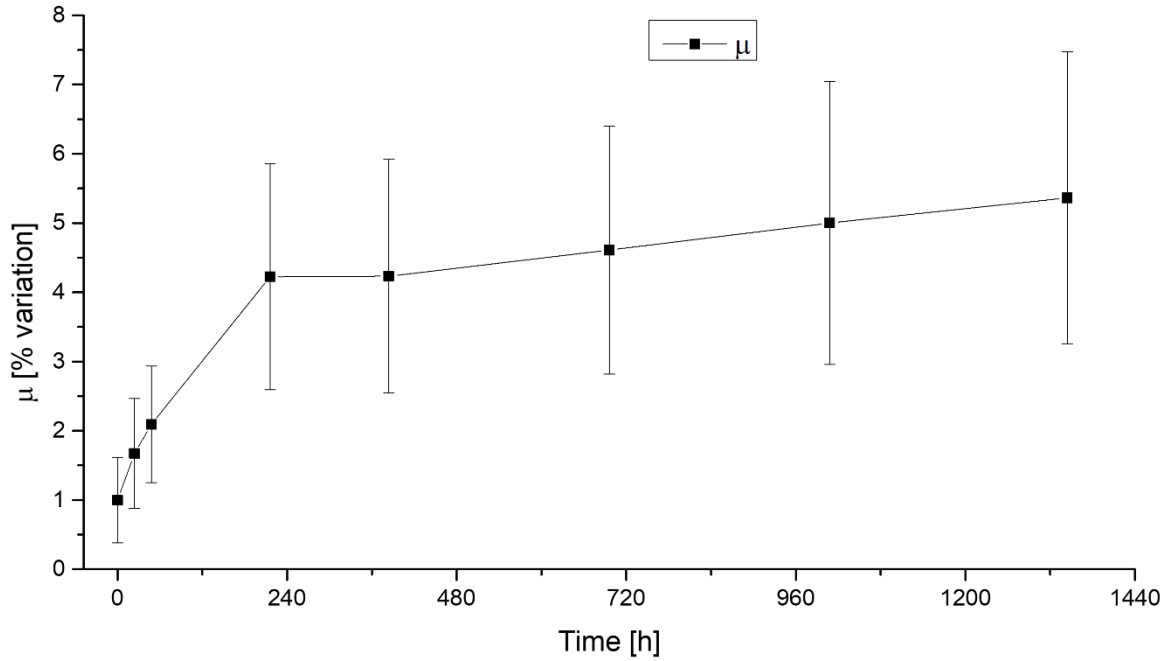


Figure 46: Average mobility evolution over time of drop-casted DPP-DTT semiconductor top gate-bottom contact transistors. Mobility has a steep increase in the first days of measurement and a slightly increasing trend in the consequent period.

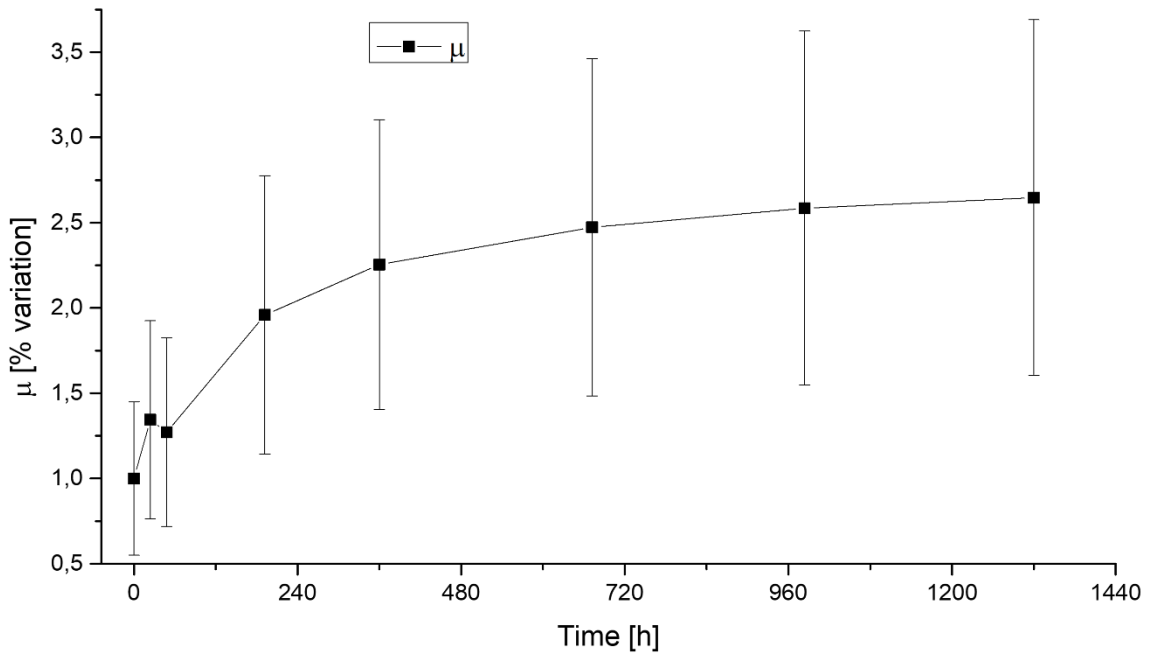


Figure 47: Average mobility evolution over time of spin-coated DPP-DTT semiconductor top gate-bottom contact transistors. Mobility has an increase in the first days of measurement and a slightly increasing trend in the consequent period.

Regarding the former set of devices, there is a steep increase in the first ten days of monitoring, followed by a slow but steady, almost linear, increase in the subsequent period.

The latter set has instead a quasi-logarithmic growth. Both are however characterized by very large shifts from the mean value, indicating that there are big differences in the statistical pool of devices. This behaviour might be related to the trapping of oxygen during the thermal annealing of the semiconductor, before dielectric deposition. As stated before, oxygen acts as a dopant for p-type organic semiconductor and a small quantity might be beneficial, since it increases the quantity of charge carriers available for conduction. Having then encapsulated the device, no more oxygen can be absorbed in the active layer, and thus degradation is heavily reduced, since the semiconductor is not exposed anymore. The intensity of this increase is consistent, but the reason might be that the mobilities were already so low to begin. Values, however, stayed very low even after this increase, very distant from those reported in literature^[169,170].

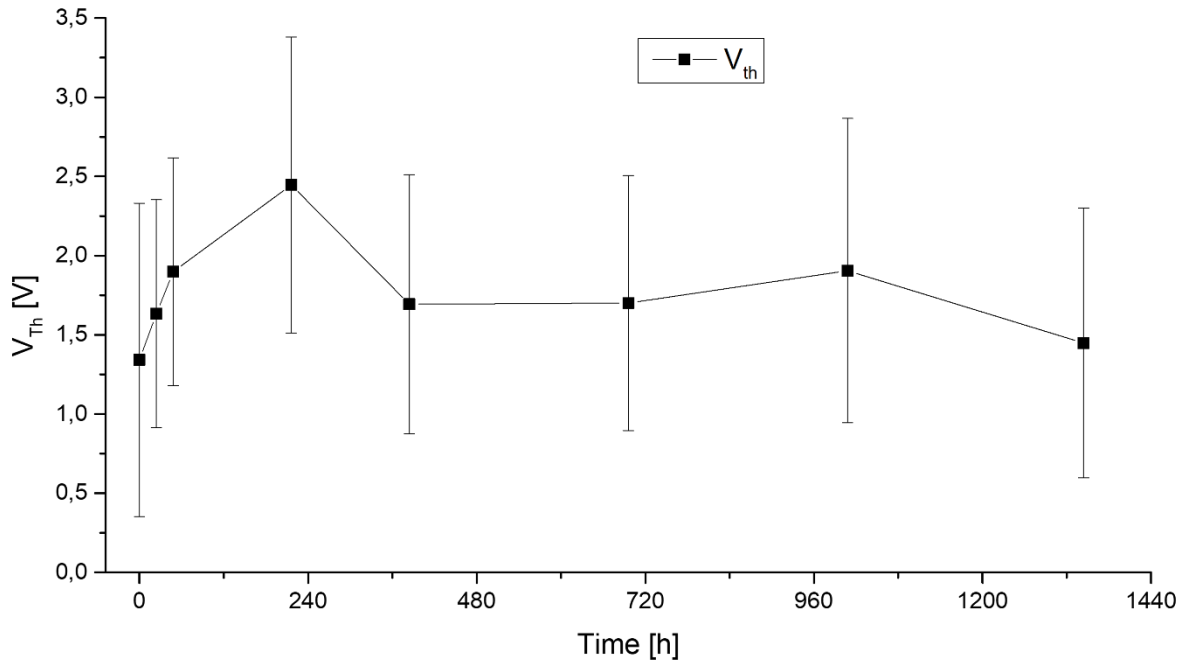


Figure 48: Average threshold voltage evolution over time of drop-casted DPP-DTT semiconductor top gate-bottom contact transistors. The average threshold voltage does not vary too much over time, however, also in this case there is much variation between the samples inside the batch.

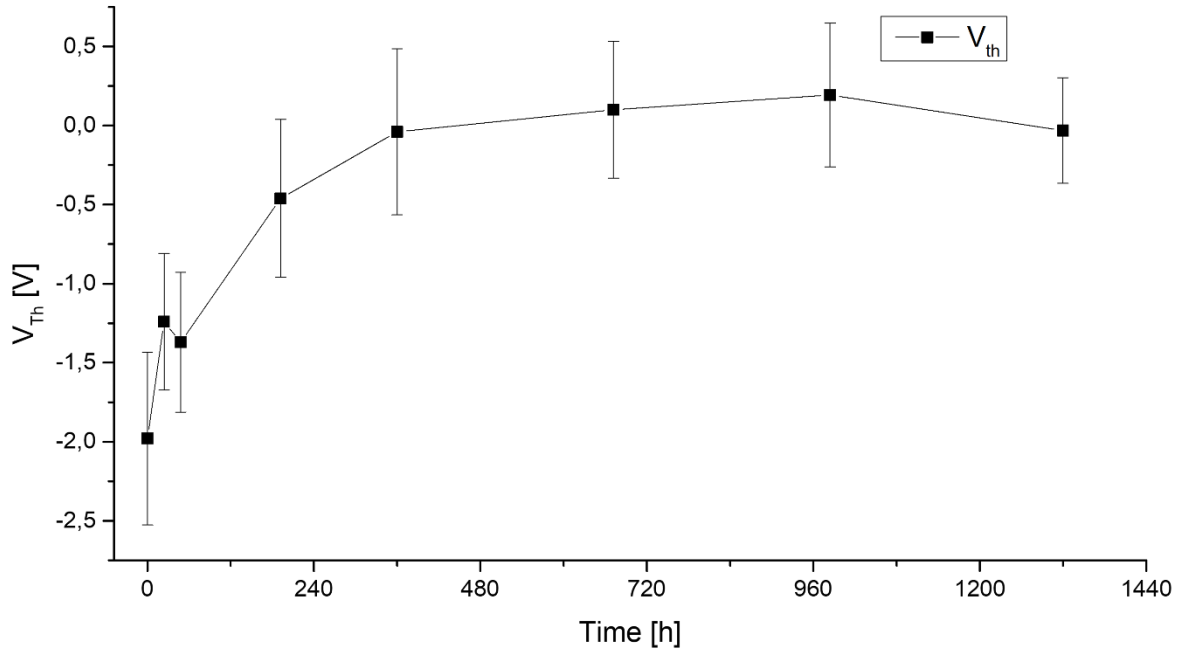


Figure 49: Average threshold voltage evolution over time of spin-coated DPP-DTT semiconductor top gate-bottom contact transistors. For this batch of devices, discrepancies among them are lower and the mean value shifts from negative toward zero.

Average threshold voltage has instead a different behaviour between the two sets of samples, with the drop-casted one, more stable around one value, while the spin-coated devices have a sensible shift, from negative values toward zero. In **Table 11** are reported the final values for both batches of samples.

Table 11: Final mean values for the main parameters of the considered set of samples for both drop-casted (top) and spin-coated (bottom). Mobility is very low, as well as I_{ON}/I_{OFF} ratio.

	V_{th} [V]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	I_{ON}/I_{OFF}
Drop-Casted	$1,5 \pm 8,5 \cdot 10^{-1}$	$1 \cdot 10^{-2} \pm 4 \cdot 10^{-3}$	10^2
Spin-Coated	$-3,1 \cdot 10^{-2} \pm 3,3 \cdot 10^{-1}$	$1,8 \cdot 10^{-3} \pm 7 \cdot 10^{-4}$	10

Even though the dielectric layer and the metallic gate offer a good protection to the semiconductor, such devices need further investigation. One hypothesis behind the low overall performance of the semiconductor in both configuration is that chlorine groups in Parylene C might have an impact on the conduction properties of DPP-DTT. Further investigation is being performed, with different top-gated devices fabricated with various dielectric to have a confirmation or denial of the truth of this hypothesis.

Moving on to the next set of devices, these are fabricated using once again, N1400 as semiconductor. In **Figure 50** are reported characteristic and transfer characteristic curves relative to a single device while in **Table 12** are reported the mean initial values of all the

devices analysed. Output current is relatively low, but comparable with the bottom-gated devices realized with same semiconductor, but, comparing it with the curves in **Figure 42**, we can say that the behaviour is more stable, allowing for a better characterization.

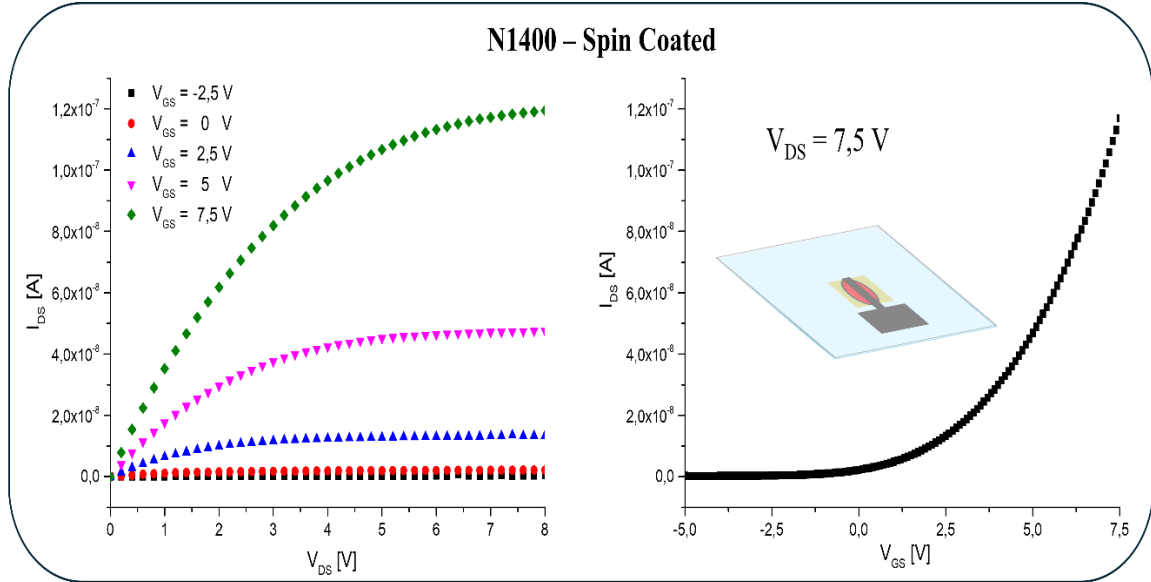


Figure 50: Characteristic (left) and transfer characteristic (right) of a transistor with n-type semiconductor N1400. A sketch of the device is presented on the right.

Table 12: Initial mean values for threshold voltage and mobility for the set of samples realized with n-type semiconductor N1400.

V_{th} [V]	μ [$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$]	I_{ON}/I_{OFF}
$7,5 \cdot 10^{-1} \pm 4,3 \cdot 10^{-1}$	$6,5 \cdot 10^{-3} \pm 2,2 \cdot 10^{-3}$	10^2

One fact that can be said, comparing this with the devices presented in **Figure 45**, is that samples realized with N1400 semiconductor in this structure have a good field effect. Moreover, contact resistance is always negligible, if present, meaning that the interface with the metal electrodes is optimal. This is very important, because the hopping mechanism is heavily dependent on the height of the energy barrier between semiconductors and electrodes, being them organic or inorganic.

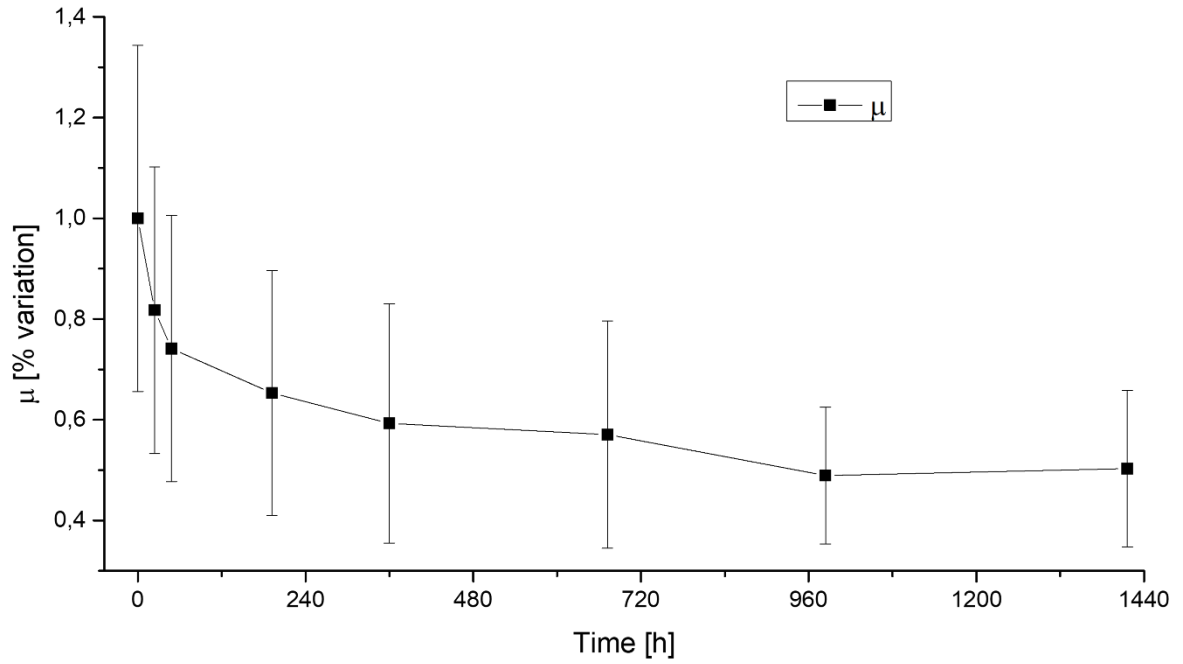


Figure 51: Average mobility evolution of the samples considered for statistical measurements. Although the dielectric layer should act as a barrier for degradation, effects of it are clearly evident. Oxygen infiltration before dielectric deposition might be the cause. Mobility is reported in percentage variation from the initial value normalized to 1.

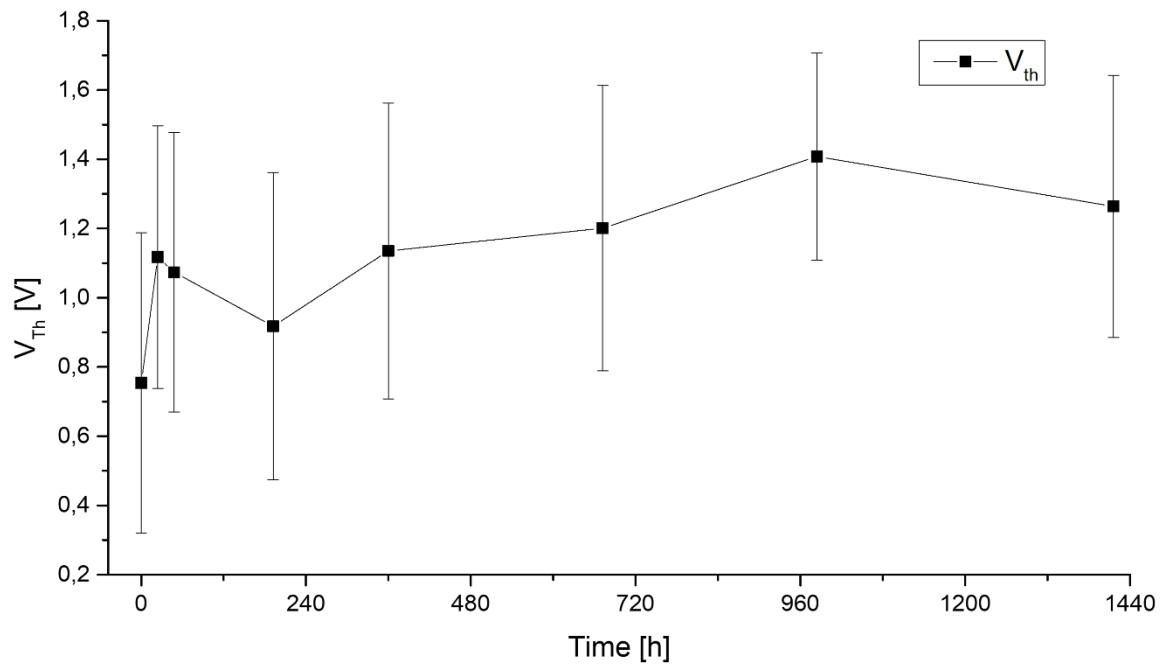


Figure 52: Average threshold voltage evolution of the samples considered for statistical measurements. In an ideal device, this value should be constant or vary very little, since it defines the working point.

Although, in principle, the top gate structure should offer protection to the active layer from degradation, it seems that in this case mobility is affected by some detrimental factor, as shown in **Figure 51**. This might be an indication of a poor quality of the Parylene C film used as dielectric, but there might be also issues directly related to the semiconductor

structure, like poor molecular planarity that could hinder charge transport. **Figure 52** shows, as for any other device analysed, that fluctuations in the threshold voltage value are present and substantial, with, sometimes, ample differences among the devices of the same set.

Top gate-bottom contact structure showed some advantages as well as disadvantages. The fact that the structure is inherently self-encapsulating, offers a level of protection to the semiconductor, effectively lengthening the lifespan of the device, even though some level of imperfection during the fabrication process, could lead to side effects that could affect negatively the device performance. Moreover, the height of the semiconductor forces the dielectric to be thicker, reducing the control of the gate over the channel.

4.2.3 Double Gate-Bottom Contact Architecture

The double gate-bottom contact architecture can be considered as a stack of the previous two. Starting from a bottom gate-bottom contact architecture, a second dielectric layer and a second gate are deposited on top of the structure. The presence of two gates offers a mean of control over the working point of the device. In fact, while one gate is used to bias the device, the other one can be used to shift the threshold voltage, setting it to a preferred value. In this way, having a set of devices that should work together, they all might be set to have the same working point. This control over the threshold voltage is demonstrated in **Figure 53** in which are reported different IDVG curves relative to a device. The tension sweep is performed from the bottom gate, while for each curve, a different top gate V_{GS} is applied. Since the semiconductor used is a p-type one, for positive V_{GS} , the output current tends to decrease, while for negative V_{GS} , output current increases.

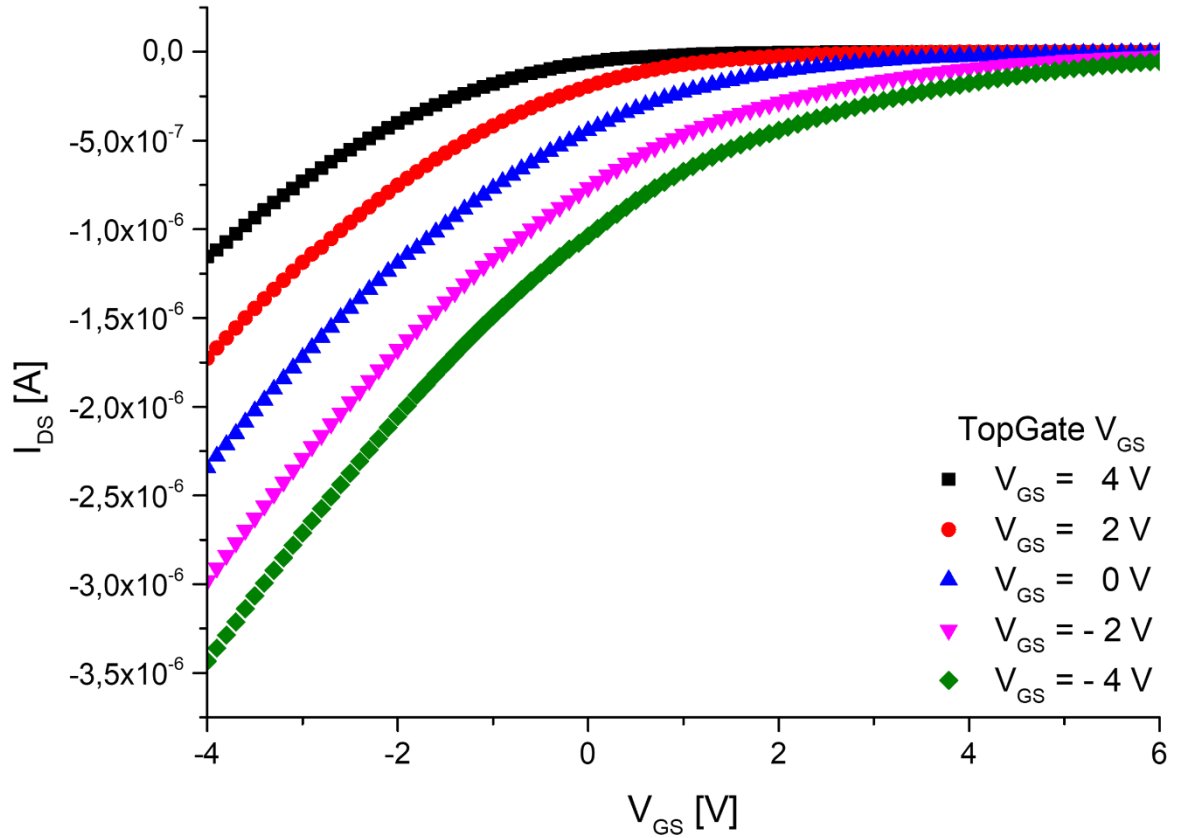


Figure 53: IDVG curves of a double gate device biased from the bottom gate, always in the same conditions, and with a different V_{GS} applied to the top gate for every curve. Output current varies sensibly due to the effect on both threshold voltage and mobility.

The variation in output current, depending on the voltage difference applied from the top gate, is sensible. The increase or decrease is strictly related to the shifts in threshold voltage, as well as mobility. For positive V_{GS} , not only the V_{Th} is shifted toward more negative values, meaning that the transistor switches on later, but also mobility is decreased, due to the inferior number of carriers available for conduction. The opposite can be said when a negative V_{GS} is applied. This happens because the semiconductor is bulk enough to support the formation of two channels, both contributing to charge transport. For thin semiconductor layers, this doesn't happen and, when biasing with the same polarity from both gates, a disruptive effect arises. One thing that is worth noting is that the response of both threshold voltage and mobility to the applied top gate voltage is somewhat linear, as shown in **Figure 54** and **Figure 55**. In these figures are reported two sample devices, one realized with TIPS-Pentacene, the other with DPP-DTT. The linearity of the response is evident, and this could be used to determine, with some prior calculation, the needed top gate V_{GS} to set the working point of the device at a desired value.

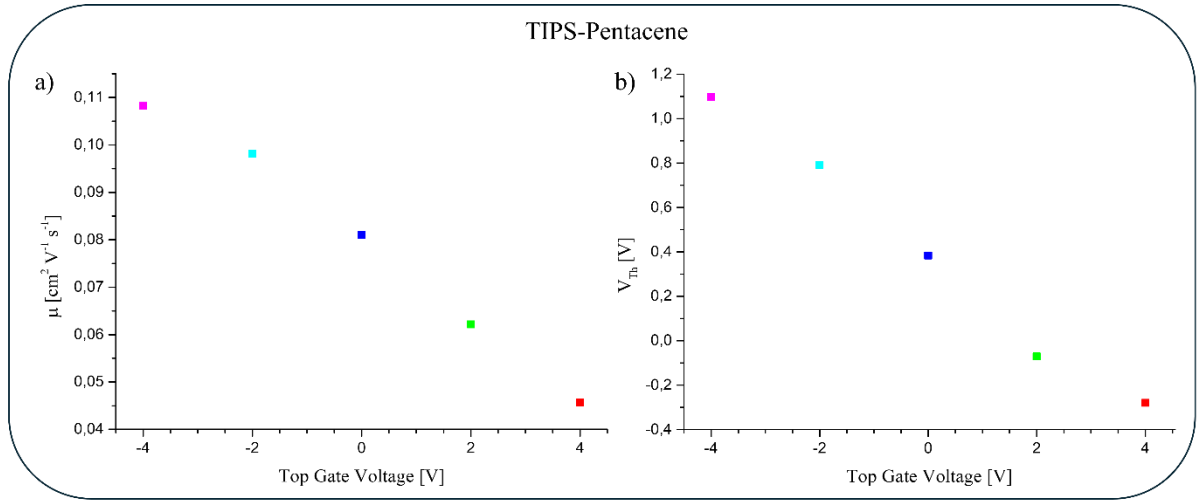


Figure 54: Device properties variation when different top gate voltages are applied: a) mobility and b) threshold voltage have a quasi-linear variation in the considered range. Semiconductor used is TIPS-Pentacene.

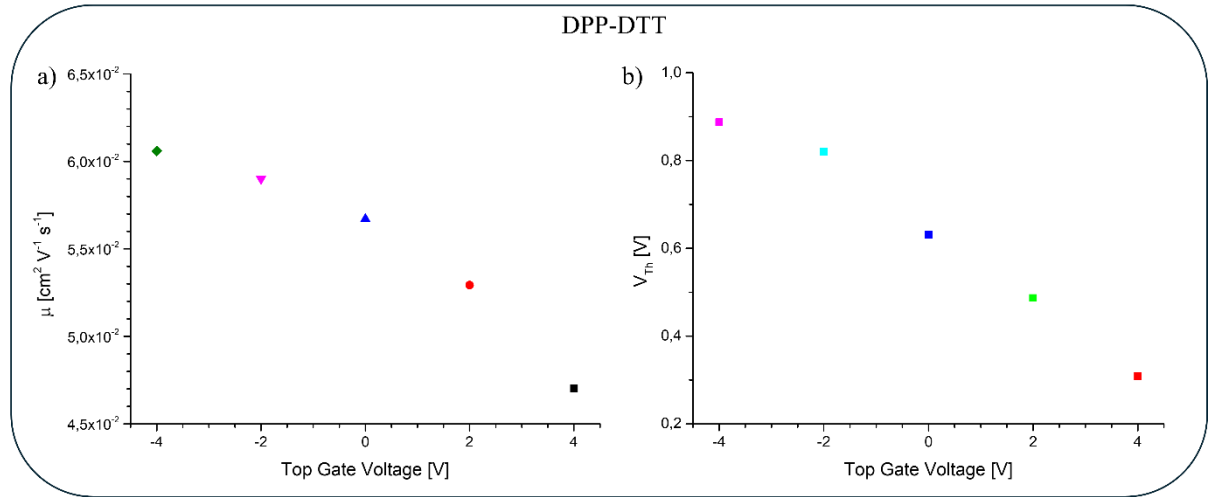


Figure 55: Device properties variation when different top gate voltages are applied: a) mobility and b) threshold voltage have a quasi-linear variation in the considered range. Semiconductor used is DPP-DTT deposited through drop casting.

Knowing this, double gate architecture already presents some advantages with respect to the other two, thanks to the possibility to tune the working point of the device through one of the gates. The top gate part not only adds a level of control over the device, but also protects the active layer from degradation that might be caused by oxygen or moisture. It therefore a self-encapsulating structure, where the encapsulation part is an active element of the device functionalities.

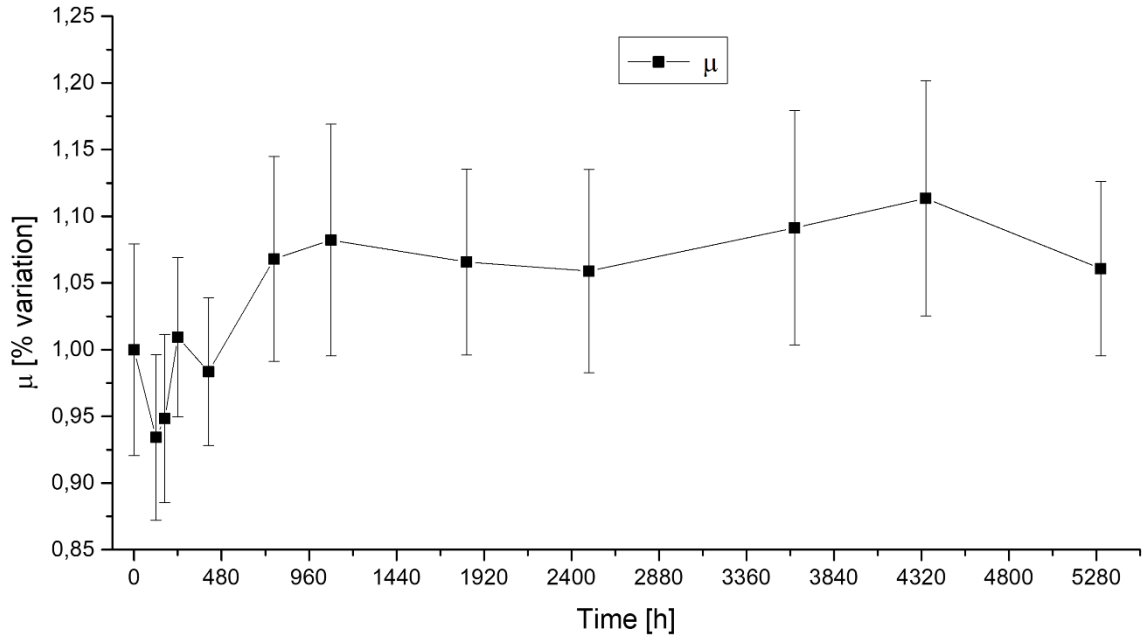


Figure 56: Average mobility evolution over time of TIPS-Pentacene semiconductor double gate-bottom contact transistors. Mobility variations over time are nearly negligible, with minimum shifts from the mean of the devices. Data is presented in percentage variation with respect to day 0 of measurement, with the value normalized to 1.

Encapsulation that is, however, crucial in the stability of the devices over time. Although oxygen and moisture are not the only elements that can cause a reduction of mobility, it is clear that devices taken into consideration are very stable for what concerns this aspect. This is an ulterior reason to favour this structure over the others, for long term applications, since it is very robust and reliable. Considering **Figure 57**, we can see a conspicuous shift toward positive values of the threshold voltage. This effect could be related to charges that were previously hold in trapped states and are released, contributing to charge mobility and allowing a faster formation of the channel. This shift, as said before, can be balanced by applying a positive voltage from the top gate, thus shifting once again the threshold voltage toward the desired value.

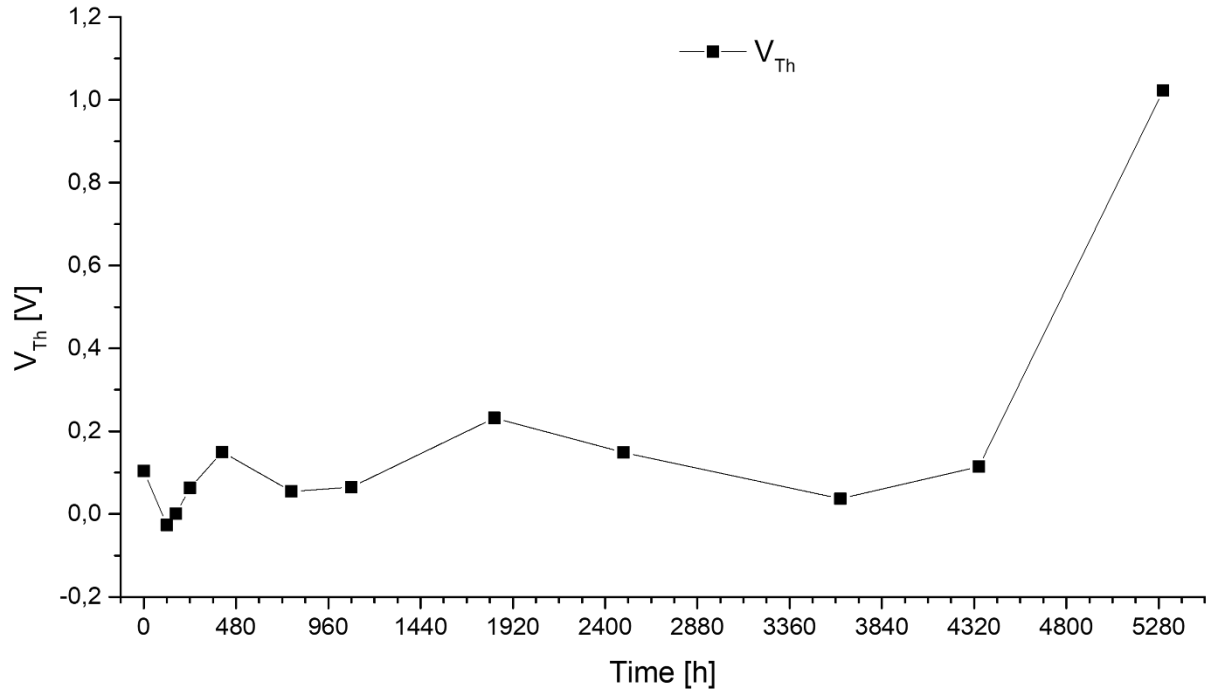


Figure 57: Average threshold voltage evolution over time of TIPS-Pentacene semiconductor double gate-bottom contact transistors. The shift toward more positive values could be related to de-trapping of charges.

To further highlight the goodness and stability of double gate architecture, **Figure 58** offers a comparison between the evolution of mobility over time in two different architectures considered, double gate and bottom gate. While the former is nearly constant, the latter has a first drop almost immediately and then another one after remaining almost constant for a good amount of time. In **Table 13** are reported threshold voltage, mobility and I_{ON}/I_{OFF} mean values relative to the sample devices examined.

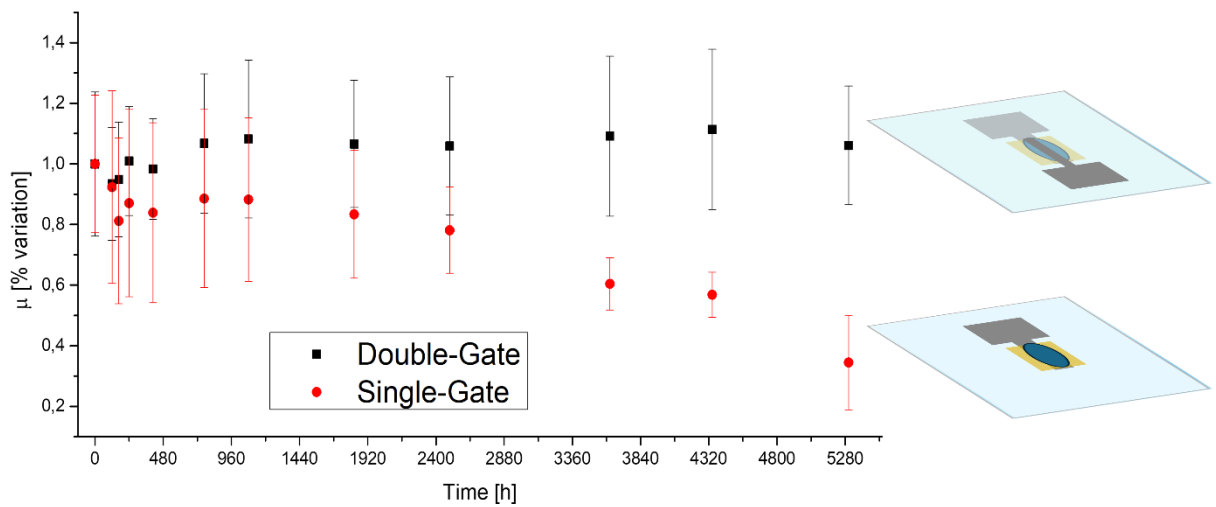


Figure 58: Average mobility evolution comparison of double gate devices vs single gate devices, realized with TIPS-Pentacene as semiconductor. On the right side, a sketch of the two species of devices is shown. Data is presented in percentage variation with respect to day 0 of measurement, with the value normalized to 1.

Table 13: Average threshold voltage, mobility and I_{ON}/I_{OFF} values relative to double gate transistors. Reported are day 0 of measurement and after 5300 hours, correspondent to 221 days.

	V_{th} [V]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	I_{ON}/I_{OFF}
Day 0 (0 h)	$1,8 \cdot 10^{-2} \pm 4,1 \cdot 10^{-1}$	$1,4 \cdot 10^{-1} \pm 1,1 \cdot 10^{-2}$	10^3
After 5300 h	$5,6 \cdot 10^{-1} \pm 1,1$	$1,5 \cdot 10^{-1} \pm 9,3 \cdot 10^{-3}$	10^3

Since DPP-DTT, for some applications, like strain sensor, is more suitable due to its structure, the same comparison has been practised for devices realized with such semiconductor. Once again, two sets of samples were realized, one in which the semiconductor was drop-casted and the other one in which it was spin-coated. Similarly to what happened with the devices realized in the same way with the other structure, performances of the latter are worse. This might be an indication that the semiconductor layer in this case is too thin to offer a good charge carrier conduction, leading to a poor mobility. Such difference in performances is evident from **Figure 59**, where the output current difference is almost two orders of magnitude.

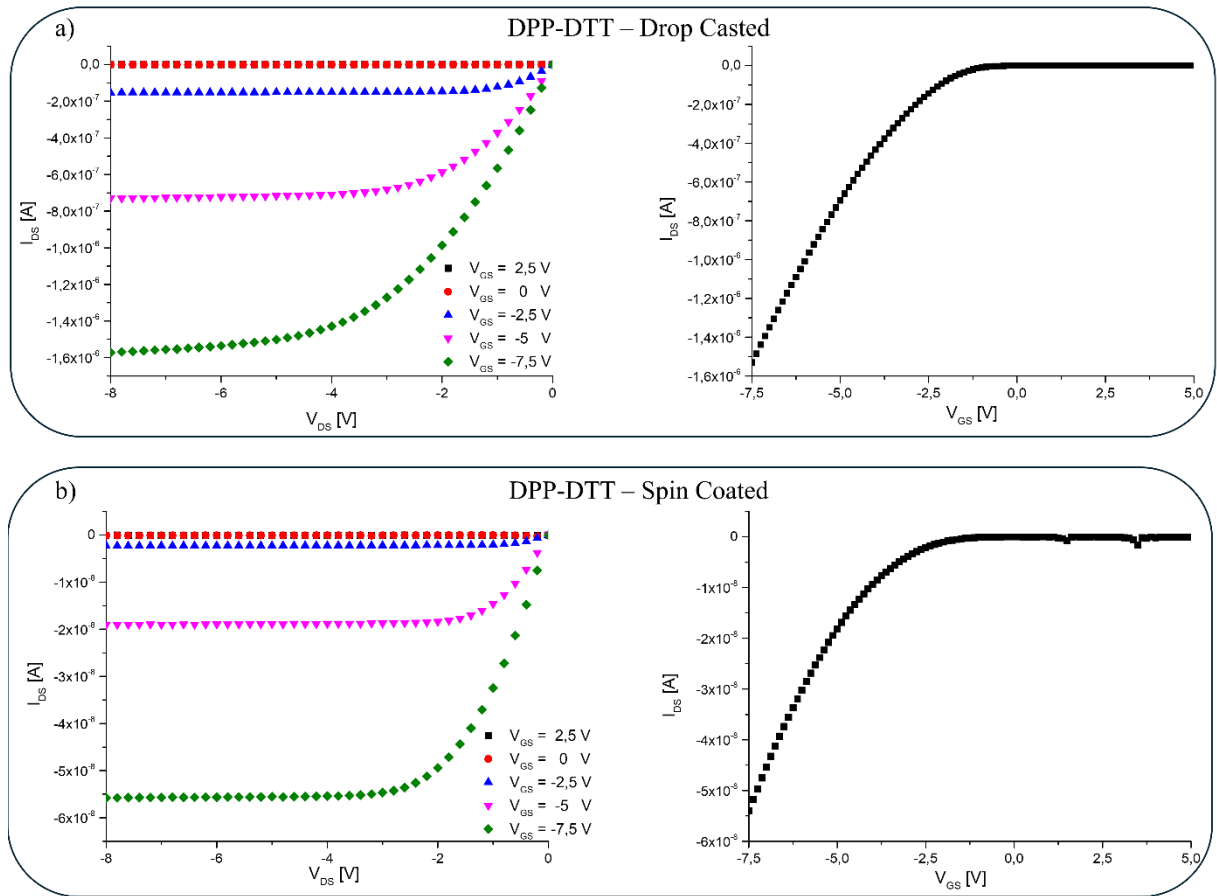


Figure 59: Characteristics and transfer characteristics of two example devices realized with the same semiconductor deposited through different techniques. Both sets of devices were tested in the same conditions. a) Semiconductor has been drop-casted. b) Semiconductor has been spin-coated. Output current of the two sets of devices has sensible difference.

Table 14: Average threshold voltage, mobility and I_{ON}/I_{OFF} values relative to double gate transistors realized with DPP-DTT as semiconductor.

	V_{th} [V]	μ [$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$]	I_{ON}/I_{OFF}
Drop-Casted	$-2,5 \cdot 10^{-1} \pm 3,3 \cdot 10^{-1}$	$3,4 \cdot 10^{-2} \pm 1,2 \cdot 10^{-2}$	10^3
Spin-Coated	$-2,1 \pm 8,3 \cdot 10^{-1}$	$2 \cdot 10^{-3} \pm 7,4 \cdot 10^{-4}$	10

In **Table 14** are reported values extracted at day 0 for both sets of samples. The combination of low mobility and late channel formation give as a result a very poor output current for the spin-coated devices. Analogously to what happened for the top-gated devices, also in this case mobility has an increase, shown by both sets of devices and reported in **Figure 60** and **Figure 61**, this time with a more sensible variation detected for the spin-coated devices. It has to be noted, however, that some of the devices of this latter set completely stopped working due to short circuits that arose between the top gate and the semiconductor. Therefore, study on this issue is still underway, to better understand the mechanisms behind the increase in mobility, that in both cases doesn't seem to follow any specific trend. Once again, trapping of limited quantities of oxygen before top dielectric deposition could partially explain this behaviour, as well as effect of the dielectric itself on the semiconductor molecules. Mobility increase is not something to be ignored, since it could enhance performances of devices, but what causes this is still under investigation. If we could find the way to control and even enhance or speed up this effect, it could lead to the realization of high performing devices.

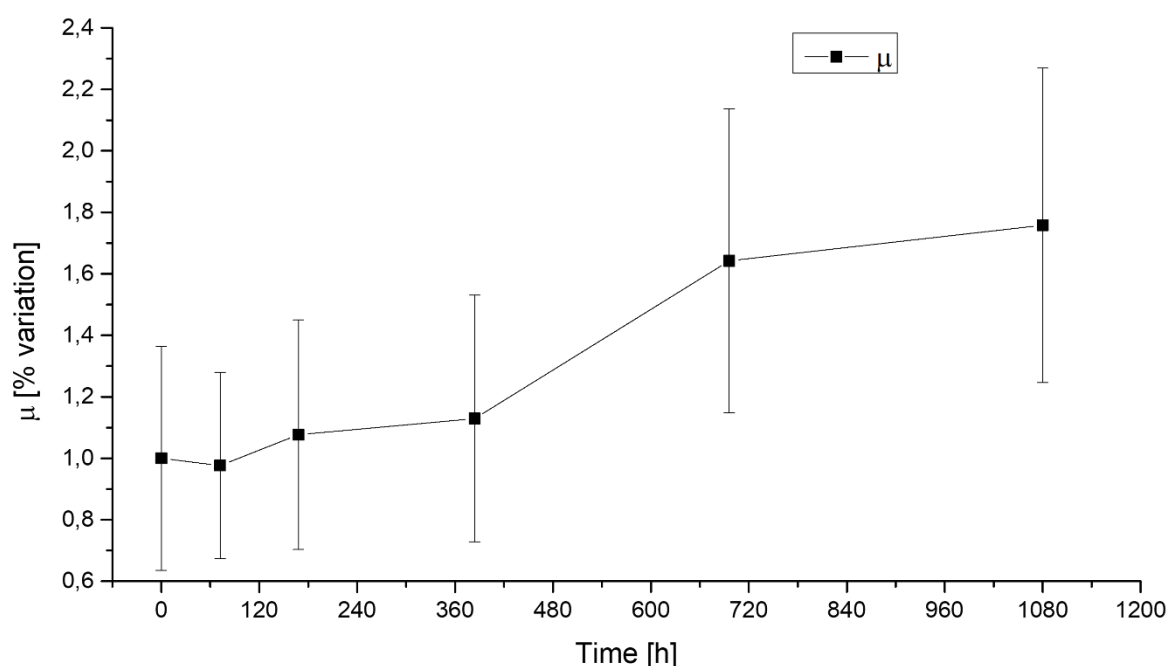


Figure 60: Average mobility evolution over time of drop-casted DPP-DTT semiconductor, double gate-bottom contact transistors. Mobility tends to increase but differences between device are remarkable. Data is presented in percentage variation with respect to day 0 of measurement, with the value normalized to 1.

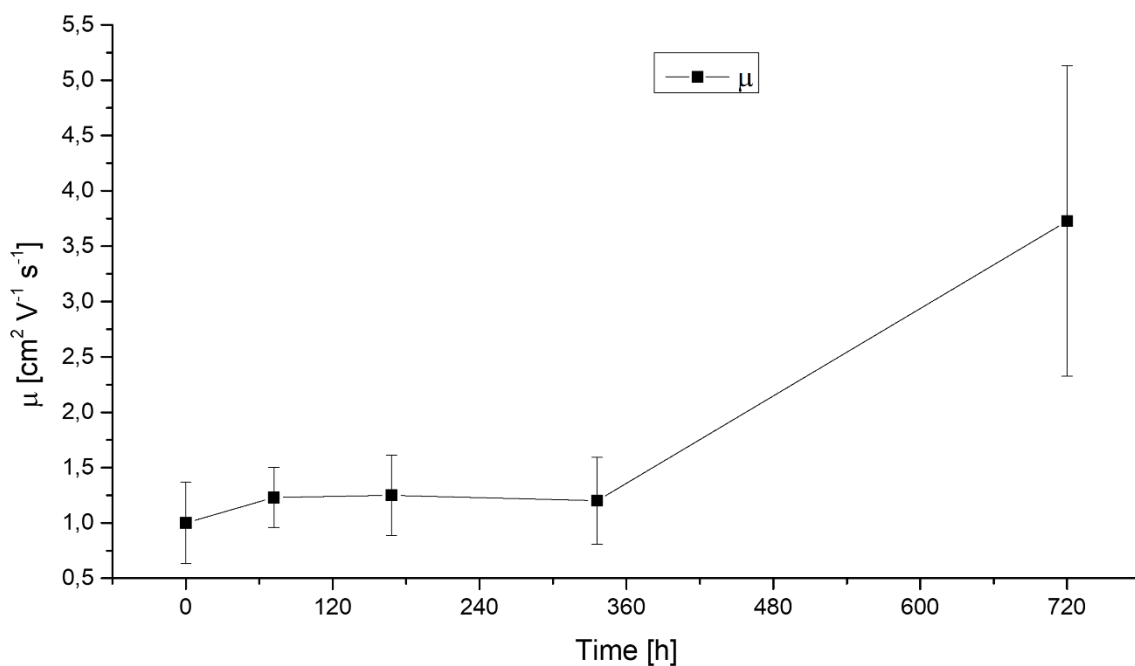


Figure 61: Average mobility evolution over time of spin-coated DPP-DTT semiconductor, double gate-bottom contact transistors. Mobility seemed to be stable, but something happened and there was a sensible increase. Data is presented in percentage variation with respect to day 0 of measurement, with the value normalized to 1.

Double gate architecture proved itself to be a reliable OTFT configuration, due to its versatility, robustness and reliability. Thanks to the presence of two gate, the control over threshold voltage, and therefore channel formation, is enabled and available in every moment of the device lifetime. In principle, it could be decided to set this parameter during fabrication process of an OTFT^[82], however, the device wouldn't have the tunability offered by a double gate configuration. Moreover, this property is joined by the protection offered to the active layer by the top gate structure and the bottom gate-bottom contact better field effect. Having a second gate, and here lies probably the most interesting aspect of such architecture, is the possibility to use the second gate as a charge sensor, effectively realizing a device that combines the amplification properties of the transistor with the sensing properties of a sensor. Although the devices perform well, limitations given by the fabrication process lead to performances lower than those reported in literature.

5. Chapter V: Mechanical characterization of flexible double-gate organic field effect transistors for tactile applications

The idea behind the fabrication of such devices is to use them as sensors. The functioning principle is quite simple. Since the top gate is easily accessible, it can be used to sense charge variation inducted by external stimuli such as temperature variations or the application of a force in a specified region. The advantage of using a transistor for such operation is its intrinsic property of amplification of electric signals. In this way, the external stimulus is directly connected to the charge passing through the channel and is recognized by the device. For this reason, a measurement protocol for the characterization of devices for recognition of mechanical quantities variation has been developed. A set of five devices has been paired with capacitors of different dimensions, realized with a commercial PVDF, and characterized in response to temperature and force stimuli. The capacitors dimensions chosen for the characterization are $1 \times 1 \text{ mm}^2$, $3 \times 3 \text{ mm}^2$, and $5 \times 5 \text{ mm}^2$. Once each device was characterized for both stimuli with every capacitor, sensitivity was calculated, to determine if such transistor structure is suitable for use as a sensor. Detailed information on measurement setups will be given in the relative sections of this chapter.

5.1 Temperature characterization

At first, devices were characterized as temperature sensors. To do so, the setup comprised a Peltier Cell, used to heat up or cool down the PVDF capacitor, power supplies to power up the Peltier Cell and the pyrocouple used to monitor the cell temperature, two source meter to supply the transistor and read the pyrocouple and a notebook to keep track of the various passages. The PVDF capacitor is positioned onto the Peltier Cell, one of the plates is connected to the top gate of the device, the other to the source. Its temperature is monitored through the optical pyrocouple which is connected to the measuring system. For this characterization it was chosen to use the hot side of the Peltier Cell. A sketch of the setup is presented in **Figure 62**. The transistor, before starting measurement, is characterized to set the optimal V_{GS} and V_{DS} to work with.

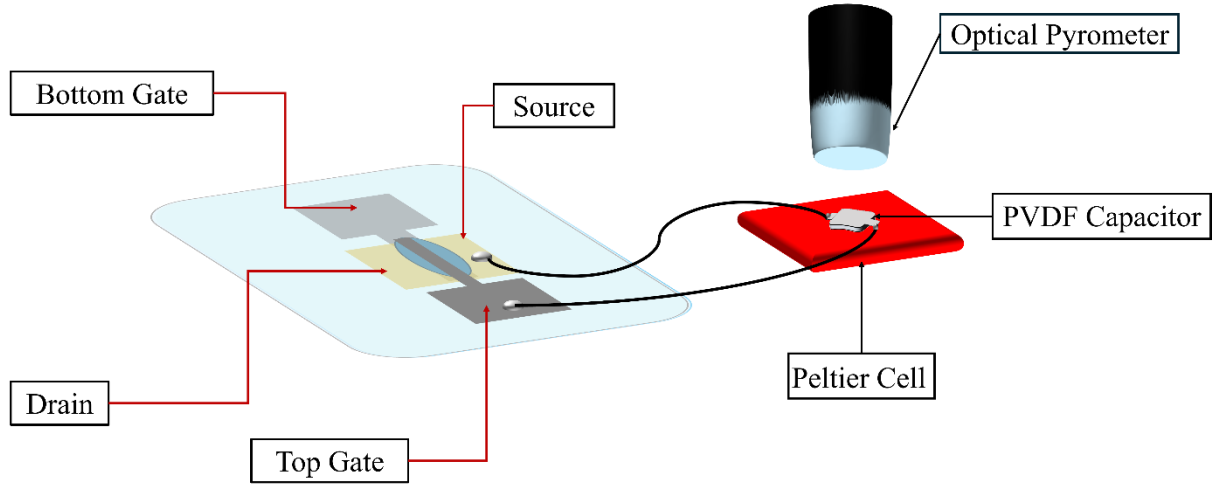


Figure 62: Setup for temperature measurement. The PVDF capacitor is positioned onto the Peltier Cell and temperature is monitored through an optical pyrocouple connected to the measuring system.

Once parameters are decided, a flipping test is performed to check if the device and the capacitor are properly connected to each other and if there isn't any loose wiring. An example of flipping test is presented in **Figure 63**, where both plates of the capacitor were alternatively connected to the top gate, inducing on it a charge that effectively modifies the overall current in the transistor's channel. For easiness of comprehension, the regime in which channel current increases will be called switch-on mode, the contrary will be addressed as switch-off mode. This test is a first step into the characterization of a transistor as a sensor and actually serves as a demonstration of the fact that it can be used as such, since the response to the external stimulus is far from being negligible.

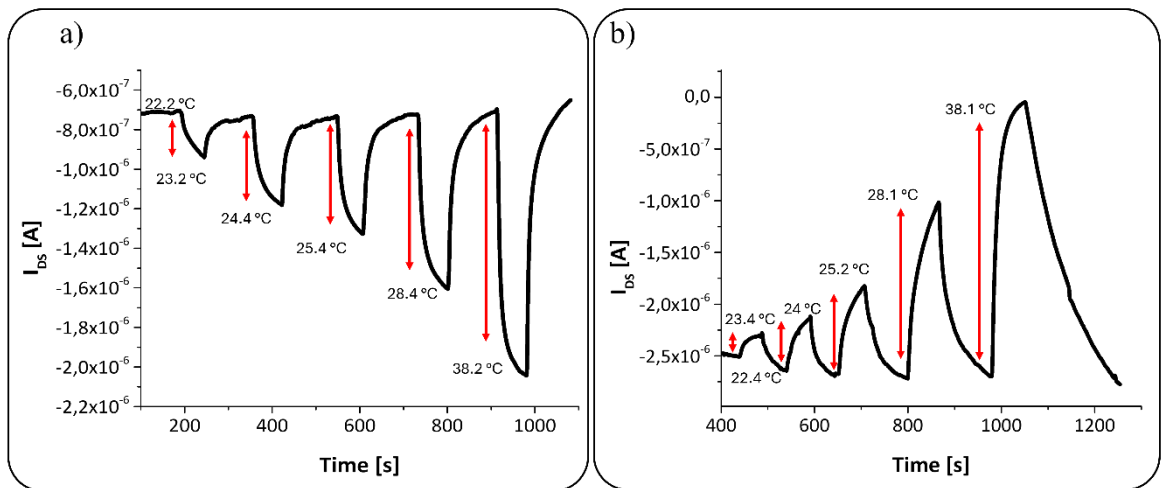


Figure 63: Flipping test of a device connected to a $3 \times 3 \text{ mm}^2$ capacitor: a) the capacitor plate connected to the top gate induces on it a negative charge, increasing the current in the channel; b) the capacitor plate connected to the top gate induces on it a positive charge, reducing the current in the channel.

The characterization protocol for each device with every considered capacitor is the following: as previously mentioned, V_{GS} and V_{DS} are decided after taking a transfer characteristic curve, so that the devices are in saturation region and fairly stable during the whole measurement, with nearly negligible drift. Each chosen temperature interval was performed five times, and each time, before every step, the temperature of the Peltier Cell was brought back to the initial temperature by waiting that it cooled down by itself, with a little help from a fan, hence the total length of the measurement. The higher the temperature shift, the higher the effect on the current.

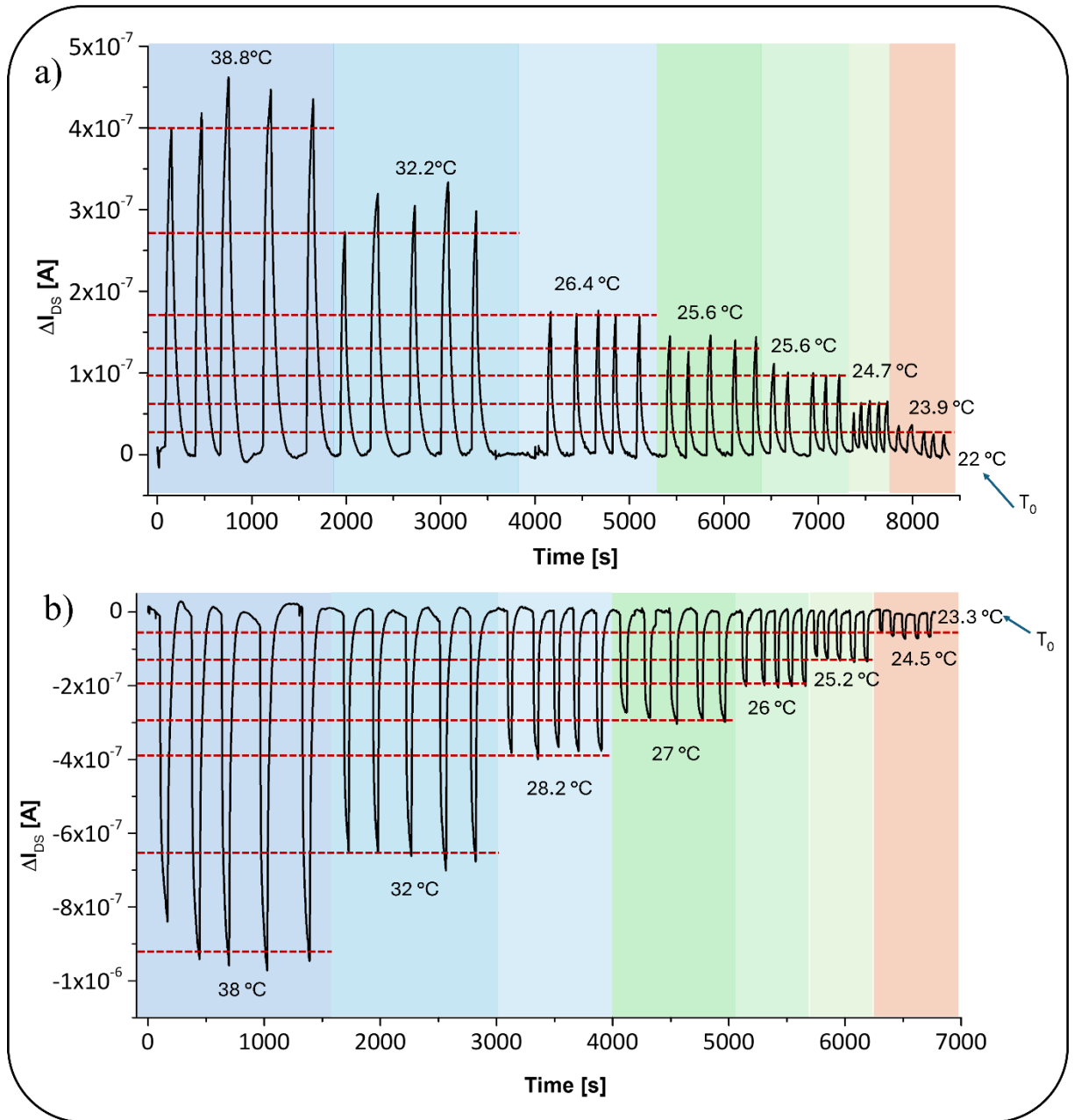


Figure 64: Channel current variation ΔI_{DS} of a device, characterized in both sense of polarization from the top gate, given by the induced charge of a PVDF capacitor: a) reduction in I_{DS} induced

by capacitor; b) increase in IDS induced by capacitor. Initial temperature and temperature reached in every step is reported in both graphs

In **Figure 64** are presented the responses in terms of current variation inside the channel over time, of a sample device under the action of the PVDF capacitor connected alternatively to the top gate with both plates. What is evident from this analysis is that the response of the device to the stimuli is quick and fairly reproducible, especially at lower ΔT . For higher ΔT , some trapped charge might have been released, leading to a higher shift in current in some cases. From the characterization of each device with all three capacitors, average sensitivities were extrapolated. In **Figure 65** are presented the graphs with the mean values for all considered device and all three capacitors employed; response is almost linear for all three, although for the 25 mm² response saturates after a certain limit of temperature variation. This is probably related to the amount of charge generated by induction, that reaches the limit of injection.

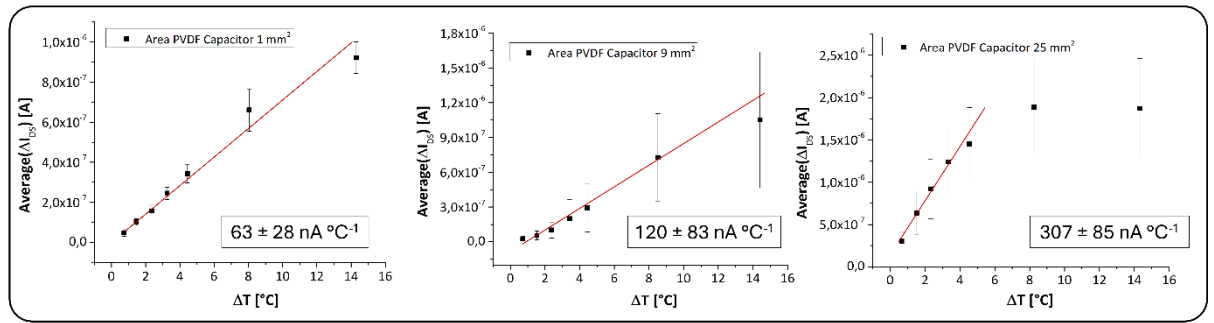


Figure 65: Average switch-off sensitivities among all the device for each capacitor, from left to right, 1x1 mm², 3x3 mm², and 5x5 mm². Response is approximately linear, apart from the last one, where response saturates after a certain temperature.

Table 15: Average sensitivities for both switch-off and switch-on modes of characterization of the devices, reported in current variation of nA per degree of temperature variation. The switch-off mode results overall more sensitive than the switch-on.

Capacitor Area [mm ²]	Average sensitivity switch-off [nA °C ⁻¹]	Average sensitivity switch-on [nA °C ⁻¹]
25	307 ± 85	200 ± 36
9	120 ± 83	68 ± 53
1	63 ± 28	22 ± 8

In **Table 15** are reported the average sensitivities relative to all the devices tested as sensors. From the data, switch-off mode seems to be more efficient than switch-on mode. What's interesting though, is the possibility to tune the device sensitivity and temperature range, simply varying the dimensions of the capacitor, which is important depending on the application chosen. For example, in artificial skin applications, it is important to have the

widest temperature range possible, to effectively monitor human parameters, and thus a smaller capacitor would reveal more efficient with respect to a bigger one. Of course, the same argument about reliability and reproducibility already discussed in the previous chapter is valid also in this case. Therefore, to prove the goodness of such device used as a sensor, a hysteresis test was performed, to see if the devices would respond in the same way in both directions of variation of the temperature. Four different temperature gradients were chosen, each one repeated three times, first ascending and then descending. The results of such test are reported in **Figure 66** and show how the devices are reliable also regarding this aspect. In fact, response in both directions is nearly symmetrical with respect to the peak temperature, and sensitivity in both forward and backward gradient shift is highly comparable.

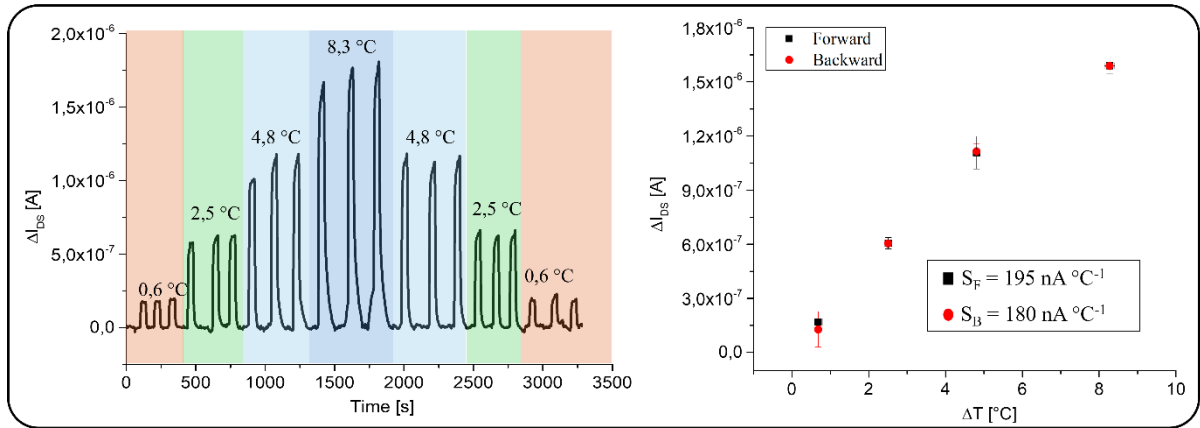


Figure 66: Hysteresis evaluation of the device when submitted to a an increase and then a decrease in temperature gradient with respect to an initial temperature. Sensitivity in both directions is highly comparable.

5.2 Force characterization

The same devices were then characterized as force sensors. To do so, the PVDF capacitors were positioned beneath the indenter of a dynamometer to apply a fixed force. To be sure that the force is applied uniformly, and no effects arise from possible pressure on the wirings, a 2 mm thick of PDMS was used. This way, since the indenter area was bigger than the capacitors' area, it was ensured to apply the force only on the intended area. A sketch of the measuring setup is presented in **Figure 67**.

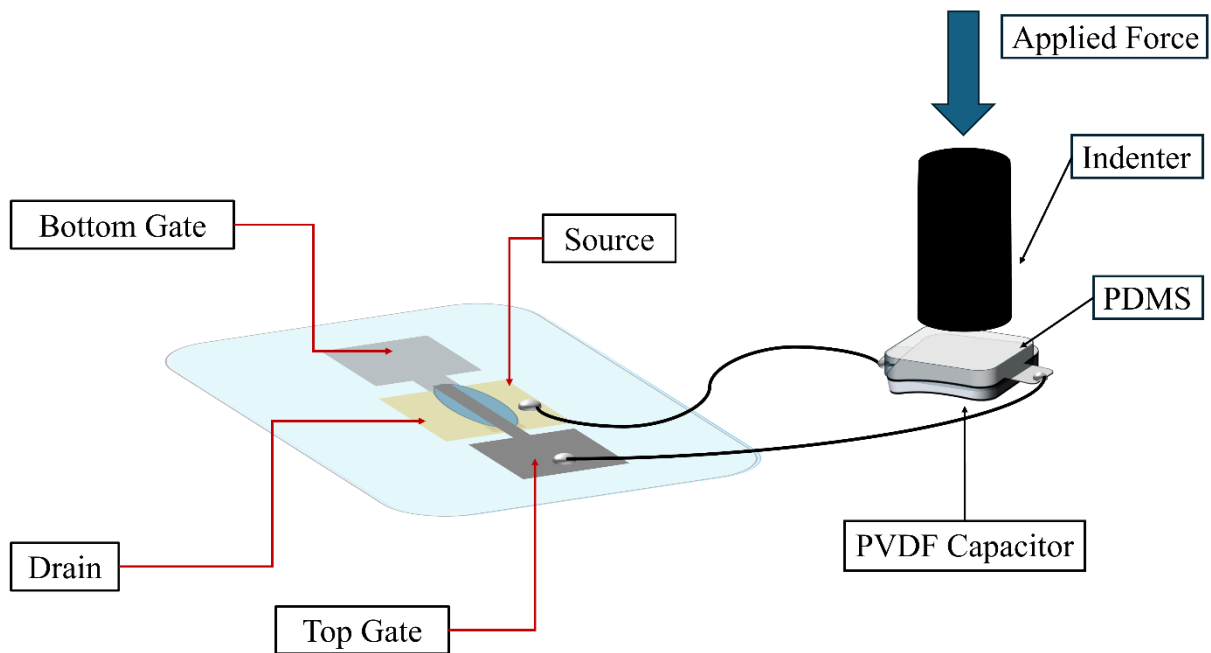


Figure 67: Setup for force measurements. An indenter, connected to a dynamometer, is used to apply a determined force uniformly on the PVDF capacitor.

The dynamometer used to apply the force is directly connected to the PC and controlled via its own program. This way, we could set the preferred force and monitor its correct application. Moreover, application cycles can be implemented, so that a force can be applied a certain number of times without modifying the interval between each application. Also, approach and release speed had been adjusted to limit proximity effects and bouncing of the PDMS. The protocol chosen to operate this characterization is quite similar to that of temperature characterization. Seven different values of force were selected, and, starting from the smaller value, they were all applied five consecutive times. After every 5 steps, force value was increased directly from the program during the rising cycle of the indenter. After the higher force value had been applied, measurement could end, and analysis made. Analogously to what had been done for temperature measurements, also forces were applied

in both switch-off and switch on modes of the capacitor. Results obtained for one of the devices are presented in **Figure 68**. The chosen forces to apply were, in Newton (N): 0.25, 0.5, 0.8, 1, 2, 3, and 5.

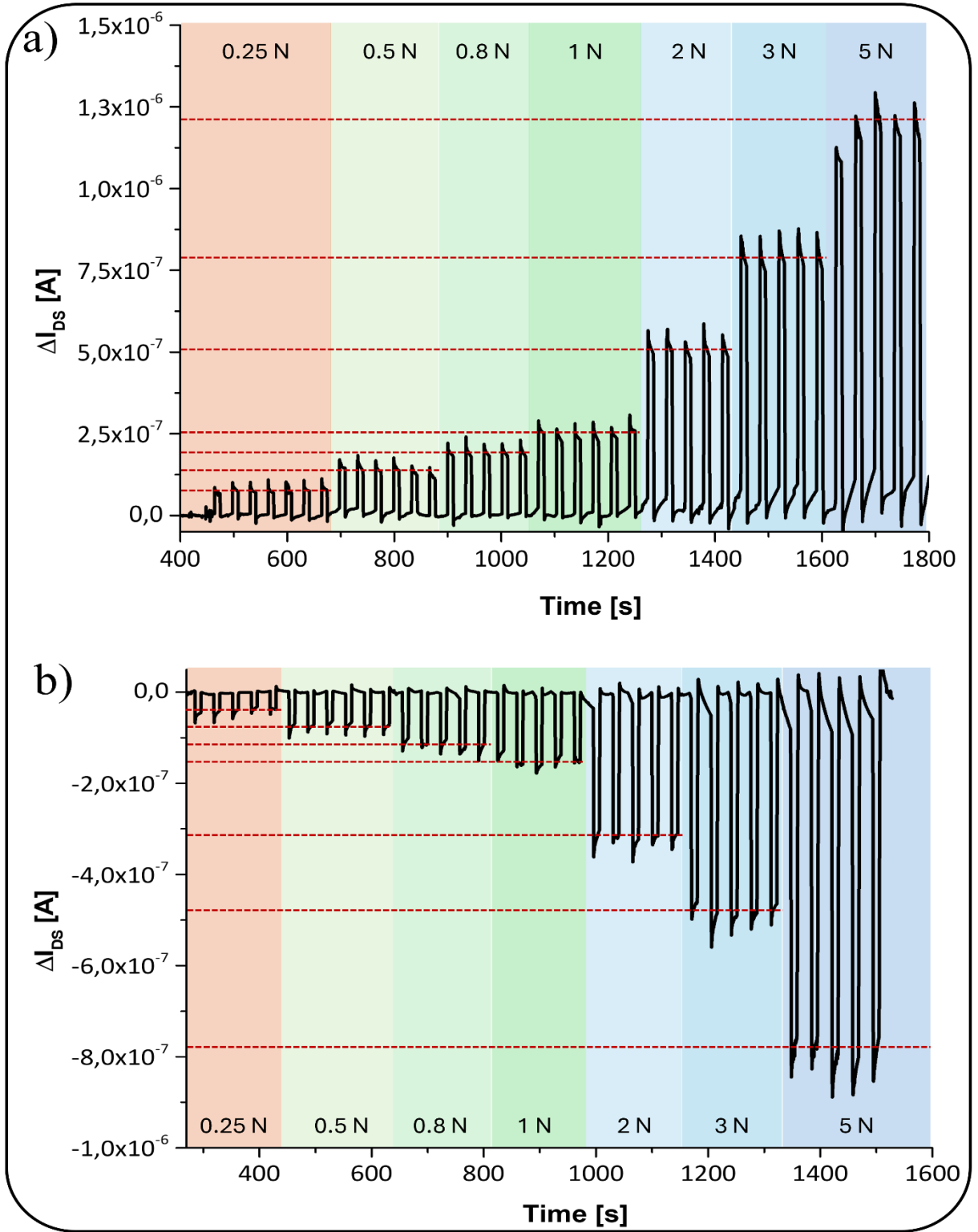


Figure 68: Channel current variation ΔI_{DS} of a device, characterized in both sense of polarization from the top gate, given by the induced charge of a PVDF capacitor submitted to a force: a) reduction in ΔI_{DS} induced by capacitor; b) increase in ΔI_{DS} induced by capacitor. Force values are indicated in the graphs.

Before release, force is maintained for 10 s, and the interval between each application is around 30 s. Very important, response to stimuli is very quick and the intensity of the variation is reproducible for each value of force. From the characterization of each device, calibration curves were extracted and sensitivities calculated. One thing to be noted is that, unfortunately, due to some limitations posed by the setup, the 1x1 mm² capacitor couldn't be used. This is because proximity effects caused by the approaching of the indenter, completely covered the sensor response, making it impossible to have a clean characterization of the device with such capacitor.

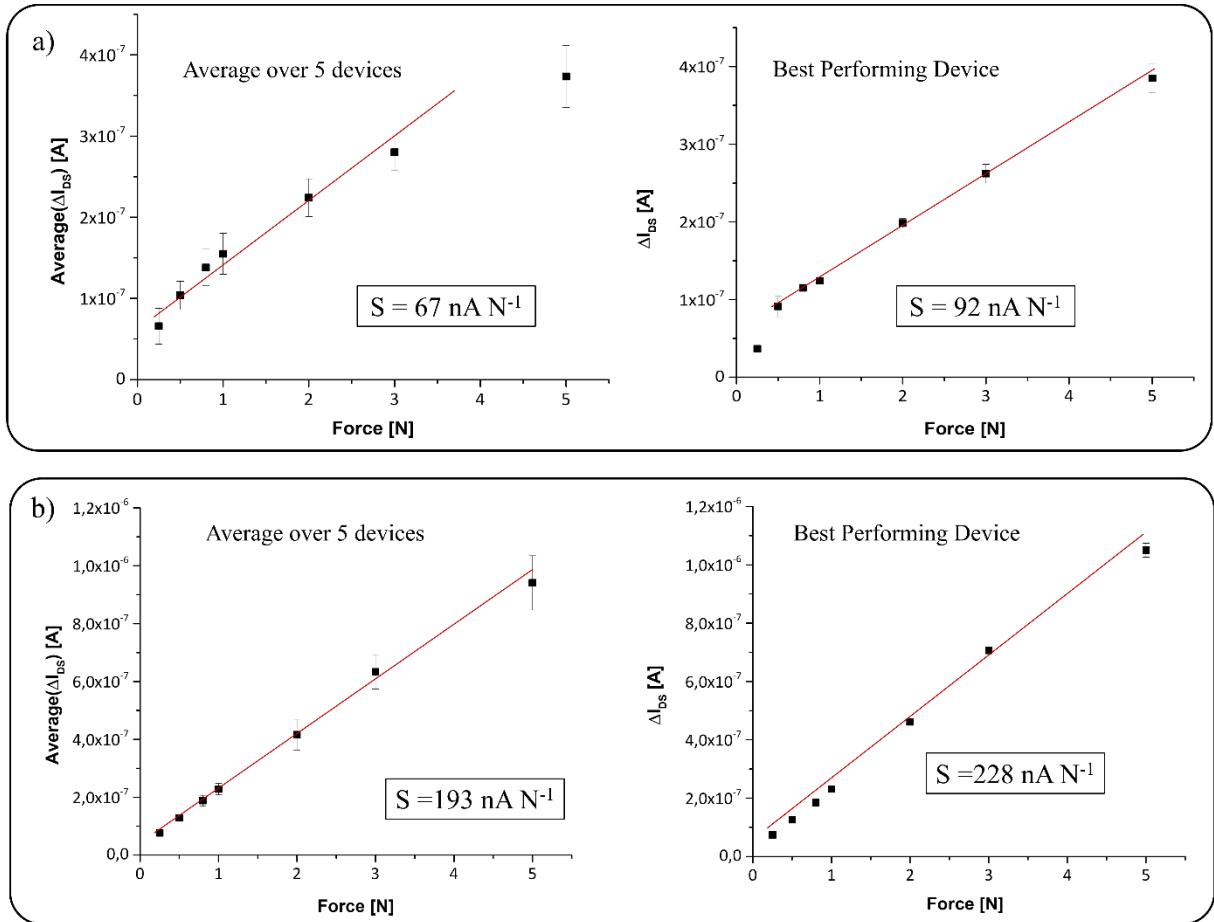


Figure 69: Average switch-off sensitivities among all the device for both employed capacitors: a) 3x3 mm² capacitor; b) 5x5 mm² capacitor. Response is approximately linear, with very small differences among the devices.

Table 16: Average sensitivities for both switch-off and switch-on modes of characterization of the devices, reported in current variation of nA per Newton applied. The switch-off mode results overall more sensitive than the switch-on, but differences are very small.

Capacitor Area [mm ²]	Average sensitivity switch-off [nA N ⁻¹]	Average sensitivity switch-on [nA N ⁻¹]
25	193 ± 30	181 ± 50
9	67 ± 29	46 ± 17

In **Figure 69** are presented the calibration curves relative to the two capacitors employed, in switch off mode: top is the 3x3 mm², bottom is the 5x5 mm². In **Table 16** are reported the extracted values of sensitivity for both switch-off and switch-on modes. Comparing them to the same values calculated for the temperature measurements, we can see that sensitivity in this case has lower values. This is mostly related to the fact that the pyroelectric constant of PVDF is bigger than the piezoelectric one. The same hysteresis test has been performed also in the case of force application. Following a similar protocol, four different values of force had been chosen, 0.5, 1, 2, and 3N. These forces had been applied three times each at regular intervals in ascending and descending direction, to verify that response of the sensor wouldn't be affected by residual charge. As evident from **Figure 70**, this is not the case, since effect on the sensor by the applied force is fairly reproducible in both directions, leading to forward and backward sensitivities nearly identical.

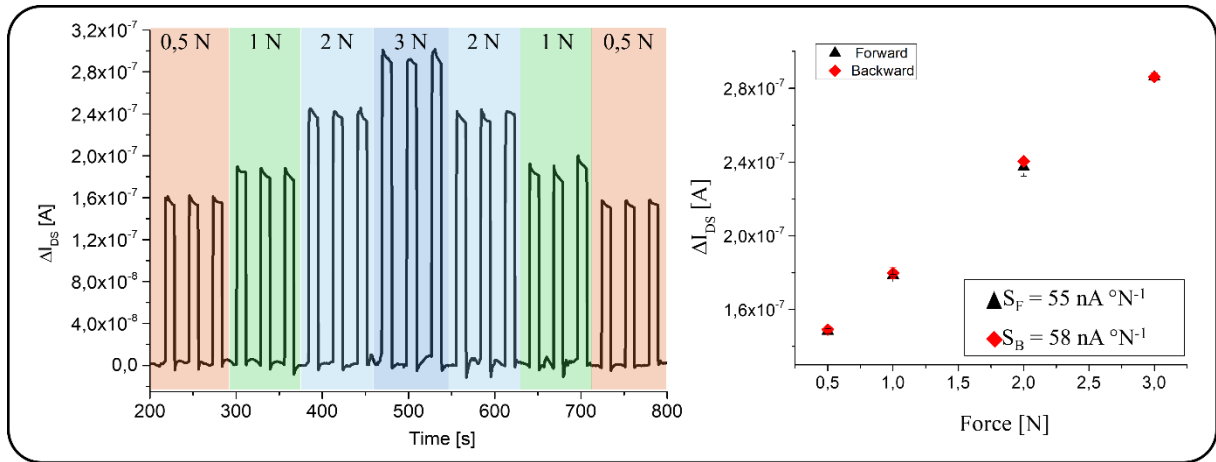


Figure 70: Hysteresis evaluation of the device when subject to application of force in ascending and then descending direction. Sensitivity in both directions is highly comparable.

5.3 Multimodal characterization

To end the characterization of these device as mechanical sensors, the last step conducted was to characterize them as multimodal sensors. To do so, both setups were joined, so that both temperature and force could be applied at the same time. The PVDF capacitor chosen to do such experiment was the 3x3 mm² one, which would be the best suitable, since the 1x1 mm² was to be excluded due to the limitations posed by the force measurements, and the 5x5 mm² had a smaller temperature range as it reached saturation in the response after a certain temperature threshold, as detailed in the relative paragraphs of each characterization. A sketch of the employed setup for these measurements is presented in **Figure 71** and is essentially a merging of the two setups employed for each characterization.

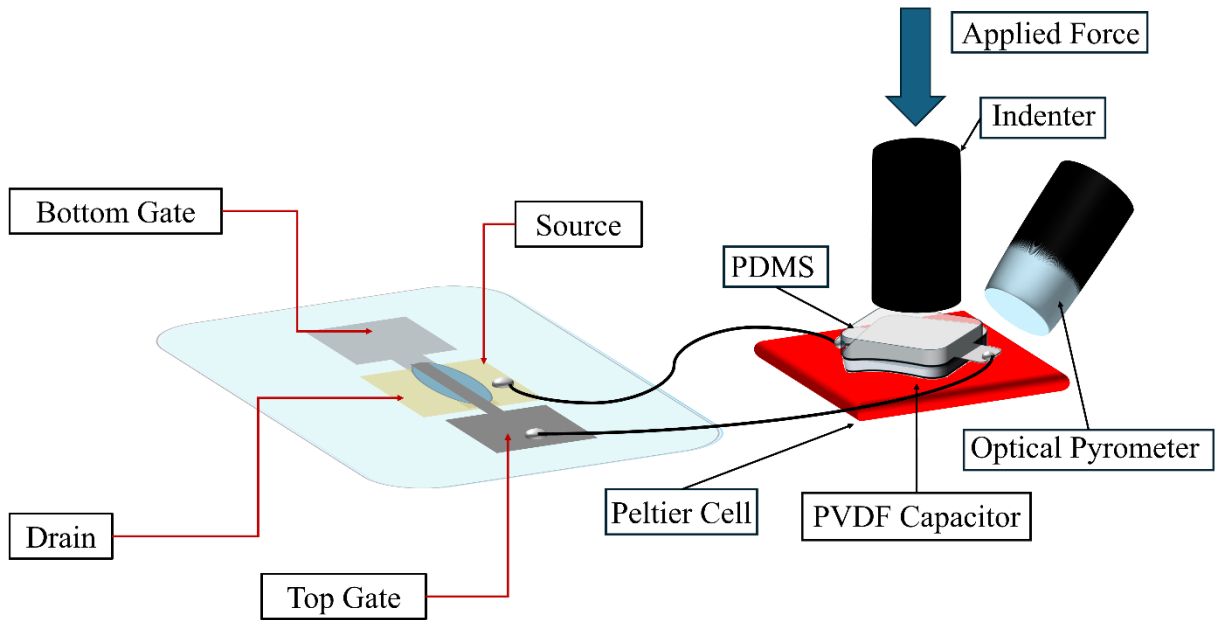


Figure 71: Setup for measuring both temperature and force effects on the device at the same time. The indenter, connected to a dynamometer, applies a force while the Peltier Cell heats up the PVDF capacitor.

The transistor is biased from the bottom gate and let to stabilize while the capacitor is already connected to both top gate and source of the device. Once stable, Peltier Cell is switched on and starts to heat up. To verify the capability of the device to detect both stimuli at the same time and discern from one another, the measurement protocol chosen was the following: after the device is stable, temperature is increased to a set value and, once reached that value, five different values of force would be applied in ascending direction; once applied the last value of force, temperature is risen to a second value and the same forces are applied in the same manner. After this, temperature is risen once again and forces are applied, following the previous two protocols. Depending on the plate connected to the top gate, a decrease or

increase in channel current would be detected by the measuring system. However, pyroelectric and piezoelectric effects have different dipole alignment vectors. This means that if the plate connected responds with a decrease in current when temperature is increased, the same plate would respond with an increase in current when a force is applied and vice versa. Following this principle, characterization curves were taken in both configurations and are presented in **Figure 72** and **Figure 73**.

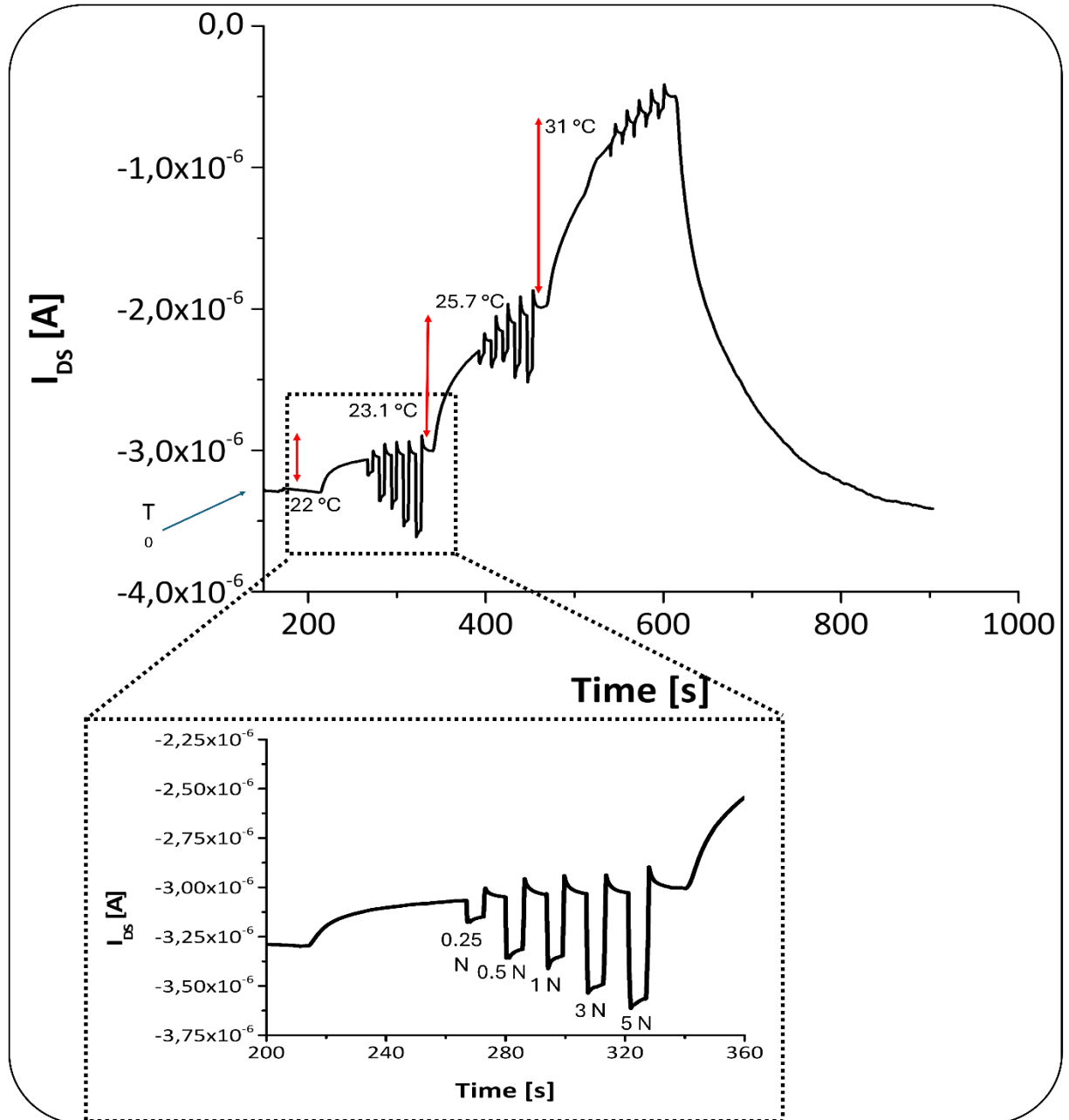


Figure 72: Multimodal characterization of a device. As temperature increases and the device switches off, applying a force reverts this effect and when the force is applied, channel current tends to increase. A close-up of the pressure is presented.

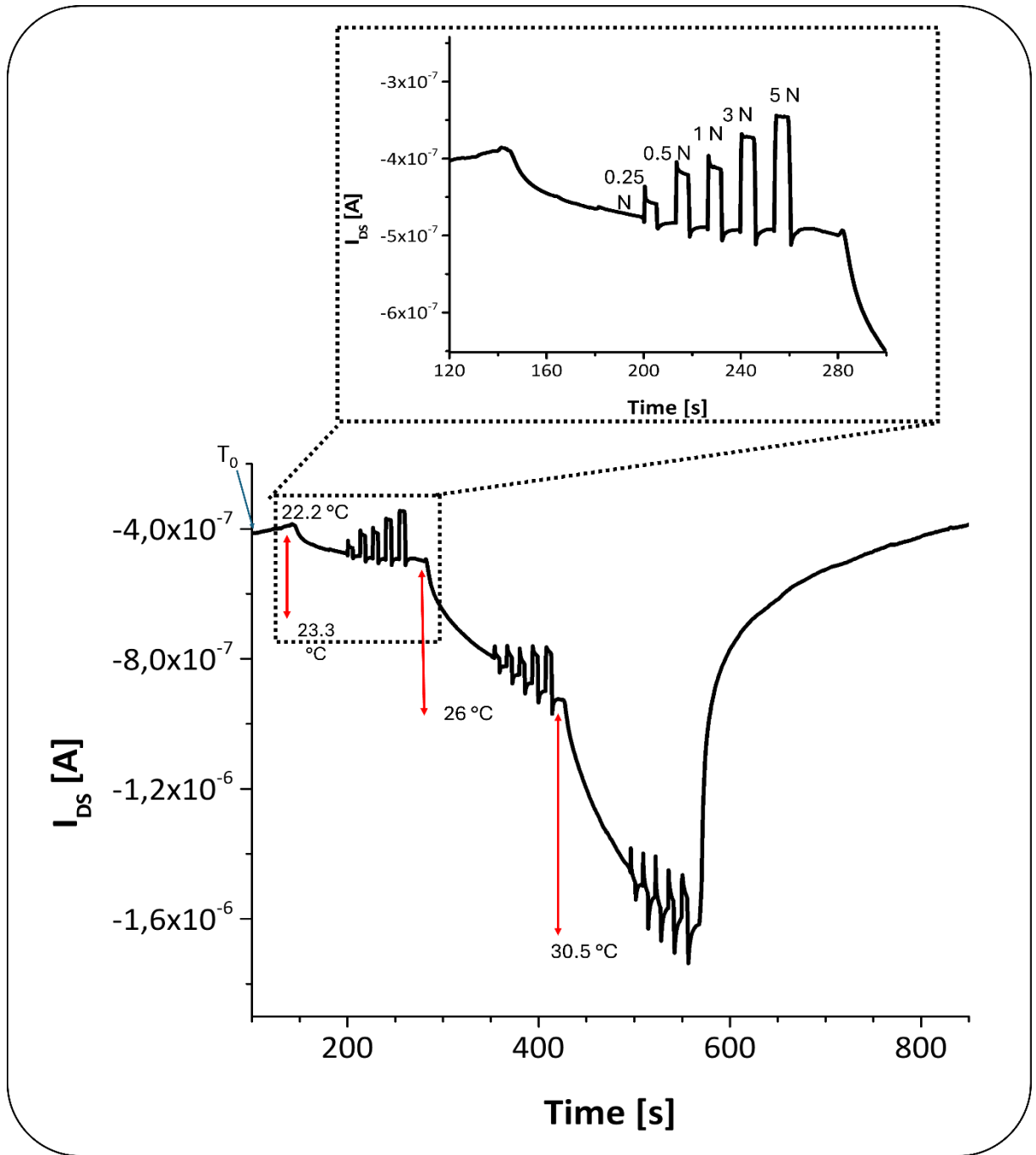


Figure 73: Multimodal characterization of a device. As temperature increases and the device switches on, applying a force reverts this effect and when the force is applied, channel current tends to decrease. A close-up of the pressure is presented.

One thing that is worth noting is that force effect on the current is always coherent in all three steps of temperature. However, the higher the temperature rises, the less defined are the plateau of the force when applied. This might be related to the fact that pyroelectric constant in PVDF is higher than piezoelectric one and thus, for higher temperatures, piezoelectric effect is suppressed by the pyroelectric one. Importantly enough, the opposite action that the two effects have on the current, allows to easily discriminate between the two.

Concluding the sensor analysis, it is worth noting that the top gate acts as the sensing material for the device, being the interface between it and the external environment. A brief comparison with resistive sensors built for the same purpose^[171,172] shows how a transistor-based sensor, even though more expensive, gives a higher range of functionality, more stability and reliability over time, with a built-in amplification that allows for the processing of small signals. Resistive sensors do have their advantages and since they are cheaper, they can be employed for situations in which high precision is not required. Moreover, as demonstrated in this chapter, transistor-based sensors have high linearity of response, and the same cannot be said for resistive sensors, due to the fact that some materials might have a non-linear response to the quantity they are measuring.

6. Chapter VI: Mechanical deformation effects on flexible thin-film transistors

Strain-induced electrical changes related to mechanical stress in organic thin-film transistors is worth investing and already have been^[173–177], since, being widely used for their flexibility, OTFT have to be resistant to mechanical deformations, like compression or elongation, otherwise they won't be considered reliable for applications like artificial skin, that vastly relies on freedom of movement. For this reason, a detailed electromechanical characterization has been performed, to validate the hypothesis under which the devices still perform in a reliable way, even after continuous deformation. To do so, two sets of organic field-effect transistors have been prepared with two different semiconductors, TIPS-Pentacene and N1400. XRD and AFM analysis have been performed to demonstrate that difference in behaviour between the two sets of devices, is mainly related to the effect that applied mechanical deformation has on the film morphology of the two semiconductors. Moreover, the same analyses are being performed on devices realized with DPP-DTT as semiconductor. Study on the effect of deformation on such devices is still underway and needs further investigation. In **Figure 74** is presented a sketch of the employed OFETs. Gate, source and drain are made of gold and realized by means of thermal evaporation; gate is realized through a shadow mask, while source and drain, having a structure that is an interdigitated one, are patterned through a photolithographic process, and have a W/L of 1200. The gate dielectric is a 1,5 μm Parylene C layer.

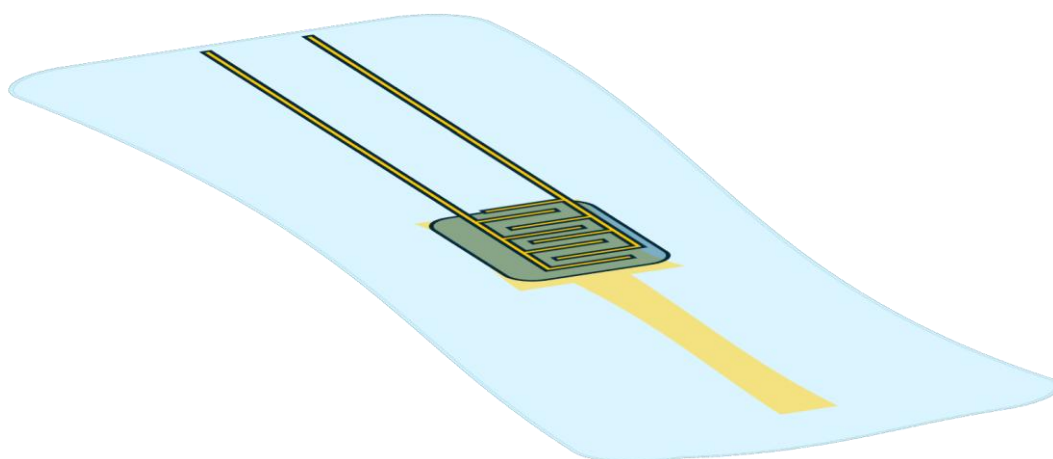


Figure 74: Representation of flexible organic field-effect transistor. All three electrodes are made of gold, and semiconductor is either TIPS-Pentacene, N1400 or DPP-DTT.

Flexibility of the substrate here plays a fundamental role, and correct position of the electrodes is key to obtain a result free of spurious effects related to contacts. For this reason,

contact pads are distant from the channel area, which is the one that will be bent to study the effect of mechanical strain on different semiconductors. Since devices are to be measured also when bent, copper wires have been glued with conductive silver paste to the end part of the electrodes. Both electrical and electromechanical characterization have been performed at room temperature and ambient conditions. To avoid damaging the contacts, a simple bending system, presented in **Figure 75** have been employed. The strain applied to the active area is calculated using the formula $\varepsilon = d/2R$, where d is the substrate thickness and R is the bending radius. For all characterized devices, surface strain ranged from 0,1% up to 4,5%.

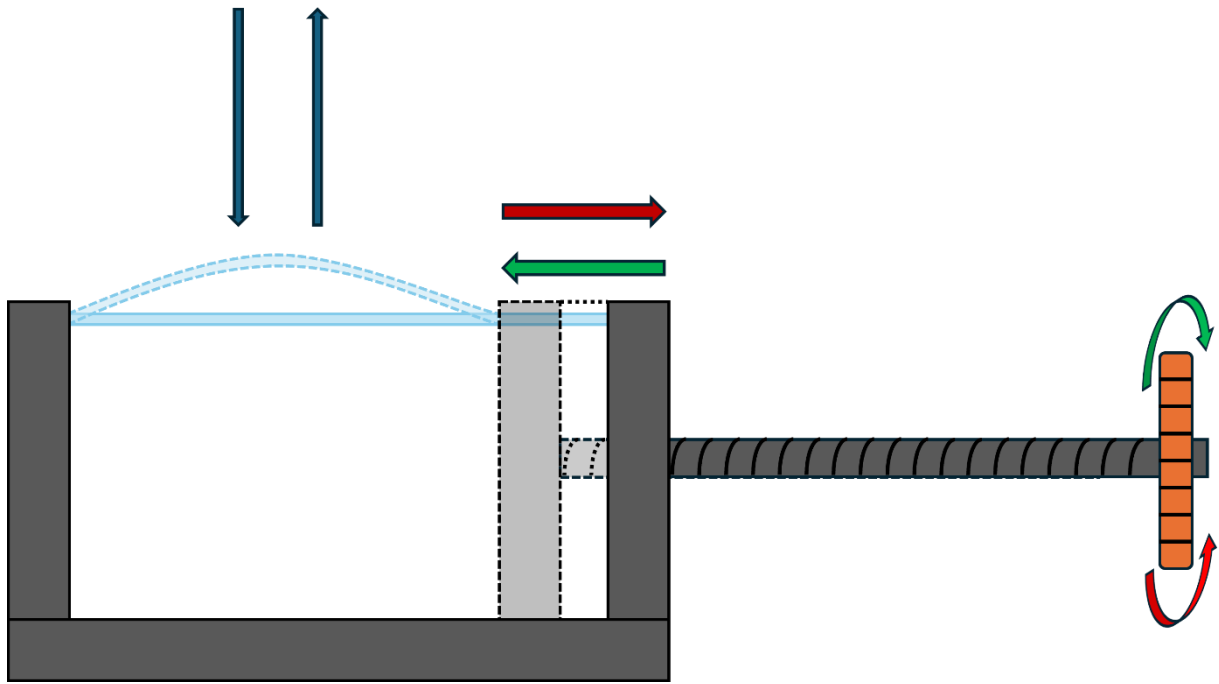


Figure 75: Sketch representation of the instrument used for bending the device. Strain applied is given by the formula $\varepsilon = d/2R$.

Since the target of the study is to characterize the effect of mechanical stress on different semiconductor, output and transfer characteristics, in flat condition, have been taken before bending the device. Typical output (a, c) and transfer (b, d) curves of such devices are reported in **Figure 76**. Notably, both voltages applied, and output current are higher with respect to the architecture proposed before. This is due to the higher dielectric thickness, that requires higher V_{GS} to effectively form the conductive channel and the channel area itself, with a W/L ratio 12 times bigger. Average values for the main parameters presented in **Table 17** and are obtained as average values of all 5 analysed devices for each set. As evident from transfer characteristics from **Figure 76(b, d)**, hysteresis is negligible and thus mobility and threshold voltage values are the same in both forward and backward gate voltage sweep.

Table 17: Comparison of the most meaningful electrical parameters for the two sets of OFETs, where values are obtained averaging the values from each transistor for both sets.

	V_{th} [V]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	I_{ON}/I_{OFF}
TIPS-Pentacene	38 ± 20	$7 \cdot 10^{-2} \pm 6 \cdot 10^{-2}$	10^6
N1400	$3,4 \pm 1,3$	$3 \cdot 10^{-3} \pm 1 \cdot 10^{-3}$	10^4

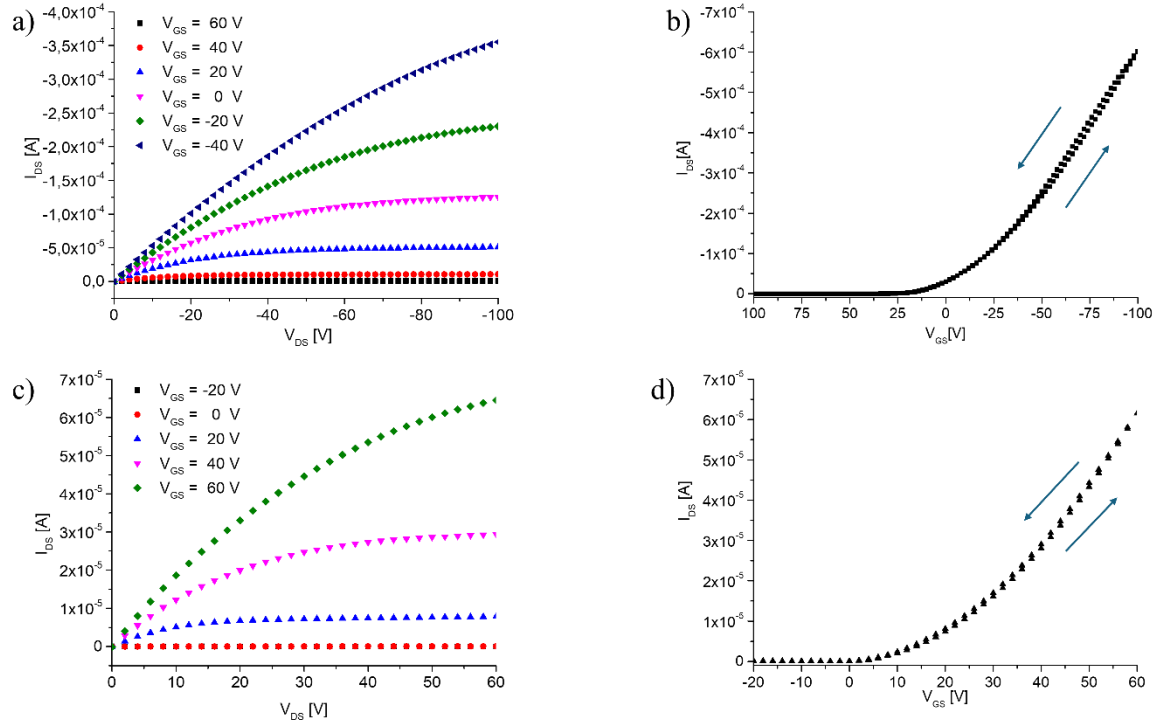


Figure 76: Typical output and transfer characteristics obtained from a,b) TIPS-Pentacene and c.d) N1400 based OFETs.

6.1 Electromechanical characterization

The electromechanical characterization testing protocol was performed as follows. At first, the device was characterized in flat conditions, prior to any bending. It was then bent to a certain radius and the transfer curves were acquired during the mechanical deformation, in static conditions. Acquisition ended, the device was brought back to a flat position and transfer curve was acquired once again. For each bending radius, deformation and acquisition were performed three times each, always passing from the flat condition between every measurement. Doing so, two aspects of devices behaviour could be evaluated: I) changes induced by mechanical deformation in parameter such as output current, mobility, and threshold voltage, and II) reversibility of devices' electrical behaviour after deformation. Variations in parameter like mobility and current are measured with respect to the transfer curve acquired right before the considered deformation. As said before, for both TIPS-Pentacene and N1400, a set of 5 samples was prepared and analysed. Representative behaviour of both species of devices are reported in **Figure 77**, as shifts in transfer characteristic. It is possible to notice that bending, inducing a surface strain on the device active layer, leads to a visible reduction of the transistor output current in both kinds of devices, and the more the device is bent (smaller radius) the more pronounced is the shift.

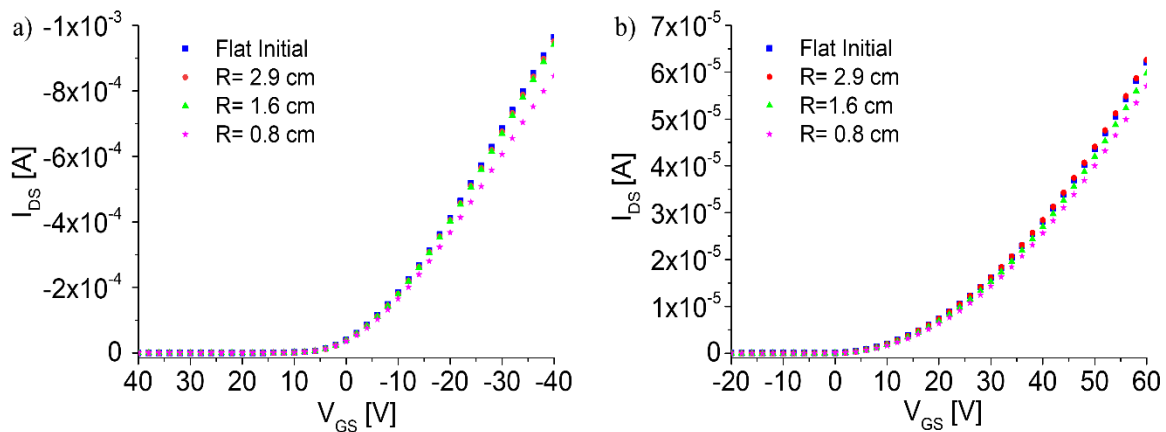


Figure 77: Transfer characteristics recorded before and during mechanical deformation at different bending radii on a) TIPS-Pentacene and b) N1400- based OFETs.

As stated before, similar behaviour has already been reported regarding different organic semiconductor-based transistors, including TIPS-Pentacene^[178,179]. In **Figure 78** are presented the average results of the evolution of the main parameter inspected, namely relative output current variation, relative mobility variation and threshold voltage variation, all reported versus the strain applied. Sensitivity in terms of current variation is reported as

$\Delta I_D/I_{D0} = (I_{\text{bent}} - I_0)/I_0$, where I_{bent} and I_0 are the current values acquired in bent and flat conditions, respectively. Mobility sensitivity is evaluated in a similar way, that is $\Delta\mu/\mu_0 = (\mu_{\text{bent}} - \mu_0)/\mu_0$, μ_{bent} and μ_0 mobility values in bent and flat condition respectively.

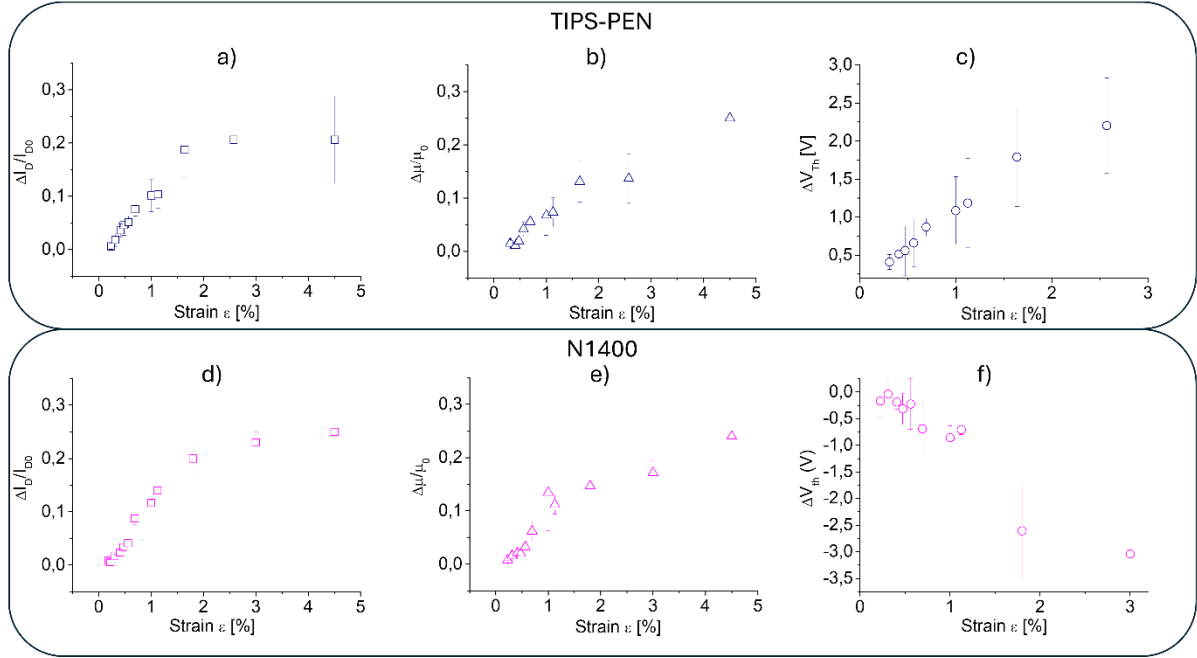


Figure 78: Relative variation of the output current and mobility and variation of the threshold voltage, all reported with respect to the strain, in a–c) TIPS-Pentacene and d–f) N1400 OFETs.

It can be clearly observed that applying a surface strain induces a very reproducible effect in all the fabricated devices, as can be observed from the limited error bars reported in the graph. In all cases, a reduction of the output current was observed in both the investigated systems. At this point several observations can be drawn. First of all, current reduction can be related to a corresponding mobility reduction observed in all the characterized devices. It can be also observed that in the two systems, the applied surface strain induces a small, but visible, variation (increase in its absolute value) of the transistor's threshold voltage. Both reported effects, concur in the overall decrease of the transistors output current during mechanical deformation. Notably, when strain is kept below 1.5%, the device's behaviour is fully reversible, and the device output current recovers to its initial state as soon as the deformation is removed. On the contrary, when deformations inducing strain values larger than 1.5% are applied, the device behaviour is no longer reversible, indicating that the device structure is irreversibly damaged. In previous works, such effect has been reported to be dependent on cracks formation in the source and drain electrodes^[175]. For such reasons, the following electrical characterization has been performed within the reversibility range and were aimed at evaluating the effects caused by fatigue on both types of devices. The fatigue

tests consisted of bending cycles that were performed by measuring output current values first in flat conditions and subsequently by applying a surface strain of 0.8% for a certain number of times. After each bending cycle, a new transfer curve was measured in flat conditions and compared to the previous one. As can be clearly observed from the plots reported in **Figure 79**, where current variation is normalized to 1, the two systems gave rise to a very different response to fatigue. Even if these experiments were performed within the reversibility range, TIPS-Pentacene based transistors are severely affected by such fatigue tests. It can be clearly observed that after 200 cycles the device's output current is reduced to around 60% of its initial value. This is correlated to a reduction of carrier mobility and an increase in the threshold voltage, which is permanent. On the contrary, N1400 devices are characterized by a much better response, as the average current and mobility reduction after a prolonged cycling test is roughly 10%.

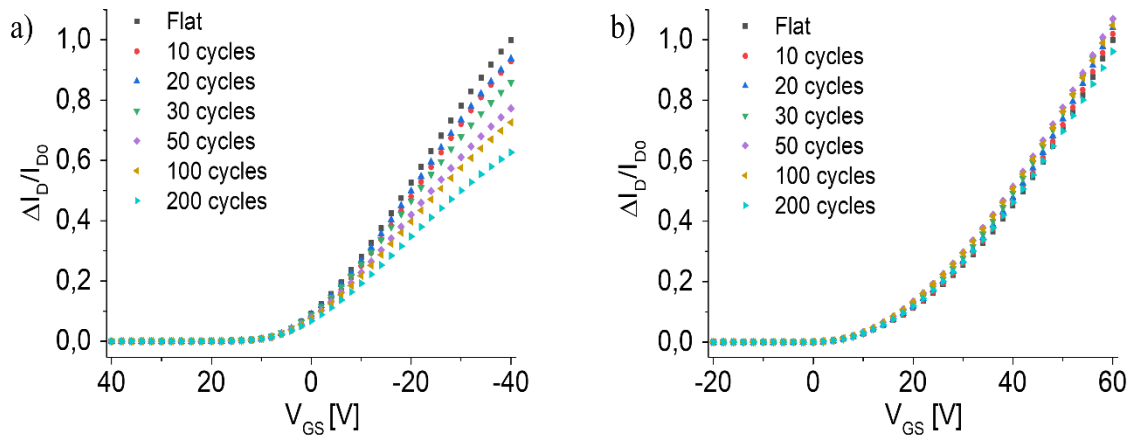


Figure 79: Fatigue tests performed on a) TIPS-Pentacene and b) N1400 based devices, by applying a deformation of 0.8% several times. It can be clearly noticed that TIPS-PEN based devices show a much more pronounced degradation upon cycling tests, even if performed under the defined critical strain value. On the contrary, N1400 devices show a much more pronounced stability.

6.2 X-ray diffraction (XRD) and atomic force microscopy (AFM)

In order to better understand the mechanism behind this observed phenomenon, a structural and morphological investigation of the deformed film has been conducted. XRD analyses were carried out on thin films of both N1400 and TIPS-PEN devices and are summarized in **Figure 80**. The XRD pattern of the PET-based polymeric substrate in the angular range 3–35 °(2 θ) strongly reflects its nature featuring four broad peaks at 2 θ = 13.8°, 15.6°, 23.8°, and 26.8°, respectively, with the latter being the most intense.

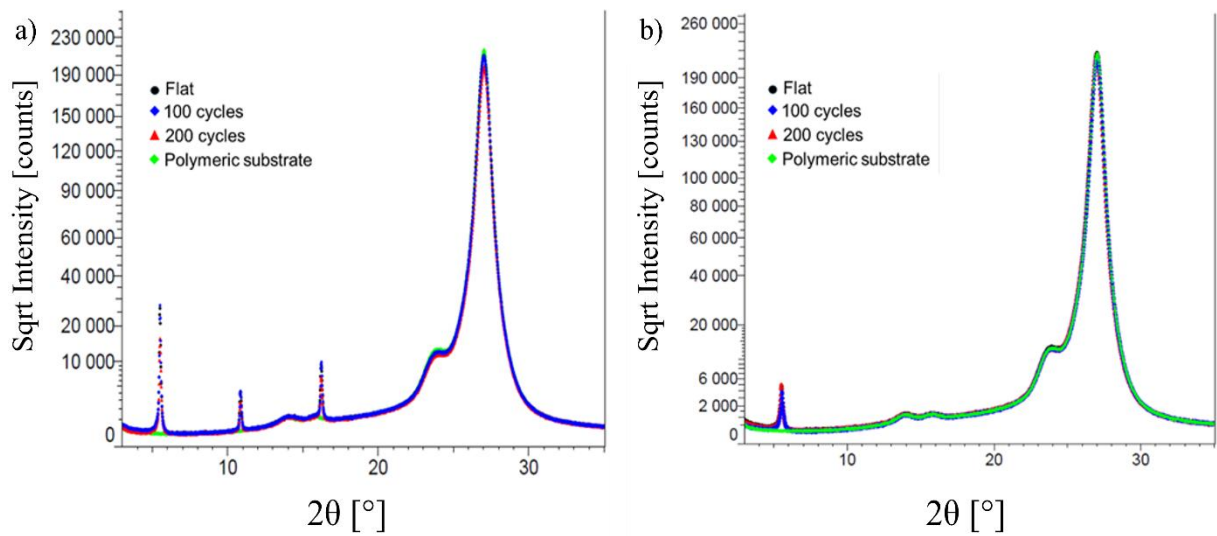


Figure 80: X-ray diffraction analyses on a) TIPS-Pentacene and b) N1400 devices before (black dots) and after 100 bending cycles at $R = 1.6$ cm (blue squares) and after additional 100 bending cycles at $R = 0.8$ cm (red triangles).

XRD analyses performed on TIPS-Pentacene devices (**Figure 80a**) before and after the bending cycles showed three sharp peaks at 2 θ = 5.3°, 10.6°, and 16.0° in agreement with what was reported in the literature^[180,181]. Peak profiles and intensities are barely affected by the bending cycles of thin films and clearly indicate that such deformations do not induce an irreversible change in the crystal structure of the deposited thin films. The presence of the crystalline organic semiconductor in N1400-based devices is reflected on the XRD patterns (**Figure 80b**) with an additional broad peak that corresponds to the (001) diffraction of the triclinic phase elucidated by means of ab-initio X-ray methods^[182]. The XRD patterns collected on the same device after 100 bending cycles at $R = 1.6$ cm and after additional 100 bending cycles at $R = 0.8$ cm showed negligible variations suggesting the preservation of its crystal structure. Therefore, to achieve a better comprehension of the thin film morphologies, AFM imaging was performed. From images presented in **Figure 81**, significant differences between the two deposited films are revealed. TIPS-Pentacene films are characterized by

very large crystallites, meanwhile N1400 thin films are characterized by a much more pronounced polycrystalline structure, with crystallite dimensions generally ranging around 200 nm. When a severe deformation is applied to both films, the effect on the morphology is significantly different. When a surface strain close to 1% is applied, cracks start to be formed in the TIPS-Pentacene crystallites, becoming much more pronounced for repeated deformations. This effect is clearly visible in **Figure 81b**, reporting the morphology of such semiconductor thin film after 200 cycles of deformations at 0.8% of strain. It can be assumed that such permanent degradation of the active layer morphology is responsible for the permanent changes in the electrical behaviour observed in the reported samples.

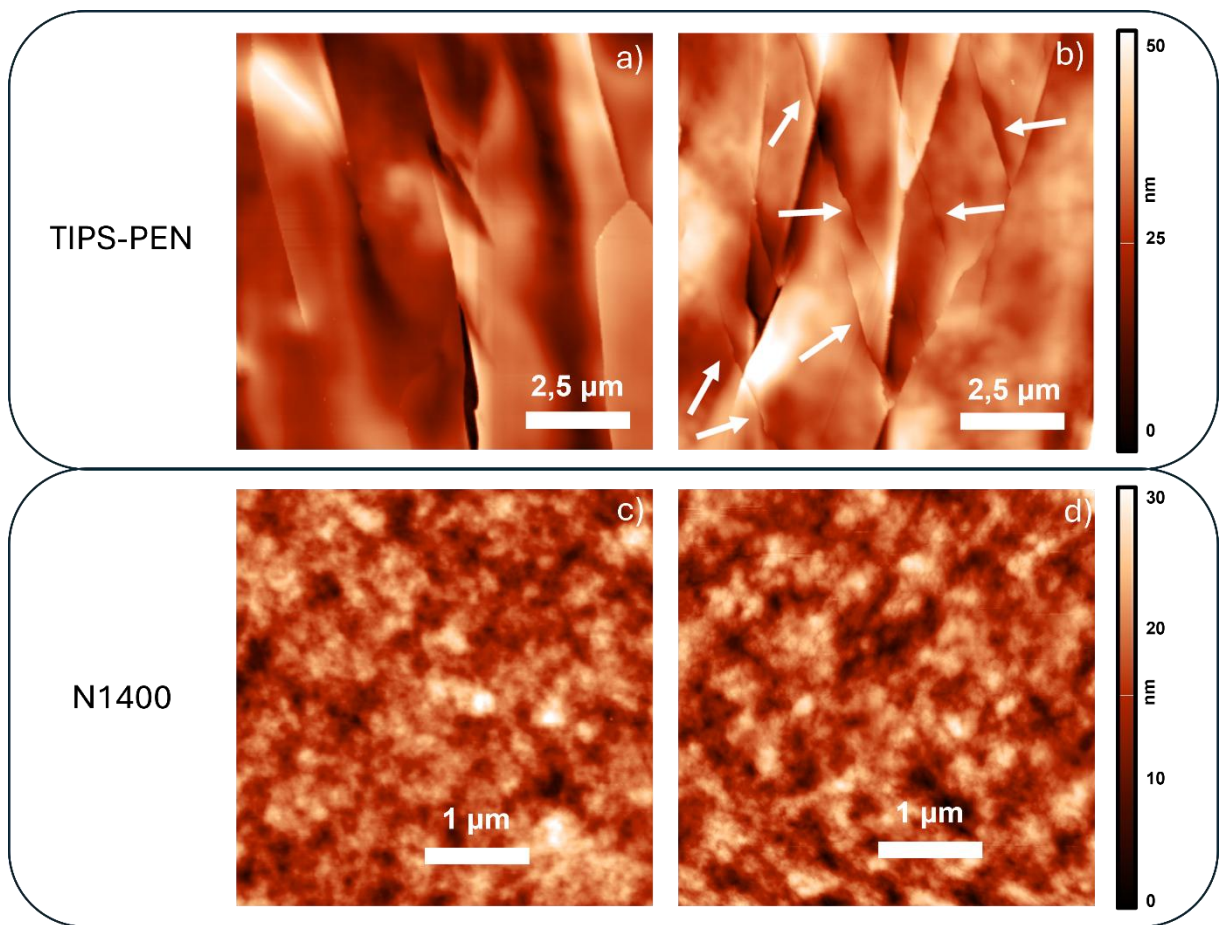


Figure 81: AFM images relative to TIPS-Pentacene film a) before bending and b) after bending, where cracks are clearly visible, and N1400 c) before bending and d) after bending where there is no evident crack in the structure.

N1400 thin film, however, seems to form a much more robust and elastic structure. In fact, no significant changes in the polycrystalline film can be observed. This effect can be clearly explained by considering the high concentration of grain boundaries present in the polycrystalline film, which are capable to accommodate such surface strain, giving the overall film a more elastic behaviour, which is not the case for TIPS-Pentacene films.

Therefore, it is possible to conclude that such irreversible morphological damages in the latter system, although they do not bring to a complete failure of the device, lead to a permanent decrease of their performances, which was not observed in the N1400 based OFETs, which are thus characterized by a much more robust morphology.

In conclusion, the effect of mechanical deformation on two commonly employed organic semiconductor-based transistors was investigated. The obtained results demonstrate that device performances are affected by mechanical deformation due to a reduction of the carrier mobility and threshold voltage shift induced by the applied surface strain. This behaviour was found to be linear and reproducible for deformations below 1%, indicating that such devices can potentially be employed for the fabrication of flexible strain sensors. However, under continuous and cyclic deformation, even at low strain levels, the two systems give rise to markedly different mechanical behaviour; particularly, TIPS-Pentacene-based OFETs show irreversible changes, whereas N1400-based devices maintain highly reproducible performance, making the latter a promising candidate for long-lasting, flexible mechanical sensors and electronic circuits. The correlation between structural, morphological, and electromechanical characterizations demonstrated that a continuous mechanical deformation does not alter the polycrystalline structure in either system. However, in TIPS-Pentacene-based devices, the deformation affects the morphology of the thin films, which likely contributes to the reduced reproducibility of their electrical behaviours. In contrast, the chemical structure of the N1400 offers greater stability under deformation, leading to more consistent performance.

6.3 DPP-DTT strain sensors

A similar protocol, with some implementation, has been followed for devices realized with the same architecture and a different semiconductor, namely DPP-DTT. The study is yet to be completed, as both XRD and AFM imaging still need to be performed, but some information can be extrapolated from electrical characterization, performed in static mode, just like the devices previously described, but also in dynamic mode, so that ulterior knowledge regarding the behaviour of such devices, when used under stress conditions, can be evaluated, in order to fully optimize the device. Further electrical characterization needs to be performed, as these devices showed some particular behaviour when under determined conditions. In **Figure 82**, different transfer characteristics curves are presented, each one relative to a selected bending radius applied to the device in elongation. Supposedly, what should happen is that reducing the bending radius, conductivity should decrease, since we are increasing the distance between the grain borders. This is exactly what is observed in this case, since starting from flat condition and pristine semiconductor, a sensible decrease in the current can be seen, as we bend more and more the device. Something interesting that can be noted is that, to the bending radius variation, corresponds a shift in both threshold voltage and mobility. In **Table 18** are reported the values for both quantities relative to the different bending radius, as well as I_{ON}/I_{OFF} ratio, all with relative errors. The decrease in mobility is in accordance with what was expected, although, given the polymer nature of the semiconductor, not so remarkable. Moreover, the I_{ON}/I_{OFF} ratio is not so good, due to the high values of I_{OFF} .

Table 18: Extracted values at different bending radii in elongation mode for threshold voltage, mobility and I_{ON}/I_{OFF} ratio.

Bending Radius (cm)	V_{th} [V]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	I_{ON}/I_{OFF}
2,9	$1,3 \pm 1,7 \cdot 10^{-2}$	$4,4 \cdot 10^{-3} \pm 1,7 \cdot 10^{-9}$	10^{-2}
1,3	$1,2 \pm 1,9 \cdot 10^{-2}$	$4 \cdot 10^{-3} \pm 1,3 \cdot 10^{-9}$	10^{-2}
0,5	$1,5 \pm 8,9 \cdot 10^{-3}$	$3 \cdot 10^{-3} \pm 6,1 \cdot 10^{-10}$	10^{-2}
Flat	$1,7 \pm 2,1 \cdot 10^{-2}$	$4,1 \cdot 10^{-3} \pm 1,9 \cdot 10^{-9}$	10^{-2}

Given the behaviour of the device observed in elongation mode, we would expect a somehow specular behaviour when the device is bent in compression mode. This however is not what happens, as can be seen in **Figure 83**. After a first increase in current when bending radius is at 2,9 cm, instead of keeping this trend, current starts decreasing when decreasing the bending radius, contrarily to what we could have expected. Important parameters for this are

reported in **Table 19**; although the behaviour is not what expected, parameters are nonetheless fairly stable, meaning that bending radius can go even lower.

Table 19: Extracted values at different bending radii in compression mode for threshold voltage, mobility and I_{ON}/I_{OFF} ratio.

Bending Radius (cm)	V_{th} [V]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	I_{ON}/I_{OFF}
2,9	$1,9 \pm 1,7 \cdot 10^{-2}$	$4,5 \cdot 10^{-3} \pm 1,8 \cdot 10^{-9}$	10^{-2}
1,3	$1,4 \pm 1,7 \cdot 10^{-2}$	$4,4 \cdot 10^{-3} \pm 1,7 \cdot 10^{-9}$	10^{-2}
0,5	$1,4 \pm 1,6 \cdot 10^{-2}$	$3,9 \cdot 10^{-3} \pm 1,4 \cdot 10^{-9}$	10^{-2}
Flat	$2 \pm 2 \cdot 10^{-2}$	$4 \cdot 10^{-3} \pm 1,7 \cdot 10^{-9}$	10^{-2}

However, even if little, a decrease in mobility is still present. This might be related to the fact that, after a certain bending radius, cracks start to appear in the semiconductor structure, and this could explain the reduction in current. DPP-DTT is a polymer, like N1400, and therefore its behaviour regarding such mechanical stress should be similar, however it also forms very ordered structures, and, since crack are dependant from a multitude of factors, like film thickness, molecular weight, crystallinity, and, of course, the mechanical stress itself, as reported in some recent works^[162,183,184], ulterior analysis are needed to improve the comprehension of the semiconductor behaviour and optimize its use in the devices. Imaging analysis like XRD and AFM are yet to be performed, and they could be helpful to shed some light on the evolution of the active layer when subjected to mechanical deformation.

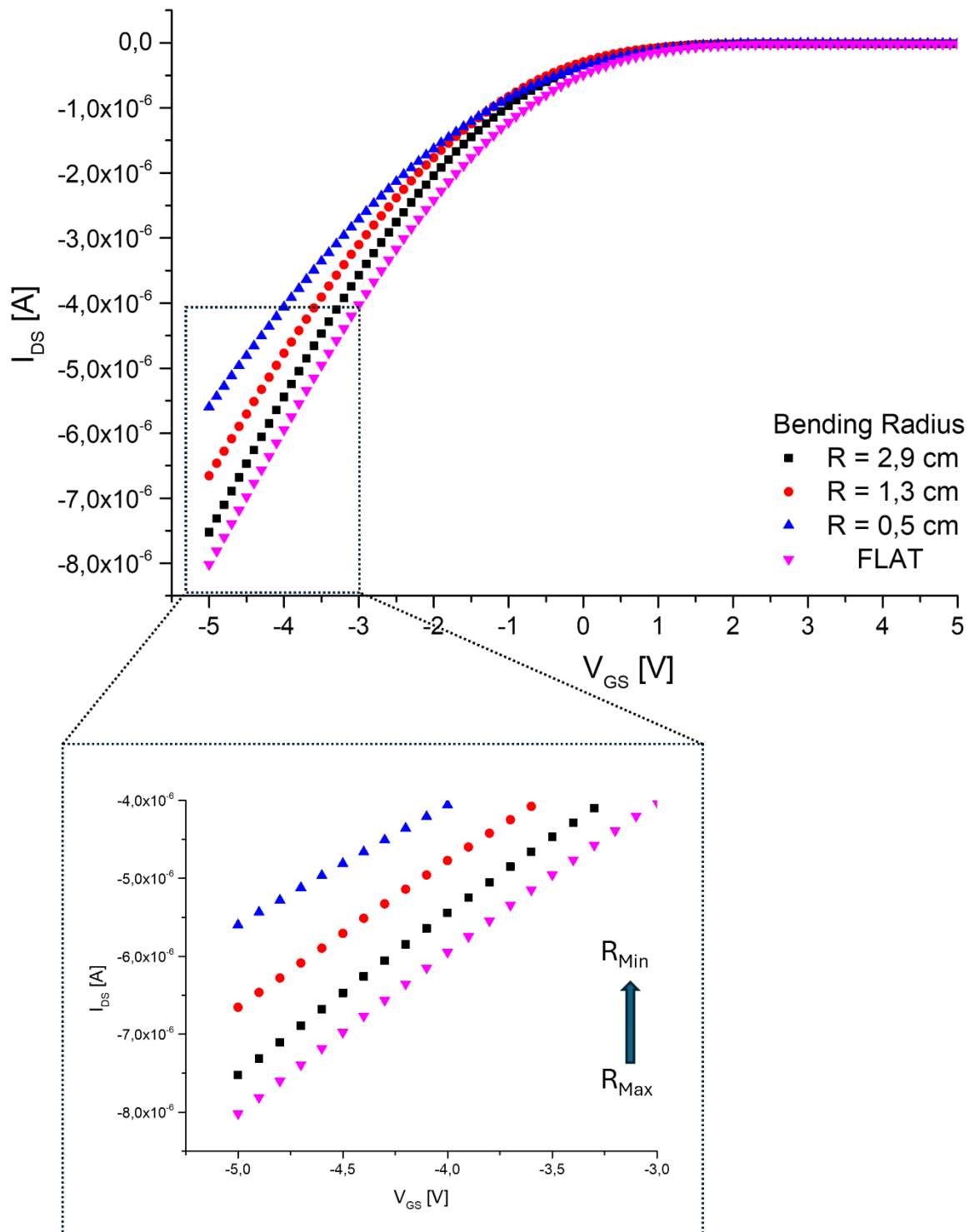


Figure 82: Transfer characteristics acquired for different bending radii in elongation condition. As expected, for smaller radii, current decreases.

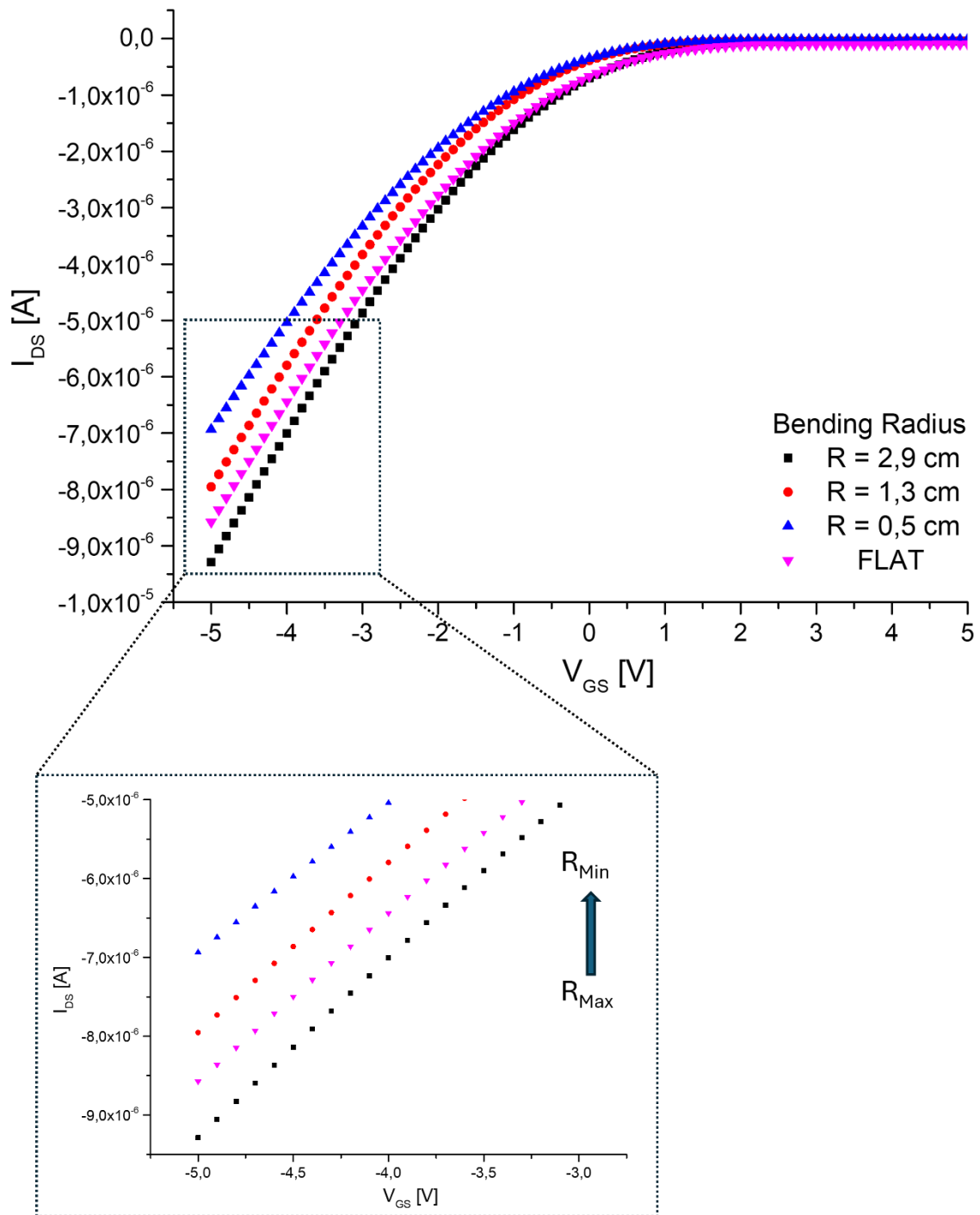


Figure 83: Transfer characteristics acquired for different bending radii in compression condition. Behaviour is different from what expected, since after a first increase, for narrower bending radii, current decreases.

However, this data is obtained as a result of a mean of just 2 bending cycles for each radius, and thus mechanical stress on the semiconductor is limited. To perform a more thorough analysis on the changes in performance induced by mechanical stress, a bending cycle was performed. The device, a fresh one, was measured first of all in flat condition, to have the reference of a pristine device. After that, a first cycle of 10 bends was performed, and the device was measured once again. After 20 other bends, for a total of 30, a new measurement is performed and then once again after 50 total bends and after 100. As evident from **Figure 84**, something happens in the interval between 30 and 50 total bends. Cracks probably start to appear, and overall conductivity of the device is reduced. However, close to none ulterior shift happens between 50 and 100 total bends, and this might be explained with the fact that the semiconductor structure is now “relaxed” and more stable. Parameters extracted from the curves are reported in **Table 20**, and show how threshold voltage shifts toward 0, while mobility has a decrease of around 20% from its initial value, symptoms of a reduced conductivity in the channel area.

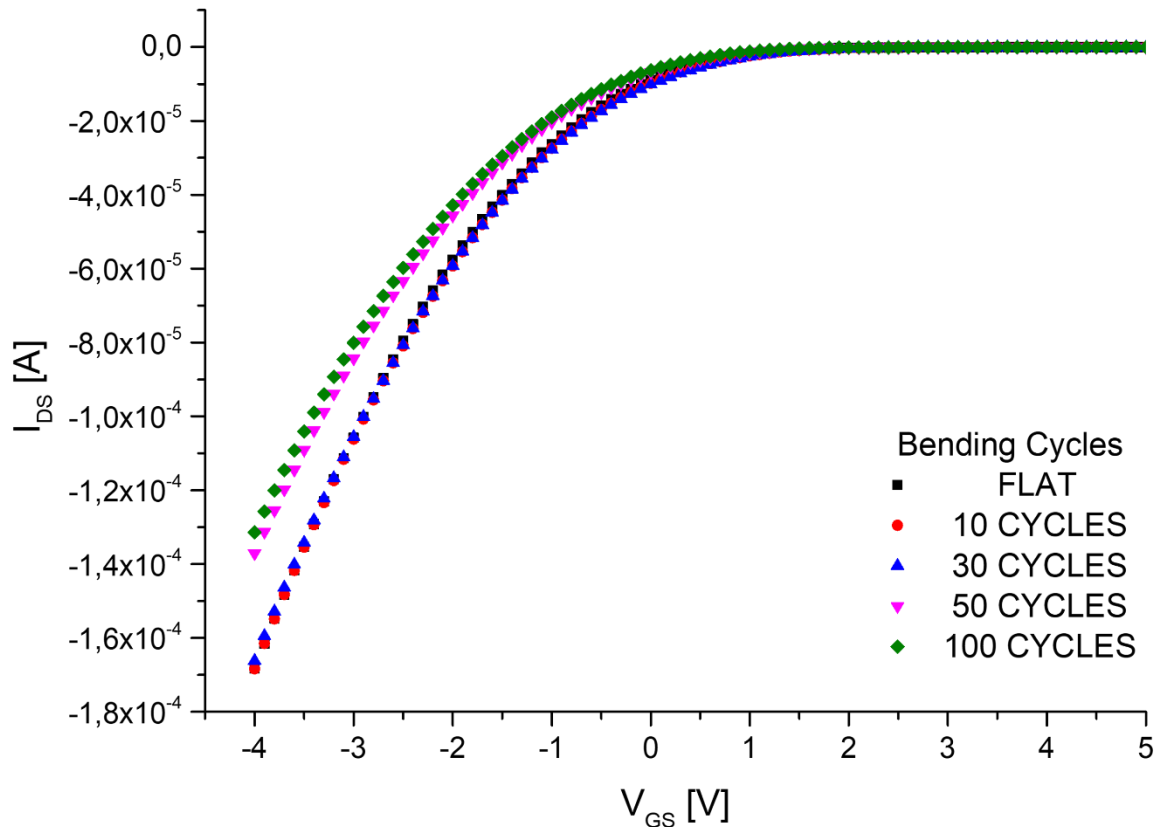


Figure 84: Stress test performed on a device. Bending cycle is performed in four steps: 10 bends, 30 bends, 50 bends and 100 total bends. Presumably, cracks start to appear between 30 and 50 cycles.

Table 20: Extracted values at different bending cycles for threshold voltage, mobility and I_{ON}/I_{OFF} ratio. Mobility values are expressed with two decimal digits to better highlight the variation.

Bending Cycles	V_{th} [V]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	I_{ON}/I_{OFF}
Flat	$8,5 \cdot 10^{-1} \pm 7,3 \cdot 10^{-3}$	$1,61 \cdot 10^{-1} \pm 3,53 \cdot 10^{-8}$	10^{-4}
10	$9,5 \cdot 10^{-1} \pm 7,1 \cdot 10^{-3}$	$1,54 \cdot 10^{-1} \pm 3,27 \cdot 10^{-8}$	10^{-4}
30	$1 \pm 6,1 \cdot 10^{-3}$	$1,48 \cdot 10^{-1} \pm 2,77 \cdot 10^{-8}$	10^{-4}
50	$7,5 \cdot 10^{-1} \pm 8,6 \cdot 10^{-3}$	$1,36 \cdot 10^{-1} \pm 3,49 \cdot 10^{-8}$	10^{-4}
100	$6,7 \cdot 10^{-1} \pm 9,3 \cdot 10^{-3}$	$1,35 \cdot 10^{-1} \pm 3,68 \cdot 10^{-8}$	10^{-4}

One thing that is worth mentioning is the responsivity of the device to mechanical deformation. As soon as the devices passes from a flat condition to a bent one, current variation occurs almost immediately, and, depending on the mode and intensity of the bending, the device responds consequently. For this test, only bending radius that would induce a strain below 1,5% where used, just to verify the reactiveness in the response and the difference in current induced by varying the banding radius. The values reported in **Figure 85** correspond, from left to right, to 0,2%, 0,3%, 0,4% and 0,7% strain, respectively.

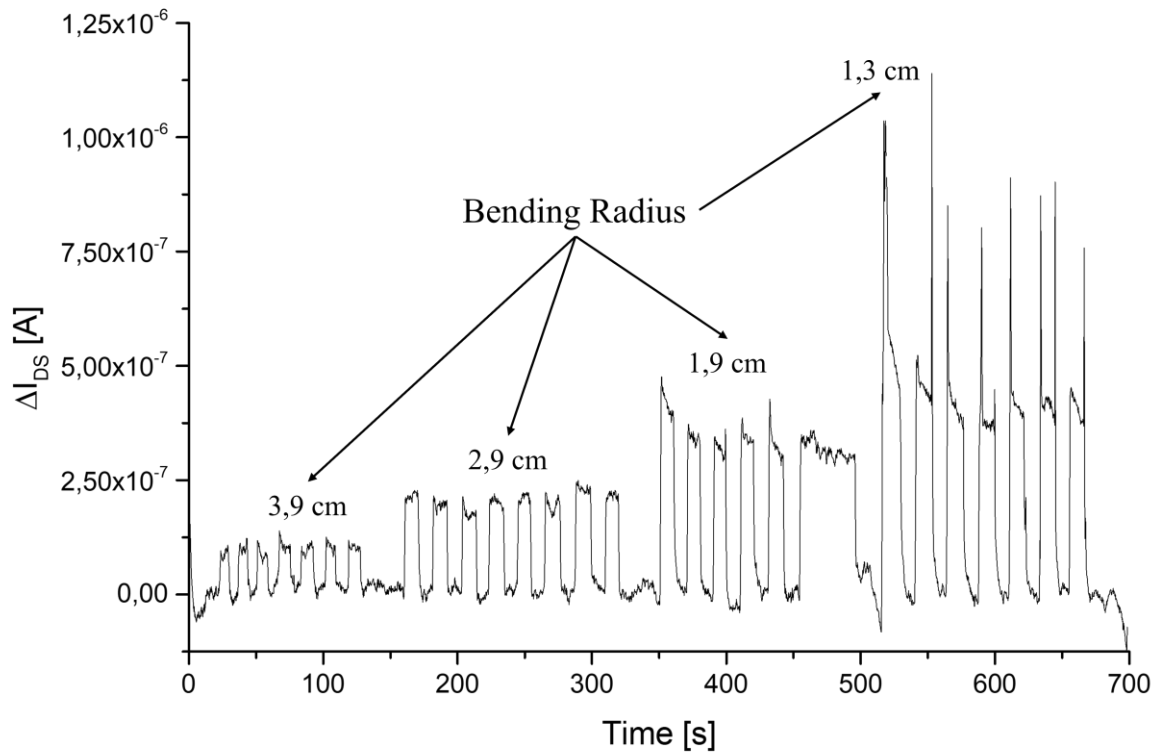


Figure 85: Current variation vs time in response to different strain applied, below the strain limit of 1,5%. The higher the strain value, the higher the current shift.

Data was acquired in elongation mode and current variation is reported in absolute value.

Noise at 1,3 cm bending radius is probably related to unstable connection of the wiring to the electrodes, during bending and release phase of the characterization. In-between, the current is fairly stable.

Concluding this preliminary analysis on strain sensors realized with DPP-DTT as semiconductor, a few things can be said. Although it is a polymeric material, cracks seem to appear once exceeded a certain strain value or after a certain amount of stress is induced on the device through continuous bending. Drop in performances in analysed cases is not worrying, but being DPP-DTT an organic semiconductor, this might not be the only detrimental factor to consider on the long term when designing such kind of sensor. A positive trait is that the device has a quick response to the stimuli, with current shifts that can be related to how much the device is bent. Reversibility of the shift is probably lost when some conditions are met, but a more thorough analysis is needed to extract more information on that regard. Another aspect that needs some optimization is the semiconductor preparation and optimization, strictly related to the solvent used. For these reasons, a new set of devices is being fabricated, so that more electrical characterization, but also XRD and AFM imaging can be performed to better understand the mechanics behind these devices' behaviour.

Conclusion

In this thesis, a summary of the research activities performed during the three years of the PhD is presented. During this period, different results have been achieved, in optimizing and understanding how organic materials fit in the world of flexible electronics. Flexibility is a property widely accredited to be fundamental in the evolution of technology, since it opens a vast new world of possibilities. Going flexible using suitable materials, but especially following the conformability route, could join the world of flexibility with that of wearable electronics. To achieve this, however, devices must be performing, robust and durable, otherwise the advantages of having some device directly on your skin would be lost due to the continuous replacement needed for damaged device. Moreover, this aspect of durability is strictly related to the economic side of each product, as better use of money would lead to the possibility to have always better devices, since research would, maybe, advance with less obstacles. For these reasons, having devices that can be realized in a relatively low-cost way, in large areas and with a high production yield is something that must not be underestimated. Moreover, improving the technologies could lead to more personalized devices, that would better meet the requirements and needs of each user.

For these reasons, this thesis focused on the fabrication, characterization and optimization of devices that could be used as sensors for mechanical quantities such as temperature and pressure, with some other activities focused on the study and optimization of strain sensors.

The first part of the PhD was focused on the optimization of the fabrication process and design of a double-gate organic thin-film transistor (DG OTFT), specifically a double-gate organic field effect transistor (DG OFET). Since aluminium (Al) is used for the realization of both gates, the etching process involved the use of a dangerous solvent, Hydrofluoric Acid (HF). To avoid using such dangerous solvent, the gate fabrication process was modified and, instead of using photolithography, shadow-mask technique was employed. This choice allowed to remove a dangerous fabrication step, meanwhile speeding up the fabrication process, reducing the amount of energy used, and allowing to redesign the gate shape to accommodate a bigger contact pad. Moreover, since the photolithographic mask was the same for both gates, this change also opened to the possibility of reducing the top gate width, leading to a minor overlap and thus reducing the capacitive coupling between each electrode. Since it is never a good idea to vary multiple parameters at once when optimizing the design of a device, the semiconductor chosen to conduct this first part of research was TIPS-

Pentacene, widely used in a lot of literature and well-known also inside the research group. The device has itself a very simple architecture but optimizing the fabrication process to achieve the best performing device possible, meanwhile reducing the total fabrication cost is a process that requires some thought. The photolithographic process could not be totally removed, due to the necessity of a high-resolution technique for the realization of the channel. Moreover, the etcher for gold, used for source and drain electrode, is a more friendly solvent, the Potassium Iodide (KI). The trickiest part was the optimization of the top dielectric layer thickness; due to the fact that semiconductor is deposited through drop-casting and is therefore dependent on the user, its roughness and height wasn't always the same and a good compromise between dielectric thickness and avoiding short circuits with the top gate had to be found. After various tests, a good value for it was found and it allowed an almost 100% yield in the fabrication meanwhile keeping a good control of the top gate over the channel.

Once optimized the device structure, two sets of devices were realized. One double gate set and one single gate set, bottom gate-bottom contact, both OFETs. The purpose of this was to study the different evolution between this two typologies of transistors, in order to validate the hypothesis that double gate structure is better for a variety of reasons. Devices used in this analysis were stored in the dark, inside a box, therefore they were at atmospheric pressure, in presence of oxygen and moisture. They were used only for the ageing analysis, to avoid modification of any sort to its properties induced by something that wasn't related to age. For this first comparison, as said before, TIPS-Pentacene was used as semiconductor. Results on the comparison between these two sets were enlightening, since it was quite obvious which one was better. Bottom gate-bottom contact OFETs showed a dramatical reduction in mobility over the course of the analysis, due to the effect that both oxygen and water had on the active layer, a problem that, more or less, all organic materials have. One reason for which the double gate structure proved to be better is exactly related to this problem, in fact, both the dielectric layer and the top gate, protect the active layer from the action of these two environmental factors. In fact, mobility in these devices stayed practically the same during all the testing, meaning that this architecture effectively protects the most fragile part of the device. Of course, protection extends also to possible mechanical damage, like scratches, that could ruin the active layer. Moreover, one thing that only double gate architecture can do, is enhance the control over the channel due to the manipulation of the device properties from each gate. In fact, while biasing the device from one of the gates, the

other one can be used to shift the threshold voltage of the device, and, since they are tightly connected, also the mobility varies, both in an almost linear fashion. This characteristic opens to the possibility to have a set of devices that need to work together, all set to the same working point, even if during fabrication process, some differences could lead to different behaviours. Following this, analysis was extended to devices in which the semiconductor is N1400 or DPP-DTT, however results weren't quite as satisfactory. For this part of the testing, the top gate-bottom contact architecture was added in the analysis, since some semiconductors work better in this configuration, but also to verify if double gate architecture joined the positive aspects of the other two. For what concerns the bottom gate-bottom contact one, with both semiconductors, a confirmation of the results previously obtained was given. Particularly, was clearly evident the different relationship that p-type and n-type have with oxygen. In fact, for the former, in the first days it acts as a dopant, increasing the number of charge carriers available, while for the latter, since majority carriers are electron, the detrimental effect is immediately evident. DPP-DTT, was deposited both through drop-casting and spin-coating and results were very different. A problem with the former technique was that the active layer thickness was considerable and therefore, also the top dielectric layer had to be made thicker to avoid shorts, losing in the process a bit of control over the channel. On the contrary, using the latter technique, the active layer was too thin, and it had difficulties forming the channel. Even by reducing the spin speed, results were still disappointing. For this reason, ulterior tests are being performed to optimize the structure using this semiconductor, that has some advantages over the TIPS-Pentacene, as in principle should have a higher mobility. For what concerns N1400, the semiconductor has shown very poor performances, and, due to some reason that is still under investigation, double gate devices never worked properly. However, other new organic semiconductor can be tested, even though it is difficult to find n-type one, stable in air as N1400.

Having characterized the devices for their electrical properties, the next step is to verify if they can be used as sensor. For this characterization, they were tested as temperature and force sensors, using some devices previously fabricated but never used for anything else, excluded the characterization when realized. The chosen devices were TIPS-Pentacene based and each of them was characterized both as a temperature and force sensor. Temperature characterization was performed by pairing each device with different capacitor made of PVDF, a pyro and piezoelectric material. Capacitors dimensions were 1 mm², 9 mm² and 25 mm². They were positioned on top of a Peltier Cell, controlled by a power supply

and temperature was monitored through an optical pyrocouple, which was connected to the reading system and another power supply. Seven different temperature steps were chosen, and each one was performed five times, to then average the response of the device to the stimuli. Devices proved to have quick and reproducible responses, in a range of temperatures that was dependent also on the capacitor used. In fact, for bigger capacitors, response tends to saturate for higher temperatures. A very important aspect of these devices is that they don't have hysteresis as sensor, since response, and thus sensitivity, is practically the same in both directions of variation of temperature. Force characterization was performed with the aid of an indenter connected to a dynamometer, the same PVDF capacitors with the exclusion of the 1 mm² one, due to some limitations in the measuring setup. In fact, proximity effects when the indenter approached to the capacitor, completely covered the response of the device, and not even a preload resolved the issue. As for temperature, seven different values of force were selected and applied five times each, to then average the response of the device. Also in this case, response was quick and reproducible and not saturation was observed. This is probably related to the fact that piezoelectric constant is smaller than the pyroelectric one, meaning that a smaller amount of charge is induced. Also, in the case of force sensing, hysteresis is practically absent, with response and sensitivity almost identical in both forward and backward direction. An ulterior test that's been performed was to join the two setups to characterize the devices in a multimodal condition. For this, three values of temperature were chosen, and for each one, five values of force were applied. Devices were able to sense both quantities and discern between them, thanks to the fact that piezoelectric and pyroelectric vectors are opposite.

Summarizing, the Double-Gate structure offers a solid solution to organic electronic problems related not only to degradation, device stability and robustness, but also for sensing applications in several field of research. In fact, this structure effectively mitigates active layer degradation, thanks to its self-encapsulating design; moreover, a second gate enables fine-tuning of device performance over time, ensuring consistent behaviour even across large production batches. In circuitry applications, the second gate can be used to adjust the working point of the devices so that the optimization process can be made easier. For sensors applications, the second gate can be used both as a sensing platform and to set the device at a specific condition, so that sensitivity and device reproducibility is optimized.

The interest in the Double-Gate organic technology opens to a variety of solutions in the field of flexible electronics. Also, from the commercial perspective, it is a device architecture

which, after optimization of design and materials, could be a prominent technology for flexible electronics used in real life contexts. Future development might lead to the realization of a fully integrated device, capable to acquire and transmit data over a short or extended period of time. Devices might be self-powered or integrated with a non-invasive power supply like a flexible solar cell or battery. They can be embedded in clothes or directly applied to the skin, as the research goes in the direction of biocompatibility. For these purposes, the Double-Gate characteristics of robustness, and durability, as well as full control over the device behaviour, are of primary importance to achieve a reliable device.

The second topic of the thesis is always related to sensing, specifically strain sensor, that is still open, since multiple tests and optimizations can be made. For this, a different kind of OFET architecture is employed, because, to reduce unwanted effects given by the bending of the connections, they must be far away from the channel area, which is the one that will be bent to characterize the response of the device, but also the behaviour of the semiconductor in response to mechanical stress. One important aspect that will be verified will be the reversibility limit for each semiconductor, expressed in strain percentage. Initially TIPS-Pentacene and N1400 were investigated. The latter showed a more stable response to bending, with negligible differences in the transfer characteristic curves acquired at different bending radius. The former showed instead a drop in performances for the smaller bending radius, indicating that something occurred in the semiconductor structure. Fatigue test, consisting of 200 bending cycles, further exacerbate this difference, with TIPS-Pentacene devices that have a drop in performances of around 40%, while N1400 sees no significative reduction. XRD and AFM imaging shed some light on such behaviour, with the former semiconductor showing cracks in its surface, not present in the latter. These cracks hinder the electrical transport, reducing the overall mobility inside the channel. A similar test was performed for devices DPP-DTT based. Although preliminary, some results can be extracted from the analysis, in accord with literature. Transfer curves acquired at different bending radius, showed a more marked effect on DPP-DTT with respect to N1400, even though they are both polymers. In principle, depending on the bending mode, elongation or compression, we should see a reduction or increase in output current, respectively. This is due to the fact that, with the former grain borders are getting away from each other, while with the latter, the opposite should happen. From the analysis, this is not what happens, because, if for the first assumption it is true, the same cannot be said for the second. In the latter case, after a first increase, a consequent decrease in performances occurs. According to literature, this might happen due to how the DPP-DTT is packed, as crystallization happens in an ordered

fashion. However, this also leads to problems present also in TIPS-Pentacene system, where cracks start to appear after a certain bending radius. Stress tests on DPP-DTT based devices show that for bending cycles, shifts in performances happen between 30 and 50 bends, while are stable before and after that threshold. This means that in that interval, something happens to the semiconductor structure, that hinders the charge conduction. As literature reports, crack formation heavily depends on semiconductor thickness and further investigation on semiconductor performances evolution, as well as XRD and AFM imaging, might shed some light on its behaviour and help optimize its use. Looking at the device performance, responsiveness is quick and reproducible, meaning that under a certain strain, variations in current output are reversible.

Future perspectives for the development and enhancement of the devices include the optimization of the fabrication process, optimization of the semiconductors' deposition recipe, and use of new ones that could help enhance the control over the device properties from the top gate by thinning the top dielectric layer. Tattooed devices with the integrated PVDF capacitor are also in the making, so that acquisition can be performed directly on human skin. A redesign of the whole structure could improve overall performances, meanwhile reducing the device's dimensions.

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