Performance Analysis of Zero-Sequence Voltage Balancing Methodologies in Grid-Tied NPC Converters for EV Charging Systems

Mauro Boi
Dept. of Electrical and Electronic Engineering
University of Cagliari
Cagliari, Italy
mauro.boi@unica.it

Zohaib Ejaz
Dept. of Electrical and Electronic Engineering
University of Cagliari
Cagliari, Italy
zohaib.ejaz@unica.it

Giuseppe Bossi
Dept. of Electrical and Electronic Engineering
University of Cagliari
Cagliari, Italy
giuseppe.bossi@unica.it

Alfonso Damiano
Dept. of Electrical and Electronic Engineering
University of Cagliari
Cagliari, Italy
damiano@unica.it

***Abstract*—The performance of zero-sequence voltage compensation algorithms in a three-phase neutral point clamped (NPC) converter acting as an interface between a DC charger for electric vehicles and the grid has been modelled, simulated and experimentally validated. In particular, the analysis of zero-sequence voltage methods has been investigated, as they provide an effective solution to this problem regardless of the modulation technique used. This study focuses on the development of an electric vehicle charging station supplied by an NPC converter, where both the linear control of the DC voltage unbalance and the optimal zero-sequence voltage detection methods are studied. Finally, the results obtained from the implementation of linear control of the DC voltage unbalance is reported.**

***Index Terms*—Balancing algorithm, NPC converters, zero-sequence voltage, DC electric vehicle charging station.**

I. Introduction

The ongoing demand for increasing power output from Electric Vehicle (EV) charging systems, coupled with the requirement to develop bi-directional technology for implementing Vehicle to Grid (V2G) paradigm, is driving the need for innovative EV charging solutions [1]. These equipments provide EV DC supply by conditioning the power delivered by the interconnected electricity network.

Considering the expected growth of electric mobility, there is an increasing demand for more efficient and flexible AC/DC power conditioning systems committed to electric vehicle charging [2]. The growing need for flexible EV charging solutions has led to innovative power electronic converter topologies [3]. These have to manage efficiently bidirectional power flow between the power system and the EV charger, enabling various operational strategies [1]. A typical DC fast charging station has two main components: an AC/DC grid-tied inverter, commonly named Power Factor Correction (PFC) stage, and a DC/DC converter. The PFC stage is responsible for ensuring proper interconnection between the power system and the DC-EV charger. It delivers the necessary power while adhering to established standards, particularly in terms of reducing current harmonics and optimizing the power factor (PF).

The next stage of the EV charger involves a DC-DC converter. This unit converts the input DC voltage according to the supply voltage specification of the EV. In particular, it must control the voltage applied to the EV battery to implement the charging/discharging process and satisfy the constraints monitored by the battery management system. Key features of a DC-DC converter include bi-directional operation, high power density, high efficiency, minimal voltage stress on components, and a wide voltage gain.

The DC-DC converters for EV applications are generally classified into two cluster: non-isolated and isolated converters [3]. For safety reasons, it is essential to maintain isolation between the EV battery and the grid. For this purpose the isolated DC-DC converters are preferred for this application. An effective way to achieve galvanic isolation is to use high frequency transformers properly supplied and managed for performing the DC-DC power conditioning. Specifically, the Dual Active Bridge (DAB) is appealing for EV charging due to their compact size, high power density and efficiency [4] [5].

In this context, the authors present their research as part of a project aimed at developing a fast-charging infrastructure. This paper outlines the activities involved in designing the Power Factor Correction (PFC) system.

As it is well known, the three-phase grid-tied converters achieve higher power levels and bidirectional operation, reduce current stress, provide a reliable control system, minimize Total Harmonic Distortion (THD), and enhance overall efficiency concerning single phase one [6]. Therefore, the study focuses on a three-phase grid-tied Neutral Point Clamped (NPC) converter, which enables a Dual Active Bridge (DAB) to effectively manage DC voltage conditioning for charging electric vehicle (EV) batteries. The NPC offers several advan-

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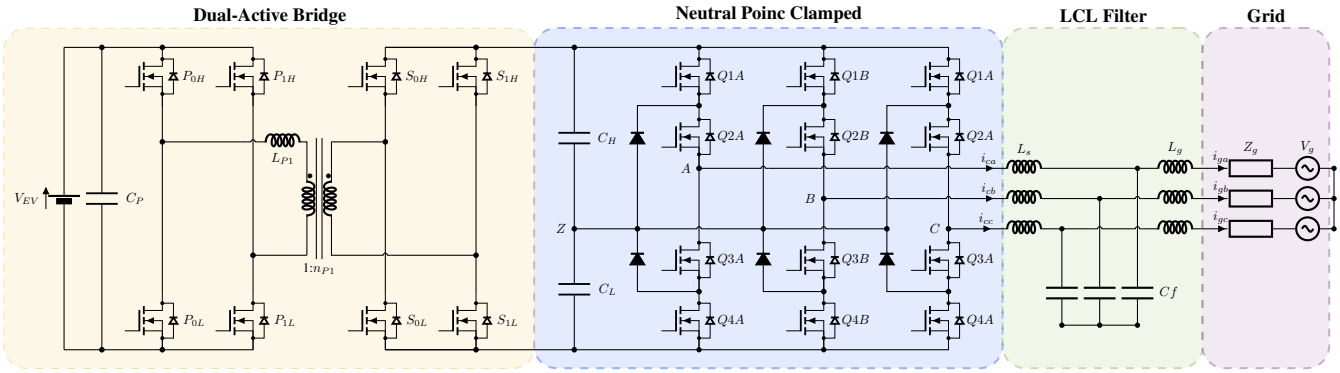


Fig. 1. Schematic of proposed EV charging station.

tages over conventional two-level converters, including lower losses, higher switching frequency, reduced filter size and weight, improved reliability, and lower costs. Additionally, the use of the NPC converter facilitates a bipolar DC infrastructure for DC-bus-fed charging stations. This setup can support higher system voltages, handle greater power loads, improve power quality, and provide more flexible options for energy management [7]. However, the NPC converter presents a critical issue associated to the DC-link neutral-point (NP) potential variation which leads to a decrease in the output quality specifically in the proposed configuration [8]. Different strategies have been suggested in scientific literature to mitigate this phenomenon according to pulse-width modulation (PWM) techniques utilized [9], [10].

The injection of zero-sequence voltage is the only one that guarantees the NP balancing independently of the modulation strategy implemented. It should therefore be emphasised when considering the NP balancing problem [7] [11] [12] [13].

With regard to the design of the EV charging station according to the proposed configuration, the NP balancing of the NPC converter plays a key role because it affects the power quality on the AC side and introduces critical operating conditions on the DC side that make the system unreliable.

Therefore, the implementation of the proposed topology requires the balancing of the voltages across the two DC side capacitors of the NPC. Consequently, a thorough analysis of the DC voltage balancing algorithms proposed in the literature based on zero-sequence voltage injection has been carried out and evaluated to determine their effectiveness in the proposed EV charging system [11] [14].

The paper is structured as follows: Section II describes the NPC converter, Section III present the digital control algorithm design. Section IV reports the voltage balancing algorithm under investigation. Section V presents the simulation study. Finally, Section VI reports and discusses the experimental tests on scaled prototype of NPC converter when PI balancing control is implemented.

II. Grid-Tied NPC Converter

The system under discussion consists of a grid-tied NPC converter connected to Dual Active Bridges (DAB) that perform EV charging process, via DC bus. The purpose of the DAB is twofold. Firstly, it galvanically isolates the EV-battery from the DC bus. Secondly, it regulates the battery voltage during the charging and discharging processes, according to the V2G control strategy. The condition of constant voltage on the DC power distribution system of the charging station is mandatory to ensure the correct operation of the designed topology.

In order to develop a scaled setup on which to validate the proposed electric vehicle charging station management methods, a prototype was developed. As a first step, the design of the three-phase NPC converter was carried out in accordance with the design specification given in Table I. The NPC converter employs IGBT switches and includes an LCL filter. The schematic representation of the three-phase grid-connected NPC converter is reported in Fig.1. An 8 kVA insulation transformer has been interposed between the filter and the main grid to prevent zero-sequence current exchange. The NPC converter is accomplished by paralleling three NPC half-bridges (PEN8010) manufactured by Imperix. The main characteristics of these components are reported in Table II. The half-bridge PEN8010 is equipped with P924F33 module manufactured by Vincotech. It is evident that each half-bridge has a DC bus, which is constituted by two banks of capacitors, named C_H and C_L each characterised by a capacitance of $517\mu F$. It can thus be concluded that, in view of the parallel connection of the three NPC half-bridges, the final values of C_H and C_L are 1.55 mF, respectively.

The LCL filter was designed with reference to the specifica-

TABLE I
Design Specifications

Rated power	P_r	8	kVA
Rated grid voltage	V_g	400	V_{RMS}
Rated current	I_r	11.5	A_{RMS}
Ratel grid frequency	f_g	50	Hz
Rated switching frequency	f_{sw}	20	kHz
DC-link voltage	V_{DC}	700	V

TABLE II
NPC HALF-BRIDGE PEN8018 MODULE RATING

DC Bus voltage	V_{DC}	800	V
Maximum continuous current	I_{DC}^{max}	18	A_{RMS}
Maximum pulsed current	I_{DC}^{pulsed}	90	A
Reference switching frequency	f_{sw}	20	kHz
DC bus capacitances	$C_H\, C_L$	517	μ F
Maximum switching frequency	f_{sw}^{max}	50	kHz

TABLE III
LCL FILTER PARAMETERS

Insulation transformer inductance	L_t	$0,68$	mH
Grid side inductance	L_g	$2,2$	mH
Resistance of grid side inductance	R_g	65	mΩ
Converter side inductance	L_s	$2,2$	mH
Resistance of converter side inductance	R_s	65	mΩ
Capacitor - Wye connection	C_f	10	μ F

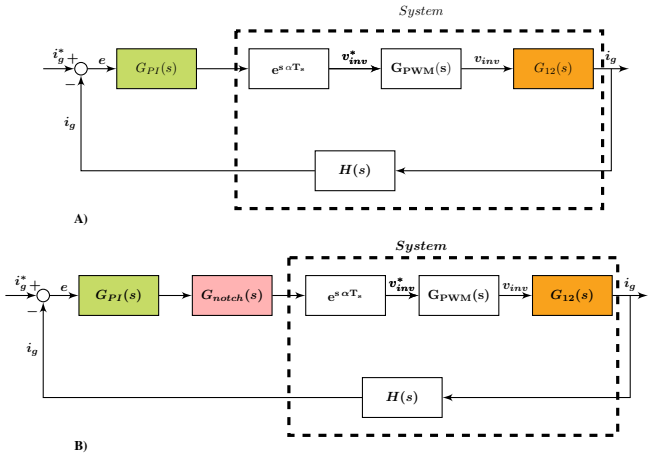


Fig. 2. Block diagrams of d-q current control of grid-tied NPC converter : A) W/O active damping and B) with active damping.

tions given in Table I. An iterative process was used to evaluate the LCL parameters to maximise the power factor, minimise the voltage drop, comply with the constraints imposed by the switching and mains frequencies on the LCL filter resonant frequency and achieve a current ripple in compliance with the power quality standards. [15]. The LCL filter design outcomes are reported in Table III [16].

III. GRID-TIED NPC CONTROL SYSTEM

The synchronous rotating frame (SRF) control strategy for the Neutral Point Clamped (NPC) inverter has been developed based on the model described in equation (1) and referring to grid current feedback configuration [18]. The phase-locked loop, known as SRF-PLL, estimates the instantaneous phase of the grid voltage space vector. The Clark and Park transformations evaluate the currents i_d and i_q, the voltages v_d and v_q on the $d-q$ axes - synchronized with the voltage space vector, through θ. The decoupling of the d and q current loops is achieved through grid voltage feed-forward and the current cross-coupling components compensation. This approach allows for the independent synthesis of the proportional-integral (PI) current controller on the $d-q$ axes using linear control theory, as shown in the block diagram reported in Fig. 2A.

The transfer function of the LCL filter is reported in (2), where the parameters ω_{res} and L' are defined as stated in (3). Given this assumption, and knowing the values of the filter, L_s, L_g, and transformer parameters, L_t, the proportional-integral (PI) current controller parameters k_p and T_i, given in (4), can be set by defining the current loop cut-off frequency ω_c.

The sampling and computation time delay $\alpha\, T_s$ is taken into account in the current control system assuming that the value of $\alpha\, T_s$ does not exceed two sampling period T_s. With regard to zero-order hold (ZOH), the transfer function of sampling and computation time delay associated to digital control and modulation assumes the form reported in (5).

$$\begin{aligned} v_d &= R\, i_d + L\, \frac{d\, i_d}{dt} + \omega_s\, L\, i_q + u_d; \\ v_q &= R\, i_q + L\, \frac{d\, i_q}{dt} - \omega_s\, L\, i_d + u_q; \end{aligned} \tag{1}$$

$$G_{12}(s) = \frac{I_2(s)}{V_1(s)} = \frac{1}{(L_s + L_g + L_t)}\, \frac{1}{s\,(L' C_f\, s^2 + 1)} \tag{2}$$

$$\omega_{res} = \frac{1}{\sqrt{L' C_f}}; \quad L' = \frac{L_s\,(L_g + L_t)}{L_s + L_g + L_t}; \tag{3}$$

$$G_{PI}\,(s) = k_p\, \left(1 + \frac{1}{T_i\, s}\right) \tag{4}$$

The investigation of the open-loop transfer function of the proposed current control system in the s-domain reveals as critical issue that the resonant frequency of the LCL filter, f_{res}, exceeds $f_s/6$. Therefore, the system is susceptible to instability, as evidenced by the Nyquist criteria [17]. The solution implemented is the introduction of a notch filter, as shown in Fig. 2B, characterised by the transfer function reported in (6). The design of the notch filter frequency f_n usually fixes it equal to the LCL resonance frequency f_{res}. However, the observed variations of the network impedance and the LCL parameters suggest to choose a higher value. Moreover, the digital implementation introduces a delay that must be taken into account to ensure that the phase margin reaches values congruent with those required to obtain the settled dynamic performances [18]. Therefore, special attention must therefore be paid to the discretisation of the notch filter.

$$G_{\mathrm{PWM}}\,(s) = \frac{1 - e^{-sT_s}}{s}. \tag{5}$$

$$G_{\mathrm{notch}}\,(s) = \frac{s^2 + +\omega_n^2}{s^2 + 2\xi\omega_n\, s + \omega_n^2} \tag{6}$$

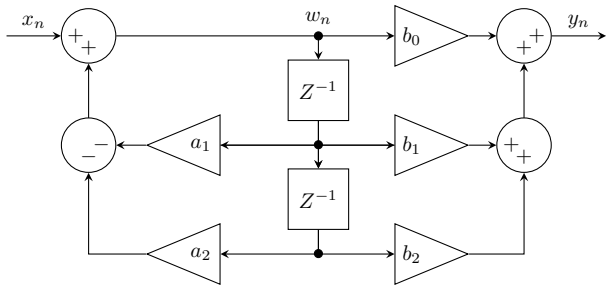


Fig. 3. Digital structure of implemented Notch Filter.

A. Digital Controller

The establishment of the frequency, f_n, is a prerequisite for the implementation of the notch filter design. In this particular instance, the value of f_n has been set at 1660 Hz. The aforementioned value has been defined with reference to the most unfavourable possible condition associated with parameter variations. In particular, the situation of grid impedance equal to zero and a simultaneous drift of 5% of the LCL passive components has been assumed worst-case scenario for the evaluation of f_n. The parameters of the PI controller have been configured to achieve a crossover frequency of 100 Hz. It can thus be concluded that the values of 3.14 V/A and 16 ms are assumed by k_p and T_i, respectively. The discretisation of the notch filter and the PI current controller has been developed by implementing the Tustin transformation to $G_{notch(s)}$ and $G_{PI(s)}$, respectively. With regard to the digital notch filter, the transfer function in the z-domain assumes the form reported in equation (7),

$$G_{notch}(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}}; \tag{7}$$

where the coefficients assume the values reported in (8) and k_1 k_2 are functions of both the natural frequency ω_n and the bandwidth BW, as reported in (9) [18].

$$\begin{cases} a_0 = 1 \\ a_1 = k_1(1+k_2) \\ a_2 = k_2 \end{cases} \qquad \begin{cases} b_0 = \frac{1}{2}(1+k_2) \\ b_1 = k_1(1+k_2) \\ b_2 = \frac{1}{2}(1+k_2) \end{cases} \tag{8}$$

$$\begin{cases} k_1 = -\cos(\omega_n) \\ k_2 = \frac{1-\tan\left(\frac{BW}{2}\right)}{1+\tan\left(\frac{BW}{2}\right)} \end{cases} \tag{9}$$

The digital notch filter $G_{notch}(z)$ can be implemented by using the Direct-Form II transposed (DFIIt) structure whose block diagram is shown in Fig.3. The analysis od closed-loop current z-transformation $W(z)$ confirms the stability of the system. This is due to the fact that all the poles are located within a circle with a radius of one [16].

IV. DC-link Voltage Balancing

A challenge associated with NPC converters pertains to the potential occurrence of unbalance phenomena between the capacitors that constitute the DC bus. This phenomenon is associated with the use of a specific switching state of the NPC, which has been shown to cause average current circulation on the neutral point of the DC bus. It is known that the zero vectors and large vectors have no effect on NP potential, but the middle vectors and small vectors have effect on it causing voltage imbalances between capacitors C_H and C_L [8], [13].

The control strategies reported in the scientific literature for balancing the neutral point Z can be classified according to the modulation algorithm employed. It has been established that the injection of zero-sequence into the voltage-modulating signal enables the compensation of this effect [14]. In particular, the utilisation of a PI controller, supplied by the voltage unbalancing occurring between the capacitors C_H and C_L, facilitates compensation. Nevertheless, the algorithm necessitates the estimation of the sign of active component of NPC output space current vector I_d and power factor PF in order to ensure stability under all operating conditions. The efficacy of the proposed strategy is contingent upon the limit imposed on the normalised zero-sequence voltage remaining within the specified range of $\pm$ 1. The main advantage of this voltage balancing technique is the simplicity. However, it requires to increase the DC bus voltage in order to assure the possibility to implement the compensation in all different operative conditions [14].

An alternative approach consists of the usage of a search-optimisation algorithm. The interpolation method is employed to calculate the exact zero-sequence voltage for NP potential balancing. The algorithm is characterised by a high degree of complexity, which is ascribable to the existence of a non-linear and discontinuous relationship between the neutral current and the zero-sequence voltage. Nevertheless, the efficacy of the compensation action is particularly pronounced [11].

In the present paper, the two methodologies have been analysed and simulated. Finally the comparison of their performances have been reported.

V. Simulation Results

To evaluate the performance of the proposed voltage compensation strategies, simulation tests were performed using Simulink Plecs software under three different conditions: the system steady-state response without compensation, the system steady-state response with compensation, and the dynamic response of the system to a step change with compensation active. These tests were specifically designed to evaluate system performance at elevated operating set points, with the grid voltage set at 220 V_{rms}, the DC bus voltage maintained at 750 V, and the reference current initially set at 4 A and then step changed at 8 A. The primary objective was to rigorously evaluate the system robustness, voltage stability and responsiveness of the zero sequence balancing algorithm under both steady state and transient operating conditions.

Fig. 4 illustrates simulation outcomes for grid voltages, currents, and NPC neutral-point voltages under conditions without the application of any balancing control. The results distinctly

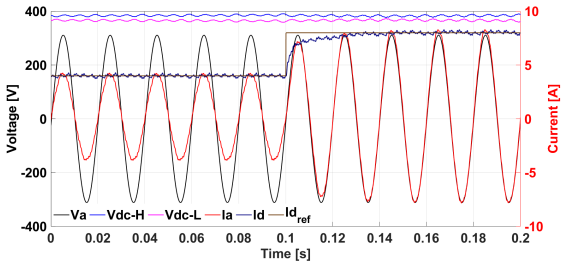


Fig. 4. Outputs of Grid Voltages, Currents and NPC neutral points voltages

highlight a disparity between upper and lower DC-link capacitor voltages (V_{DC}^{H} , V_{DC}^{L}). This voltage imbalance arises due to inherent neutral-point currents in the NPC topology, manifesting as fluctuations that compromise power quality and stability. Consequently, the absence of active balancing significantly affects converter reliability, elevates stress on the DC-link capacitors, and potentially deteriorates grid interfacing performance. Such discrepancies underscore the critical necessity for appropriate zero-sequence voltage compensation techniques within NPC-based converter systems.

A. Linear Zero-Sequence Voltage balancing Test

In the linear control approach for neutral-point (NP) voltage balancing, a proportional-integral (PI) controller has been employed to mitigate voltage discrepancies between the upper and lower DC-link capacitors of the NPC converter [14]. This PI controller operates by monitoring the differential voltage across these capacitors, subsequently generating a zero-sequence voltage component integrated with the SVPWM reference voltages. The PI parameters, specifically set at k_p=0.2 and k_i= 31.4, have been tuned according to the DC-link capacitor characteristics, establishing a bandwidth of 30 Hz to ensure robust balancing performance. Extensive simulations conducted in both steady-state and dynamic load variations confirm the effectiveness of this controller. Results illustrated in Fig. 5 highlight the response of outputs of the system and also demonstrate the dc link balanced.

In particular, the system is initially tested under steady-state conditions with parameters of voltages and current defined for the system, while maintaining a constant current set-point of 4 A. The results are reported in the Fig. 5(a). This scenario confirms stable and balanced DC bus voltages (V_{DC}^{H} , V_{DC}^{L}), alongside satisfactory output current and voltage waveforms, validating the system's reliable steady-state operation. Subsequently, Fig. 5(b) depicts the dynamic response of the DC-link voltages and converter outputs during a step increase of the current reference from 4 A to 8 A. Even under this abrupt transient condition, the PI-based controller efficiently maintains the DC bus voltage equilibrium, demonstrating robustness and efficacy in mitigating potential unbalances under varying operational loads. This PI-based voltage balancing strategy shows considerable potential for enhancing operational reliability and ensuring optimal power.

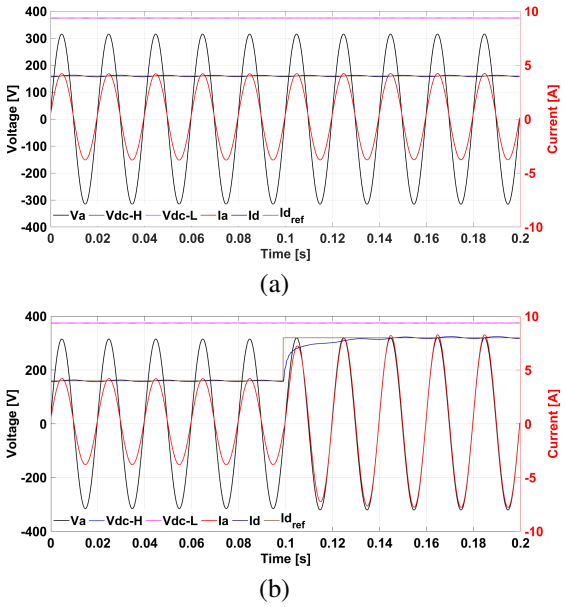
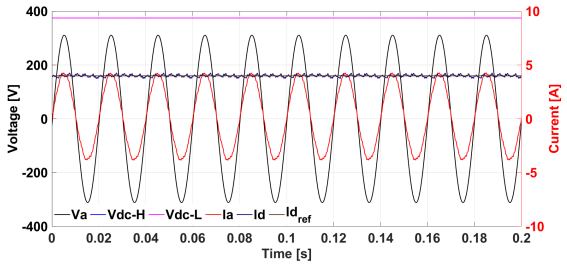


Fig. 5. Steady-state performance of the NPC converter with a constant current set point of 4 A (a); Transient response during a step variation of the current setpoint from 4 A to 8 A for assessing the PI voltage balancing capability (b).

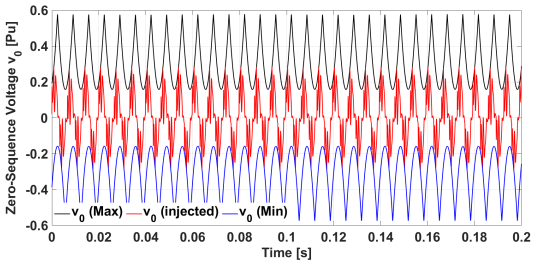
B. Optimal Zero-Sequence Voltage balance Test

The Optimal Zero-Sequence Voltage balancing approach precisely calculates the required zero-sequence voltage to manage the NPC converter's DC-link neutral-point potential [11]. In this test, the optimal zero-sequence voltage balancing algorithm is precisely evaluated by calculating the zero-sequence voltage (v_0) within defined constraints of v_0^{min} and v_0^{max}, effectively preventing overmodulation scenarios. The algorithm meticulously identifies the correct zero-sequence voltage through interpolation, ensuring that any calculated v_0 exceeding the permissible range is appropriately limited. The implementation systematically attenuates DC-link voltage discrepancies, maintaining symmetrical voltages across the high and low DC capacitors V_{DC}^{H} , V_{DC}^{L}. Technical validation specifically targets critical operational conditions to verify that the neutral-point potential remains balanced and the converter output maintains optimal performance, especially during transient load variations. Fig. 6 show the results of the system and evolution of the zero sequence voltages that contribute to balance the DC link of NPC.

Fig. 6 demonstrates the operational effectiveness of the optimal zero-sequence voltage balancing algorithm under a constant current set point of 4 A. Specifically, Fig. 6(a) shows the three-phase current waveforms, confirming the controller's capability in accurately tracking the imposed reference (id), thus maintaining superior current quality with negligible harmonic distortion. Fig. 6(b) illustrates the calculated zero-sequence voltage (v_0) alongside its corresponding boundary conditions, v_0^{min} and v_0^{max}. It is evident from the plot that the computed zero-sequence voltage remains strictly within these defined limits, ensuring that overmodulation conditions are effectively prevented. Furthermore, the neutral-point (NP) po-

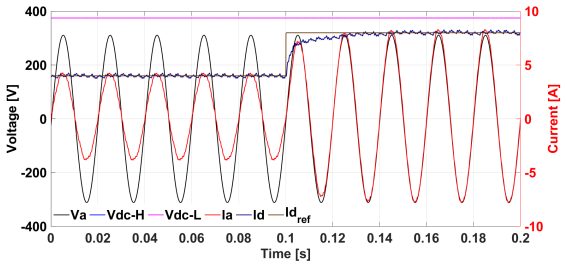


(a)

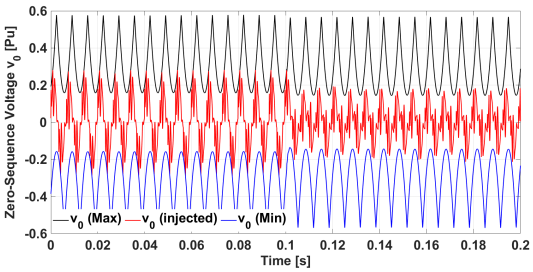


(b)

Fig. 6. Output current evolution with Id reference tracking under optimal zero-sequence control (a). Zero-sequence voltage (v_0), its bounds (v_0^{min} and v_0^{max}), NP potential, and zoomed DC-link voltages (V_{DC}^H , V_{DC}^L) at 4 A reference (b).



(a)



(b)

Fig. 7. Output currents and Id tracking during a step change from 4 A to 8 A (a). Evolution of zero-sequence voltage (v_0), limits (v_0^{min} and v_0^{max}), NP potential, and zoomed DC-link voltages (V_{DC}^H , V_{DC}^L) under dynamic load (b).

tential remains consistently balanced, indicating minimal voltage fluctuations between the DC-link capacitors (V_{DC}^H , V_{DC}^L) under the steady state condition.

Fig.7 evaluates the dynamic response of the optimal zero-sequence voltage control under a current step from 4 A to 8 A. In Fig.7 (a), the converter maintains high-quality voltage and current waveforms with smooth i_d tracking across the transition. In Fig.7 (b), the zero-sequence voltage remains bounded within v_0^{min} and v_0^{max}, ensuring modulation remains linear and distortion-free. The NP potential stays tightly regulated, while the DC-link capacitor voltages remain balanced throughout the transient, confirming the robustness of the control algorithm under variable load conditions. This demonstrates strong dynamic performance and effective suppression of DC-link unbalance.

VI. Experimental Results

The control algorithms have been implemented on the prototype according to the design procedure reported in Section III, using a rapid prototyping controller (B-Box RCP 3.0) employing Matlab/Simulink [16]. The B-Box RCP 3.0 is equipped with a dual-core 1 GHz ARM processor, which allows for a closed-loop control frequency up to 250 kHz. The sampling frequency has been set at 20 kHz. Three isolated voltage sensors with a measurement bandwidth of 60 kHz, an accuracy of 0,15 % and input voltage ranging till 800 V have been installed on the PCC. Three isolated current measurement sensors (LAH 50-P) provide the feedback signals for current loop control. A four-quadrant grid simulator (Regatron TC.ACS) with a rated power of 50 kVA is used as a grid voltage source. The test bench is shown in Fig.8.

To perform the test, a symmetrical sinusoidal three-phase voltage of 220 V_{RMS} at a frequency of 50 Hz was imposed as the mains voltage. The DC bus voltage V_{DC} was set at 750 V. The performances were evaluated for different operating current conditions.

The initial test was executed by employing the PI regulator as the voltage balancing algorithm, with the objective of imposing a zero sequence voltage on the NPC converter. The PI parameters k_p and k_i of voltage balancing controller have been fixed at 0.2 and 31.4, respectively. The PI voltage balancing configuration has been subjected to rigorous testing in both steady-state and step-current application modes. The results are presented in Fig.9 and Fig.10. The test in steady state demonstrates that the grid voltage and the current injected are characterised by a satisfactory power quality. In particular, the current harmonic spectrum reveals, as would be expected,

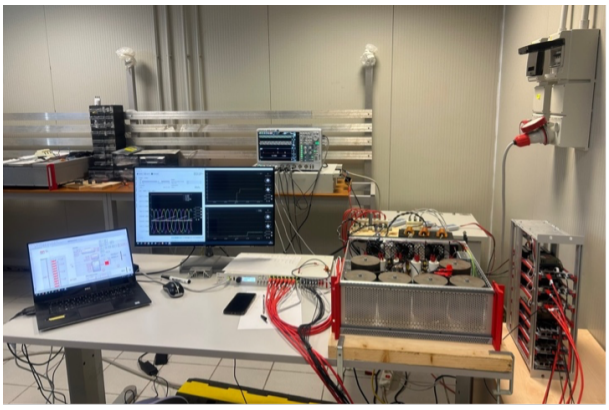


Fig. 8. The Test bench used for the experimental validation

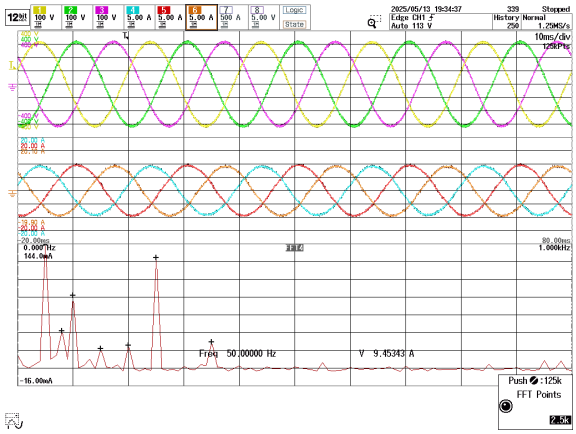


Fig. 9. Steady-state test results when PI control of DC voltage unbalances is implemented: Grid Voltage time evolutions 220 V_{rms} (upper traces); Grid current injected by NPC when a i_d set-point of 10A is imposed (middle traces); current harmonic spectrum (lower trace).

the presence of odd and even components characterised by small amplitude. The component of greatest magnitude is the fifth, the amplitude of which is less than 1% of the fundamental one. The existence of harmonic components has been demonstrated to be concomitant with fluctuations in the DC bus voltage. It can thus be concluded that the low amplitude of the signal is indicative of the efficacy of the DC voltage balancing algorithm.

The next test is performed imposing a step current variation for 4 A to 8 A on the i_d current component on the SRF. The results reported in Fig.10 confirms the goodness of the current control that has dynamic performance coherent with the imposed bandwidth of 100 Hz. In order to evaluate the voltage evolution on the capacitors C_H and C_L the experimental evolutions of measured voltages during the step current application are reported in Fig.11. The voltages on the DC bus capacitors remain permanently at 375 V, unaffected by step current variation. Nonetheless, an oscillation of voltage at 50 Hz is evident on the capacitors C_H and C_L, with an increase

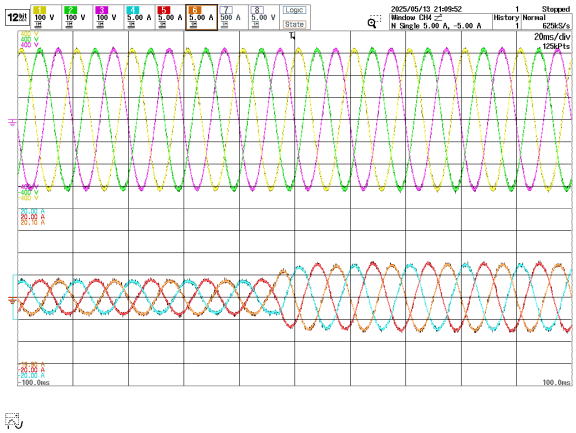


Fig. 10. Transient evolution during the application of a i_d step current variation from 4 to 8 A PI control of voltage unbalances: Grid Voltage time evolutions 220 V_{rms} (upper traces); Grid current injected by NPC (lower trace).

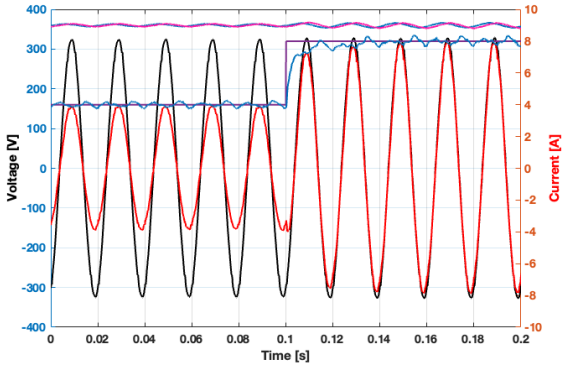


Fig. 11. Transient evolution during the application of a i_d step current variation from 4 to 8 A when linear control of voltage unbalances is implemented. Phase voltage (black trace) and current (red trace) evolution on grid side; i_d current set-point (magenta trace) and measured one (light blue trace); C_H and C_L voltage measurements (upper traces).

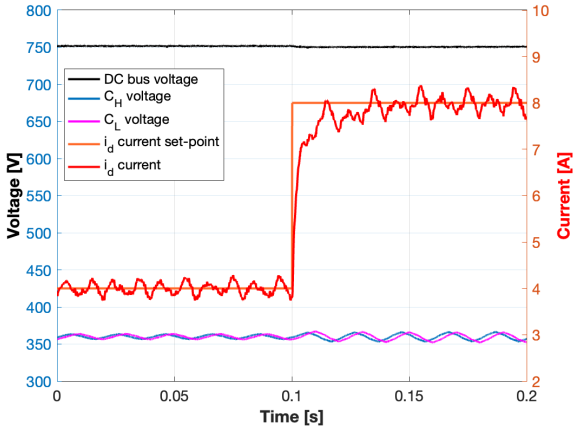


Fig. 12. Zoom of transient evolution during the application of a i_d step current variation from 4 to 8 A when linear control of voltage unbalances is implemented.

in amplitude concomitant with an increase in current. In order to emphasise the correlation between this phenomenon and voltage imbalance, a detailed analysis is presented in Fig.12. This figure comprises a zoomed-in view of the transient, in conjunction with the measurement of the DC bus voltage.

VII. Conclusion

The present paper reports on the design of a grid-connected three-phase neutral point clamped (NPC) converter, with a view to facilitating the development of a fast-charging infrastructure. The hardware and control design is reported to be a scaled prototype. A specific study has been developed on the compensation of unbalancing phenomena occurring on the NPC. Specifically, the mitigation of unbalancing DC voltage based on zero-sequence voltage injection has been investigated. A simulation study was conducted to analyse the utilisation of both linear and non-linear control strategies. This study was informed by a developed NPC topology, and the experimental validation was subsequently performed on the linear strategy.

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REFERENCES

[1] A. Rachid, H. El Fadil, K. Gaouzi, K. Rachid, A. Lassioui, Z. El Idrissi, and M. Koundi, "Electric vehicle charging systems: Comprehensive review," *Energies*, vol. 16, no. 1, 2023.

[2] S. Ali Qasem Mohammed, S. Saleh Hakami, M. Kassas, and M. M. Almuhaini, "Critical review on powertrain technologies for electric vehicles: Classification, broadly adopted topologies, and future challenges," *IEEE Access*, vol. 13, pp. 71 755–71 772, 2025.

[3] R. P. Upputuri and B. Subudhi, "A comprehensive review and performance evaluation of bidirectional charger topologies for v2g/g2v operations in ev applications," *IEEE Transactions on Transportation Electrification*, vol. 10, no. 1, pp. 583–595, 2024.

[4] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional dc–dc converter for high-frequency-link power-conversion system," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091–4106, 2014.

[5] G. Bossi, C. Song, A. Sangwongwanich, F. Blaabjerg, and A. Damiano, "A harmonic-based triple phase shift modulation strategy for a dual active bridge converter in an all electric aircraft application," in *2024 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2024, pp. 1117–1123.

[6] A. Mallik, W. Ding, C. Shi, and A. Khaligh, "Input voltage sensorless duty compensation control for a three-phase boost pfc converter," *IEEE Transactions on Industry Applications*, vol. 53, no. 2, pp. 1527–1537, 2017.

[7] L. Tan, B. Wu, V. Yaramasu, S. Rivera, and X. Guo, "Effective voltage balance control for bipolar-DC-bus-fed EV charging station with three-level DC–DC fast charger," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4031–4041, 2016.

[8] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting*, 1993, pp. 965–970.

[9] M. Porru, A. Serpi, I. Marongiu, and A. Damiano, "Suppression of dc-link voltage unbalance in three-level neutral-point clamped converters," *Journal of the Franklin Institute*, vol. 355, no. 2, pp. 728–752, 2018.

[10] H. Wang, L. Ha, J. Lin, S. Wang, S. Xie, X. Chen, and M. Su, "A mathematical structural modulation method for neutral-point potential balancing of three-level neutral-point-clamped converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 2, pp. 1573–1582, 2024.

[11] Chenchen Wang and Yongdong Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2262–2271, 2010.

[12] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Transactions on Power Electronics*, vol. 15, no. 2, pp. 242–249, 2000.

[13] F. Chen, W. Qiao, H. Wang, and L. Qu, "A simple zero-sequence voltage injection method for carrier-based pulsewidth modulation of the three-level npc inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4687–4699, 2021.

[14] C. Newton and M. Sumner, "Neutral poit control for multi-level inverters: theory, design and operational limitations," in *IEEE Industry Applications Socity IAS Annual Meeting*, 1997, pp. 1336–1343.

[15] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an lcl-filter-based three-phase active rectifier," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1281–1291, 2005.

[16] M. Boi, G. Bossi, and A. Damiano, "Digital notch filter design for grid side current control of lcl-filtered grid-connected converter," in *2024 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2024, pp. 332–338.

[17] S. G. Parker, B. P. McGrath, and D. G. Holmes, "Regions of active damping control for lcl filters," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 424–432, 2014.

[18] W. Yao, Y. Yang, X. Zhang, F. Blaabjerg, and P. C. Loh, "Design and analysis of robust active damping for lcl filters using digital notch filters," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2360–2375, 2017.