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Solar powered high gain DC-DC converter with FPGA controller for portable devices

Vijayalakshmi Nanjappan [a], Suganthi Ramasamy [b], Gianluca Gatto [b], Amit Kumar [b,*]

[a] Department of Computer Science and Engineering (Data Science), Dayananda Sagar College of Engineering, Bangalore, India
[b] Department of Electrical and Electronic Engineering, University of Cagliari, Cagliari 09123, Italy

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ABSTRACT

A solar-powered converter design is necessary for portable devices with increased gain and reduced ripple in overall operation. This research presents a photovoltaic-powered Field Programmable Gate Array (FPGA) based on increased gain multiple output converter design and analysis. The dynamic panel input makes it difficult to operate the load. To control and make the input static to satisfy the demand, perturb and observe with a load balancing algorithm technique are used. The converter gained output is high, and batteries are used to balance the loads when solar irradiance is low. Simulation results were carried out with the presented converter circuit that can be operated with a 12 V supply as input from a renewable power source. The output gain ratio of 14 to a minimum of 40 % duty cycle operating at a switching frequency of 20 kHz has been achieved. The proposed methodology is transferred to hardware by connecting with the reconfigurable FPGA Spartan-6 development board to manage the dynamic load control system's complex logic and high processing ability. The overall performance is compared with various pre-existing systems, tabulations are made with the analysis, and experimental results are also illustrated at the end.

1. Introduction

The general block diagram of the proposed solar-powered High Gain Dual Output (HGDO) converter system with Field Programmable Gate Array (FPGA) based MPPT with load balancing algorithm is shown in Fig. 1. The energy harvested from the array of photovoltaic (PV) cells needs to be regulated for empowering the dynamic DC loads. Battery based energy storage is required for solar PV systems to maintain the system's reliability [1]. So, the proposed topology combines PV power with a battery storage system to improve the performance of the overall output needs. Also, the voltage produced from the PV panels will not satisfy the varying load demand. So, this hybrid system can be implemented with higher efficiency and reduced ripple boost converter to fulfill the load needs despite irregular supply. The solar cell's Maximum Power Point Tracking (MPPT) mainly depends on the solar irradiance at a location and temperature. To maximize the power output of solar PV panels, tracking maximum power continuously for varying irradiation is necessary. Nowadays, several studies have mainly focused on various MPPT control based decisive algorithms to obtain maximum power from the panel.

Previously, authors proposed an interleaved converter with a voltage doubler and energy-distributing circuit to achieve high gain and efficiency for DC applications [2]. For a high-power application of 450 W, the gain of approximately nine times was achieved with the interleaved converters. However, the high duty ratio is not applicable for hybrid/-integrated power generation systems [2-4]. The boost converters with and without a transformer are discussed, in which transformer-type boost converters have an isolated transformer that only transfers the energy. However, the non-isolated type can store flux in the core, which helps reduce electromagnetic interference. The isolated converter presents two [5] and three [6,7] inductor types. Boost converters are developed in different design types, analysed, and developed for load balancing. In [8], for the voltage lift technique with a switched capacitor, an applicable Luo converter was presented that has the advantage of being compact and low EMI. However, it has a small gain compared to isolated converters [9]. The design of better gain achievability in boost converters, along with mode control options for the input and output voltage, is discussed in [10,11] to maintain the output voltage for PV distributed systems. It has a highly boosted output voltage without any voltage doubler circuit but a single output. In [12], authors

* Corresponding author.
E-mail addresses: viji365@gmail.com (V. Nanjappan), suganthirvk@gmail.com (S. Ramasamy), gatto@unica.it (G. Gatto), amit.kumar@unica.it, amit369@gmail.com (A. Kumar).

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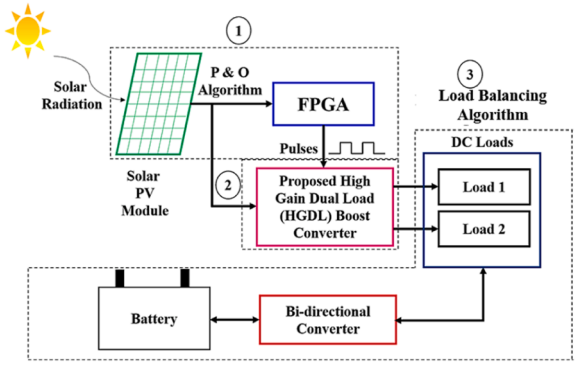


Fig. 1. General Block Diagram of the proposed FPGA-based HGDO converter with Load Balancing Algorithm.

implemented a single input three output boost converter for multi-port operation, which displayed low performance compared to in [13]. The advantages of using MOSFET-based switching devices were discussed, and a comparison of conventional switches with MOSFET devices was made [14]. In [15,16], authors discuss the FPGA-based load predictive MPPT controller for low power, high speed, and energy-saving systems. An interleaved boost converter [17] is used for greater power applications because of reduced ripple content. Nevertheless, the demerits of interleaved boost converters [17] have voltage gain limitations and increased conduction losses due to high power dissipation.

The parameter analysis on high switching speed design and slew rate analysis that helped to identify various switching losses were done in [18]. Authors in [19] presented a non-isolated converter with one voltage multiplier circuit, but in [20,21], two or more voltage multiplier circuits were introduced, increasing the system burden. The combination approach of switched mode and switching capacitor design in the converter can be attained due to the magnetization of the inductor for both switches ON and OFF conditions. In [22], the need for efficient design of DC-DC converters for portable devices was analysed based on power loss analysis. In [23,24], a high gain up-converter is achieved with two MOSFET switches, increasing the system cost and switching loss. To accomplish the tracking speed and accuracy, authors in [25] proposed the MPPT algorithm associated with modified fractional voltage and current with a sensor-less operation for auto modulation. The MPPT algorithm automatically changes the step size according to the variable solar irradiation conditions. In [26], the need for effective silicon-based switches was discussed to achieve reduced switching losses and higher efficiency. In [27], the authors proposed a hybrid MPPT system validated by simulation and experiment, implemented with only one voltage sensor to reduce cost and complexity. Adaptive predictive error filter based MPPT is discussed in [28]. It explains that the discrete PID controller and tracking of the maximum power in a single stem is unsuitable for continuous PID control. Authors in [28] have presented a new adaptive MPPT for portable solar-powered devices, and the performance was analysed.

The structure of this paper is part II, explaining the implementation of MPT tracking with an FPGA-controlled load balancing algorithm for solar-powered DC-to-DC converters. Part III analyses the proposed boost converter with High Gain Dual Output (HGDO) and its modes of operation. The operation of the HGDO converter is explained in part IV. The overall performance analysis of the system is presented in part V. Part VI illustrates the hardware implementation of the proposed HGDO. In part VII, we discuss the inference and conclusion of the proposed converter.

2. Implementation of FPGA-based P & O with load balancing algorithm

Xilinx-ISE tool is employed to develop HDL code dumped in the FPGA processor. The architecture of FPGA consists of Input/output blocks, interlink wire, and configurable logic blocks (CLB). In the proposed system, due to the varying nature of the sunlight, FPGA-based control signal generation has better dynamic performance and an easily rewritable (reprogrammable) code nature compared to microcontroller-based pulse generation. Here, we develop a Load Balancing algorithm-based Verilog code that generates the required gate

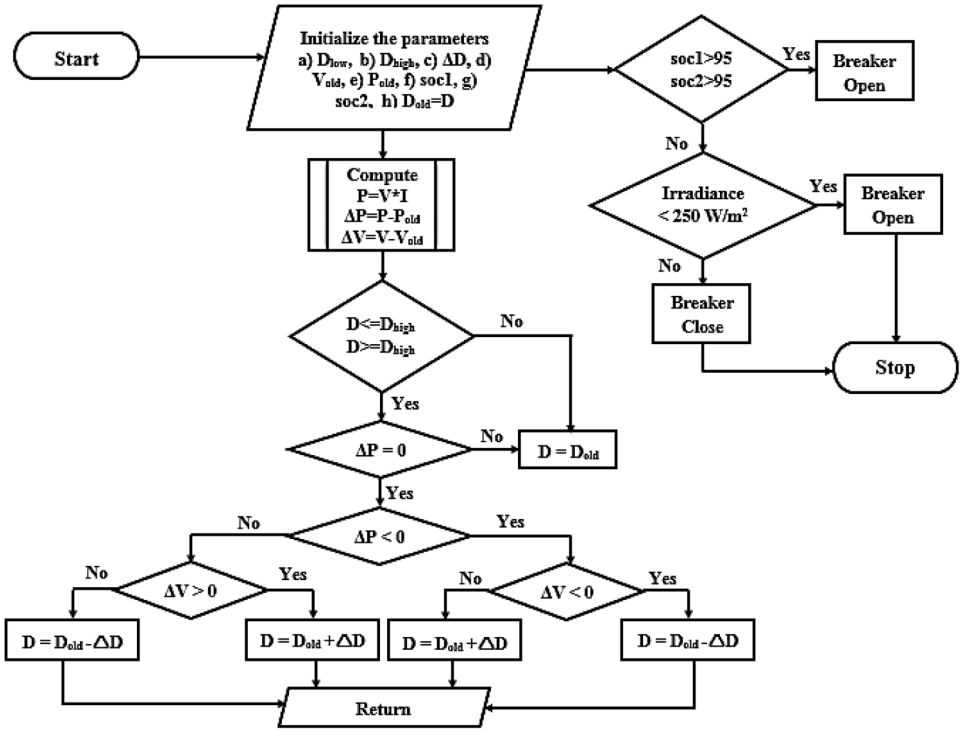


Fig. 2a. MPPT with load balancing algorithm - Flow chart.

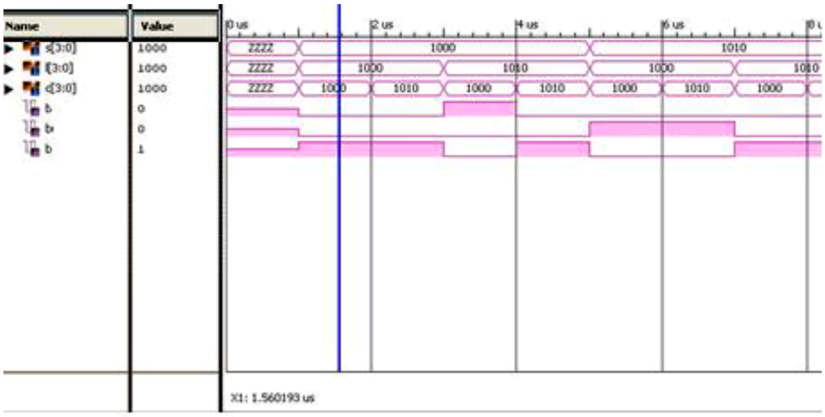


Fig. 2b. Pulse generated from the FPGA controller.

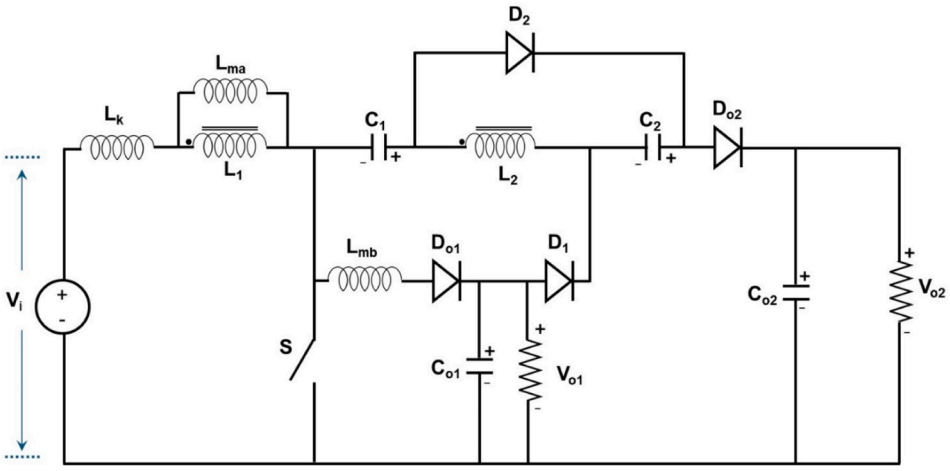


Fig. 3. Proposed High Gain Dual Output (HGDO) Boost Converter.

pulse for the switches of the proposed converter. Fig. 2(a) shows the algorithmic steps in forming the controller code implementations and the succeeding steps describing the process involved in the load balancing algorithm. The flow chart of the algorithm is as follows.

Step 1: Start the process.
Step 2: Initialize the parameters such as low duty (D_{low}), high duty cycle (D_{high}), incremental value of duty ratio (ΔD), previous voltage and power as (V_{old} and P_{old}) respectively, state of charging of battery 1 and 2 as (SOC1 and SOC2), and set the duty ratio, $D = D_{old}$.
Step 3: Compute the power, change in power and voltage values.
Step 4: Compare the duty ratio, D, with high-value initialization.
Step 5: If yes, check that the power change equals zero. Otherwise, set $D = D_{old}$.
Step 6: If $\Delta P = 0$, then check $\Delta P < 0$; if yes means, check the change in voltage, $\Delta V < 0$. Then, add or subtract the change in duty ratio from the old duty ratio.
Step 7: Return to the initialization step and set the new duty ratio. Again, continue from step 3.
Step 8: Check the state of the charge status of batteries 1 and 2. If SOC > 95 %, open the breaker.
Step 9: Otherwise, check the irradiance level $\langle$ 250 W/m^2. If yes, close the breaker. If radiation $\rangle$ 250 W/m^2, open the breaker.
Step 10: End the process.

The clock frequency of the FPGA is 50 MHz, and the period is 0.02 μs. This minimum time range is significantly less noticeable. Fix the maximum count as (4096) for the system requirement and vary the sample time.

Fig. 2(b) shows the PWM signal generated by the FPGA controller. Timer parameters are automatically generated depending on the HDL code's clock frequency, which helps generate varying duty cycle PWM signals. The bit resolution has to control the duty cycle range, which can be increased or decreased in a single step. Here, the duty cycle of the pulse can be varied from 30 % to 50 %.

3. Proposed High Gain Dual Output (HGDO) boost converter

3.1. Converter description and its advantages

The proposed High Gain Dual Output (HGDO) boost converter is illustrated in Fig. 3. The components contain leakage inductor (L_k), coupled inductors (L_1, L_2), magnetizing inductors (L_{ma} and L_{mb}), MOSFET switch (S), input voltage (V_i), energy storage capacitors (C_1 and C_2), clamp capacitor (C_{o1}), output capacitor (C_{o2}), clamp diode (D_{o1}), output diodes (D_{o2}) and junction diodes (D_1 and D_2). Their benefits over the conventional boost converter topology are discussed below.

1. The proposed HGDO converter is expected to provide a voltage gain of 14–16 times the input voltage, V_i, at 40–50 % of duty cycles, respectively.
   The achieved voltage gain value is appropriate to interface directly with the low-voltage source.
   The turn ratio can be adjusted flexibly between the coupled

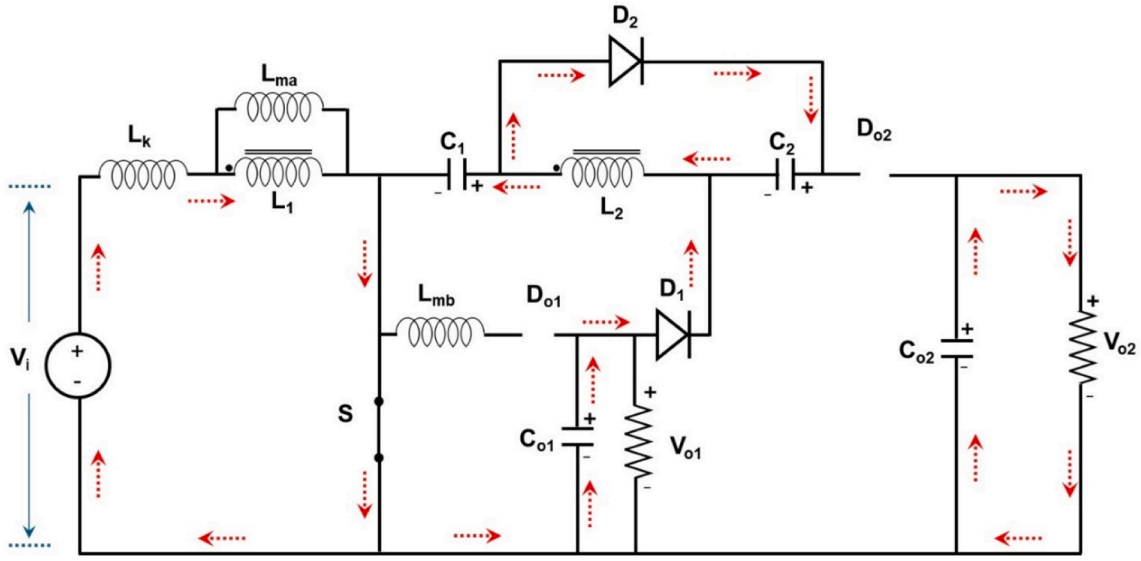


Fig. 4. Mode 1 operation.

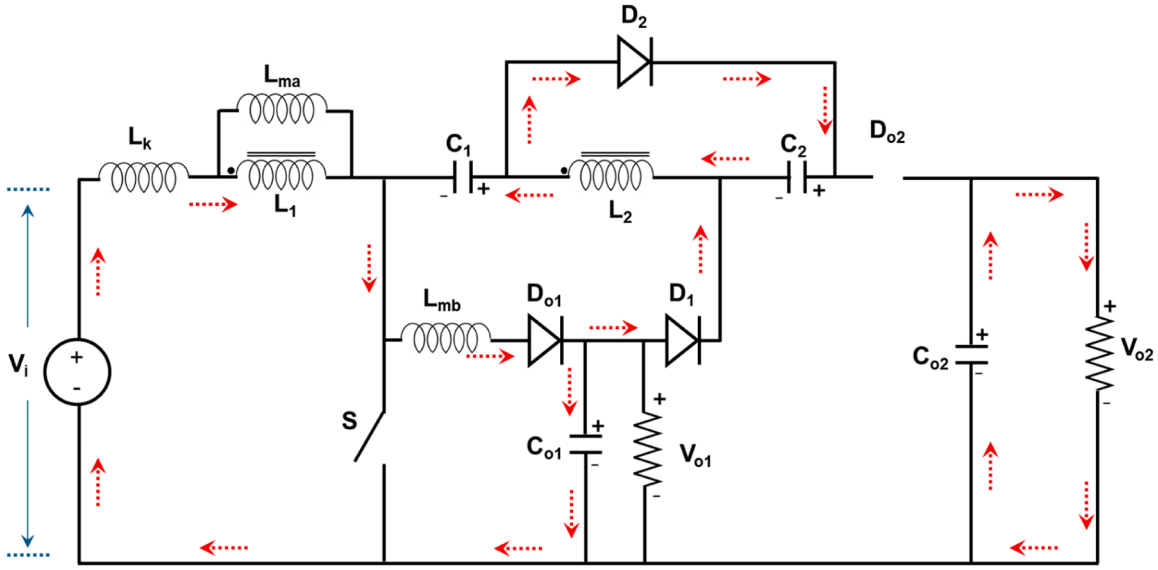


Fig. 5. Mode 2 operation.

inductors, L_1 and L_2. The coupled inductor leakages are recovered effectively through passive storage capacitors.

2. The intermediate storage capacitors help to improve the voltage gain of the design.
3. The switching stress of the switches is minimized due to the low-duty cycle of the converter.

Leak inductance minimizes switching losses, L_k, with the coupled inductor L_1. It also helps to increase the voltage level during the voltage boost operation.

4. The clamp circuit consists of two diodes, D_{o1} and D_{o2}, and two capacitors, C_{o1} and C_{o2}, help to obtain the continuous output across the load throughout the operation.

The proper arrangements of clamp diodes, D_{o1} and D_{o2}, will help to protect the energy leakage from the output capacitors, C_{o1} and C_{o2}. It helps to maximize the efficiency of the converter.

3.2. Operation of the proposed converter

The operating methods of the high gain dual output FPGA controlled DC to DC converter are analysed in the following four modes from t_0 to t_4. The modes of operation are as follows.

Mode 1 (t_0–t_1): The mode 1 operation is shown in Fig. 4. During operational mode 1, switch S is in the closed position. When the input voltage (V_i) is applied, the magnetizing inductor L_{ma} is charged. This magnetizes the coupled inductors L_1 and demagnetize L_2. Additionally, the energy storage capacitors C_1 and C_2 are charging, while diodes D_1 and D_2 are forward-biased, and diodes D_{o1} and D_{o2} are in a reverse-biased state. Since D_{o1} is reverse-biased, there is no current flow in the magnetizing inductor L_{mb}. However, the load has a current flow due to the voltage across the output capacitor C_{02}.

Current flow through the magnetizing inductors, L_{ma} at (t_0–t_1) can be expressed as,

$$\Delta i_{L_{ma}} = \frac{V_i}{L_{ma} + L_k}\,(t - t_0) \; + \; i_{L_{ma}}(t_0) \tag{1}$$

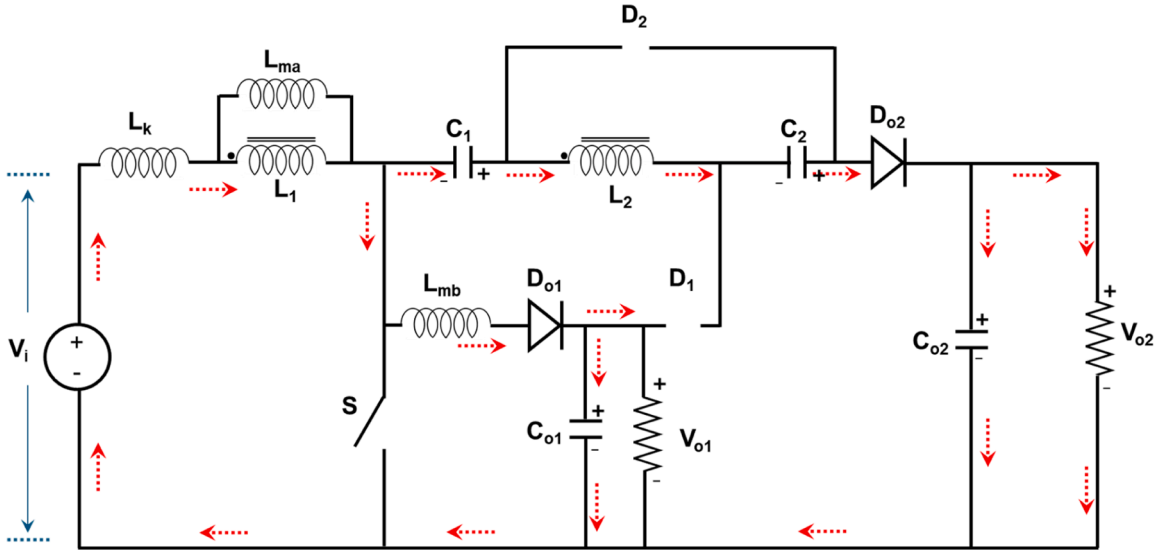


Fig. 6. Mode 3 operation.

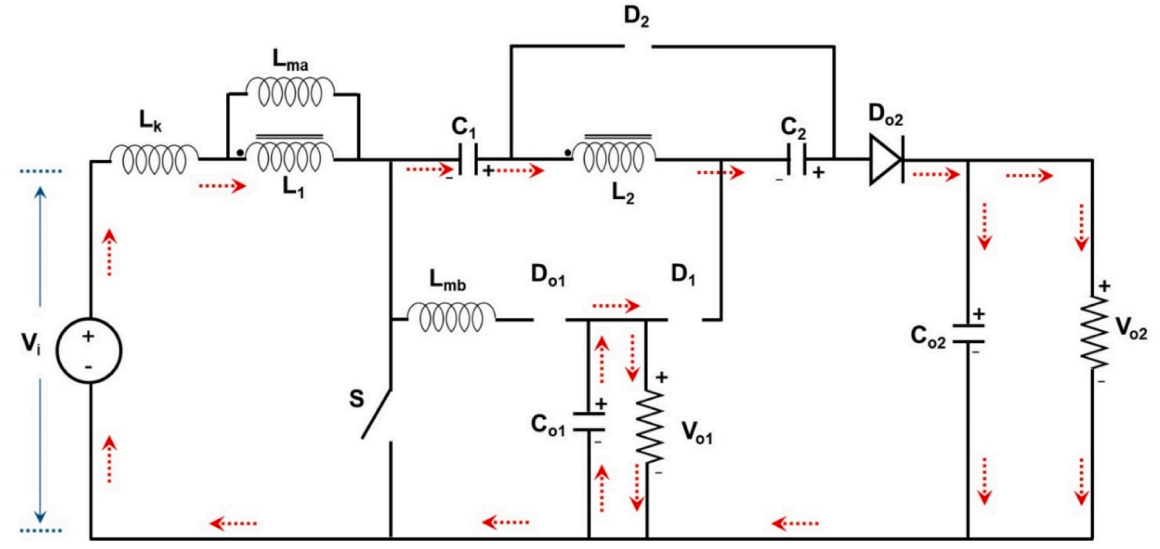


Fig. 7. Mode 4 operation.

Current flow through the magnetizing inductors, L_{mb} at (t_0–t_1) is equal to zero. It can be expressed as,

$$\Delta i_{L_{mb}} = 0 \tag{2}$$

Mode 2 (t_1–t_2): During this mode 2, switch S is in the open position. When the input voltage V_i is applied, inductors L_{ma}, L_{mb} starts to magnetize and L_1, L_2 demagnetize, the capacitors C_1, C_2 and C_{01} are charging, while diodes D_1, D_2 and D_{o1} are forward-biased, and diode D_{o2} is in a reverse-biased state. However, the current flow in the load continues due to the voltage across the output capacitor C_{02}. The mode 2 operation is shown in Fig. 5. The current flow through the magnetizing inductors, L_{ma} at (t_1–t_2) can be expressed in the Eqs. (3), (4),

$$\Delta i_{L_{ma}} = \frac{V_{C01} - V_i}{L_{ma} + L_{mb} + L_k}\,(t - t_1) + i_{L_{ma}}(t_1) \tag{3}$$

The current flow through the magnetizing inductors, L_{mb} at (t_1–t_2) can be derived as,

$$\Delta i_{L_{mb}} = \frac{V_{C01}}{L_{mb}}\,(t - t_1) + i_{L_{mb}}(t_1) \tag{4}$$

Mode 3 (t2–t3): During mode 3, switch S remains in the open position. When the input voltage V_i is applied, inductors L_{ma}, L_{mb} continues to magnetize and L_1, L_2 starts to magnetize, the capacitors C_1, C_2 are discharging and C_{01}, C_{02} are charging, while diodes D_1, D_2 are reverse biased and D_{o1}, D_{o2} are forward-biased, the current flow in the load continues due to the input supply voltage and the capacitors C_1, C_2 through D_{o2}.

The mode 3 operation current flow path is shown in Fig. 6. The magnetized inductors, L_{ma} currents at (t_2–t_3), can be derived as,

$$\Delta i_{L_{ma}} = \frac{V_{C01} - V_i}{L_{ma} + L_{mb} + L_k}\,(t - t_2) + i_{L_{ma}}(t_2) + \frac{V_{C01} - V_{C1} - V_{C2} - V_i}{n(L_{ma})}\,(t - t_2) \tag{5}$$

The current flow through the magnetizing inductors, L_{mb} at (t_2–t_3) can be expressed as,

$$\Delta i_{L_{mb}} = \frac{V_{C01} - V_i}{L_{mb} + L_k + L_{ma}}\,(t - t_2) + i_{L_{mb}}(t_2) \tag{6}$$

Mode 4 (t_3–t_4): During this mode, switch S remains in the open

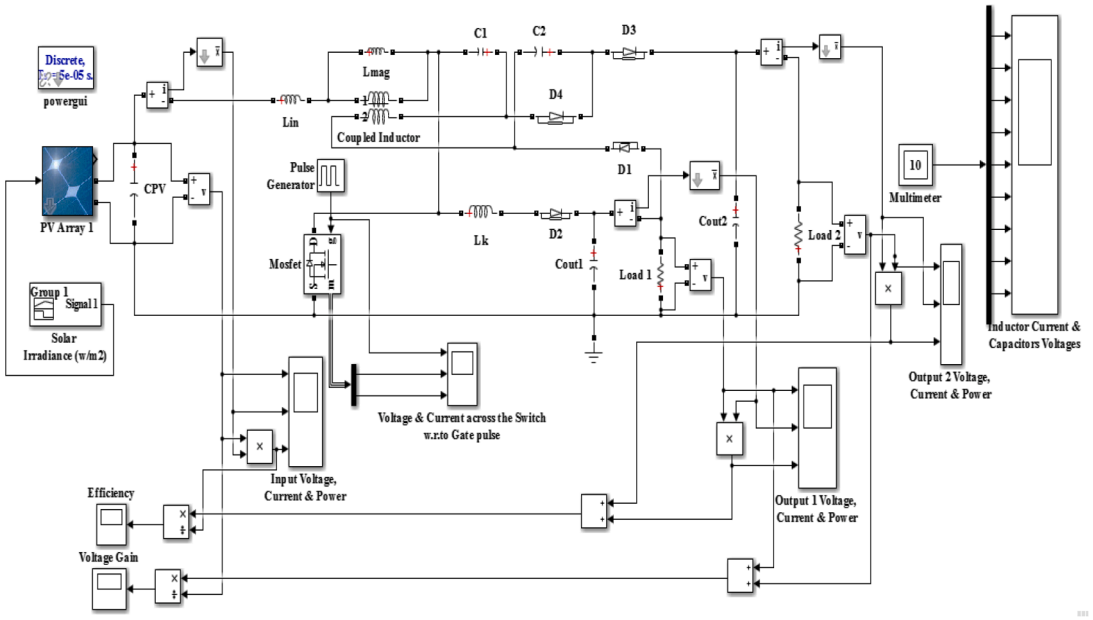


Fig. 8a. Simulation model of proposed HGDO converter with PV panel.

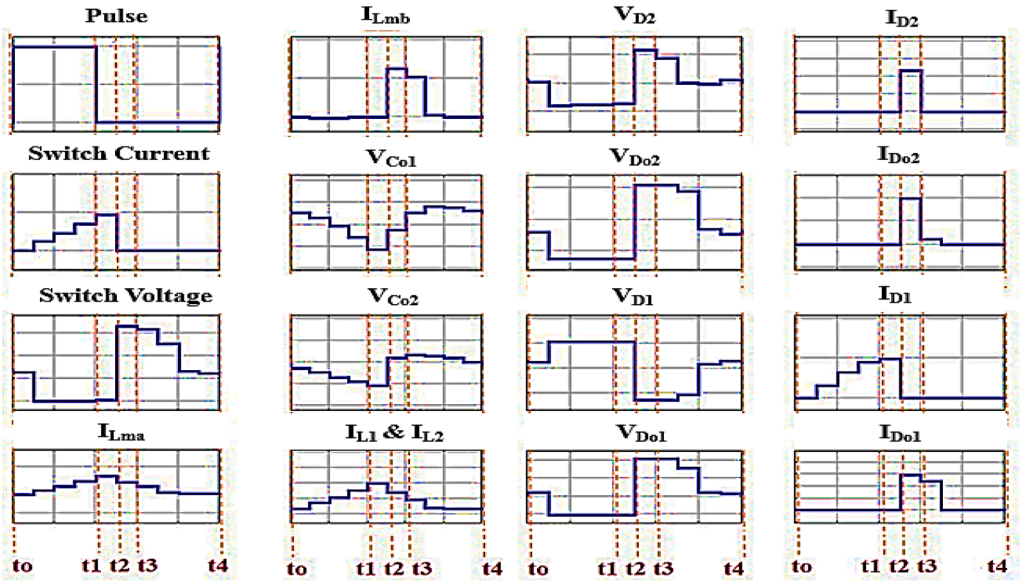


Fig. 8b. Key waveforms of the proposed HGDO boost converter.

position. When the input voltage V_i is applied, inductors L_1 de-magnetizes and L_2 continues to magnetize, the capacitors C_1, C_2 are discharging and C_{01}, C_{02} are charging, while diodes D_1, D_2, and D_{o1} are reverse biased and D_{o2} is forward-biased, the current flow in the load continues due to the input supply voltage and the capacitors C_1, C_2 through D_{o2}. The mode 4 operation is shown in Fig. 7.

The current flow through the magnetizing inductors, L_{ma} at (t_3–t_4) can be expressed as,

$$\Delta i_{L_{ma}} = \frac{V_{C01} - V_{C1} - V_{C2} - V_i}{n(L_{ma})}\,(t - t_3) + i_{L_{ma}}(t_3) \tag{7}$$

The current flow through the magnetizing inductors, L_{mb} at (t_3–t_4) can be obtained as,

$$\Delta i_{L_{mb}} = 0 \tag{8}$$

The simulation model of the proposed HGDO converter with PV panel is given in Fig. 8a and the simulated output waveforms of the proposed DC to DC converter are provided in Fig. 8b.

4. Analysis of the proposed DC to DC converter

Analyzing the proposed converter helps to choose suitable ratings of the elements used in the circuit design and construction. Assumptions for this analysis are that all the elements used in the converter except the leakage inductor L_k are ideal. This analysis is made up of three sub-divisions. They are a) continuous conduct mode (CCM) operation, b) design considerations of the components, and c) efficiency calculation of the converter.

4.1. Continuous conduction mode (CCM) operation

The voltage across the coupled inductor can be derived in two

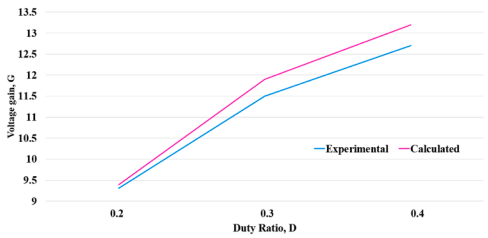


Fig. 9. Voltage gain (G) vs Duty ratio (D).

modes, i.e., one is when the MOSFET switch S, is truned ON and another when it is turned OFF. When switch S is turned ON or in the closed state, the Eq. (9) is employed to determine the voltage across the primary coil of the coupled inductor L_1,

$$V_{L1}\ (ON) = V_i \tag{9}$$

The voltage across coupled inductor L_2 is the potential difference among the storage capacitor, C_2 and output capacitor, C_{o1} is given as,

$$V_{L2}\ (ON) = V_{C2} - V_{Co1} \tag{10}$$

$$V_{L2}(ON) = nV_i = V_{C2} \tag{11}$$

When switch S is off or closed state, the input voltage, V_i and output capacitor, V_{Co1} difference is the voltage drop across the coupled inductor, L_1. It can be derived as,

$$V_{L1}(OFF) = V_i - V_{Co1} \tag{12}$$

The voltage across the coupled inductor, L_2 when the switch is off condition is derived as,

$$V_{L2}(OFF) = V_{Co1} + V_{C1} + V_{C2} + V_{Co2} \tag{13}$$

The turn's ratio of the coupled inductor, n is equal to the ratio between the voltage across the coupled inductor, L_1 and L_2.

$$V_{L1} = n\ V_{L2} \tag{14}$$

The voltage across the storage capacitor, C_2 is equal to the n times of the input voltage, V_i. It can be written as,

$$V_{C2} = nV_i \tag{15}$$

4.1.1. Voltage drop across the diodes

The voltage drop occurs in the diodes on the reverse biased condition or OFF condition. By substituting the Eqs. (9), (10), (11) and (12) in the Eq. (13), we get the voltage expression in switch OFF condition as,

$$V_{L2} = V_i + V_{Co1} + nV_i - V_i + V_{Co1} + nV_i - V_{Co2} \tag{16}$$

$$V_{L2} = 2V_{Co1} + 2nV_i - V_{Co2} \tag{17}$$

By substituting (11), (12), and (13) into (17), it becomes,

$$V_{L2}(OFF) = 2\left\{V_i - V_{L1(OFF)}\right\} + 2nV_i - V_{Co2}$$

$$V_{L2}(OFF) + 2V_{L1}(OFF) = 2V_i + 2nV_i - 2V_{Co2}$$

$$V_{L1}\ (OFF) = \frac{(2n+2)V_i}{(n+2)} - \frac{V_{Co2}}{(n+2)} \tag{18}$$

4.1.2. Voltage gain calculation

The sum of the voltage across the inductor, L_1 when the switch is in on and off condition is equal to zero (voltage-*sec* balance). By using (9) and (18), we obtain:

$$V_{L1}(ON)d + V_{L1}(OFF)(1-d) = 0 \tag{19}$$

Substituting Eq. (9) and (18) into Eq. (19), one gets:

$$V_i d + \left[\frac{(2n+2)V_i}{(n+2)} - \frac{V_{Co2}}{(n+2)}\right](1-d) = 0 \tag{20}$$

From the above Eq. (20), voltage conversion ratio, G is given by,

$$G = \frac{V_{Co2+Co1}}{V_i} = \frac{(n+2)}{(1-d)} + n \tag{21}$$

Where V_i, input voltage, output voltage, $V_{Co2} + C_{o1}$, n gives the turns ratio between the coupled inductor, and d is the duty ratio. Here, the proposed HGDO converter is considered for selectable low-duty cycle, i. e. d is 0.4 and turns ratio 'n' is 4. The voltage gain (G), as per the duty ratio (D), is illustrated in Fig. 9. Substituting the obtained values of 'd' and 'n' in the Eq. (21), G equals 4.05.

Substituting the Eq. (21) in the Eq. (18), voltage across the inductor, L_1 during the switch off position becomes,

$$V_{L1}(OFF) = \frac{(2n+2)V_i}{(n+2)} - \frac{nV_i + 2V_i + nV_i - nV_i d}{(1-d)(n+2)} \tag{22}$$

When the switch off condition, 'n' is completely independent of the voltage, and it can be neglected from the equation. It becomes,

$$V_{L1}(OFF) = \frac{-d}{1-d}\ V_i \tag{23}$$

4.1.3. Voltage across the switch calculation

During the non-conducting period of the switch, the drain-source voltage is given by,

$$V_{DS} = V_i - V_{L1}(OFF) \tag{24}$$

By substituting the Eq. (23) into the Eq. (24) gets,

$$V_{DS} = V_i + \frac{d}{(1-d)}\ V_i \tag{25}$$

By expanding the terms, V_{DS} becomes,

$$V_{DS} = \frac{V_i}{(1-d)} \tag{26}$$

The voltage drop across the capacitor, C_{o1} remains constant which is almost equal to the input supply voltage, V_i. By using Eqs. (12) and (23), the voltage available across the clamp capacitor, C_{o1} is given by,

$$V_{Co1} = \frac{V_i}{(1-d)} \tag{27}$$

4.1.4. Storage capacitor voltage calculation

The storage capacitor, C_1 voltage can be determined from the Eq. (10),

$$V_{C1} = V_{Co1} + V_{L2}(ON) \tag{28}$$

Substituting Eq. (11) and (27) in Eq. (28), we obtain,

$$V_{C1} = \frac{V_i}{(1-d)} + nV_i \tag{29}$$

$$V_{C1} = \left(\frac{1}{1-d} + n\right)V_i$$

$$V_{C1} = \frac{n(1-d)+1}{1-d}V_i \tag{30}$$

4.1.5. Diode voltage calculation

The clamp diode, D_{o1} voltage equation when the switch S is ON. The diode, D_{o1} acts as reverse biased state. The voltage across D_{o1} is given as,

$$V_{Do1} = V_{L1}(ON) + V_{Co1} \tag{31}$$

Substituting V_{L1} (ON) from the Eq. (9) and V_{Co1} from the Eq. (27), the Eq. (31) becomes,

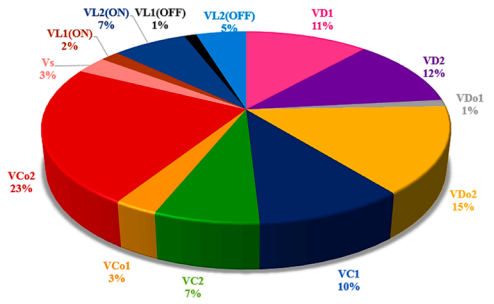


Fig. 10. Voltage drop across the components in the converter.

$$V_{Do1} = -V_i^* + \frac{V_i}{(1-d)} \tag{32}$$

$$V_{Do1} = -\frac{d}{(1-d)}V_i \tag{33}$$

(*-ve sign indicated the diode oppose the input voltage due to reverse biased nature.)

The Diode voltage V_{D1}, is given by,

$$V_{D1} = V_{L2}(OFF) - V_{C1} + V_{Co1}$$

From Eq. (17),

$$V_{L2}(OFF) = 2V_{Co1} + 2nV_i - V_{Co1}$$

From Eq. (21), (27) and (28), V_{L2} (OFF) becomes,

$$V_{L2}(OFF) = 2\frac{V_i}{1-d} + 2nV_i - \left(\frac{(n+2)}{(1-d)} - n\right)V_i$$

$$V_{L2}(OFF) = -\frac{nd}{1-d}V_i$$

$$V_{D1} = \frac{-nd}{(1-d)}V_i - \frac{n(1-d)+1}{(1-d)}V_i + \frac{V_i}{(1-d)} \tag{34}$$

Substitute the Eq. (16), (23) and (28) in Eq. (34), yields,

$$V_{D1} = -\frac{nV_i}{(1-d)} \tag{35}$$

The voltage across the diode, D_2 can be expressed as,

$$V_{D2} = -\frac{n}{(1+d)}V_i \tag{36}$$

The voltage across the output diode, D_{o2} can be described as,

$$V_{Do2} = V_{C1} + V_{C2} - V_{Co2} - V_{L2}(ON)$$

$$V_{Do2} = \frac{n(1-d)+1}{(1-d)}V_i - \left(\frac{n+2}{1-d} - n\right)V_i$$

$$V_{Do2} = -\left(\frac{n+1}{1-d}\right)V_i \tag{37}$$

The voltage drop in various components of the converter design is explicitly illustrated in Fig. 10, with the help of the above analysis and the equations obtained from them.

4.2. Design considerations of the components

The converter's output gain and efficiency mainly depend on the storage capacitor, output capacitor and magnetizing inductor ratings. The output capacitor and magnetizing inductor are responsible for the output voltage ripple and input current ripple, respectively. The values of the storage capacitors C_1 and C_2 can be calculated as,

$$C_1\frac{dV_{C1}}{dt} = C_2\frac{dV_{C2}}{dt} = I_{L2}(ON) = (1-d)(I_{O2} - I_{o1})$$

Considering, C_1 and C_2 as equal, and then dV_{C1} and dV_{C2} are ΔV_c.

$$C = \frac{(V_{o2} - V_{o1})d(n+2+n(1-d))T_s}{(R_2-R_1)(1-d)(\Delta V_{Co2} - \Delta V_{Co1})} \tag{38}$$

Where ΔV_{Co1} and ΔV_{Co2} are the output voltage ripples between the ON and OFF time of the switch, R_1 and R_2 are the load resistances, d is the duty ratio, and T_S is the total switching period of the converter.

The output filter capacitors reduce the voltage ripple in the output. Typically, voltage ripple is inversely proportional to the sizing of the capacitor. Increasing the capacitor's sizing, a smooth output voltage waveform is obtained. The value of the output capacitor can be obtained from the Eq. (39),

$$C_{o1}\frac{dV_{o1}}{dt} = I_{o1} = \frac{V_{o1}}{R}$$

Similarly,

$$C_{o2}\frac{dV_{o2}}{dt} = I_{o2} = \frac{V_{o2}}{R}$$

In general,

$$C_o = \frac{V_o \cdot D \cdot T_S}{R\Delta V_o} \tag{39}$$

The remarkable advantage of the proposed HGDO converter is the size of the output filter capacitor. Minimizing the capacitor's size, one can achieve a low output voltage ripple and settling time of the voltage. This indirectly reduces the converter size, makes the converter compact, and makes the converter cost-effective for implementation.

The coupled inductor and magnetizing inductor design are the essential features of the converter design. The magnetizing inductor current is double the average value of the coupled inductor current. The equation for the calculation of the magnetizing inductance of the coupled inductor is calculated as,

$$L_{ma} = \frac{V_i \cdot D \cdot T_S}{\Delta i_{ma}} \;\&\; L_{mb} = \frac{V_i \cdot D \cdot T_S}{\Delta i_{mb}} \tag{40}$$

Where Δi_{ma} and Δi_{mb} are the input current ripples concerning L_{ma} and L_{mb}, respectively, the analysis of the different magnetizing inductors for the input current ripple reductions are made. From the analysis, a low value (in terms of μH) of magnetizing inductance gives the minimum input current ripples to the converters.

4.3. Analysis of converter efficiency

The proposed system's efficiency depends entirely on the losses in the active and passive elements present in the converter. They are i) switch loss, ii) coupled inductor losses, and iii) diode losses.

4.3.1. Loss in the switch

The conduction losses of the MOSFET switch can be obtained from,

$$P_{S\ (loss)} = \frac{1}{2}\left(V_{S(OFF)} * I_{S(peak)} * T_f * f_s\right) \tag{41}$$

$$P_{S(loss)} = R_{ON}.d\left[\frac{(n+2)+n(1-d)}{(1-d)}(I_{o1}+I_{o2})\right]^2 \tag{42}$$

Where R_{ON} is ON time resistance, V_S & I_s are Source node voltage and current of the MOSFET.

4.3.2. Losses across coupled inductor

The losses occurs in the coupled inductor ($L_2 \| L_1$) are calculated from the following equations:

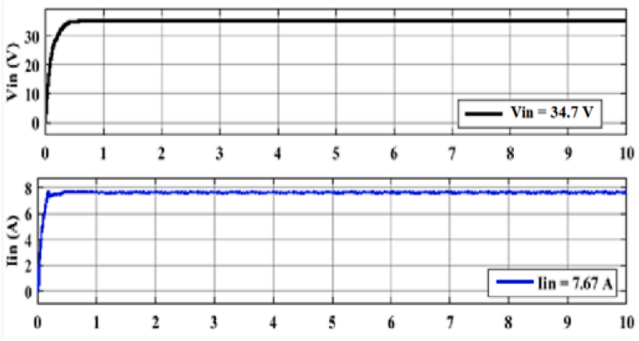


Fig. 11. Input voltage and current to the proposed HGDO converter.

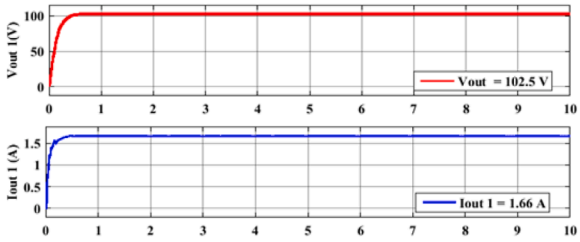


Fig. 12. Output voltage and current from the load 1.

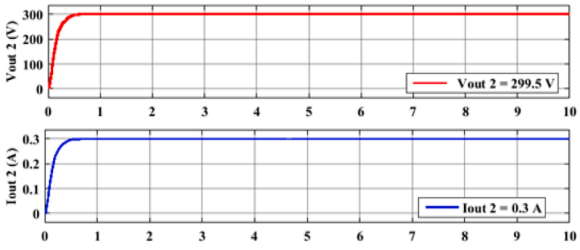


Fig. 13. Output voltage and current from the load 2.

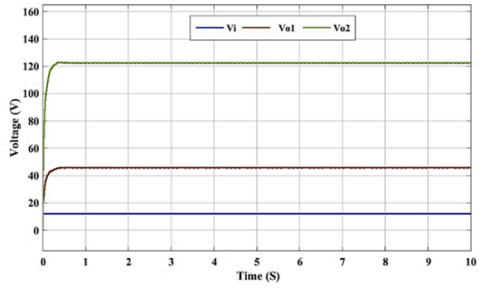
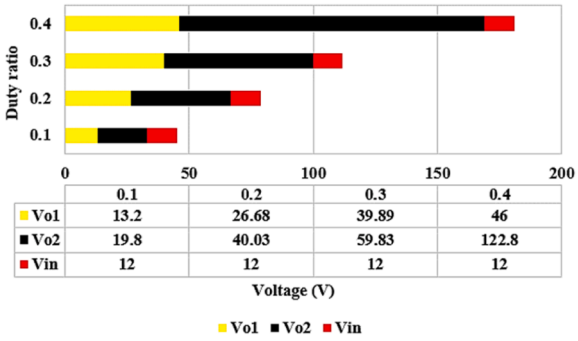


Fig. 14. Input and output voltages of the HGDO converter.



	0.1	0.2	0.3	0.4
Vo1	13.2	26.68	39.89	46
Vo2	19.8	40.03	59.83	122.8
Vin	12	12	12	12

Fig. 15. Output voltages for different duty ratio with constant input voltage.

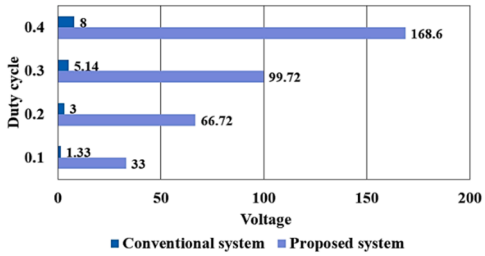


Fig. 16. Duty ratio, D vs Voltage, V for conventional and proposed system.

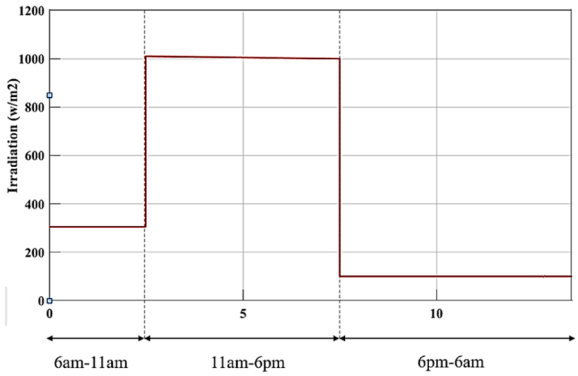


Fig. 17. Solar irradiance (w/m^2) with respect to time.

Table 1
Batteries and panel ratings.

S.No.	Parameters	Ratings
1	Open circuit voltage (V_{oc})	30.8V
2	Short circuit current (I_{sc})	8.2A
3	Maximum voltage (V_m)	24.7V
4	Maximum current (I_m)	7.7A
5	Battery 1 SOC	40 %
6	Battery 1 Nominal voltage	20V
7	Battery 2 SOC	40 %
8	Battery 2 Nominal voltage	70V

$$P_{L1} = {I_{L1}}^2 \times r_{L1} \tag{43}$$

$$P_{L1} = r_{L1}.d\left[\frac{(n+2)+n(1-d)}{(1-d)}(I_{o1}+I_{o2})\right]^2 \tag{44}$$

$$P_{L2} = {I_{L2}}^2 \times r_{L2} \tag{45}$$

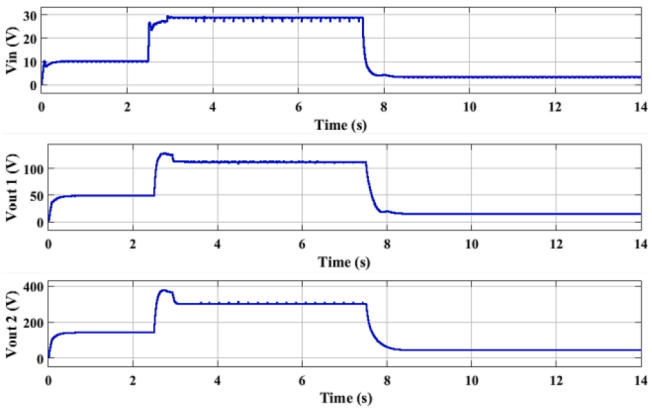


Fig. 18a. Voltage across the output variations without battery storage.

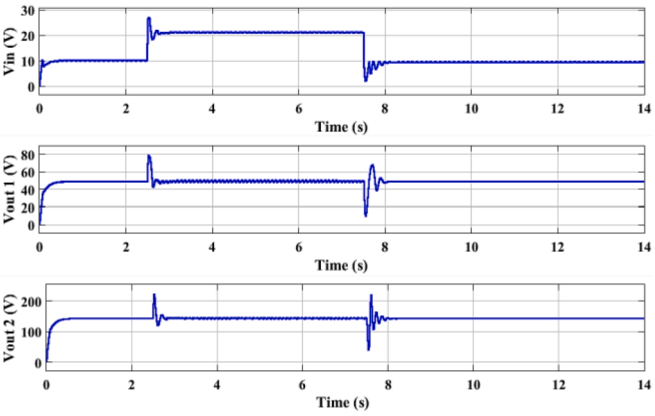


Fig. 18b. Constant output voltages using battery backup.

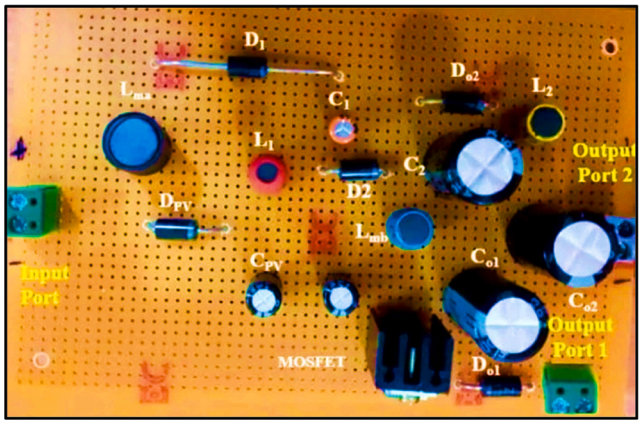


Fig. 19. Hardware setup of proposed HGDO converter.

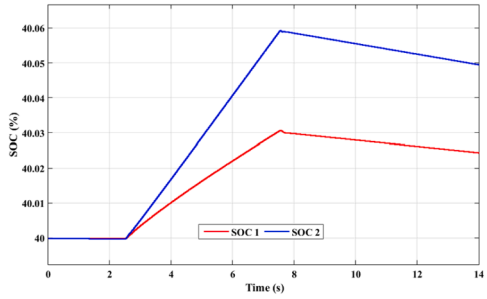


Fig. 20. State of Charging (SOC) of batteries 1 and 2.

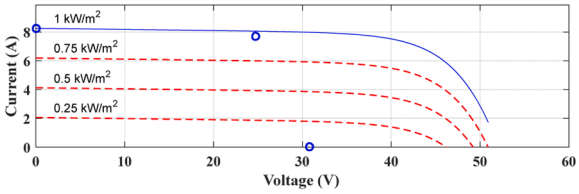


Fig. 21. V-I characteristics of solar panel.

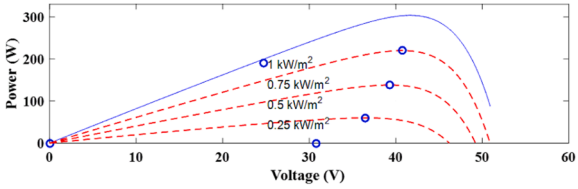


Fig. 22. PV characteristics of the solar panel.

$$P_{L2} = r_{L2}.d\left[\frac{(n+1)\{(n+2)+n(1-d)\}}{n(1-d)}(I_{o1}+I_{o2})\right]^2 \quad (46)$$

Where P_{L1}, I_{L1}, r_{L1} denotes Load 1 power, current and internal resistance respectively and P_{L2}, I_{L2}, r_{L2} denotes Load 2 power, current and internal resistance respectively.

4.3.3. Losses across diodes

The diode D_{o1}, D_1, D_2 and D_{o2} losses are calculated as,

$$P_{Do1} = (I_{Do1} \times V_{Do1}) + \left(I_{Do1}^2 \times r_{Do1}\right) \quad (47)$$

$$P_{Do1} = V_{FDo1}(1-d)\left[\frac{(n+2)+n(1-d)}{(1-d)}(I_{o1})\right] \quad (48)$$

$$P_{D1} = (I_{D1} \times V_{D1}) + \left(I_{D1}^2 \times r_{D1}\right) \quad (49)$$

$$P_{D1} = V_{FD1}.d\left[\frac{(n+2)+n(1-d)}{2n(1-d)}(I_{o1})\right] \quad (50)$$

$$P_{D2} = (I_{D2} \times V_{D2}) + \left(I_{D2}^2 \times r_{D2}\right) \quad (51)$$

$$P_{D2} = V_{FD2}.d\left[\frac{(n+2)+n(1-d)}{2n(1-d)}(I_{o2})\right] \quad (52)$$

$$P_{Do2} = V_{FDo2}(1-d)I_{o2} \quad (53)$$

Where P_{Do1}, I_{Do1}, V_{Do1}, r_{Do1}, V_{FDo1} represent power, current, voltage, internal resistance and forward voltage, respectively for Clamp Diode D_{o1} and P_{Do2}, I_{Do2}, V_{Do2}, r_{Do2}, V_{FD02} represents power, current, voltage, internal resistance and forward voltage respectively for Clamp Diode D_{o2}

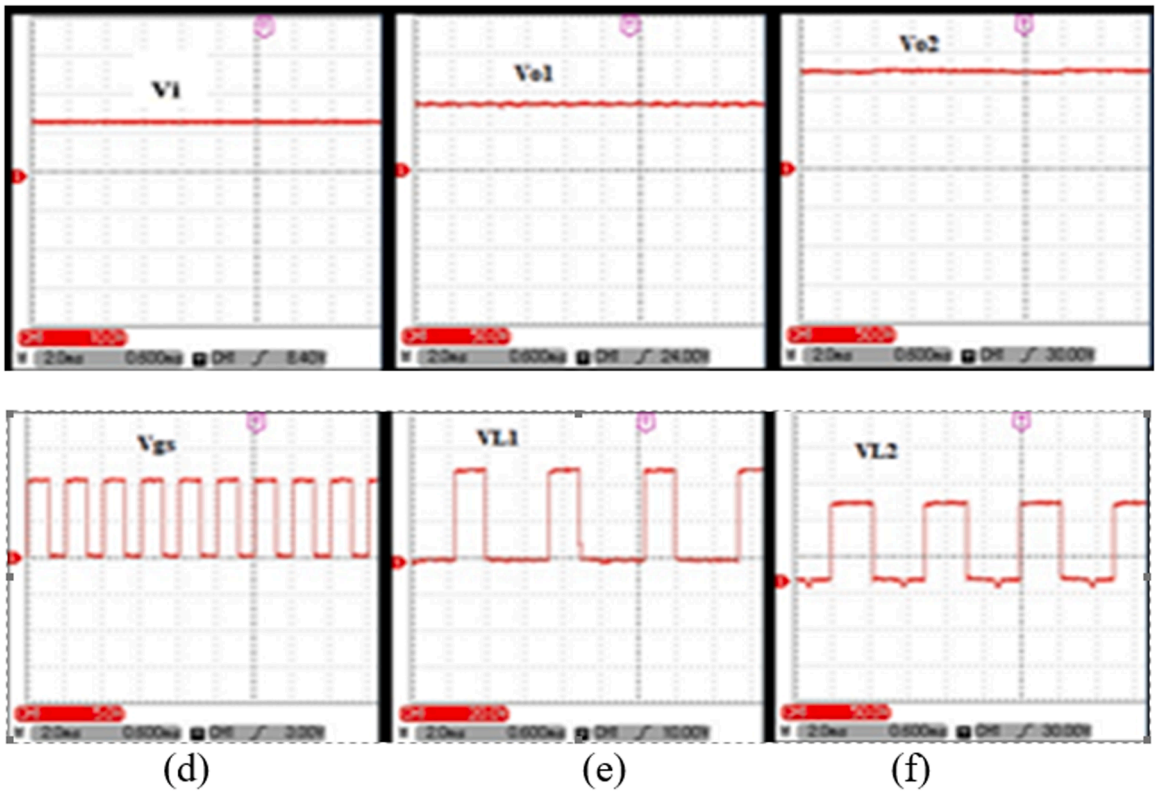


Fig. 23. Experimental waveforms of the converter (a) Input voltage, V_i, (b) Output voltage 1, V_{o1}, (c) Output voltage 2, V_{o2}, (d) Gate source voltage, V_{gs}, (e) Voltage across inductor L_1, V_{L1}, and (f) Voltage across inductor L_2, V_{L2}.

Table 2
Simulation and hardware values used.

S. No.	Parameters	Simulated Values	Hardware Values
1	Input Voltage V_i	12 V	12 V
2	Magnetizing Inductor, L_{ma} and L_{mb}	0.1 mH	10 mH
3	Output capacitor C_{o1}	470 μF	4700 μf, 50 V
4	Output capacitor C_{o2}	150 μF	470 μf, 200 V
5	Capacitor, C_1	650 μF	650 μF
6	Capacitor, C_2	470 μF	470 μF
7	Load resistor R_1	350 Ω	–
8	Load resistor R_2	650 Ω	–
9	Output voltage, V_{o1}	67 V	53 V
10	Output voltage, V_{o2}	101 V	105 V
11	Duty ratio, D	0.4	0.4
12	Turns ratio	4	4

5. Performance analysis of the proposed system

The performance analysis of the proposed FPGA-based HGDO boost converter for solar PV applications is analyzed by using MATLAB simulation. A solar PV cell array with dynamic irradiation conditions is given as a source for the proposed HGDO converter. The main components of the converter are coupled inductors, magnetizing inductors, clamp and output capacitors, clamp and output diodes and storage capacitors.

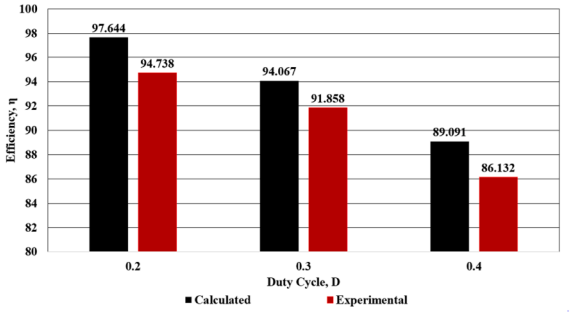
The coupled inductors L_1 and L_2 have a turns ratio of 1:4 ($n = 4$), and the magnetizing inductors help increase the output's gain value. The novelty of the proposed converter topology is that the high gain value and dual output deviate from the conventional and existing converter reported in [10]. Each load is connected to the battery through the bi-directional converter. In the proposed converter, the MOSFET switch gets the input pulse from the PV-fed FPGA-based P & O with a load-balancing algorithm. For the controlling of batteries, V_{f1} and V_{f2} are taken as the feedback voltage from the batteries, which is compared with the reference voltage, V_{ref}. The voltage difference is given to the PI controller and compared with the carrier saw tooth waveform. Then, the controlled gate pulses are obtained and given to the MOSFET switch, which is present in the bi-directional converter. To analyse the voltage gain ratio, 12 V is given as input to the converter. The pulsating current is measured as 2.1 A, for the duty ratio D is 0.4. The input voltage and pulsating current for the converter are shown in Fig. 11. For the given input, the output voltages for loads 1 and 2 are 46 V and 122.8 V, and the output currents are 0.2 A and 0.18 A, respectively, which is shown in Figs. 12 and 13.

Fig. 14 shows the input and output voltages of the proposed converter at $D = 0.4$. The total output voltage is 168.6 V, and the input voltage is 12 V. The calculated voltage conversion ratio is 14.05 times, proven by the output result waveform.

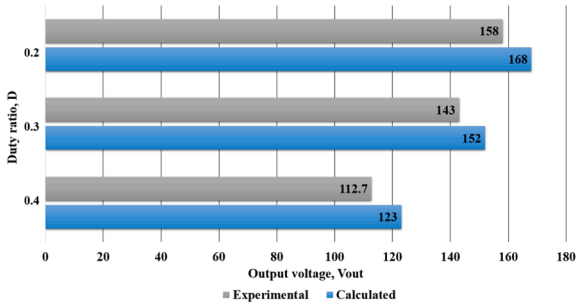
The converter is designed to work with minimum switching on time and reduce the voltage stress across the MOSFET switch. The voltage conversion ratio is analysed for the low switch on time (i.e. D is 0.1 to 0.4). The given input voltage is kept constant for all the duty ratios. Depending upon the duty ratio variations, the output voltages are also changed. The dual output voltages for duty cycle 0.1 to 0.4 are shown in Fig. 15.

The voltage gain ratio for the proposed HGDO and conventional boost converter for the different duty ratios is shown in Fig. 16. The voltage gain between the conventional and the proposed converter is varied from 21 to 24 times for the duty ratio range of 0.4, 0.3, 0.2 and 0.1 respectively. Due to the earth's revolution around the sun, solar radiation is non-uniform throughout the day. For analysis, three different dynamic solar irradiance conditions are considered.

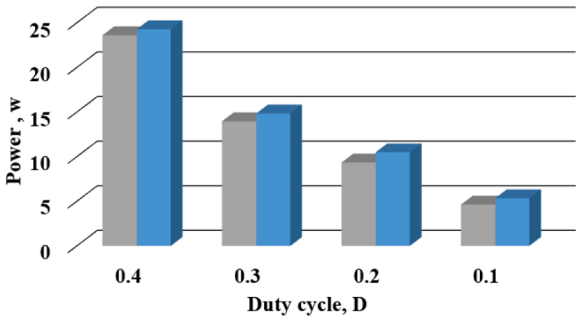
The solar radiance is measured in W/m^2 and continuously varies from time to time. In order to simply the analysis, the medium range (320 W/m^2) is set for the early morning time from 6am to 11am, the



(a)



(b)



(c)

Fig. 24. (a), (b), (c) Efficiency, output voltage and output power with respect to duty ratio, D.

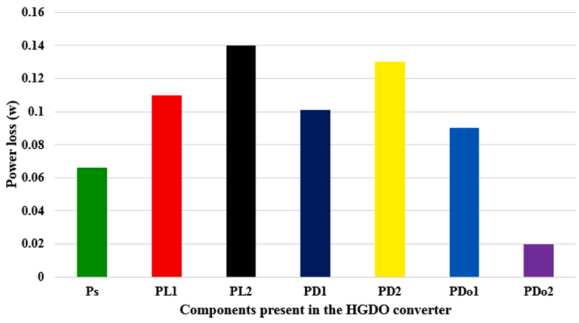


Fig. 25. Power losses in the different parts of the proposed converter.

high range (1000 W/m^2) is set for the daytime from 11am to 6pm, and the low range of irradiance (100 W/m^2) is set for the time from 6pm to 6am. The total simulated time of 14 s is segregated into three ranges, and its time range with irradiances is mentioned in Fig. 17. The batteries and panel ratings used for the analysis are given in Table 1. The voltage, VPV, and current IPV obtained for the solar irradiance from the solar PV

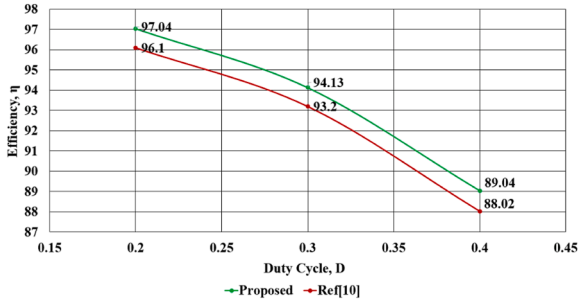


Fig. 26. Comparison of the proposed converter and other existing converter efficiency.

panel are dynamic and are given as input to the converter.

As mentioned, the three dynamic input voltages, VPV, are obtained for solar irradiance. The input and output voltages vary concerning changes in radiation due to the direct connection of the panel, converter and the load without any energy storage devices. Depending upon the dynamic input ranges, the gained output voltages are also varied for the dual output load and are shown in Fig. 18(a). The continuous variations of the voltage input to the load are not recommended for the effective system.

The solar input panel and proposed converter setup are connected with the battery through the bi-directional converter via breaker switches for analysis purposes. The two batteries are connected to the system. The static output voltages are obtained even in the variations on the input voltages from the solar panel, and its waveform is explicitly given in Fig. 18(b).

6. Hardware implementation

The simulation results are verified practically with the help of a hardware prototype model of the proposed converter design with a 12 V solar PV panel of 50 W is used as an input source. This investigation uses MPPT with a load-balancing algorithm. The PV diode and DPV protect the panel from the fault current. The inductors L_1 and L_2 connect in series as a couple of inductors. The magnetizing inductors L_{ma} and L_{mb} are used to magnetize the coupled inductor when the voltage is applied to the circuit. The hardware setup of the proposed HGDO converter is illustrated in Fig. 19.

When the solar irradiance is medium (i.e. 320 W/m^2), the voltage produced from the panel is enough to satisfy the loads. So, the batteries are isolated from the system by using a load-balancing algorithm to open the breaker. When the solar irradiance is high (i.e. 320 - 1000 W/m^2), the voltage produced from the panel is enough to satisfy the load demand and is also used to charge the batteries.

Fig. 20 shows the State of Charge (SOC) for batteries 1 and 2 at the period of 2.5 s to 7.6 s, which denotes the charging of the batteries. In a real-time implementation, the batteries are charged up to 95 %, and the load-balancing algorithm automatically opens the breaker. Practically, the batteries' complete charging and discharging time cannot be shown graphically. So, the sample charging and discharging nature of batteries 1 and 2 are shown in Fig. 20. During the solar irradiance of the panel in the low range (i.e. 0 - 100 W/m^2), the voltage production is insufficient to satisfy the load. At the time, batteries are used to support the loads, and the SOC discharging waveform indicates the battery-supported operation.

Fig. 21 shows the solar panel's voltage(V) and current(I) characteristics under dynamic conditions. Panel voltage decreases from 50 V to the minimum voltage produced at the lowest solar radiation. Correspondingly, the current values concerning solar irradiance are increasing. For constant solar radiation, the maximum power can be easily determined. However, it is not easy in the solar energy harvesting system for the variable solar irradiance occurrence conditions. Hence,

the proposed MPPT with load balancing algorithms is used to track the maximum power at different voltage levels and is named as the panel's PV characteristics shown in Fig. 22.

When 12 V of input is given, the load voltages V_{o1} and V_{o2} are 82 V and 123 V respectively, are measured. The switch voltage V_{gs} of 12 V is obtained, and coupled inductor voltages V_{L1} and V_{L2} are 53 V and 105 V respectively and are shown in Fig. 23. The values used for the simulation and hardware implementation of the converter system are given in Table 2.

The overall efficiency of the system is 97 % for $D = 0.4$ (Fig. 24), and power losses in the individual components present in the circuit are calculated from the Eqs. (40-52). The losses are illustrated in Fig. 25. The comparison of the proposed converter and other existing converters' efficiency is shown in the comparison chart Fig. 26.

7. Conclusion

A reduced ripple, higher gain, low duty ratio converter with load balancing algorithm and FPGA digital controller for solar-powered portable applications, are designed, analyzed with simulation and implementation also verified. It is uniquely designed to minimize the switching stress and reduce the voltage drop across it. The low duty ratio with 97 % efficiency is the notable advantage of this proposed system. The FPGA-based pulse generation ensures a cost-effective approach and low power dissipation by utilizing its reconfigurable nature over the other controllers. The load balancing algorithm ensures continuous load operation even in low radiation from the sunlight. The proposed system has to improve for high-power applications by replacing the coupled inductor with the transformer as a future scope of work.

CRediT authorship contribution statement

Vijayalakshmi Nanjappan: Writing – review & editing, Writing – original draft, Validation, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Suganthi Ramasamy:** Writing – review & editing, Writing – original draft, Validation, Software, Methodology, Investigation, Formal analysis. **Gianluca Gatto:** Writing – review & editing, Supervision, Resources, Project administration, Investigation, Funding acquisition, Formal analysis. **Amit Kumar:** Writing – review & editing, Writing – original draft, Validation, Supervision, Resources, Investigation, Formal analysis, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgement

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References

[1] P. Santhosh, G. Kathiravan, M. Jayaram, M. Deepanraj, L. Ajhai Kumar, N. Devipriya, IoT based supervisory and diagnosis system for solar farm, in: 2023 9th International Conference on Advanced Computing and Communication Systems (ICACCS), Coimbatore, India, 2023, pp. 914–918, https://doi.org/10.1109/ICACCS57279.2023.10112993.

[2] Ching-Ming Lai, Ching-Tsai Pan, Ming-Chieh Cheng, High-efficiency modular high step-up interleaved boost converter for DC micro grid applications, IEEE Trans Ind. Appl. 48 (1) (2012) 161–171.

[3] Shelas Sathyan, H.M. Suryawanshi, M.S. Ballal, A.B. Shitole, Soft switching DC-DC converter for distributed energy sources with high step up voltage capability, IEEE Trans. Ind. Electron. 33 (11) (2018) 9496–9505, https://doi.org/10.1109/TIE.2015.2448515.

[4] P. Santhosh, Y. Susmitha, M. Sowndharya, A.S. Shameer, S. Vasanthakumar, N. Devipriya, Design and modelling of a CSC converter with a variable DC link voltage to drive a brushless DC motor drive, in: 2020 Fourth International Conference on Inventive Systems and Control (ICISC), Coimbatore, India, 2020, pp. 493–499, https://doi.org/10.1109/ICISC47916.2020.9171170.

[5] S. Ramasamy, Z. Ahmad, Y. Bindu, J.R. Torres, Simulation based analysis of transformerless photovoltaic inverter topologies for reactive power handling capability, in: 2020 Second International Conference on Inventive Research in Computing Applications (ICIRCA), Coimbatore, India, 2020, pp. 1028–1034, https://doi.org/10.1109/ICIRCA48905.2020.9182839.

[6] Kuo-Ching Tseng, Jang-Ting Lin, Chi-Chih Huang, High step up converter with three winding coupled inductor for fuel cell energy source applications, IEEE Trans. Power Electron. 30 (2) (2015) 574–581.

[7] S. Ramasamy, S.Meo R.Baccoli, G. Gatto, A. Kumar, Neutral point clamped non-isolated three phase grid-integrated PV inverter topologies for leakage current reduction, Int. Rev. Electric. Eng. 18 (2) (2023), https://doi.org/10.15866/iree.v18i2.23629.

[8] Fang Lin Luo, Hong Ye, Positive output multiple-lift push-pull switched-capacitor Luo-converters, IEEE Trans. Ind. Electron. 51 (3) (2004) 594–602.

[9] Gang Wu, Xinbo Ruan, Zhihong Ye, Non-isolated high step-up Dc-DC converters adopting switched-capacitor cell, IEEE Trans. Ind. Electron. 62 (1) (2015) 383–393, https://doi.org/10.1109/TIE.2014.2327000.

[10] Shubham Goyal, Mukti Barai, Modeling, design and implementation of High gain boost converter with voltage-mode control for PV systems, Int. J. Sci. Eng. Res. 8 (5) (2017) 1636–1645.

[11] P. Santhosh, et al., Fuzzy based landsman converter for pumping application, in: 2021 International Conference on Computational Performance Evaluation (ComPE), Shillong, India, 2021, pp. 040–043, https://doi.org/10.1109/ComPE53109.2021.9752064.

[12] P. Ravi Kumar, C. Gowri Shankar, High-performance single-input three-output DC-DC high gain converter for fuel cell-based electric vehicles, Electric. Eng. (2020), https://doi.org/10.1007/s00202-020-00990-z. Springer.

[13] Moumita Das, Monidipa Pal, Vivek Agarwal, Novel high gain, high efficiency DC-DC converter suitable for solar PV module integration with three-phase grid tied inverters, IEEe J. Photovolt. 9 (2) (2019) 528–537.

[14] A. Kumar, M. Losito, M. Moradpour, G. Gatto, Current source gate driver for SiC MOSFETs in power electronics applications, in: 2022 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Sorrento, Italy, 2022, pp. 523–527, https://doi.org/10.1109/SPEEDAM53979.2022.9842111.

[15] N. Vijayalakshmi, P. Maruthupandi, An optimal low power digital controller for portable solar applications, J. Renew. Sustain. Energy 10 (5) (2018), https://doi.org/10.1063/1.5043500.

[16] M. Ricco, P. Manganiello, E. Monmasson, G. Petrone, G. Spagnuolo, FPGA-based implementation of dual kalman filter for PV-MPPT applications, IEEE Trans. Ind. Electron. (2017) 176–185.

[17] Vijay Joseph Samuel, Gna Keerthi, Prabhakar Mahalingam, Interleaved quadratic boost DC-DC converter with high voltage gain capability, Electric. Eng. (2019), https://doi.org/10.1007/s00202-019-00901-x. Springer.

[18] P. Pirino, M. Losito, A. Kumar, G. Gatto, S. Meo, W.T. Frank, M. Moradpour, Multi-objective gate driver design for a GaN-based half-bridge converter to optimize efficiency and near-field EMI, Int. Rev. Electric. Eng. 16 (2) (2021) 95–103.

[19] Kuo-Chin Tseng, Chi-chih Huang, High step-up, high efficiency interleaved converter with voltage multiplier module for renewable energy system, IEEE Trans. Ind. Electron. 61 (3) (2014) 1311–1319.

[20] Ilhan Kocaarslan, Sude Kart, Naci Genc, Hasan Uzmus, Design and application of PEM fuel cell-based cascade boost converter, Electric. Eng. (2019), https://doi.org/10.1007/s00202-019-00871-0. Springer.

[21] Hamed Pourfarzad, Mohammad Saremi, Tohid Jalilzadeh, An extended high-voltage-gain DC-DC converter with reduced voltage stress on switches/diodes, Electric. Eng. (2020), https://doi.org/10.1007/s00202-020-01040-4. Springer.

[22] M. Moradpour, G. Gatto, Efficiency analysis of two DC-DC universal converters for electric vehicles: single-phase paralleled GaN and two-phase SiC-GaN-based, in: 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, 2019, pp. P.1–P.7, https://doi.org/10.23919/EPE.2019.8915117.

[23] J.-K Kim, G.-W Moon, Derivation, analysis and comparison of non-isolated single-switch high step-up converters with low voltage stress, IEEE Trans. Power Electron. 30 (3) (2015) 1336–1344.

[24] Yu Tang, Dongjin Fu, Ting Wang, Zhiwei Xu, Hybrid switched-inductor converters for high step-up conversion, IEEE Trans. Ind. Electron. 62 (3) (2015) 1480–1490, https://doi.org/10.1109/TIE.2014.2364797.

[25] S. Ramasamy, V. Sivasubramaniyam, G. Gatto, A. Kumar, DC link voltage control based energy management strategy for standalone solar PV fed hybrid system, in: 2023 AEIT International Conference on Electrical and Electronic Technologies for Automotive (AEIT AUTOMOTIVE), Modena, Italy, 2023, pp. 1–6, https://doi.org/10.23919/AEITAUTOMOTIVE58986.2023.10217257.

[26] M. Moradpour, G. Gatto, Controller design of a new universal two-phase SiC-GaN-Based DC-DC converter for plug-in electric vehicles, in: 2018 IEEE 18th

International Power Electronics and Motion Control Conference (PEMC), Budapest, Hungary, 2018, pp. 236–241, https://doi.org/10.1109/EPEPEMC.2018.8521884.
[27] C.C. Hua, Y. Hsiung Fang, Hybrid maximum power point tracking method with variable step size for photovoltaic systems, IET Renew. Power Gener. 10 (2) (2016) 127–132, https://doi.org/10.1049/iet-rpg.2014.0403.
[28] R. Pradhan, B. Subudhi, Adaptive predictive error filter-based maximum power point tracking algorithm, for a photo-voltaic system, J. Eng. 4 (4) (2016) 54–61, https://doi.org/10.1049/joe.2015.0195.

Dr. N. Vijayalakshmi is currently Assistant Professor in Department of Compture Science and Engineering (Data Science) at Dayananda Sagar College of Engineering, Bangalore, India. She has a teaching experience of 15 years at Engineering Colleges. She has completed her BE.ECE in 2007 and ME. VLSI Design in 2013 from Karpagam Academy of Higher Education, Coimbatore. She obtained her PhD (Information and Communication Engineering) from Anna University, Guindy, Chennai, India in 2022. Her areas of interest includes FPGA design and implementation, EV vehicle, Renewable energy and Artificial intelligence. She has published 05 technical papers in refereed journals, 3 book chapters and 10 research papers in national and International conferences. She has published 04 patents. She is an active member in various professional societies like ISTE, SESI, IAENG, UACEE-IRED and ISRD. She has been contributing herself as a reviewer for 3 refereed journals which includes Circuit world, Springer Wireless personal Communication and Artificial Intelligence Reviews.

Dr. R. Suganthi received B.E. in Electrical and Electronics Engineering from Anna University Chennai, India, in 2010. She received an M.E. in Power Electronics and Drives at Anna University Chennai, India 2013. She completed her PhD degree in Electrical Engineering at Anna University, Chennai, in 2022. She is currently working as a Researcher in the Department of Electrical and Electronics Engineering, University of Cagliari, Italy. Her research interest includes power electronics, DC-DC converters and the renewable energy sector. She is actively participating in PNRR projects, further solidifying her commitment to cuttingedge research and development in her field.

Prof. Gianluca Gatto graduated in Electrical Engineering in November 1994 at the University of Cagliari. From October 1997 is at the Department of Electrical and Electronic Engineering at the University of Cagliari where he is a Full Professor of Converters, Electrical Machines and Drives since 2019. He is a member of the IEEE Society with an affiliation with the Industrial Electronic Society, the Electromagnetic Compatibility Society and the Power Electronic Society. He is author of more 110-papers published in international peer-reviewed journals and conference proceedings. In 2003, he started a research activity in the Laboratory of Electromagnetic Compatibility (EMC) of the Department of Electrical and Electronic Engineering at the University of Cagliari and currently serving as its Scientific director. The Laboratory offers EMC evaluation of electro-hydraulic actuators used in oil refineries and the evaluation of the electromagnetic noise emission of power electronic converters employed in wind and solar power plants. He is also Director of the POLILAB – interdepartmental Laboratory of the Faculty of Engineering. His research interests are on power electronic converters, electrical machine, electromagnetic compatibility in industrial and hospital environments, management of the cognitive buildings innovative DC/DC converter topology for electrical vehicle battery management and wide band gap technology.

Dr. Amit Kumar obtained B.Sc. and M.Sc. degrees in Physics from Sri Sathya Sai Institute of Higher Learning, Prashanti Nilayam, India, in 2002 and 2004, respectively. He received PhD degrees in Physics and Innovation Sciences and Technologies University of Cagliari, Cagliari, Italy, in 2010 and 2018, respectively. He is a member of the IEEE Society. He has published over 70 papers in international peer-reviewed journals and conference proceedings. He is Editoral board member of PLOS ONE journal since 2023. He is currently a Researcher at the Department of Electrical and Electronic Engineering, University of Cagliari, Italy. His main research interests include designing novel materials for optoelectronic applications, DC-DC converters, wide band gap devices, renewable energy systems, and electrical vehicle battery management systems.