Phasor Measurement Unit With Digital Inputs: Synchronization and Interoperability Issues

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***Abstract*— In recent years, electrical substations are experiencing a rapid transition toward a fully digital measurement infrastructure in terms of data acquisition, storage, and processing. The IEC Std 61850-9-2 defines the data format, also known as sampled value (SV), to be employed by instrument transformers, merging units, and controller devices. In this scenario, it is reasonable to expect that the phasor measurement units (PMUs) will be directly connected with digital instrument transformers and will be required to process directly the SV data stream. In this article, we present the design and development of a stand-alone PMU based on digital inputs. The prototype has been characterized in terms of estimation accuracy and enriched with a novel functionality that allows for monitoring the time quality of the SV data stream. In this way, the device truly becomes an intelligent electronic device (IED) that guarantees higher interoperability and a more robust management of sporadic synchronization issues. The proposed results confirm the potential of SV-based PMUs and highlight the possibility of further enhancement for synchrophasor measurements based on digital inputs only.**

***Index Terms*— Digital substation, IEC 61850, interoperability, phasor measurement unit (PMU), sampled value (SV), synchronization, time quality.**

I. Introduction

MODERN power systems are characterized by an ever-increasing penetration of distributed generation and renewable energy sources [1], [2]. Due to their inherent volatility and lack of rotating inertia, such resources are likely to produce faster dynamics and high distortion levels, which might interfere with the traditional monitoring and control schemes [3]–[5].

In order to address these issues, electrical substations are experiencing a rapid transition toward a fully digital measurement infrastructure, which promises to guarantee higher levels of control, responsiveness, cost management, and safety. In this context, the IEC Std 61850 defines the substation communication protocols and the need for interoperability between systems from different vendors [6]–[8].

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Such communication protocol includes different message types, specifically designed for applications such as device synchronization, actuators' control, and measurement data. In this regard, the IEC Std 61850-9-2 [9] and its recent amendment [9] (IEC Std) introduce the sampled values (SVs) protocol as a publisher/subscriber communication for information exchange between stand-alone merging units (SAMUs) and intelligent electronic devices (IEDs) over the Ethernet.

Among the different fields that compose the SV message, the application protocol data unit (APDU) is the actual payload: up to eight application-specific data units (ASDUs), each consisting of a three-phase current and voltage measurement (32-bit resolution). Each measurement is timestamped by means of a counter that is reset to zero at each new second occurrence. As the IEC Std relies on the Ethernet, the most common synchronization source is represented by the precision time protocol (PTP) [10]. In the SV protocol, the publisher sends messages (typically, the digitized values of an instrument transformer secondary circuit) with a fixed rate that depends on the nominal system rate (i.e., 50 or 60 Hz) and the number of samples per cycle (i.e., 80 or 256), divided by the number of ASDUs (i.e., from 1 to 8).

The SV protocol was originally conceived to efficiently store and transmit the output of nonconventional or electronic instrument transformers (EITs) and SAMUs. In recent years, though, measurement devices are disseminated in the most important nodes of the network in order to extract relevant parameters and features of the power signal. In this context, a primary role is played by the phasor measurement units (PMUs) that provide an estimate of the amplitude, phase, frequency, and rate-of-change-of-frequency (ROCOF) of the acquired voltage and/or current waveforms based on a common coordinated universal time (UTC) reference. In particular, the amplitude and phase information is condensed in the so-called synchrophasor [11] defined as a phasor whose magnitude and phase are computed from the fundamental component of a signal that is synchronized to UTC time.

These new measurement capabilities combined with the ever-increasing deployment of PMUs also at the distribution level are pushing for integration between phasor estimation and digital data stream [12]. In this way, the data stream transmitted from the substation to the control room would be twofold: on the one side, the real-time (RT) digitized output of EITs and SAMUs; on the other side, a more compressed format consisting of the synchrophasor, frequency, and ROCOF associated with the fundamental component [13].

In the digital substation framework, PMUs are supplied with digital inputs only: the acquisition stage is outsourced to the EIT or SAMU, whereas the so-called SV-PMU is responsible

only for the processing of the SV and for the definition of the measurement timestamp. In this regard, the IEC/IEEE Std 60255-118-1 (PMU Std) defines the performance requirements and the compliance limits in terms of estimation accuracy, reporting latency, and time quality [11].

In this scenario, SV-PMUs are expected to introduce several advantages. First, the data format is standardized and independent of the instrument transformer type, thus allowing easier portability of SV-PMUs in different substations and different configurations. Moreover, the SV data stream is timestamped, and the accuracy of the master clock can be used to infer useful information about the reliability and stability of the acquisition process [14].

On the other hand, the handling of the SV data stream poses several significant challenges from the communication point of view [15]. In the IEC Std protocol, the SVs are transmitted using the data link layer: in the absence of a retransmission policy, packet losses may occur. In a similar way, the SV-PMU should be equipped with a network adapter and sufficient computational capability to be able to deal with a fixed-rate data stream, whereas the traditional scheme with analog inputs allows for much more flexible solutions.

In view of full interoperability between digital inputs and synchrophasor measurements [16], though, the main challenge is represented by the necessity of harmonizing two independent time sources [17], [18]: on the one side, the clock that drives and triggers the merging unit; on the other side, the clock for timestamping the PMU measurements [19]. The two clocks are subject to independent and not necessarily correlated requirements, e.g., the traceability to UTC is a constraint for the PMU only. As a consequence, the occurrence of a synchronization issue at the merging unit side causes the interruption of service and cannot be compensated or circumvented at the PMU side.

In the recent project FutureGrid II, the potential of SVs in electrical substations has been investigated from a metrological perspective. To this end, a new calibration infrastructure for transmitting and receiving SVs has been developed [20], [21] and fully characterized [22]. The introduction of general-purpose libraries for handling SV data streams has facilitated the implementation of the IEC Std communication protocol in a wide variety of low-cost RT controllers [23].

In this context, a recent paper has proposed the implementation of an SV-PMU in an industrial controller consisting of an RT processor and a reconfigurable field-programmable gate array (FPGA) board [24]. The analysis has proven the potential of such applications, as well as the challenges in terms of software design and computational burden [25]. This article is an extension of [24] and investigates the possibility of improving the interoperability capabilities of SV-PMUs. To this end, we propose a novel approach for the management of time quality information within SV-PMUs: an online routine assesses the synchronization state of the entire measurement chain (i.e., SAMU plus PMU) and detects possible issues in the merging unit time source without causing the irreparable interruption of SV-PMU service and the corresponding measurement data stream.

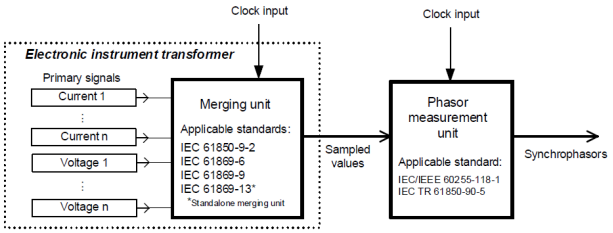

Fig. 1. Block scheme of the measurement chain of a PMU with digital input [11]. For each component, the applicable standards are also reported.

This article is organized as follows. Section II introduces the issues related to the management of different time sources and their impact on the interoperability of SV-PMUs. In Section III, we describe the hardware architecture of the SV-PMU. Section IV describes the software libraries for the efficient management of SV data streams, as well as of time quality information. In Section V, we characterize the SV-PMU in terms of estimation accuracy and capability of detecting time source degradation. Finally, Section VI provides some closing remarks and outlines the research following steps.

II. Synchronization and Interoperability Issues

In this section, we discuss the interoperability challenges inherent in a measurement chain composed of a PMU supplied with the digital SV data stream output by a merging unit (being either an EIT or an SAMU). In particular, we investigate the propagation of potential synchronization errors in the two devices and propose an alternative approach capable of guaranteeing a continuous and consistent operation of the PMU even in the presence of synchronization issues at the level of the EIT or the SAMU.

A synchronization error propagates directly to the final synchrophasor estimate in terms of phase error. Given a signal frequency of 50 Hz, a synchronization error of 1 μs produces a phase error of 314 μrad. In the absence of amplitude errors, this corresponds to a total vector error (TVE) equal to 0.03%. Moreover, synchronization errors represent a challenge also in terms of continuity of operation. The PMU Std dedicates Annex E to the specific case of PMUs supplied with digital inputs and introduces *ad hoc* requirements in terms of synchronization accuracy and reporting latency.

In this context, Fig. 1 shows the entire measurement chain of a synchrophasor measurement based only on digital inputs and indicates the applicable standards for both the merging unit and the PMU side. Without loss of generality, in the following, we consider a configuration where the SAMU is compliant with the IEC Std 61850-9-2, and the PMU is compliant with the IEC Std 60255-118-1 as they are widely employed in many commercial solutions. Nevertheless, similar considerations hold for any other possible combination.

In this measurement setup, each component has an independent clock input. This redundancy is motivated by the fact that SAMU and PMU shall satisfy different requirements in terms of traceability and accuracy of the time source. On the SAMU side, no traceability to UTC is required, and thus,

the SV packet includes a subsecond timestamp field, i.e., a counter reset at each transition of a full second. On the PMU side, instead, a synchrophasor measurement packet includes a second-of-century (SOC) timestamp, thus traceable to an absolute time source. In order to monitor the proper functioning of the measurement chain, both the components periodically transmit information regarding the quality of their time source.

In the SAMU case, the SV data packet includes the attribute SmpSynch that accounts for degraded time quality or loss of time source. More precisely, if the SAMU is synchronized to a global area clock with uncertainty not larger than 1 μs, SmpSynch is equal to 2. If the time source is a local area clock, SmpSynch is equal to 1. In the absence of any time source, SmpSynch is equal to 0. The IEC Std does not specify a minimum update rate of this attribute but allows for defining a holdover period, i.e., a time interval during which the SAMU keeps publishing the SV data packets independently of possible variations in SmpSynch. This policy has been introduced in order to address sporadic or erroneous fault conditions that do not affect the overall accuracy of the measurement chain.

In the PMU case, each measurement is associated with a timestamp that includes an SOC count, a fraction-of-second (FRACSEC) count, and a message time quality flag. The timestamp resolution shall be at least 1 μs within a specified 100-year period. The time quality flag takes into account three main aspects, namely, the traceability to UTC, the clock accuracy, and the leap second status. This hexadecimal flag discriminates a wide range of operating conditions, ranging from a clock failure to a perfect lock to UTC. In between, the clock accuracy is characterized in terms of the order of magnitude of the deviation between PMU time and UTC, e.g., a flag equal to 3 corresponds to a deviation within 100 ns.

In such a diverse scenario, it is difficult to guarantee the continuity of operation and the interoperability between devices compliant with different standards and requirements. The most conservative approach would interrupt the stream of synchrophasor measurements as soon as any of the two devices experiences degradation of the time quality. In this sense, even the transition of the SmpSynch from a global to a local clock might cause the invalidation of the PMU measurements. Despite its consistency, this policy might result in frequent service interruption and, thus, make unfeasible many monitoring and control applications, e.g., state estimation and fault location.

Different techniques can be implemented to mitigate the time synchronization issues of PMUs. For instance, in the PMU data frames, the STAT field includes the PMU Sync Error bit, which is 0 when synchronization with UTC source is granted and 1 otherwise. The other three bits, dedicated to the PMU Time Quality binary code, provide information about the maximum uncertainty in the measurement time tag at the time of the measurement. These fields allow understanding of the quality of time synchronization of the overall system represented by the PMU [26]. However, considering the IEC Std, the information about synchronization quality is missing.

In this article, we propose to evaluate synchronization quality while continuously monitoring the SV data stream. In this way, the same quality of time information provided by a stand-alone PMU can be kept with a PMU based only on digitalized data with the final scope to maintain the interoperability of different devices connected in the same network. In this context, all the applications based on PMU data for RT and off-line analysis can consider the information of time quality to make decisions based on the quality of measurements, e.g., excluding data with an insufficient time quality level.

First, it is important to introduce the normative scenario that defines the maximum allowed limits for both SAMU and PMU sides as follows.

1) The maximum publishing latency of the SAMU shall not exceed 2 ms.
2) The maximum transmission delay between SAMU and PMU shall not exceed 400 ms.
3) The maximum reporting latency of the PMU is increased by 2 ms with respect to the standard requirements in the case of analog inputs.

Within this framework, we propose a method for the online verification of the SAMU time quality directly at the PMU side. As further discussed in the following section, the PMU timestamps each SV data packet as soon as it is received by the network adapter. By comparing the timestamp with the FRASEC count, we evaluate the SV packet latency. A moving average algorithm allows for computing the latency mean and standard deviation over 1 s. If this latency exceeds the 400-ms limit, the PMU measurement process is interrupted. Otherwise, we check whether the current latency value is consistent with the mean and standard deviation as computed in the previous second. If not, the SAMU clock is considered unreliable, and the time quality flag depends only on the PMU clock. It is important to underline that the resolution of this detection routine descends directly on the standard deviation of the SV data latency and the maximum deviation from UTC of the PMU clock.

III. Hardware Implementation

The SV-PMU relies on an NI cRIO-9068 (National Instruments, Austin, TX, USA), i.e., an embedded industrial controller equipped with a Linux RT Operative System (OS) and a reconfigurable FPGA board. More precisely, the cRIO-9068 relies on a 667-MHz dual-core ARM Cortex-A9 (Arm Holdings, Cambridge, U.K.) processor and a Xilinx Artix-7 (Xilinx, San Jose, CA, USA) FPGA board. In principle, the RT controller is responsible for capturing the SV data stream, whereas the second one can be used to expedite the processing of the current and voltage measurements. The FPGA board with the GPS receiver (NI 9467) is in charge to provide the absolute time source to the RT controller within an accuracy level of $\pm$100 ns. For this analysis, the cRIO-9068 has been programed in LabVIEW 2020 RT with the addition of Shared Object libraries, specifically developed for the Linux RT OS (further details in Section IV).

As shown in Fig. 2, the cRIO-9068 is equipped with two independent Ethernet boards, compatible with the IEEE Std

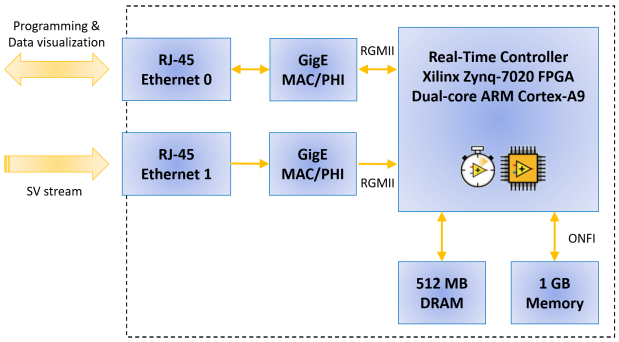

Fig. 2. Block scheme of the data communication and processing paths within the NI cRIO-9068 employed for the implementation of the SV-PMU.

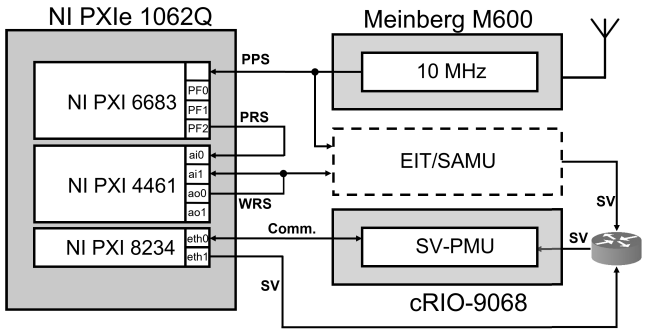

Fig. 3. Measurement setup for the calibration of the SV-PMU.

802.3 (Gigabit Ethernet) and characterized by a communication rate of 100 Mb/s (if autonegotiated, up to 1000 Mb/s). The first board (Ethernet 0) is reserved for the bidirectional communication with the host computer and allows for programming the controller and retrieving in RT the measurement results. The second board (Ethernet 1), instead, is responsible for capturing the SV data stream. The Ethernet transceivers communicate with the RT by means of a Reduced Gigabit Media-Independent Interface (RGMII). Once received the SV messages, the RT extracts the ASDUs, stores the current and voltage measurements, and processes them in order to extract the parameters of interest. In this sense, it is worth noticing that the volatile and nonvolatile memories are limited to 512 MB of Double Data Rate 3 Synchronous Dynamic Random Access Memory and 1 GB of NAND flash drive.

For the characterization of the SV-PMU, the measurement setup in Fig. 3 has been employed. A Meinberg LANTIME M600 Time Server (Meinberg Funkuhren, Bad Pyrmont, DEU) provides the time reference in terms of a pulse-per-second signal that is aligned with UTC-CH by means of the PTP synchronization protocol. An NI PXIe 1062Q hosts the IEC Std calibrator that consists of three main units [21], [22]:

1) a synchronization board (NI PXI 6683) that is disciplined by the reference clock PPS and provides the trigger signals (PRS) for the other boards;
2) a data acquisition board (NI PXI 4461) that generates the analog test waveforms (WRS) and reacquires them (along with the PRS) for defining the reference values;

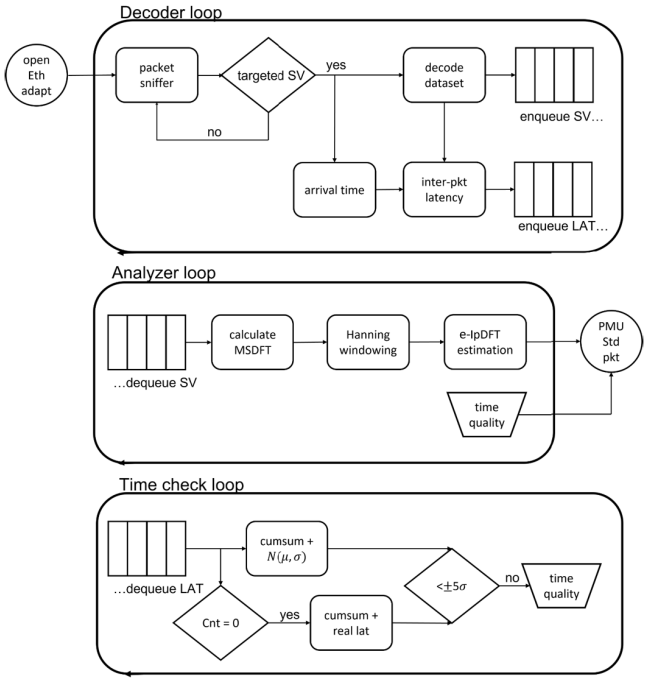

Fig. 4. Logical blocks of the SV-PMU with IED functionalities.

3) an Ethernet interface module (NI PXI 8234) that is responsible for the communication with the SV-PMU and generates the SV data stream, synchronously with the analog output WRS signal.

In the typical calibration setup, the device under test (DUT) is represented by an EIT or an SAMU that receives the analog test waveform and converts it into an equivalent SV data stream. In this context, the SV-PMU can receive its digital input either from the IEC Std calibrator or from the DUT. Both instruments are connected to a network transparent switch.

In this article, we consider the first option. In order to characterize the SV-PMU performance, the IEC Std calibrator allows for a perfect knowledge of the SV data stream and facilitates the debugging process. Once validated the prototype, it will be possible to test it in real-world conditions, i.e., directly connected to an EIT supplied with a known analog input.

IV. Software Implementation

The NI Linux RT version 8.0 is the OS, which manages the tasks of the RT controller. This guarantees that the time constraints of each process are respected within predefined and fixed execution times. The SV-PMU software has been developed in the LabVIEW 2020 RT programming environment by means of a point-to-point Ethernet connection between the cRIO-9068 and a host computer (in our case, the NI PXIe 1062Q; see Fig. 3).

The SV-PMU code is structured in three main parts, running in parallel on the RT OS, as illustrated in the flowchart of Fig. 4. The first part, named *Decoder*, consists of a packet sniffer functionality, which is able to capture the targeted SV data and differentiated it from other streams, e.g., PTP packets, transmitted over the same network. Once captured,

the packets are associated with an absolute timestamp that accounts for their arrival time and decoded in order to extract the informative fields. On the one side, the sequence of measured currents and voltages is clustered and stored into a dedicated first-in–first-out (FIFO) queue. On the other side, the arrival time is compared against the packet time inferred from the SmpCnt field. The latter is a measure of the transmission latency between the SAMU and the SV-PMU, and is stored in another dedicated queue, together with the corresponding SmpCnt.

The second one, named *Analyzer*, reads the current and voltage values from the queue and processes them in order to define the corresponding synchrophasor, frequency, and ROCOF associated with the fundamental component. In particular, a simple algorithm that combines a modulated sliding discrete Fourier transform (MSDFT) [27] and a two-point interpolation with the compensation of the long-range spectral leakage [enhanced interpolated discrete Fourier transform (e-IpDFT)] [28] has been implemented in the SV-PMU. In compliance with the PMU Std, the measurement packet shall contain also the time quality flag. In this design, this information does not depend only on the state of the PMU time source but also on the information coming from an online analysis of the latency values that account for possible inconsistencies in the SAMU synchronization.

The third part, named *Time check*, reads the latency values and determines their statistical variability in terms of mean and standard deviations as computed over a sliding window. In correspondence of each SmpCnt equal to zero, i.e., in correspondence of the full second transition in the SAMU time reference, we evaluate whether the latency value is consistent with the estimated distribution, namely, if it lies within a threshold defined as mean plus five standard deviations.

In the following paragraphs, we better describe the functioning principles of each loop, and we discuss the most suitable setting of their parameters.

A. Decoder

The *Decoder* loop is responsible for three main tasks: the packet sniffing of the Ethernet traffic on the Ethernet 1 port, the selection of streams compatible with the IEC Std communication protocol, the definition of the SV packet arrival time by means of an absolute timestamp, and the decoding and storing of the informative fields, namely, the sequence of currents and voltages, as well as the SmpCnt. To this end, an *ad hoc* Shared Object library has been deployed in the cRIO-9068. It is worth noticing that the library has been derived from a C/C++ code, previously employed for producing an equivalent Dynamic Linked Library for Windows OS [21], [29]. More precisely, the C/C++ source code has been suitably modified and cross-compiled in such a way as to be compatible with the Linux RT OS. Furthermore, since the packet sniffer relies on some functions of the library for packet capture `pcap` [30], also the corresponding Shared Object library has to be correctly installed in the cRIO-9068, and its path has to be accordingly included in the source code cross-compilation.

First, we open the adapter associated with the MAC destination address of the SV data stream. Once initialized in the promiscuous mode, the packet sniffer transmits all the received messages to the central processing unit (CPU), independently of the adopted communication protocol. At the CPU level, the SV messages are identified as the ones whose Ether Type field has a hexadecimal value equal to 88BA. In the case of multiple SV data streams, further refinement is possible by selecting just the messages with a specific MAC source address and SV ID. In this way, it is possible to discriminate the SV data stream of interest from other ongoing communications, e.g., PTP synchronization packets.

Once identified an SV packet that belongs to the stream of interest, the code performs two actions in parallel. On the one side, it extracts from the APDU the sample counter index and the measured values of the three-phase current and voltage for each ASDU. These values are clustered and stored in an FIFO queue for the SV data processing. On the other side, the arrival time of the SV packet is obtained in terms of an absolute timestamp provided by the timekeeper running on the FPGA. By comparing this value with the expected arrival time based on SmpCnt, we estimate the transmission latency associated with each received SV packet, and we store it in another FIFO queue for the management of time quality. It is worth noticing that the two queues allow for the simultaneous execution of dedicated processing routines and run with different time requirements in the other two parallel loops.

In order to optimize the RT performance, the *Decoder* is realized by means of a timed loop with an iteration duration of 250 μs, which corresponds to the publishing rate of the captured SV stream. Moreover, the employment of the FPGA timekeeper guarantees traceability of the arrival time up to the PMU time source and minimizes the variability due to the nondeterministic behavior of the SV data stream.

B. Analyzer

As soon as a new element enters the SV queue, a dedicated notifier triggers the *Analyzer*. In compliance with a reporting rate of 50 frames/s, the loop considers a sliding window of three nominal cycles (i.e., 240 samples at 4000 Hz) that is progressively shifted by 20 ms.

The cluster is extracted from the queue, and each current and voltage channel is treated separately and independently. The first subtask performs the MSDFT, a recursive sliding algorithm that allows for efficiently computing a limited set of DFT coefficients. Being interested in the fundamental component only, we consider just the DFT bins in the range from 0 to 100 Hz (i.e., the second harmonic of the nominal system rate). Differently from the traditional DFT that process sample windows, the MSDFT adopts a sample-by-sample procedure. The convergence of this approach depends on the target frequency resolution. For instance, a frequency resolution of 16.67 Hz corresponds to a window length of three nominal cycles, and the MSDFT will require just 240 samples to converge to the same results as a traditional DFT. As a consequence, the MSDFT allows for drastically reducing the computational complexity of the DFT bin computation by efficiently exploiting its inherent recursive structure.

Given the DFT bins between 0 and 100 Hz, the estimation of the synchrophasor, frequency, and ROCOF associated with the fundamental component is performed by the IpDFT task. First,

it invokes the Hanning subtask that combines the consecutive DFT bins in order to apply a Hanning weighting function, which is meant to reduce the spectral leakage contributions from the negative image components. Then, a two-point interpolation routine is applied to the DFT bins at around 50 Hz. As further discussed in the following section, this algorithm does not guarantee full compliance with the PMU Std performance requirements. Nevertheless, it accounts for a realistic computational burden to be reserved just for the estimation stage and allows for checking whether all the samples are correctly decoded and shared between the different loops.

The IpDFT estimates are now ready to be encapsulated in a measurement packet compatible with the PMU Std and transmitted over the Ethernet 0 communication channel. In the same packet, it is necessary to include the time quality flag, whose value is defined based on the synchronization status of the PMU clock but also on the latency analysis performed in the *Time check* loop. Finally, the analyzer is also in charge to send the synchrophasor in a transmission control protocol (TCP) data packet according to [31] with a rate of up to 50 frames/s.

C. Time Check

The queue for the interpacket latency is triggered as soon as the first SmpCnt equal to zero is identified. The queue has a dimension corresponding to 2 s of acquisition, i.e., 8000 samples at 4000 Hz. In the *Time check* loop, the analysis considers 1 s of acquisition at each time. On the one side, we compute the cumulative sum of the interpacket latency for the first 4000 samples. On the other side, we compute their mean and standard deviation. Based on these values, it is possible to forecast the arrival time of the next sample, i.e., the next SV with SmpCnt equal to zero, as the sum of the cumulative latency plus the mean latency. By assuming that the latency values are normally distributed, the actual arrival time shall differ from the expected value by no more than five times the standard deviation. Otherwise, an inconsistency in the SV data stream is detected, and the time quality of the SAMU is considered unreliable.

The present version of the code implements the time check only in correspondence of an SmpCnt equal to zero as this largely simplifies its experimental validation. Indeed, performing a check every second allows for minimizing the computational burden assigned to this loop. Furthermore, it is easier to reproduce plausible perturbations of the SAMU time source taking as reference the full second transition. Nevertheless, the same criterion is perfectly modular and can be scaled to be run much more frequently, e.g., every nominal cycle (80 samples) or even every sample.

V. Performance Characterization

The performance assessment of the SV-PMU has been carried out in the following configuration. The implemented e-IpDFT algorithm allows for verifying the different software parts required to guarantee a synchrophasor computation based on the SVs. Indeed, as shown in [28], the e-IpDFT algorithm complies with the PMU Std P-class requirements. On the other hand, the main purpose of the proposed system is to be a developer platform able to integrate different algorithms to study the impact of SVs in synchrophasor estimations. In this sense, the e-IpDFT represents a preliminary attempt of synchrophasor and frequency estimator, valuable for verification testing, rather than for actual measurement campaigns. The future steps of the research though will involve its extension in view of a minimization of the leakage contributions [32] and/or the computation of a dynamic phasor that accounts also for time-varying parameters [33].

The SV message contains a single ASDU, with a nominal system rate f_0 and the number of samples per cycle N_c equal to 50 Hz and 80, respectively. This corresponds to a set of three-phase current and voltage signals, sampled at $F_s = 4000$ Hz and with a 16-bit resolution. Given the considered calibration scenario, the following figures and tables refer to a single-phase signal, but similar results hold for the other phases.

Without loss of generality, A and φ are fixed to 1 p.u. and 0 rad, respectively, whereas f is varied between 45 and 55 Hz, which corresponds to the signal frequency range for the M-class compliance requirements in the most recent PMU standard (PMU Std), namely, the IEC/IEEE Std 60255-118-1 [11].

Unless otherwise stated, the test duration is set equal to 3 s, and the PMU reporting rate is set equal to the sampling rate,[1] apart from the ROCOF that is computed as the finite difference between frequency values spaced by 20 ms. In this way, we can get a statistically relevant set of estimates and evaluate the SV-PMU performance as a function of the initial phase.

The test signals $x(t)$ refer to a purely sinusoidal model

$$x(t) = A \cdot \cos(2\pi f t + \varphi_0) \tag{1}$$

where A, f, and φ are the amplitude, frequency, and initial phase of the fundamental component. As digital input to the SV-PMU, the test signals consist of a sample series $x[n]$

$$\begin{aligned} x[n] &:= x(t = nT_s) + \varepsilon \\ T_s &= 1/F_s, \quad n = 0, 1, \ldots, (f_0 \cdot N_c - 1) \end{aligned} \tag{2}$$

where T_s is the sampling period, i.e., 250 μs, and n is the SV counter index that accounts for the time shift with respect to the PPS, i.e., the second occurrence. The additive term ε accounts for any distortion introduced by the SV conversion and should consists of quantization noise only.

A. Test Waveform Quality

First, we have verified the validity of the modeling assumptions. To this end, for each considered frequency value, we have fitted the SVs against the model (1) and evaluated the goodness of fit in terms of the sum of squared residuals (SSR): in the worst case, SSR was equal to $2.943 \cdot 10^{-4}$ p.u. In this context, Fig. 5 shows the residuals' distribution in the time and frequency domains for $f = 51$ Hz. In the time domain,

[1]The IEC/IEEE Std 60255-118-1 defines a maximum reporting rate of 100 frames/s for a nominal system rate of 50 Hz. Nevertheless, a high reporting rate is here employed just for metrological characterization purposes.

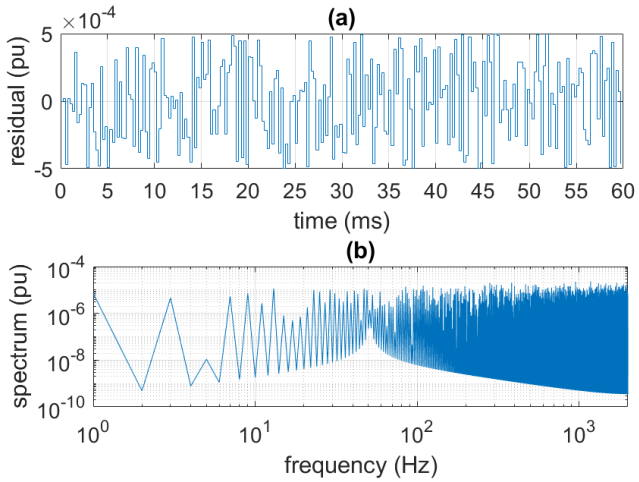

Fig. 5. Test waveform residuals when fitted against an ideal sinusoidal model in (a) time domain and (b) frequency domain.

the residual follows the typical quantization error trend. In the frequency domain (1-Hz spectral resolution), it is noticeable how the energy is spread uniformly from dc to Nyquist rate, and the leakage effects (suggested by the Dirichlet kernel-like trend around 51 Hz) are practically negligible.

Over the same dataset, we have also evaluated the purity of the test waveforms in terms of the total harmonic distortion (THD) and the signal-to-noise ratio (SNR). In the worst case, THD and SNR are equal to −95.624 and 96.348 dB, respectively. It can be noticed how both these values are consistent with an equivalent number of 16 bits.

B. Estimation Accuracy

The estimation accuracy of the SV-PMU has been characterized in two tests: the signal frequency range and the amplitude and phase modulation, as representatives of the static and dynamic compliance verification of the PMU Std.

In the first test, we varied the frequency between 45 and 55 Hz with a step of 0.25 Hz. In order to evaluate the dependence on the frequency resolution, the window length for the MSDFT has been set equal to 3 and 5 nominal cycles, corresponding to 240 and 400 samples, respectively.

For each considered frequency, Fig. 6 shows the maximum value of TVE, frequency error (FE), and the rate of change of FE (RFE) for both the selected window lengths. The performance indices correspond to the performance of the e-IpDFT estimator already published in the literature [28], as further proof of the correct implementation of the processing routine. By compensating for the spectral leakage contribution of the negative image component, it is possible to achieve accuracy levels that outperform the PMU Std limits by nearly one order of magnitude in all the considered configurations.

In the second test, we considered a signal characterized by a simultaneous amplitude and phase modulation. We fixed the modulation depth to 0.1 p.u. and 0.1 rad for amplitude and phase, respectively. We varied the modulation frequency between 0.1 and 5 Hz with a step of 0.05 Hz. In this case, the performance limit corresponds to the M-class requirements as it is the only one to cover entirely the considered range of modulation frequency.

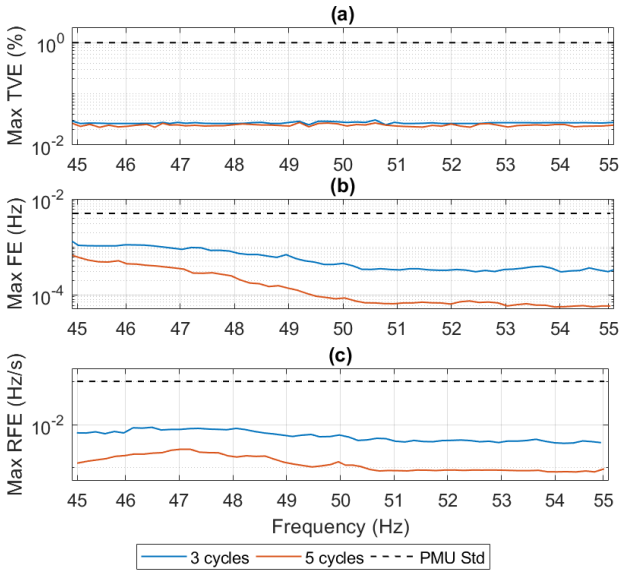

Fig. 6. Signal frequency range test: estimation accuracy in terms of maximum (a) TVE, (b) FE, and (c) RFE for a window length of three and five nominal cycles in blue and red, respectively. The black dashed line denotes the PMU Std performance limit.

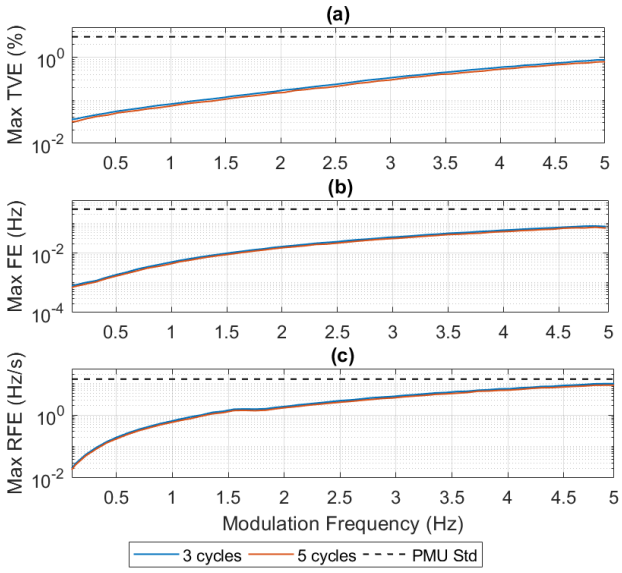

Fig. 7. Amplitude and phase modulation test: estimation accuracy in terms of maximum (a) TVE, (b) FE, and (c) RFE for a window length of three and five nominal cycles in blue and red, respectively. The black dashed line denotes the PMU Std performance limit.

In this regard, Fig. 7 shows the maximum value of TVE, FE, and RFE for both the selected window lengths. As expected, the estimation accuracy degrades as the modulation frequency increases since the e-IpDFT is a static estimator relying on a stationary signal model. Nevertheless, it is interesting to observe that the estimation accuracy is compliant with the PMU Std requirements in all the considered configurations.

C. Synchronization Management

The functionality of time quality assessment has been validated by means of a measurement setup that allows for suitably distorting the SAMU time source. As shown in

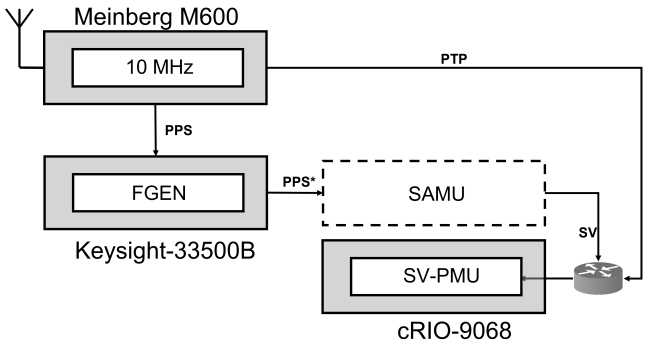

Fig. 8. Measurement setup for the characterization of the time quality monitoring functionality.

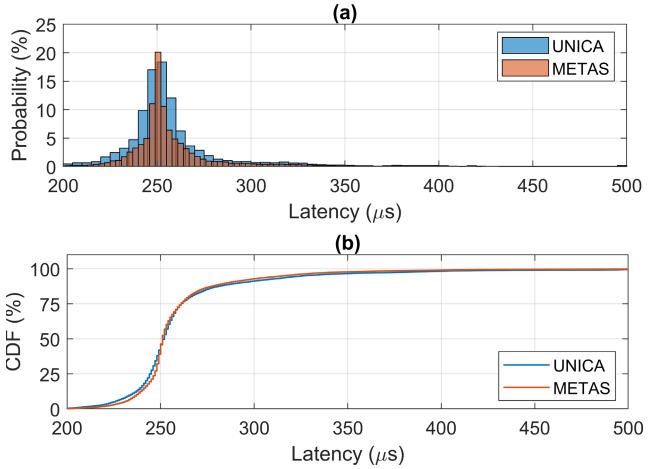

Fig. 9. (a) Histograms and (b) cdfs of the interpacket latency on two different SAMUs as measured at UNICA and METAS laboratories.

Fig. 8, the Meinberg M600 operates as the master clock. The time reference is available in two formats: PTP and PPS. The former is transmitted to the SV-PMU through a network transparent switch. The latter triggers a Keysight 33500B Function Generator (Keysight Technologies, Santa Rosa, CA, USA) that, in turn, synthesizes a square wave used to synchronize the SAMU. In this way, we are able to derive a new time reference PPS*, which is locked to the PPS, but can be shifted according to a static or a dynamic time offset. The measurement chain is completed by the SAMU that transmits the SV data stream through the same switch as the PTP traffic.

The same setup has been implemented at the Electrical Energy and Power Laboratory, Swiss Federal Institute of Metrology (METAS), and the Department of Electrical and Electronic Engineering, University of Cagliari (UNICA). The SV-PMU is realized with the exact same hardware and software configurations. The only significant difference is represented by the SAMU and the switch. As regards the SAMUs, we employed two commercial devices, namely, a Condis EFOCT (Condis SA, Rossens, Switzerland) and an Omicron CMC 256plus (Omicron Electronics, Klaus, Austria), configured with the same publishing rate and the number of ASDUs. As regards the switch, instead, the different technologies and different numbers and types of connected devices allow for reproducing noncoincident yet comparable network traffic scenarios.

The first test involved the precision of the PPS* output by the function generator. In order to guarantee the precision and stability of its internal time base, we evaluated the deviation and jitter between the PPS and the PPS* in normal conditions, i.e., in the absence of any perturbation. For this analysis, we measured the delay between the two squared waveforms by means of a WaveSurfer 3000z Digital Oscilloscope (Teledyne Lecroy, Chestnut Ridge, NY, USA) characterized by a sampling rate and a pass bandwidth of 2 GHz and 200 MHz, respectively. Over an observation interval of 10 min, the delay means and standard deviation did not exceed 1.0 and 2.5 ns, respectively. Since these discrepancies are way below the variability introduced by the SV transmission, it is, thus, reasonable to assume that the PPS* is perfectly locked to the original PPS and reproduces the same statistical variability.

Then, we quantified the expected distribution of the latency values in normal operations. For this analysis, we considered an entire observation interval of 15 s, corresponding to 60 000 latency values in the given SV configuration. In this context, Fig. 9 shows the distribution obtained at METAS and UNICA laboratories in blue and red, respectively. In the two datasets, the latency variation range can be assessed in terms of mean and standard deviation: 258.80 ± 32.34 μs for METAS and 260.48 ± 43.32 μs for UNICA.

In the upper graph, the histogram representation is adopted. It is worth noticing that the distributions are quite consistent and centered around the expected nominal interpacket latency, i.e., 250 μs. On the other hand, it is also important to underline that the two datasets do not follow a normal distribution but present a limited yet nonnegligible set of occurrences where the latency is incremented up to 400 μs. The presence of these outliers is reasonably due to the nonideal network configuration due to the concurrent presence of other streams (e.g., PTP) and the nonlinear effect of the switch.

Similar considerations hold for the lower graph where the cumulative distribution functions (cdfs) are plotted. Once more, the correlation between the two datasets is remarkable, as well as the fact that the distributions have a single mode centered at 250 μs. In this sense, if we define outliers as any latency value larger than 300 μs, it is interesting to observe that they represent less than 8% of the overall dataset.

In the first operative test, we reproduced a synchronization issue, where the PPS* is delayed by a sudden offset of 10 ms. In particular, the system is kept in normal conditions for nearly 20 s in order to guarantee a full stabilization of all the processes. Then, the offset is applied and kept for nearly 20 s. In Fig. 10, we compare the expected and the measured arrival time of the SV packets with SmpCnt equal to zero. In order to enhance the readability of the variation range of the two datasets, the arrival times have been normalized by 1 s. In this sense, it should be noticed how the average deviation of 6.5 ms is compatible with the propagation of the statistical distributions shown in Fig. 9.

The estimated and measured values present uncorrelated yet similar trends. In correspondence with the offset application, though, the deviation between real measurements and statistical inference becomes significant and exceeds the detection

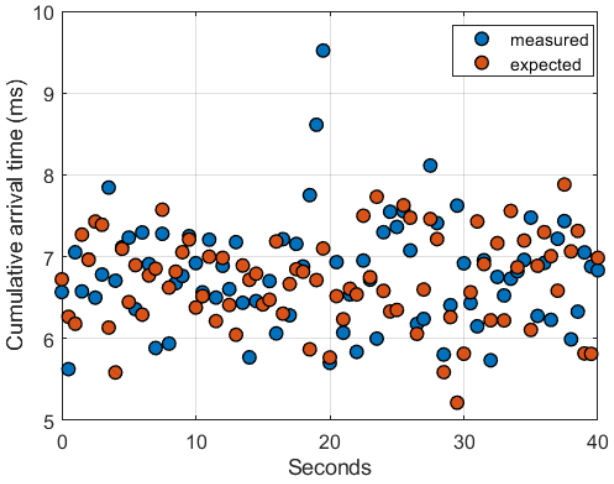

Fig. 10. Comparison between expected (red) and measured (blue) arrival time of the next SV packet with SmpCnt equal to zero.

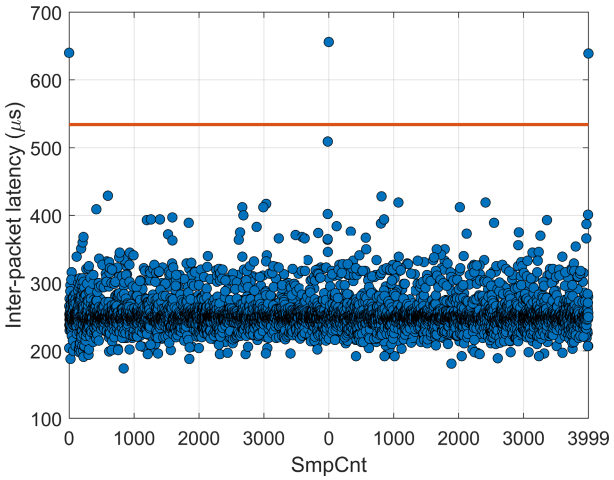

Fig. 11. Blue markers indicate the interpacket latencies as a function of the SmpCnt in the presence of a PPS* used as SAMU time source that is linearly drifting by 1 ms per second. The horizontal red line represents the 5σ deviation from the expected values.

threshold equal to five times the latency standard deviation. On the other hand, it is interesting to observe how such discrepancy is noticeable in a single occurrence. In fact, by applying a constant offset to the PPS, the subsequent cumulative arrival times will be shifted with respect to the absolute PTP time but consistent with the SV data latency.

As the final test, we generated a distorted PPS* that starts locked to the PPS but then drifts according to a linear ramp such that each new second transition is delayed by 1 ms. In this regard, Fig. 11 presents the interpacket latency as a function of the SmpCnt of the corresponding packet over an observation interval of 2 s, namely, the content of the queue of the *Time check* loop. The red solid line, instead, indicates the threshold value used to detect possible anomalies and computed as five times the standard deviation.

It is worth noticing that the latency values are consistent with the aforementioned distribution, apart from the ones associated with SmpCnt equal to zero. In that case, the distorted PPS* causes a significant increment in the interpacket latency that is repeated periodically at each second transition. On the contrary, the other SV packets are captured with a nearly stable arrival time and keep the overall statistical distribution nearly constant over time. Therefore, the proposed policy proves to be able to detect also slowly drifts in the SAMU time sources and vary accordingly the time quality of the SV data stream.

VI. Conclusion

In this article, a novel design for a PMU operating with digital inputs based on the SV communication protocol is presented. Along with the synchrophasor measurement, the device integrates a new functionality for the online management of time quality information not only from the PMU side but also from the SAMU side. In this way, the SV-PMU guarantees higher interoperability and allows for dealing with temporary synchronization issues while keeping the full operation of the measurement chain. This article describes in detail the hardware and software architecture of the instrument and discusses the possible bottlenecks in terms of the measurement procedure and computational requirements.

The performance of the proposed SV-PMU was assessed by means of a calibration system for IEC Std 61850-9-2. In this context, we evaluated the quality of the SV data streams in terms of quantization noise and harmonic distortion. The SV-PMU estimation accuracy was characterized in terms of TVE, FE, and RFE in the signal frequency range test of the IEC Std 60255-118-1. Finally, we validated the online time quality check by means of a dedicated measurement setup that allows for reproducing different realistic scenarios.

The results confirm the potential of the proposed architecture; even the performance is limited by the network configuration and the available computational resources. Nevertheless, the capability of handling in the same device both measurements and synchronization streams represents a crucial requirement for the development and establishment of monitoring and control applications based on digital inputs only.

The future steps of the research will involve the implementation of more sophisticated estimation algorithms and the further optimization of the time quality check functionality.

References

[1] G. T. Heydt, "The next generation of power distribution systems," *IEEE Trans. Smart Grid*, vol. 1, no. 3, pp. 225–235, Dec. 2010.

[2] M. Paolone *et al.*, "Fundamentals of power systems modelling in the presence of converter-interfaced generation," *Electr. Power Syst. Res.*, vol. 189, Dec. 2020, Art. no. 106811.

[3] A. Angioni, J. Shang, F. Ponci, and A. Monti, "Real-time monitoring of distribution system based on state estimation," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 10, pp. 2234–2243, Oct. 2016.

[4] G. Frigo, A. Derviškadic, Y. Zuo, and M. Paolone, "PMU-based ROCOF measurements: Uncertainty limits and metrological significance in power system applications," *IEEE Trans. Instrum. Meas.*, vol. 68, no. 10, pp. 3810–3822, Oct. 2019.

[5] G. Rietveld, P. S. Wright, and A. J. Roscoe, "Reliable rate-of-change-of-frequency measurements: Use cases and test conditions," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 9, pp. 6657–6666, Sep. 2020.

[6] N. Higgins, V. Vyatkin, N.-K. C. Nair, and K. Schwarz, "Distributed power system automation with IEC 61850, IEC 61499, and intelligent control," *IEEE Trans. Syst., Man, Cybern., C, Appl. Rev.*, vol. 41, no. 1, pp. 81–92, Jan. 2011.

[7] M. Uslar and R. Bleiker, "Automation for the smart grid: IEC 61850—Substation automation and DER communication," in *Standardization in Smart Grids*. Berlin, Germany: Springer, 2013, pp. 115–128, doi: 10.1007/978-3-642-34916-4_7.

[8] D. D. Giustina *et al.*, "Smart grid automation based on IEC 61850: An experimental characterization," *IEEE Trans. Instrum. Meas.*, vol. 64, no. 8, pp. 2055–2063, Aug. 2015.
[9] *IEC/IEEE International Standard—Communication Networks and Systems for Power Utility Automation—Part 9–2: Specific Communication Service Mapping (SCSM) Sampledvalues Over ISO/IEC 8802-3*, IEC/IEEE Standard 61850-9-2, 2011, pp. 1–18.
[10] D. M. E. Ingram, P. Schaub, and D. A. Campbell, "Use of precision time protocol to synchronize sampled-value process buses," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 5, pp. 1173–1180, May 2012.
[11] *IEC/IEEE International Standard—Measuring Relays and Protection Equipment—Part 118–1: Synchrophasor for Power Systems—Measurements*, IEC/IEEE Standard 60255-118-1:2018, 2018, pp. 1–78.
[12] P. Castello, P. Ferrari, A. Flammini, C. Muscas, and S. Rinaldi, "An IEC 61850-compliant distributed PMU for electrical substations," in *Proc. IEEE Int. Workshop Appl. Meas. Power Syst. (AMPS)*, Sep. 2012, pp. 1–6.
[13] P. Castello, A. D. Femine, D. Gallo, M. Luiso, C. Muscas, and P. A. Pegoraro, "Measurement of synchrophasors with stand alone merging units: A preliminary study," in *Proc. IEEE Int. Instrum. Meas. Technol. Conf. (I2MTC)*, May 2021, pp. 1–6.
[14] M. G. Kanabar, T. S. Sidhu, and M. R. D. Zadeh, "Laboratory investigation of IEC 61850-9-2-based busbar and distance relaying with corrective measure for sampled value loss/delay," *IEEE Trans. Power Del.*, vol. 26, no. 4, pp. 2587–2595, Oct. 2011.
[15] D. M. E. Ingram, P. Schaub, R. R. Taylor, and D. A. Campbell, "Performance analysis of IEC 61850 sampled value process bus networks," *IEEE Trans. Ind. Informat.*, vol. 9, no. 3, pp. 1445–1454, Aug. 2013.
[16] E. Y. Song, K. B. Lee, G. J. FitzPatrick, and Y. Zhang, "Interoperability test for IEC 61850-9-2 standard-based merging units," in *Proc. IEEE Power Energy Soc. Innov. Smart Grid Technol. Conf. (ISGT)*, Apr. 2017, pp. 1–6.
[17] Q. Yang, D. Keckalo, D. Dolezilek, and E. Cenzon, "Testing IEC 61850 merging units," in *Proc. Western Protective Relay Conf.*, 2017, pp. 1–8. [Online]. Available: https://cms-cdn.selinc.com/assets/Literature/Publications/TechnicalPapers/
[18] P. Castello *et al.*, "An active phasor data concentrator suitable for control and protection applications," in *Proc. Int. Conf. Smart Grid Synchronized Meas. Analytics (SGSMA)*, May 2019, pp. 1–7.
[19] P. Castello, P. Ferrari, A. Flammini, C. Muscas, P. A. Pegoraro, and S. Rinaldi, "Assessment of time synchronization quality in a distributed PMU," in *Proc. IEEE Int. Instrum. Meas. Technol. Conf. (I2MTC)*, May 2015, pp. 1549–1554.
[20] T. Lehtonen and J. Hallstrom, "A reference merging unit and calibration setup for sampled values over Ethernet," in *Proc. Conf. Precis. Electromagn. Meas. (CPEM)*, Jul. 2016, pp. 1–2.
[21] M. Agustoni and A. Mortara, "A calibration setup for IEC 61850-9-2 devices," *IEEE Trans. Instrum. Meas.*, vol. 66, no. 6, pp. 1124–1130, Jun. 2017.
[22] M. Agustoni and G. Frigo, "Characterization of DAC phase offset in IEC 61850-9-2 calibration systems," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–10, 2021.
[23] S. M. Blair, A. J. Roscoe, and J. Irvine, "Real-time compression of IEC 61869-9 sampled value data," in *Proc. IEEE Int. Workshop Appl. Meas. Power Syst. (AMPS)*, Sep. 2016, pp. 1–6.
[24] G. Frigo and M. Agustoni, "Phasor measurement unit and sampled values: Measurement and implementation challenges," in *Proc. IEEE 11th Int. Workshop Appl. Meas. Power Syst. (AMPS)*, Sep. 2021, pp. 1–6.
[25] Y. Seferi, R. G. Q. Cetina, and S. M. Blair, "Review of PMU algorithms suitable for real-time operation with digital sampled value data," in *Proc. IEEE 11th Int. Workshop Appl. Meas. Power Syst. (AMPS)*, Sep. 2021, pp. 1–6.
[26] P. Castello, C. Muscas, P. A. Pegoraro, and S. Sulis, "Trustworthiness of PMU data in the presence of synchronization issues," in *Proc. IEEE Int. Instrum. Meas. Technol. Conf. (I2MTC)*, May 2018, pp. 1–5.
[27] E. Jacobsen and R. Lyons, "The sliding DFT," *IEEE Signal Process. Mag.*, vol. 20, no. 2, pp. 74–80, Mar. 2003.
[28] P. Romano and M. Paolone, "An enhanced interpolated-modulated sliding DFT for high reporting rate PMUs," in *Proc. IEEE Int. Workshop Appl. Meas. Power Syst. (AMPS)*, Sep. 2014, pp. 1–6.
[29] S. M. Blair, F. Coffele, C. D. Booth, and G. M. Burt, "An open platform for rapid-prototyping protection and control schemes with IEC 61850," *IEEE Trans. Power Del.*, vol. 28, no. 2, pp. 1103–1110, Apr. 2013.
[30] V. Jacobson, C. Leres, and S. McCanne. (1994). *LIBpcap Lawrence Berkeley Laboratory*. Berkeley, CA, USA. Accessed: Jun. 10, 2021. [Online]. Available: http://www.tcpdump.org/
[31] *IEEE Standard for Synchrophasor Data Transfer for Power Systems*, IEEE Standard C37.118.2-2011, 2011.
[32] A. Derviškadić, P. Romano, and M. Paolone, "Iterative-interpolated DFT for synchrophasor estimation: A single algorithm for P- and M-class compliant PMUs," *IEEE Trans. Instrum. Meas.*, vol. 67, no. 3, pp. 547–558, Mar. 2018.
[33] G. Frigo, A. Derviskadic, Y. Zuo, A. Bach, and M. Paolone, "Taylor-Fourier PMU on a real-time simulator: Design, implementation and characterization," in *Proc. IEEE Milan PowerTech*, Jun. 2019, pp. 1–6.

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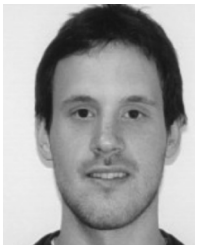

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