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# A Battery-Based Auxiliary Power System for an All-Electric Aircraft: A Novel Converter Configuration

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***Abstract*—In all-electric airctaft, the Auxiliary Power Units (APU) based on fossil fuels are replaced by energy storage systems equipped with batteries or fuel cells. This paper proposes a novel 115V$_{rms}$, 400Hz DC/AC converter for a 5kW APU of a lightweight all-electric aircraft. The proposed DC/AC converter employs a Five-Level Cascaded H-Bridge (5-LCHB) supplied by a Triple-Active Bridge (TAB). The TAB allows the independent control of its two output ports while connected to a single electrochemical battery pack. The three-winding high-frequency transformer provides galvanic isolation, endowing reliability to the conversion system. The inherent decoupling condition established between the TAB output ports is modelled, and the proposed DC/AC converter design is assessed with a co-simulation study on PLECS and Matlab/Simulink. The proposed system has been experimentally validated on a scaled converter prototype. The results show that the TAB inherent decoupling condition is reached between the output ports achieving the proper implementation of the Selectvie Harmonic Elimination Pulse Active Width Modulation (SHE-PWM) in the 5-LCHB. Moreover, the control system exhibits good performance dynamics even under output step-load variations.**

***Index Terms*—DC/AC converter, multilevel converter, triple active bridge, auxiliary power unit, all electric aircraft.**

## I. INTRODUCTION

THE CO$_2$ emissions from the transport sector continue to rise due to to the ever-increasing demand for mobility. In fact, the International Energy Agency (IEA) reports that between 2016 and 2019, the amount of CO$_2$ emitted into the atmosphere changed from 7.86Gt/y to 8.24Gt/y, an increase of 4.83% in four years. In this trend, the aviation sector represents the most polluting category after road transport, with a share of 12.62% of CO$_2$ emitted in 2019 [1]. With global demand for air transport growing at 4.5% per year, air pollution from aviation sector is also expected to increase [2]. The targets proposed in *Flightpath 2050* to reduce the impact of aviation are achievable through the electrification of aircraft systems [3]. To begin, the More Electric Aircraft (MEA) concept has been developed, in which in-flight fuel consumption is reduced by replacing several non-propulsive systems with more efficient electric devices (e.g. hydraulic actuators are replaced by electric ones). Furthermore, MEAs present an enhanced electrical system that also includes additional energy sources such as electrochemical batteries, fuel cells and supercapacitors. As a result, the Electric Power System (EPS) of a MEA becomes more complex than that of a conventional aircraft, looking like an isolated terrestrial microgrid [4], [5]. In this perspective, particular attention must be paid to the safety and reliability, as the risks of EPS failure increase. Among several aspects to be considered, the arc fault and the partial discharge phenomenon need to be addressed [6], [7] . In this respect, improved circuit breaker fault protection strategies and intelligent fault tolerant control are under investigation [8], [9].

In the EPS, the Auxiliary Power Unit (APU) provides energy for both the auxiliary systems and the main engine starting system, both during ground operations and in the event of an in-flight emergency. In traditional architectures, the APU consists of a kerosene-fueled gas turbine that powers cabin pressurisation and air conditioning systems, landing gear, multiple hydraulic actuators, fuel systems, avionics, electrical controls, de-icing systems and more. In the MEA, the APU's electrical power generation is boosted to become a hybrid electric system using electrochemical energy storage systems and fuel cells [5], [10], [11].

This more sophisticated EPS configuration has led the aviation standard to address the need to overcome multiple DC and AC voltage levels. In this respect, power electronics play a crucial role in aircraft EPS, both for the propulsion system and the APU [12]–[14]. Regarding DC equipment, the most relevant power demand is observed on the 270V$_{DC}$ bus [10]. Several research activities have been carried out in the field of DC/DC conversion systems to increase the conversion efficiency, using improved modulation strategies [15]. Furthermore, multi-port converter topologies have been proposed to reduce system volume and weight [16]. In addition, other research activities are aimed at increasing the conversion system power rate [17]. The management of the two DC busses with remarkable voltage diversity, used in the avionics sector (e.g. between 270V$_{DC}$ and 28V$_{DC}$ busses), has been investigated and the usage of higher voltage conversion ratios is proposed. [18], [19]. On the other hand, most aircraft AC devices operate on the 115V$_{rms}$ 400Hz bus and much research activity has been done on suitable AC conversion systems [10]. A dual inverter configuration is proposed as the electrical drive for equipment such as flight control systems, fuel pumps

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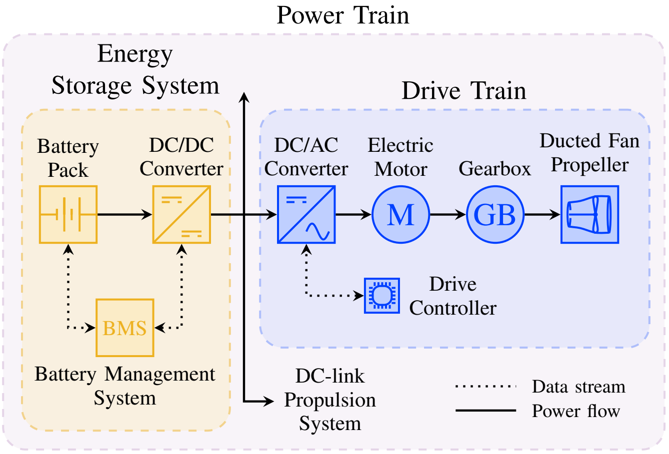

Fig. 1. Power train schematic representation of an All-Electric Aircraft.

and environmental control systems to provide redundancy and fault tolerance capability using a reduced number of devices [20]. Nevertheless, multilevel converters are one of the most quoted topologies due to their better power quality and high efficiency. Neutral Point Clamped (NPC) configurations are proposed in [21] and [22]. The former proposes a three-level T-type NPC with a novel modulation strategy to ensure NP balancing, which is one of the major issues to be addressed in this type of converter, while the latter proposes a hybrid seven-level active NPC topology that allows for improved EMI emissions.

The evolution of MEA towards complete electrification of aircraft systems is represented by the All-Electric Aircraft (AEA). In this advanced architecture, jet engines are replaced by more efficient electric power trains, as shown schematically in Fig. 1 [23]. It consists of a Drive Train (DT) and an Energy Storage System (ESS). The DTs consist of thrust units, electrical machines, drives and, optionally, gearboxes. Thrust units usually consist of simple propellers or more efficient ducted fans, where the propeller is enclosed by an annular airfoil, resulting in higher thrust and lower energy consumption. A distributed electric propulsion system is usually considered to distribute the propulsion power, provide redundancy and improve system reliability. Brushless is the most common type of electric machine used for propellers. In addition, other prototypes such as superconducting electric motors are being developed for future electric commercial aircraft designs. An electric drive controls the speed of the motor and a gearbox, if used, adapts the propeller speed ratio [5]. The ESS generally consists of three subsystems: the electrochemical battery, the Battery Management System (BMS) and the power conversion system. As they are at the top of the drivetrain, the DC/DC power converter and electrical energy sources play a crucial role in AEA designs as they define the power and energy system capability and must ensure high reliability standards [5], [23].

The APU of an AEA avoids gas turbines and relies on electrical energy sources such as electrochemical battery packs. The benefits of replacing the gas turbine are not limited to pollution reduction. As the main causes of APU failure on an aircraft are ascribed to fuel distribution and control, cracks in the exhaust ducts and failure of rotating parts, the replacement of the APU generation system reduces the risk of flight delay or cancellation. This aspect is reinforced by the fact that the 50% of the time that an APU-based gas turbine fails, it has to be replaced, resulting in increased maintenance time and cost [24]. Since the APU for AEA is a DC energy source, it must be properly conditioned to supply the AC loads. The busiest AC bus in the aircraft is the $115\text{V}_{\text{rms}}$ , 400Hz, and proper DC/AC converters must be employed. Multilevel conversion systems allow to improve harmonic content and EMI pollution. In these devices, each voltage level has to be precisely addressed to preserve the stability and reliability of the system to comply with the strict regulations of the aeronautical standards.

In this contest, a novel $115\text{V}_{\text{rms}}$ , 400Hz DC/AC conversion system for an AEA APU was proposed in [25] and an extension is developed in this work. The Fig. 2 shows a schematic representation of the proposed system. A Five-Level Cascaded H-Bridges (5-LCHB) interfaces the $115\text{V}_{\text{rms}}$ , 400Hz aircraft bus by modulating the voltage signal characterised by five voltage levels. A Triple-Active Bridge (TAB) converter is employed to interface the energy storage system to the 5-LCHB and feed its two independent DC sources at the required voltage levels. The TAB consists of three H-bridges connected to a Three-Winding High-Frequency Transformer (3W-HFT), as shown in Fig. 2 [26]. The 3W-HFT allows the use of a lighter conditioning system if compared to two separate DC conversion stages. However, the power decoupling between the TAB output ports has to be ensured. Improved control strategies have been proposed and synthesised from TAB modelling [27]–[30]. On the other hand, many solutions rely on a hardware approach that allows an inherent decoupling condition achieved by suppressing the external leakage inductor at one of the TAB ports. The adoption of this configuration avoids to increase the complexity of the control algorithms

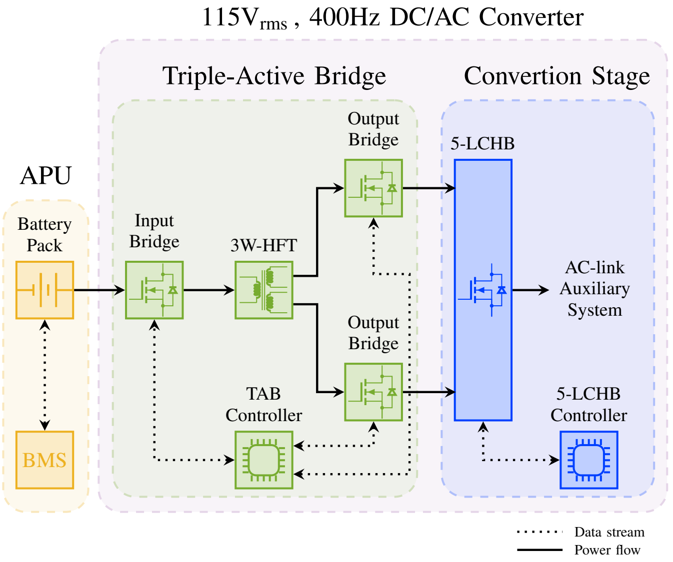

Fig. 2. Auxiliary Power Unit and DC/AC converter for the $115\text{V}_{\text{rms}}$ , 400Hz systems of an All-Electric Aircraft.

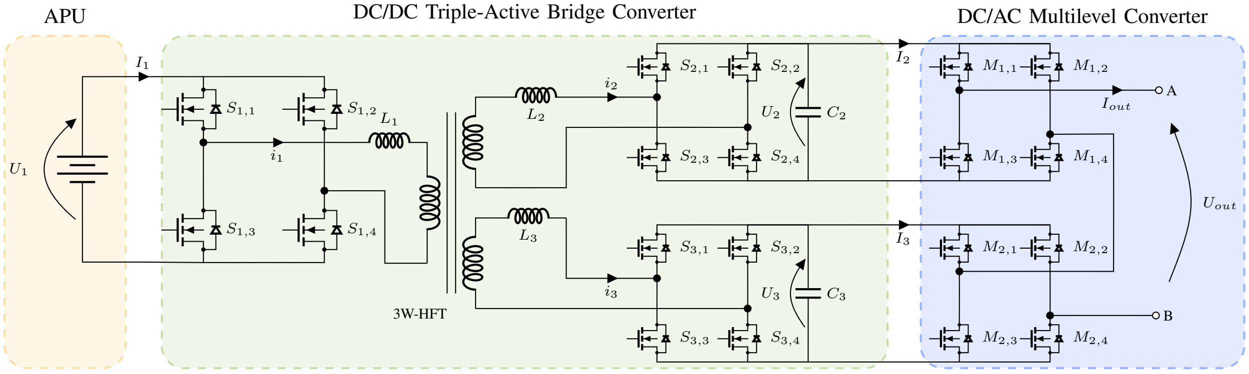

Fig. 3. Auxiliary Power Unit schematic with the proposed $115\mathrm{V_{rms}}$, 400Hz DC/AC converter topology for an AEA.

[31]–[33]. In this paper, the hardware solution approach is implemented and a complete analysis of the TAB decoupling condition is presented. In addition, the effect of the internal leakage inductance is addressed and the design requirements of the 3W-HFT to suppress the transformer coupling effects are outlined.

The choice of this particular configuration avoids the problem of voltage balancing, typical of NPC converters. This ensures the reliability and stability of the system in compliance with aeronautical standards. In addition, the use of a TAB allows the power to be split between two cascaded branches. This allows more suitable power transistors (e.g. MOSFET, SiC or GaN) to be selected, improving conduction resistance and allowing the system to modulate at higher frequencies. The 5-LCHB reduces harmonics and EMI emissions, increasing efficiency and reliability while reducing power losses. This results in a more compact design and reduces the cost of transformers, inductors and heatsinks. The use of Selective Harmonic Elimination Pulse Active Width Modulation (SHE-PAWM) permits specific voltage harmonics to be suppressed, resulting in a lighter filter stage at the AC bus interface [34].

## II. PROPOSED APU DC/AC CONVERTER TOPOLOGY

The design targets for an AEA conditioning system must deal with the rigorous voltage standards of the aeronautic sector, whether it is meant for the propulsion powertrain or an APU. Aiming at the complete electrification of auxiliary equipment in Lightweight All-Electric Aircraft (LAEA), a 5kW, $115\mathrm{V_{rms}}$, 400Hz APU DC/AC power conditioning system supplied by an ESS has been assumed as the design target. The 5-LCHB converter topology is selected to accomplish the DC/AC conversion. Specifically, the SHE-PAWM allows for the selective cancellation of specific voltage harmonic components if defined values of DC bus amplitude and commutation pattern are applied to cascaded H-Bridge converters [34]. Therefore, the SHE-PAWM implementation on the 5-LCHB converter requires an accurate and decoupled management of the DC bus voltages. Thus, a TAB converter is chosen as a candidate since it allows for managing the two 5-LCHB DC voltage levels independently, guaranteeing galvanic isolation. This endows high power density to the APU DC/AC conditioning system, and phase shift modulation strategies allow for accurately controlling the DC output voltage set-points. The proposed APU DC/AC power conditioning topology is shown in Fig. 3.

### A. Triple-Active Bridge Model

The schematic structure of the TAB is shown in Fig. 3. Under Single-Phase Shift (SPS), the modulation of active bridges generates three square wave voltages with a 50% duty cycle at a fixed switching frequency $f_s$. The control is achieved by managing the phase shift $\delta_{kj}$ between the voltage of $j$-isium active bridge concerning $k$-isium one [26]. Employing SPS in TAB endows control simplicity and allows to achieve soft switching conditions. Besides, its disadvantages are the presence of high peak currents on the HFT and flow-back currents for the DC side. In addition, the soft switching conditions and the zero circulation power condition impose limitations on the definition of voltage and power set-points. To model the TAB, an equivalent circuit model is proposed in Fig. 4a. This has been conceived replacing the H-bridges with the square wave voltage generators $u_1$, $u_2$ and $u_3$, and the 3W-HFT transformer with its magnetising inductance $L_m$ and its leakage inductances $L_1$, $L_2$ and $L_3$.

The TAB model is developed taking Port #1 as the reference. Therefore, the parameters and electrical quantities are related to this port according to (1)

$$u'_k = \frac{N_1}{N_k}u_k; \quad i'_k = \frac{N_k}{N_1}i_k; \quad L'_k = \left(\frac{N_1}{N_k}\right)^2 L_k, \quad k = 2,3; \tag{1}$$

where $N_1 : N_2$ and $N_1 : N_3$ are the respective turns ratio of ports #2 and #3 concerning the reference one.

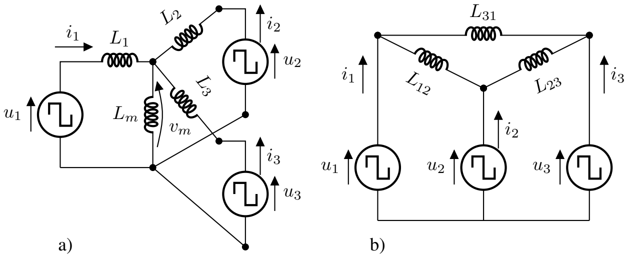

Fig. 4. Equivalent circuits of TAB converter: a) TAB Y configuration and b) TAB $\Delta$ configuration.

The voltage across $L_m$, namely $u_m$, is evaluated as a function of the voltages $u_k$ by applying the law of superposition. Consequently, $u_m$ assumes the form given in (2) [35].

$$u_m = \frac{u_1 L_2' L_3' + u_2' L_1 L_3' + u_3' L_1 L_2'}{L_1 L_2' + L_1 L_3' + L_2' L_3'} \tag{2}$$

Therefore, the power delivered at each Port #$k$, $P_k$, is determined by (2) implementing the equation of the SPS modulation strategy, referring to the voltage $u_k$ of the port $k$ and the voltage $u_m$. Under this hypothesis, the power $P_k$ assumes the explicit forms reported in (3), (4) and (5) considering $k = 1, 2, 3$, respectively [35].

$$P_1 = \frac{U_1 U_2' L_3' \, \delta_{12} \, (\pi - |\delta_{12}|) + U_1 U_3' L_2' \, \delta_{13} \, (\pi - |\delta_{13}|)}{2\pi^2 \, f_s (L_1 L_2' + L_1 L_3' + L_2' L_3')} \; ; \tag{3}$$

$$P_2 = \frac{U_1 U_2' L_3' \, \delta_{21} \, (\pi - |\delta_{21}|) + U_2' U_3' L_1 \, \delta_{23} \, (\pi - |\delta_{23}|)}{2\pi^2 \, f_s (L_1 L_2' + L_1 L_3' + L_2' L_3')} \; ; \tag{4}$$

$$P_3 = \frac{U_1 U_3' L_2' \, \delta_{31} \, (\pi - |\delta_{31}|) + U_2' U_3' L_1 \, \delta_{32} \, (\pi - |\delta_{32}|)}{2\pi^2 \, f_s (L_1 L_2' + L_1 L_3' + L_2' L_3')} \; . \tag{5}$$

The $U_2'$ and $U_3'$ are the DC bus voltages of the active bridges connected to Port #2 and #3 respectively, concerning #1. Furthermore, $\delta_{jk}$ is the phase shift between the square wave voltage applied by the $k$-isium active bridge with respect to the $j$-isium one.

It can be noted that the power at the $k$-isium active bridge is the sum of two power contributions in which the $\Delta$ equivalent leakage inductances $L_{jk}$ can be identified, regarding their expression reported in (6). Therefore, a more effective approach to evaluate the TAB power distribution is to resort to the $\Delta$ equivalent circuit shown in Fig. 4b. Implementing the SPS modulation strategy between the $j$-isium and the $k$-isium ports, the power $P_{jk}$ is evaluated in (7), and the relationship between the power supplied by each active bridge on the $k$-isium port $P_k$ and the power transferred between each port of the $\Delta$ equivalent circuit $P_{jk}$ assumes the form given in (8) as a consequence of (3-5).

$$\begin{cases} L_{12} = & \dfrac{L_1 L_2' + L_1 L_3' + L_2' L_3'}{L_3'}; \\[2ex] L_{23} = & \dfrac{L_1 L_2' + L_1 L_3' + L_2' L_3'}{L_1}; \\[2ex] L_{31} = & \dfrac{L_1 L_2' + L_1 L_3' + L_2' L_3'}{L_2'}; \end{cases} \tag{6}$$

$$P_{jk} = \frac{U_j' U_k'}{2\,\pi^2 \, f_s \, L_{jk}} \delta_{jk} \, (\pi - |\delta_{jk}|) \, ; \tag{7}$$

$$\begin{cases} P_1 = & P_{12} - P_{31}; \\ P_2 = & P_{23} - P_{12}; \\ P_3 = & P_{31} - P_{23}. \end{cases} \tag{8}$$

The relationships between the phase shifts $\delta_{jk}$ described in (9) and the power relationship reported in (7-8) highlight the presence of cross-coupling effects, i.e. an unwanted power flow between Port #2 and #3. This requires the implementation of software or hardware decoupling solutions. A more specific discussion is presented in the following section.

In addition, the zero power flow circulation inside the TAB must be guaranteed to avoid power losses and maximise efficiency. This condition is achieved by satisfying the power balance given in (10) and (11).

$$\delta_{23} = \delta_{13} - \delta_{12} \tag{9}$$

$$P_{12} + P_{23} + P_{31} = 0 \tag{10}$$

$$\begin{cases} P_{12} = & -\frac{2}{3} \, P_2 - \frac{1}{3} \, P_3; \\[1ex] P_{23} = & -\frac{2}{3} \, P_3 - \frac{1}{3} \, P_1; \\[1ex] P_{31} = & -\frac{1}{3} \, P_2 - \frac{2}{3} \, P_1; \end{cases} \tag{11}$$

These relationships highlight the existence of constraints in the power flows between two of the TAB ports depending on the third one.

### *1) Inherent Decoupled Topology:*

The inherent cross-coupling power that flows between TAB ports is a key issue for this DC/DC converter class, and its settlement involves the hardware and control design. The technical literature proposed software and hardware solutions to overcome this issue. Essentially, the software solution are based on the TAB model and consists in synthesising decoupling algorithms by implementing inverse matrix compensators [26]. This class of decoupling algorithms is characterised by high computational efforts and centralised controller architectures. However, they achieve good performance in a wide operative range.

Another control strategy aimed at getting TAB decoupling is based on dynamic differentiation of implemented control loops by fixing different bandwidths. In particular, a specific control state variable is chosen as dominant, and its controller is synthesised to have the highest bandwidth for imposing the phase-shift evolution during transients [30]. This approach reduces the computation effort and allows a decentralised controller design.

Recently, a hardware approach, oriented to inherently decouple the power flow in a multi-active bridge converter, has been proposed [31]. This configuration has been deeply investigated because it seems suitable for developing an AEA power conditioning system powered by a single battery pack. The solution proposed consists of removing the external inductor in one port of the TAB that assumes the role of *"master"* port and designing the HFT and the leakage inductors on the other two sides properly. This hardware approach allows an inherent power decoupling between the TAB ports without additional components. This hardware configuration makes the TAB equivalent to two different separated DC/DC converters connected to the same power source – i.e. on the master port – and controlled independently. However, the control design requires particular attention due to the TAB asymmetrical characteristics and its non-linear behaviour.

A linearised model is proposed and analysed to evaluate the features of the inherent decoupled TAB topology. At this scope, the general formulation of the power provided to the $k$-isium port reported in (12) allows to evaluate the cycle-by-cycle average (CCA) TAB current $I_k$ under the hypothesis of constant voltage on the active bridges.

$$P_k = \sum\nolimits_{j\neq k} P_{kj} = \sum\nolimits_{j\neq k}^{3} \frac{U'_j U'_k}{2\,\pi^2\, f_s\, L_{kj}} \delta_{kj}\,(\pi - |\delta_{kj}|)\,; \quad k = 1,2,3. \tag{12}$$

$$I_k = \frac{P_k}{U_k} = \sum\nolimits_{j\neq k}^{3} \frac{U'_j}{2\,\pi^2\, f_s\, L_{kj}} \delta_{kj}\,(\pi - |\delta_{kj}|)\,; \quad k = 1,2,3. \tag{13}$$

The relationships (13) highlight that the current $I_k$ is related to the phase displacement (14) through a non-linear function $f(\delta_{kj})$. Therefore, a linearisation is proposed in (15) to simplify the modelling. The Fig. 5 reports the comparison between the $f(\delta_{jk})$ of both (14) and (15). It highlights that the linearisation can be performed by (15) but it limits $\delta_{kj}$ in a range between $\mp\pi/5$ since the linearised model makes an unacceptable error over the real one beyond this limits.

$$f(\delta_{kj}) = \delta_{kj}\,(\pi - |\delta_{kj}|) \qquad \forall \delta_{kj} \in \left[-\frac{\pi}{2}, \frac{\pi}{2}\right] \tag{14}$$

$$f(\delta_{kj}) \cong \frac{8}{\pi}\,\delta_{kj} \qquad \forall \delta_{kj} \in \left[-\frac{\pi}{5}, \frac{\pi}{5}\right] \tag{15}$$

Under these assumptions, the TAB model assumes the linear form reported in (16) where the terms $a_{rc} \neq 0$ (with $r, c = 1, 2, 3$) reported in (17) are constant. Again, the linearised TAB model clearly shows the presence of current cross-coupling phenomena.

Nevertheless, if the leakage inductance of one TAB port is equal to zero, the cross-coupling contributions disappear and the TAB model assumes a decoupled form. For instance, if the Port # 1 is set as master, the inductances $L_{jk}$ assume the values $L_{12} = L'_2$, $L_{23} = \infty$ and $L_{31} = L'_3$, respectively. As a consequence, the terms $a_{22}$ and $a_{32}$ become null. Therefore, the currents $I_2$ and $I_3$ depend only on the phase displacement between the master port and the respective port voltages. The current $I_1$ provided by the master port is the sum of the other two, as reported in (18). Moreover, the zero power circulation condition is always satisfied since $L_{23}$ assumes an infinite value.

$$\overline{I} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} a_{11} & 0 & a_{13} \\ a_{21} & a_{22} & 0 \\ 0 & a_{32} & a_{33} \end{bmatrix} \begin{bmatrix} \delta_{12} \\ \delta_{23} \\ \delta_{31} \end{bmatrix} \tag{16}$$

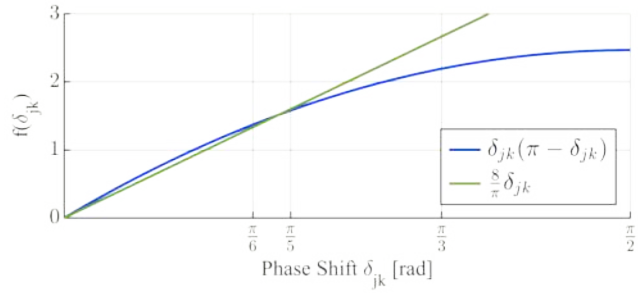

Fig. 5. $\delta_{kj}$ functions: TAB model and linearisation.

$$\begin{aligned} a_{11} &= \frac{4\,U'_2}{\pi^3\, f_s\, L_{12}} & a_{13} &= -\frac{4\,U'_3}{\pi^3\, f_s\, L_{13}} \\ a_{21} &= -\frac{4\,U_1}{\pi^3\, f_s\, L_{12}} & a_{22} &= \frac{4\,U'_3}{\pi^3\, f_s\, L_{23}} \\ a_{32} &= -\frac{4\,U'_2}{\pi^3\, f_s\, L_{23}} & a_{33} &= \frac{4\,U_1}{\pi^3\, f_s\, L_{13}} \end{aligned} \tag{17}$$

$$I_1 + I'_2 + I'_3 = 0 \tag{18}$$

*2) Effect of the Transformer Leakage Inductance:* The assumption that the leakage inductance on the master Port #1 is equal to zero is purely theoretical as the HFT always has a leakage flux which magnitude depends on the transformer design. Therefore, it is essential to analyse the effect of the inner HFT leakage inductance on the TAB master port to define the conditions in which the quasi-inherent decoupling occurs.

By fixing an equal rated output power on Port #2 and #3, the inductances $L'_2$ and $L'_3$ are set equal to $L$. In addition, the HFT leakage inductance magnitude in # 1 can be defined as a fraction "$\alpha$" of $L$. Hence, the relationships between the TAB leakage inductances assumes the form reported in (19)

$$\begin{aligned} L'_2 = L'_3 = L; \qquad & L_1 = \alpha\, L; \\ L_{12} = L_{31} = (2\,\alpha + 1)\, L; \qquad & L_{23} = \left(\frac{2\alpha + 1}{\alpha}\right) L. \end{aligned} \tag{19}$$

Since the TAB currents $I_k$ are related by (18), the linearised TAB model (16) can be rearranged to express the currents on Port #2 and #3 as a function of the corresponding phase displacement $\delta_{1k}$. Under this assumption, the TAB model achieves the formulation reported in (20)

$$\begin{bmatrix} I_2 \\ I_3 \end{bmatrix} = \frac{4\,U_1}{\pi^3\, f_s\, L} \frac{1 + M_{13}\alpha}{2\alpha + 1} \cdot \\ \cdot \begin{bmatrix} -1 & \dfrac{M_{13}\,\alpha}{1 + M_{13}\,\alpha} \\ \dfrac{M_{12}\,\alpha}{1 + M_{13}\,\alpha} & \dfrac{1 + M_{12}\,\alpha}{1 + M_{13}\,\alpha} \end{bmatrix} \begin{bmatrix} \delta_{12} \\ \delta_{31} \end{bmatrix}, \tag{20}$$

where $M_{12}$ and $M_{13}$ are the voltage ratios $U'_2/U_1$ and $U'_3/U_1$, representing the respective step-up or step-down operative condition if they are greater or less than one, respectively.

Under the assumption of $M_{1k} = M$, the (20) assumes the form (21)

$$\begin{bmatrix} I_2 \\ I_3 \end{bmatrix} = \frac{4\,U_1}{\pi^3\, f_s\, L} \frac{1 + M\alpha}{2\alpha + 1} \begin{bmatrix} -1 & D(M,\alpha) \\ D(M,\alpha) & 1 \end{bmatrix} \begin{bmatrix} \delta_{12} \\ \delta_{31} \end{bmatrix}$$
$$D(M,\alpha) = \frac{M\alpha}{1 + M\alpha}, \tag{21}$$

where $D(M,\alpha)$ represents the normalised cross-coupling weight. As much as $D$ is lower than one, such smaller is the coupling effect, allowing for assuming the currents $I'_2$ and $I'_3$ *"quasi-decoupled"* when $D$ is less than 0.05. Moreover, the evolution analysis of $D$ concerning $\alpha$ and $M$, shown in Fig. 6, highlights that the coupling effect presents small variations

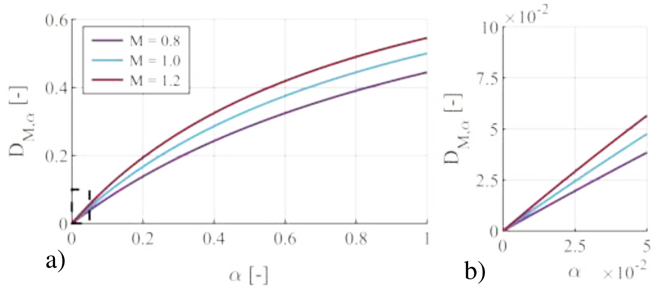

Fig. 6. a) Normalized cross coupling term $D$ evolution vs $\alpha$ parametrized for $M$ varing between 1.2 and 0.8; b) zoom of the quasi-inherent decoupling range.

alongside $M$ thus, for $\alpha$ less than 0.05, the coupling effects are considered negligible since $D$ varies less than 0.02. This result is particularly relevant in the proposed battery-based APU since the battery voltage – i.e. the voltage on the TAB master ports – varies, for example, along with the State of Charge (SoC).

## III. SELECTIVE HARMONIC ELIMINATION PULSE ACTIVE WIDTH MODULATION FOR A 5-LEVEL INVERTER

The SHE-PAWM of H-Bridge multilevel converters allows the selective suppression of specific harmonic components by resorting to an analytical methodology that achieves the defined target through the evaluation of unequal amplitude values of DC buses and equally spaced switching angles. The Fourier series expansion of the output phase voltage waveform of a multilevel Cascaded H-Bridges (CHB) converter, $U_{out}\left(\omega t\right)$, truncated to $2N-1$, is defined and reported in the following formula (22)

$$U_{out}\left(\omega t\right)=\sum_{k=1}^{N}H_{2k-1}\sin\left[\left(2k-1\right)\omega t\right] \tag{22}$$

where $H_{2k-1}$ is the amplitude of the harmonic of order $(2k-1)$. A five level CHB inverters is considered in this study, therefore $H_{2k-1}$ is expressed as (23)

$$H_{2k-1}=\frac{4}{\pi\left(2k-1\right)}\sum_{i=1}^{2}U_{(i+1)}\cos\left[\left(2k-1\right)\beta_i\right] \tag{23}$$

The adopted SHE-PAWM method assumes a sinusoidal waveform at fundamental frequency ($f=400\,Hz$) as the modulating signal (MS) and imposes the switching angles $\beta_1$ and $\beta_2$ as (24)

$$\beta_i=\frac{\left(2i-1\right)\pi}{10} \qquad i=1,2 \tag{24}$$

and the unequal dc voltage sources $U_{i+1}$, $i=1,2$ such that the obtained staircase output phase voltage intersects the MS in the midpoints between two consecutive switching angles, as shown in Fig. 7. Therefore, the values $U_{(i+1)}$, $i=1,2$ are given by (25) and (26)

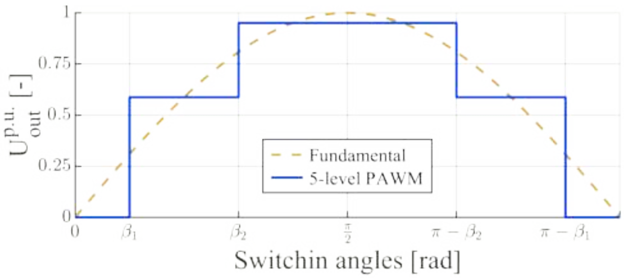

Fig. 7. Output voltage waveform $U_{out}$ for a 5-level inverter.

$$U_2=\hat{U}_{out}\sin\left(\frac{\beta_1+\beta_2}{2}\right) \tag{25}$$

$$U_3=\hat{U}_{out}\left[\sin\left(\frac{\beta_2+\frac{\pi}{2}}{2}\right)-\sin\left(\frac{\beta_1+\beta_2}{2}\right)\right] \tag{26}$$

where $\hat{U}_{out}$ is the peak value of the MS assumed to be equal to $1\,p.u.$ if the modulation index $m=1$.

The choices (24) of the switching angles and the voltage sources (25) and (26), guarantee that all harmonics of the output phase voltage disappear, except those of order $2lk\pm1$, where $l$ the number of levels and $k=1,\,2,\,\ldots$. In the case of a 5-level inverter, the output voltage harmonic analysis is shown in Fig. 8. The THD is evaluated resorting to (27) and, in the case of a 5-level inverter it assumes the value of 17%.

$$THD(\%)=\frac{\sqrt{\sum_{j=3,5,\ldots}^{49}H_j^2}}{H_1}100 \tag{27}$$

## IV. DESIGN OF THE PROPOSED DC/AC CONVERTER

The design of the proposed converter has been developed, referring to specific targets: output voltage of 115V$_{\mathrm{rms}}$ and 400Hz for a rated power of 5kW. The design has been developed according to an energy-balancing approach. Therefore, the starting point is represented by the instantaneous power evolution on the AC load when the rated condition occurs. For this specific application, a pure resistive load has been considered. Under these assumptions, the evolutions of the DC current and power expected by each H-bridge composing

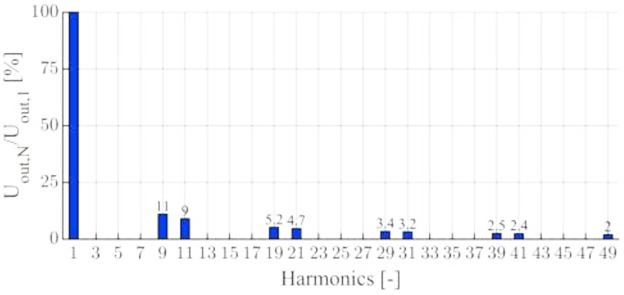

Fig. 8. Harmonic analysis in a 5-level CHB inverter.

the 5-LCHB converter have been evaluated. Specifically, the peak power provided by each DC bus has been determined.

Therefore, the DC-link voltages on the multilevel H-bridges for achieving the target amplitude output voltage can be determined by referring to the model presented in Section III. To accomplish an RMS first harmonic output voltage at $115\text{V}_{\text{rms}}$, the DC busses must be set equal to $96\text{V}_{\text{DC}}$ and $59\text{V}_{\text{DC}}$, respectively. The instantaneous peak power requested by the AC power system at the rated condition is 10kVA, and under the DC bus voltage conditions, is shared between the two H-Bridges with a rate of 40% on the H-Bridge with the lower DC bus voltage and 60% on the higher one, according to the DC bus voltage setting. Therefore, by setting at $100\text{V}_{\text{DC}}$ the input DC bus voltage $U_1$, the turn ratios of HFT $N_1/N_2$ and $N_1/N_3$ can be fixed at 1 and 2, respectively. This choice allows to define the TAB converter gains $M_{1k}$ as reported in (28). The constraints imposed by the achievement of TAB zero voltage switching and the definition of the TAB switching frequency $f_s$, selected at 20kHz, allow for evaluating the leakage inductances through (29)

$$M_{12} = \frac{U_2'}{U_1} \;\; M_{13} = \frac{U_3'}{U_1} \tag{28}$$

$$L_{1k} = \frac{U_1^2\, M_{1k}}{2\, f_s\, P_{1k}}\, \delta_{1k}^{pu}|_{max} \left(1 - \delta_{1k}^{pu}|_{max}\right) \;\; k = 2, 3; \tag{29}$$

where $\delta_{1k}^{pu}$ is equal to $\delta_{1k}/\pi$. In particular, the definition of the TAB leakage inductances has been developed, imposing $L_1$ equal to zero and evaluating the $L_2'$ and $L_3'$ according to the current stress optimization approach. It allows the identification of $\delta_{1k}^{pu}|_{max}$ that minimises the peak currents occurring on each inductor considering the power previously evaluated. In the case under investigation, an upper bound $\delta_{1k}^{pu}$ equal to 0.2 – i.e. $\pi/5$, see (15) – has been fixed [36].

The outcomes of the inductors design are $L_2$ and $L_3$ equal to 6.3$\mu$H and 3$\mu$H, respectively.

The capacitors have been sized referring to the relation (30). In particular, a voltage variation of $\pm 3\%$ on the capacitor at the lower voltage i.e. under higher stress, has been considered. Therefore, the outcome of (30) is 6mF for both the capacitors $C_2$ and $C_3$.

$$\begin{gathered} i_k^{CAP} = i_k^{TAB} - i_k^{L} \quad k = 2, 3; \\ C_k\, \frac{dU_k}{dt} = \frac{U_1}{2\, fs\, L_k} \delta_{1k}^{pu} \left(1 - \delta_{1k}^{pu}\right) - \frac{p_k}{U_k} \end{gathered} \tag{30}$$

Regarding the battery pack designed to supply the AEA auxiliary systems, the LiB Kokam SLPB100216216H cells have been considered since they are characterised by a very high power rate, making them suitable for achieving the high peak power required in this specific application (see Table I). The auxiliary battery pack has been designed referring to the flight path and duration to provide the required energy at a DC-rated voltage of $100\text{V}_{\text{DC}}$. Hence, a 27s2p battery pack i.e. characterised by two parallel modules composed of 27 cells connected in series, has been sized, achieving a rated capacity of 80 Ah.

TABLE I
LiB Kokam SLPB100216216H cell specifications.

| | |
|---|---|
| **Rated Capacity** | 40Ah |
| **Maximum Disch. Current** | 320A (8C) |
| **Maximum Charge Current** | 120A (3C) |
| **Maximum Voltage** | 4.0V |
| **Rated Voltage** | 3.7V |
| **Minimum Voltage** | 3.2V |
| **Weight** | 940g |
| **Volume** | 0.53L |

### A. Control System

The TAB control algorithm is distinguished by two distinctive phases: an initial start-up stage and a subsequent voltage regulation stage. The former is imperative in order to successfully manage the occurrence of high inrush currents. This is accomplished when the TAB is switched on for the purpose of charging the output capacitors, which subsequently leads to the modulation of the bridges.

To implement the SPS, each bridge is modulated using a Carrier-Based PWM (CB-PWM). The duty-cycles of the output voltages $u_2$ and $u_3$ are fixed at 50% according to the SPS control strategy, while the one of the input voltage $u_1$, namely $\tau$, is controlled during start-up as shown in Fig. 9. In particular, $\tau$ starts at a sufficiently low value to keep the initial current low; it then rises with a chosen slew rate to avoid inrush currents at $C_2$ and $C_3$; when $\tau$ reaches 50% and the output voltages achieve 70% of the set-points $U_{2,set}$ and $U_{3,set}$, the voltage loop controllers are activated. Two independent PI regulators control the TAB output voltages $U_2$ and $U_3$. The PIs output the phase shift value $\delta_{1k}$ by which the CB-PWM of $u_2$ and $u_3$ are shifted with respect to $u_1$.

Considering the implementation of the inherent decoupled configuration, the synthesis of the PI regulators have been performed by referring to the linear modelling, as reported in Fig. 10. It consists of the PI controller, the TAB model, deduced from the equations (16) and (17), and the output impedance of the DC-link capacitors. The voltage control target has to ensure both a defined and constant voltage on the DC-link and the load current supply, modelled as a disturbance to be fully rejected. Referring to the model reported in (31), the PI synthesis started from Port #2, in which $96\text{V}_{\text{DC}}$ is set and the 60% of the power load is absorbed.

$$PI(s) = K_p\, \frac{s + T^{-1}}{s}, \;\; T = \frac{K_p}{K_i}. \tag{31}$$

The load current on each DC side is a rectified signal at 800Hz. As a consequence, a significant disturbance current rejection at this frequency is required. For this purpose, the time constant $T$ of the PI has been set for achieving a zero placement at a frequency sufficiently lower that the current disturbance one. The $K_p$ has been chosen in order to achieve a bandwidth of the voltage closed-loop system at least 20 times lower than the frequency of current disturbance. This assumption avoids the interaction between the two control action. Hence, the time constant $T$ has been set at 0.01s for assuring an effective starting rejection by $100\,rd/s$. The

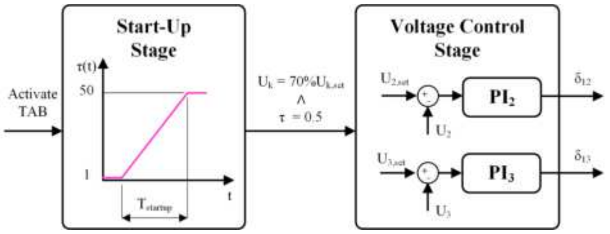

Fig. 9. Control strategy of the TAB.

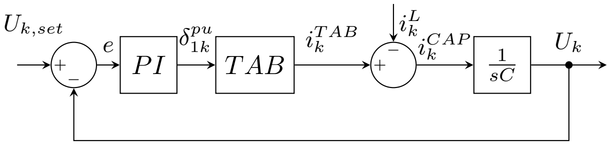

Fig. 10. Block diagram of voltage control system of one TAB output.

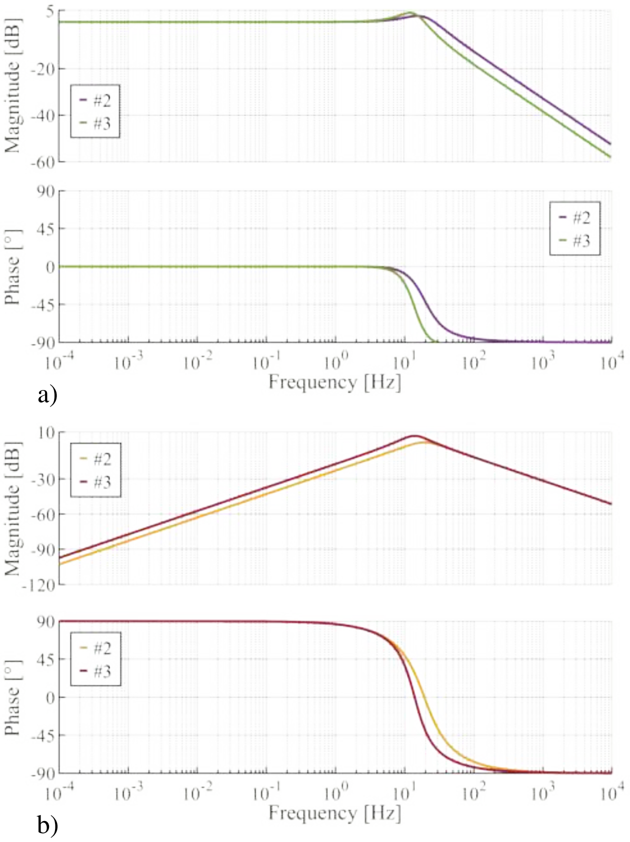

Fig. 11. a) Bode plot of the Port #2 and #3 closed-loop system; b) Bode plot of the Port #2 and #3 disturbance rejection ability.

proportional coefficient $K_p$ is evaluated for achieving voltage bandwidth of 40Hz and ensuring a disturbance current rejection of -20dB at at 800Hz. The PI synthesis of Port #3 has been performed to keep the same controller time constant $T$, i.e. 0.01s. Fig. 11 shows the bode plots of both the closed-loop control and the disturbance rejection of Port #2 and #3, demonstrating the expected performances to be achieved, and Table II summarises the resulting synthesised PI parameters.

TABLE II
PARAMETERS OF THE PI VOLTAGE REGULATORS

| | **Output 1:1** | **Output 1:0.5** | |
|---|---|---|---|
| $K_p$ | $8.6 \cdot 10^{-3}$ | $4.3 \cdot 10^{-3}$ | rd/V |
| $K_i$ | $860 \cdot 10^{-3}$ | $430 \cdot 10^{-3}$ | rd/Vs |

## B. Design Simulation results

To verify the achievement of design targets, the proposed DC/AC power converter has been co-simulated on PLECS and Matlab/Simulink imposing a load step variation from zero to the rated output power of 5kW. The control algorithm has been implemented in Matlab/Simulink, employing as feedback signals the voltage sampled at 20 kHz on the converter model developed in PLECS. The simulation results reported from Fig. 12 to Fig. 14 confirm the achievement of the design target. Specifically, Fig. 12a shows the steady state output AC voltage and current evolutions provided by the 5-LCHB converter when a load resistance of 2.64Ω, corresponding to the output rated power, is imposed. The output voltage is affected by a variation about 3% when the peak value is achieved. As a result, the voltage Fast Fourier Transformation (FFT), shown in Fig. 12b, highlights the presence of some harmonics that are theoretically cancelled by the SHE-PAWM. The voltage THD is 17.75%, higher than the theoretical value of just 0.75%. This enables to consider the results obtained in accordance with the objectives that were set. The time evolutions of TAB voltages and currents in steady-state at rated power are reported in Fig. 13a and Fig. 13b, respectively. As expected, the peak values of the TAB currents assume significant amplitude achieving a peak value of around 100A. The Fig. 14 reports the DC voltages on TAB during a step-load application. The result confirms the performance of voltage regulators in the presence of such significant load variation.

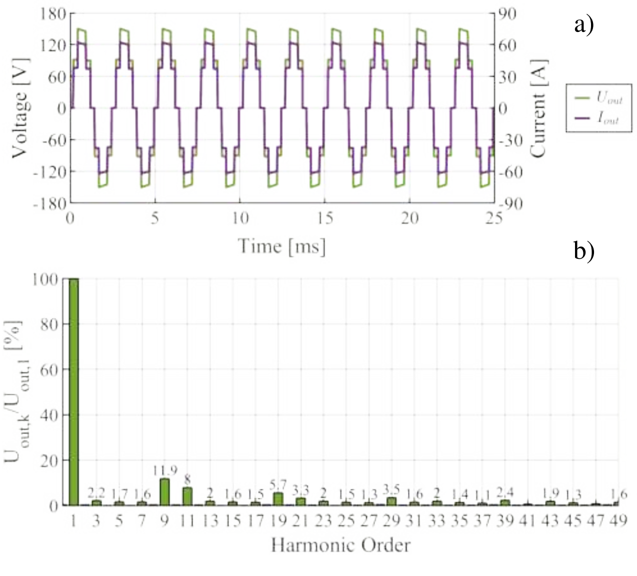

Fig. 12. a) Voltage and current evolution of the 5-LCHB converter output; b) FFT analysis of the 5-LCHB simulated voltage.

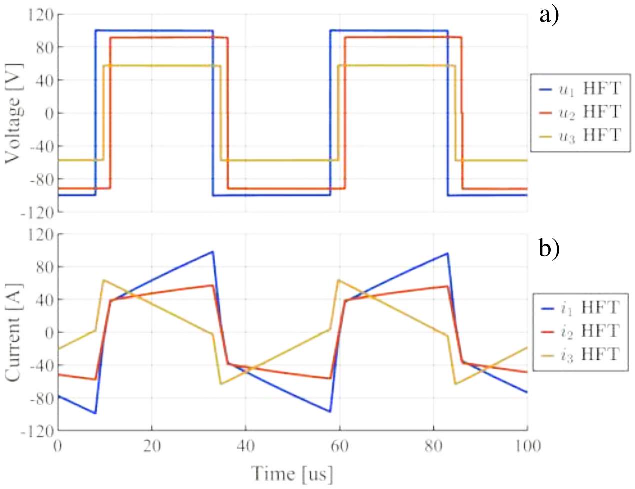

Fig. 13. Steady state TAB voltage (a) and current (b) evolutions: on primary HFT winding (Blu trace), on secondary HFT 1:1 (red trace), on secondary HFT 1:0.5 (yellow trace).

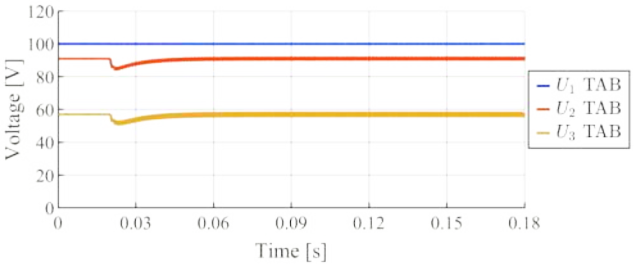

Fig. 14. Transient evolution of DC-link voltages during step-load variation from zero to 5kW: $U_1$ blu trace, $U_2$ red trace, $U_3$ yellow trace.

## V. EXPERIMENTAL VALIDATION

The proposed DC/AC conversion system is validated concerning a scaled laboratory prototype. The experimental test during start up is shown and discussed. Moreover, the voltage control system of the TAB has been tested under a step load variation from 300W and 600W. The experimental tests are compared with the co-simulation study performed resorting to the design simulation tool, thus validating the working principle of the proposed DC/AC convertion system.

### A. Laboratory Prototype

The laboratory prototype is shown in Fig. 15. The component (#1) is the Power Supply Elektro-Automatic 10750-120 4U, which can supply up to 30kW and feeds the TAB input. The TAB converter is the component (#2) and consists of six Imperix PEB 8024 half bridges equipped with Silicon Carbide (SiC) MOSFETs whose characteristics are given in Tables III and IV, respectively. The TAB magnetic tank consists of a 3W-HFT and the external leakage inductors. The 3W-HFT is manufactured by SIRIO s.r.l. and its main characteristics are shown in Table V. The leakage inductances $L_2$ and $L_3$ are 100$\mu$H and 50$\mu$H respectively, as shown in Table V. In particular, $L_2$ consists of two modular inductors of 50$uH$ and a maximum current of 20A connected in series, and $L_3$ consists of a series of two 25$\mu$H inductors of 40A, all manufactured by Payton Planar. Since the internal leakage inductance of the transformer is 4.1$\mu$H, the $\alpha$ parameter assumes a value of 0.041 for both ports. Therefore, the TAB outputs are able to be inherently decoupled depending on the value of $M_{12}$ and $M_{13}$. The 5-level inverter is the component (#3) equipped with four IGBT Imperix PEB 8032 half bridges, whose main characteristics are listed in the Table VI. Component (#4) is the load connected to the output of the 5-level inverter, while components (#5), (#6) and (#7) are the converter controllers Imperix B-Box, the oscilloscope Yokoghawa DLM5058HD for acquiring measurements, and finally the PC from which the controller code is compiled.

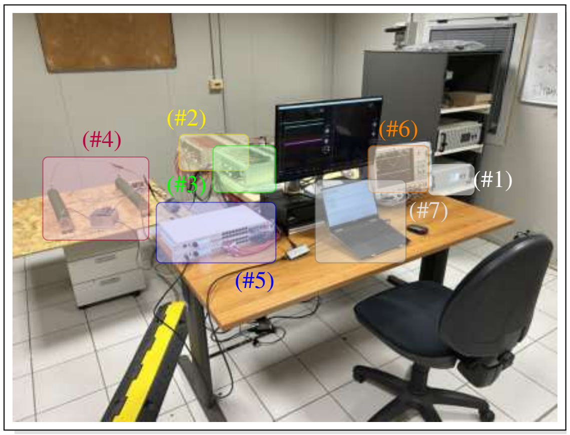

Fig. 15. Proposed laboratory prototype DC/AC converter: 1) DC power supply EA PS 10750-120 4U 30kW; 2) Triple-active bridge prototype; 3) Five-level cascaded H-bridge prototype; 4) Load; 5) Imperix B-Box controller; 6) Oscilloscope Yokoghawa DLM5058HD; 7) PC for code development and compilation.

TABLE III
TRIPLE-ACTIVE BRIDGE MODULES DATASHEET

| | | | |
|---|---|---|---|
| **DC Bus voltage** | $V_{DC}$ | 800 | $V$ |
| **Maximum continuous current** | $I_{DC}^{max}$ | 24 | $A_{RMS}$ |
| **Maximum pulsed current** | $I_{DC}^{pulsed}$ | 80 | $A$ |
| **reference switching frequency** | $f_{sw}$ | 20 | $kHz$ |
| **DC side bus capacitance** | $C_{DC}$ | 260 | $\mu F$ |

TABLE IV
SIC MOSFET C2M0080120D DATASHEET

| | | | |
|---|---|---|---|
| **Drain-Source Voltage** | $V_{ds}$ | 1200 | $V$ |
| **Continuous Drain Current** | $I_D$ | 24 | $A$ |
| **Power Dissipation** | $P_{ToT}$ | 192 | $W$ |
| **Reference switching frequency** | $f_{sw}$ | 20 | $kHz$ |
| **Drain-Source On-State Resistance** | $R_{ds}^{on}$ | 128 | $m\Omega$ |
| **Turn-On Switching Energy** | $E_{on}^{sw}$ | 265 | $\mu J$ |
| **Turn-Off Switching Energy** | $E_{off}^{sw}$ | 135 | $\mu J$ |

### B. Experimental Results

The test campaign is performed considering the APU battery pack set at 100V$_{\mathrm{DC}}$ on the TAB input. The TAB output

TABLE V
SIRIO 3W-HFT TRANSFORMER PARAMETERS

| | | | |
|---|---|---|---|
| **Transformer voltage ratio** | $n$ | $1:1:0,5$ | |
| **Rated switching frequency** | $f$ | 20 | $kHz$ |
| **Short circuit inductance** | $L_\sigma$ | 4.1 | $\mu H$ |
| **External leakage inductance 1:1** | $L_2$ | 100 | $\mu H$ |
| **External leakage inductance 1:0.5** | $L_3$ | 25 | $\mu H$ |
| **Magnetization inductance** | $L_m$ | 1700 | $\mu H$ |

TABLE VI
MULTILEVEL CONVERTER MODULES DATASHEET

| | | | |
|---|---|---|---|
| **DC Bus voltage** | $V_{DC}$ | 800 | $V$ |
| **Maximum continuous current** | $I_{DC}^{max}$ | 32 | $A_{RMS}$ |
| **Reference switching frequency** | $f_{sw}$ | 10 | $kHz$ |
| **DC side bus capacitance** | $C_{DC}$ | 260 | $\mu F$ |

voltages are set in compliance with the SHE-PAWM voltage levels for achieving a $115\mathrm{V_{rms}}$. Particularly, the voltages of Port #2 and #3 are set to $96\mathrm{V_{DC}}$ and $59\mathrm{V_{DC}}$, respectively. The $96\mathrm{V_{DC}}$ output feed the 5-LCHB lower level, while the $59\mathrm{V_{DC}}$ output feeds the converter higher level setting the TAB voltage gains $M_{12}$ and $M_{13}$ to 0.96 and 1.18, respectively, which satisfy the inherent decoupling condition between the output ports of the TAB. It is also assumed that the PI gains are the same as those given in Table II.

The Fig. 16 reports the main signals of the TAB during the converter startup. The jagged envelope of the HFT input current signal (the cyan curve) is due to an aliasing effect. The first part is the startup stage, in which a peak current of 5A is recorded. The voltage controls are activated at the end of the startup and set the output voltages. In this stage, the current achieves a peak value of 2.5A. Thus, the effectiveness of the startup stage in mitigating the inrush currents of the TAB is confirmed. The SHE-PAWM is activated after the TAB has been fully powered up, taking into account an initial load of 300W. In this condition, the TAB operates with phase shifts $\delta_{12}^{pu}$ and $\delta_{13}^{pu}$ equal to 0.084 and 0.036 respectively, where $\delta_{1k}^{pu}$ is equal to $\delta_{1k}/\pi$. A step load variation to 600W is then performed to test the stability of the voltage controllers. Figs. 17a,b shows the result of the test. It demonstrates good stability and fast voltage dynamics, reaching steady state in 0.035s, as expected by the PI controller design. In particular, Fig. 17e focuses on the dashed square of Fig. 17a, showing a good mitigation of the voltage dynamics of the TAB controllers. At 600W, $\delta_{12}^{pu}$ and $\delta_{13}^{pu}$ are equal to 0.20 and 0.070 respectively, where $\delta_{12}^{pu}$ is on the edge of the linearity limit defined in (15). The co-simulation study using the simulation tool of Section IV is performed and the results are shown in Figs. 17c,d and f. They highlight a good agreement with the experimental ones, validating the converter modelling of the simulation tool.

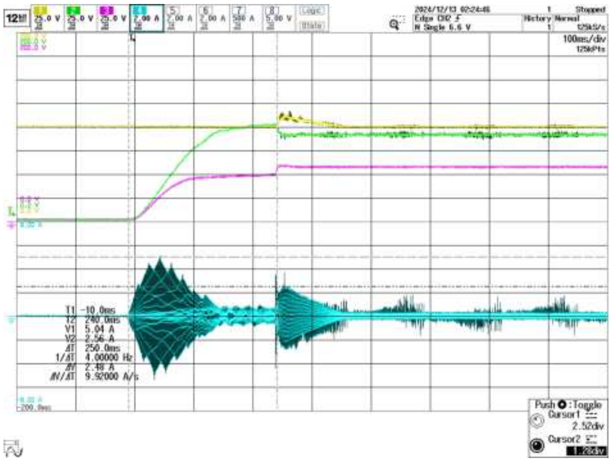

Fig. 16. Triple-Active Bridge converter startup: input voltage (yellow); output voltage $U_2$ (green); output voltage $U_3$ (purple) and HFT input current $i_1$ (cyan).

Fig. 18 shows the 600W steady state current and voltage evolutions of both the DC/AC converter input and output sides. Fig. 19 shows the comparison with the simulation results, demonstrating a good overlapping. Finally, Fig. 20 shows the FFT of the experimental voltage, confirming the achievement of the objective set by the SHE-PAWM, achieving a THD value of 17.19%. In fact, only the $10k \pm 1$ harmonics components are present in the spectrum, making the THD very close to the expected theoretical value.

## VI. CONCLUSION

This paper proposes a design methodology for a novel 5kW, $115\mathrm{V_{rms}}$, 400Hz DC/AC topology for an AEA Auxiliary Power Unit (APU). Particulary, an inherent decoupled Triple-Active Bridge (TAB) converter feeds the 5-level cascaded H-bridge converter (5-LCHB) from a single battery unit. The 5-LCHB is modulated according to the Selective Harmonic Elimination Pulse Active Width Modulation (SHE-PAWM) approach to mitigate the output voltage harmonic content. The design outcome is validated on a scaled laboratory prototype. The experimental tests demonstrate a good performance in terms of converter dynamics, even during step load variations, and the expected harmonic content mitigation due to the SHE-PAWM. In addition, the experimental results validate a co-simulation study performed on PLECS and Matlab/Simulink, which shows a good overlap with the experimental results. The outcomes confirm the value of the proposed topology and the trustworthiness of the developed co-simulation tool.

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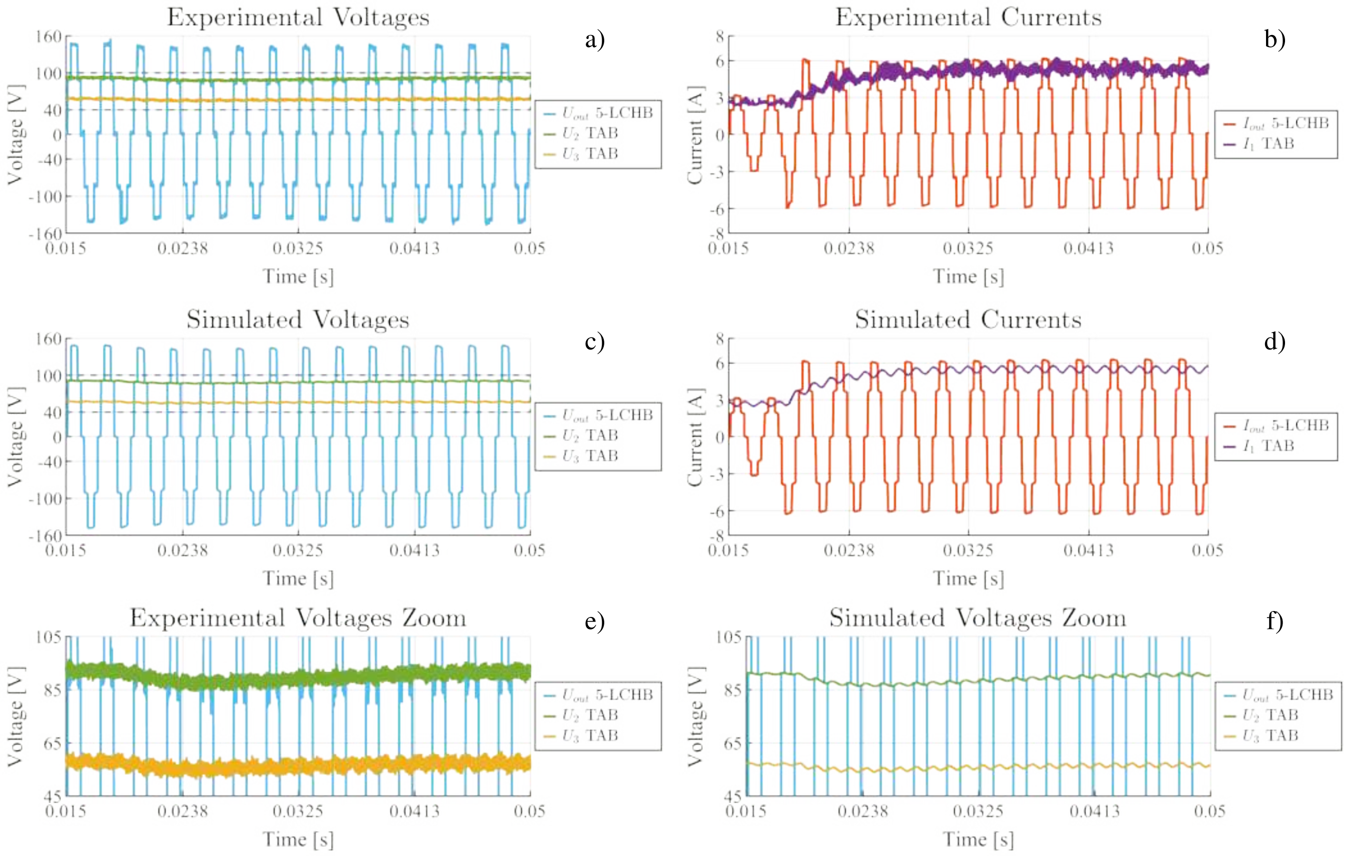

Fig. 17. Comparison between co-simulation and experimental results during a load step from 300W to 600W: a) and b) are the experimental voltages and currents; c) and d) are the simulated voltages and currents; e) and f) are the zoom of the experimental and simulated voltages, highlighting the dynamic response of the TAB output voltage controls.

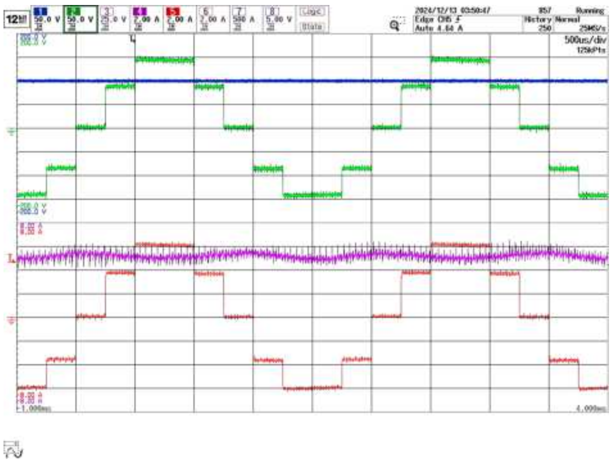

Fig. 18. DC/AC converter input and output evolutions: input voltage (blue); output voltage (green); input current (purple) and output current (red).

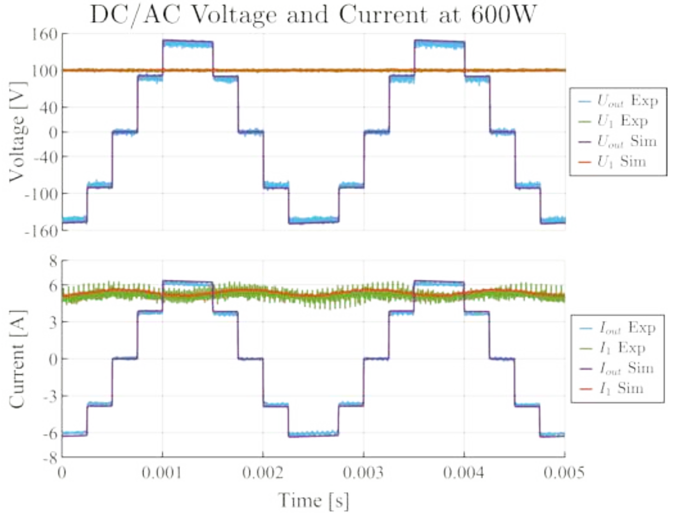

Fig. 19. Comparison between the co-simulation and experimental results of the DC/AC converter input and output signals.

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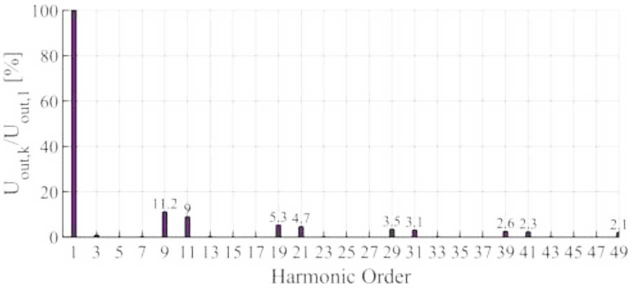

Fig. 20. FFT analysis of the 5-LCHB experimental voltage.

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