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Research article

A novel artificial neural network based selection harmonic reduction technique for single source fed high gain switched capacitor coupled multilevel inverter for renewable energy applications

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ABSTRACT

Multilevel inverters (MLIs) are commonly used in renewable energy systems for their high-quality output, low total harmonic distortion (THD), and reduced component count. This study presents a high-gain, single-source MLI designed for renewable applications like solar or wind power. It features a novel topology with twice the voltage-boosting factor, utilizing a single DC source. The inverter achieves thirteen voltage levels using just 10 power switches and three switched capacitors. The voltage gain is achieved without the need for bulky DC-DC converters or transformers. This is accomplished by configuring the switched capacitors in series and parallel arrangements to attain the desired voltage boost. Additionally, the self-balancing capacitors eliminate the need for extra sensors. Both symmetric and asymmetric variants of the extensible configuration are investigated. The suggested design lowers the total standing voltage (TSV) while achieving high gain. A selective harmonic removal technique using artificial neural networks (ANN) reduces THD by up to 6.07 %. An extensive review of recent literature reveals significant advancements and applications of ANNs in this field. The proposed system's benefits, such as gain factor, total standing voltage (TSV), and minimized device count, are assessed. Comparative analysis reveals that the proposed topology employs fewer components and features a more simplified design. Additionally, the inverter achieves an efficiency of 96.9 %. The design is validated through an experimental prototype after being confirmed with MATLAB/SIMULINK.© YEAR The Authors. Published by Elsevier Ltd.

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1. Introduction

The multilevel inverter (MLI) is highly advantageous for medium and high-voltage applications due to its modular design, low dv/

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dt, and superior efficiency, which leads to near-sinusoidal output voltage waveforms and minimized harmonic distortion. Traditional MLI topologies, such as Diode Clamped Inverter (DCI), Flying Capacitor (FC), and Cascaded H-Bridge (CHB), each have distinct challenges: DCI involves a high number of diodes and complex power flow regulation; FC struggles with intricate voltage regulation and larger size; CHB requires multiple isolated DC sources to achieve reduced total harmonic distortion (THD). MLIs are further divided into symmetric and asymmetric configurations based on the use of isolated DC sources examining these conventional approaches and proposing enhancements to improve MLI performance for medium and high-voltage applications [1]. In symmetric MLI topologies, higher output voltage levels require multiple input DC sources of equal amplitude. In contrast, asymmetric MLIs achieve higher levels with fewer input sources of varying magnitudes, which reduces the need for numerous isolated DC source, which is a common limitation in traditional inverter designs. As MLIs with a single DC input become more common, especially for renewable energy applications, there is a growing emphasis on minimizing device count and reducing the number of isolated DC sources [2]. To address this, switched capacitor-based MLIs (SCMLIs) utilize capacitors to replace multiple DC sources, enabling the delivery of various output voltage levels through charging and discharging from the single input supply [2,3].

The 13-level Cascaded H-Bridge (CHB) High-Frequency AC (HFAC) power distribution system with two modified structures: $3 \times 2V_{dc}$ and $2 \times 3V_{dc}$. The $3 \times 2V_{dc}$ design requires more diodes and capacitors than the $2 \times 3V_{dc}$ but reduces device count compared to conventional CHB systems, though it increases size and cost has been discussed [3]. Later, The 11-level switched capacitor-based inverter with fewer components and a detailed power loss analysis has been made [4]. The developed single-phase CHB inverter achieving 11 levels with three capacitors but requires two power sources and H-bridges, increasing TSV and cost. A customizable design with a full power loss analysis has also been discussed. Though it has merit of reduced device count it demands two input power sources and two h-bridges for polarity reversal which will increases the TSV and cost of the inverter [5]. Later, single-input MLI with two capacitors, generating 9 levels with only 7 switches but needing extra sensors and control algorithms for voltage management [6].

The nine-level PUC converter with fewer components but lacks voltage boosting capability. The voltage boosting facility, however, is not accessible [7]. A cascaded inverter with minimal devices that can generate the desired number of levels by connecting additional DC sources. However, polarity reversal needs an H-bridge, which increases voltage stress across the switches [8]. Nine-level single sourced MLI with twice boosting factor is proposed in Ref. [9]. Though it has an intrinsic topology for polarity reversal, it lags behind in device optimization when voltage levels are increased. Similarly, another 9-level inverter with twice the output voltage gain with dual input source is presented in Ref. [10]. Though it requires lesser number of capacitors the number of input sources seems higher.

A dual sourced 13-level inverter with 1.5 times boosting gain is presented in Ref. [11]. As the topology has both the symmetric and asymmetric configuration, the symmetric configuration requires 13 switches to generate 13 levels of output voltage. A crisscross capacitor unit (CCU) MLI with single input source has been described in Ref. [12]. It has the merit of high gain factor but requires very high number of switching devices for generating 13-levels. The solar application based 13-level inverter with only nine switches has been discussed but it requires two different voltage sources and four capacitors for the required levels, utilized ANN-based Selective Harmonic Elimination (SHE) techniques in cascaded MLIs, achieving significant reductions in harmonic distortion compared to conventional methods. This study highlights ANN's potential for fine-tuning harmonic profiles effectively [13,14]. The purpose of the paper is to explore the values of these parameters using a multi-objective optimization approach to simultaneously optimize both η and EMI. To achieve this, the impact of high and low sides on EMI in the half-bridge configuration is first examined [15]. Various, three-phase non-isolated inverter topologies based on neutral point clamping, utilizing a modified discontinuous pulse width modulation technique. The study focuses on their effects on common-mode voltage (CMV), LC filter size reduction, current total harmonic distortion (THD), conduction losses, and overall efficiency of the inverter structures [16,17].

A nine-level inverter that achieves double the voltage gain while maintaining a Total Harmonic Distortion (THD) of 9.35 % [19]. They developed an innovative Selective Harmonic Elimination (SHE) technique for this inverter, which significantly enhances harmonic reduction and optimizes overall performance. Extended, nine-level single-sourced MLI with a voltage-boosting factor of two and intrinsic polarity reversal. However, the design does not optimize for higher voltage levels [18]. The study also investigated integrating Artificial Neural Networks (ANN) with Model Predictive Control (MPC), enhancing dynamic performance but requiring significant computational resources. The switched capacitor topologies, achieving a 13-level configuration with symmetric topology, but necessitating multiple DC sources. They compared traditional modulation techniques with Artificial Neural Network (ANN)-based approaches, demonstrating significant enhancements in Total Harmonic Distortion (THD) and control precision with the ANN-based methods [21]. The Phase Disposition PWM strategy for seven-level inverters, noting the need for more devices to increase levels [20]. The single-sourced 13-level K-type inverter with 1.5x voltage gain and 13-level inverter with four switched capacitors, offering two fewer switches and three times the voltage gain compared to Ref. [22]. A sextuple gain with 13 levels, requiring different capacitor and device ratings. Later, single-sourced double-wing T-type model with a half-bridge unit, which generates 13 levels with a threefold boosting factor using fourteen switches and four capacitors [24,25]. A similar boosting topology but with two fewer switches and one fewer capacitor, utilizing the nearest level control technique to achieve high gain and a level-shifted multicarrier PWM method for achieving 13 voltage levels with three capacitors and thirteen switches to get maximum output [26,27]. This approach requires four switches rated for twice the input supply's peak inverse voltage and two capacitors with different ratings. Their comparative analysis of ANN-based MLI topologies highlighted the benefits of ANN in reducing component count and improving performance. Although ANNs enhance MLI performance, they can be complex and computationally demanding. This paper introduces an ANN-based Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) technique that balances harmonic reduction, voltage control, and implementation complexity for high-gain, single-source MLI [24,27].

Later the MLI proposed with encounters complexity and increased cost due to the extensive number of capacitors and switches required for their 13-level inverter design [28]. The face implementation challenges stemming from the complex control algorithms needed to achieve reduced harmonics and fewer switching devices [29]. The computational complexity with their APSO-GA-based

selective harmonic elimination, which may hinder real-time processing. MLI has been grapple with high costs and intricate switching strategies associated with their step-up switched-capacitor inverter. This proposed APSO-GA technique addresses the voltage balancing and efficiency concerns despite their efforts to minimize switch count and driver components [30–32]. This technique experience difficulties related to control complexity and the precise matching of components in their hybrid T-Type inverter, affecting practical implementation and performance [33].

The paper proposes multilevel inverter with high efficiency but requires complex control algorithms and multiple DC sources [34]. Later the MLI design proposed to achieve high efficiency but struggles with challenges related to capacitor voltage balancing and thermal management. While this topology, effectively reduces harmonic distortion, it relies on additional components and complex switching strategies, which can complicate the design and increase the overall cost of the inverter system [35,36]. The high efficient MLI developed to improve the overall system performances but suffers from high switching losses due to the intricate arrangement of switches. This complexity can lead to increased heat generation and reduced overall system efficiency [37]. The inverter design has been developed with sophisticated control mechanisms that may not be practical for all applications, particularly in systems where ease of implementation and lower costs are prioritized. This paper presents a novel five-level common ground type (CGT) inverter utilizing switched capacitors (SCs) with dual voltage boosting. The proposed design lowers capacitor voltage ratings, enhancing power density and reliability while incorporating self-voltage balancing and sensorless operation [38,39].

The following are the unique characteristics of the proposed 13-level SC based MLI.

1. Only 10 switches and three capacitors are required.
2. All the switches, with the exception of two, have peak inverse voltages within the magnitude of the input dc source voltage.
3. As capacitor voltages are self-balancing, no extra sensors or devices are needed.
4. Includes inherent polarity reversal capability.
5. Only four out of ten switches conduct in each state, resulting in lesser switching losses.
6. The ANN-based SHEPWM technique significantly reduces THD, optimizes switching operations, increases overall system efficiency, and adapts to varying load conditions for consistent performance.

The study introduces the basic (PB) 13-level inverter circuit, detailing its different operating modes and calculations for total

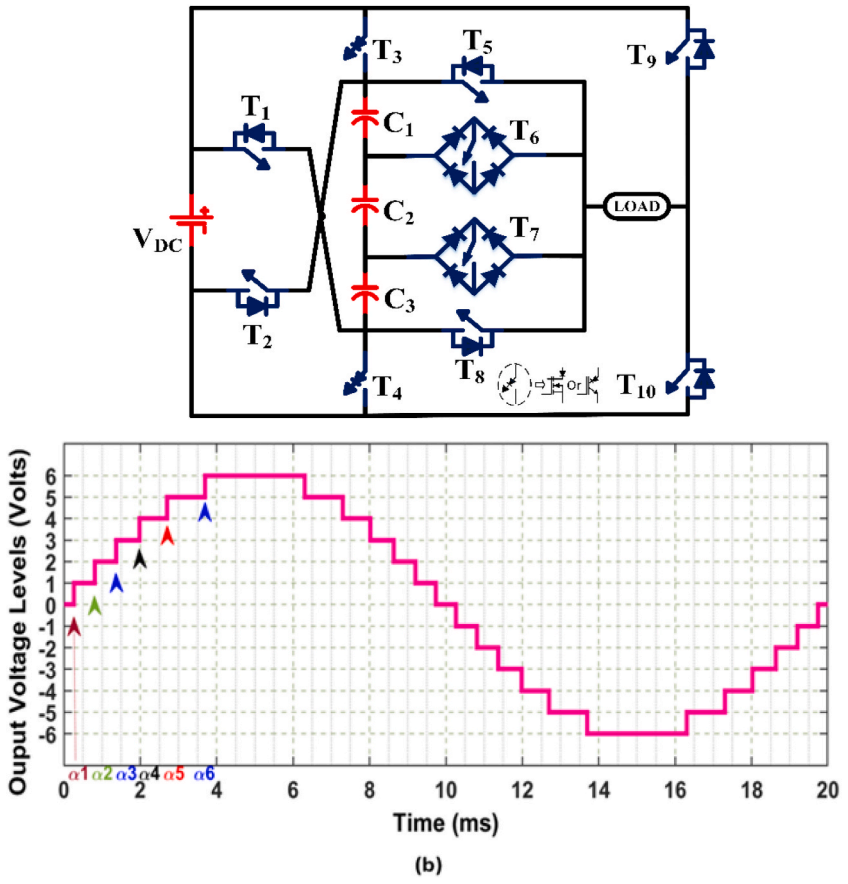


Fig. 1. (a) Circuit diagram of the PB 13-level inverter.Fig. 1(b) Output voltage levels with firing angle (α).

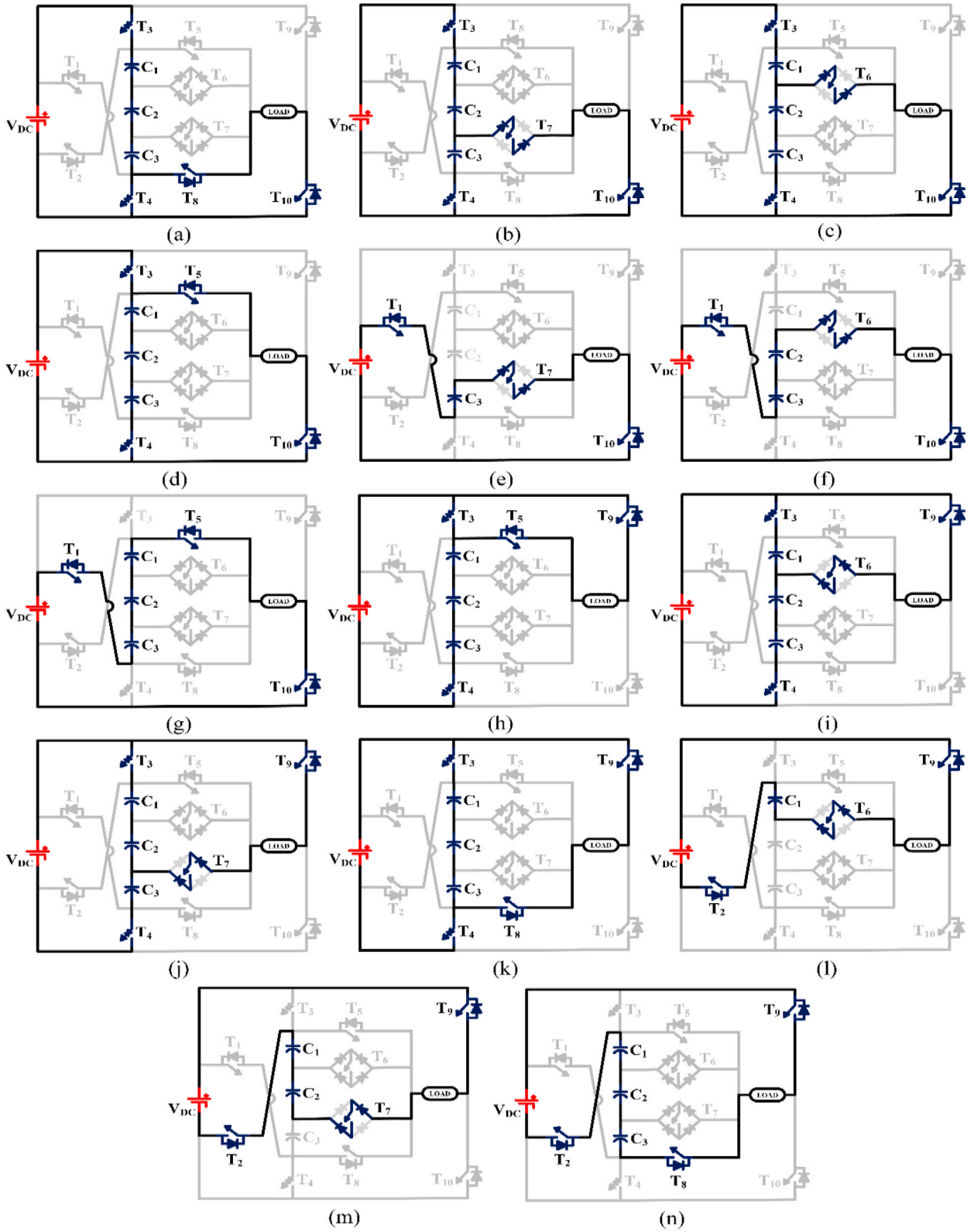


Fig. 2. Modes and output voltage levels of the proposed 13L inverter (a) 0 (b) + $V_{DC}/3$ (c) $+2V_{DC}/3$ (d) + V_{DC} (e) $+4V_{DC}/3$ (f) $+5V_{DC}/3$ (g) $+2V_{DC}$ (h) 0 (i) $-V_{DC}/3$ (j) $-2V_{DC}/3$ (k) $-V_{DC}$ (l) $-4V_{DC}/3$ (m) $-5V_{DC}/3$ (n) $-2V_{DC}$.

standing voltage. It investigates both extendable and asymmetric topologies of the PB inverter, alongside power loss analysis using NLC and ANN-based SHEPWM techniques. The performance of the PB 13-level inverter is compared with other topologies, followed by an evaluation of simulation results. The study concludes with a review of the hardware results and findings related to the 13-level SCMLI topology.

2. Proposed topology

Fig. 1(a) illustrates the proposed single-phase, single-sourced switched-capacitor-based multi-level inverter (MLI) structure. The configuration of the proposed basic (PB) 13-level inverter topology includes ten switches (eight unidirectional and two bidirectional) and three capacitors. A bidirectional switch (T_6 and T_7) is positioned between the capacitors (C_1 and C_2, C_2 and C_3) and consists of a diode bridge and a switch. The capacitors' blocking voltages are managed by switches T_6 and T_7. When the bidirectional switch is active, a pair of diodes along with the switch will conduct. Switches T_9 and T_{10} are complementary to switches T_1 and T_2, creating an intrinsic topology. One end of the load is connected between switches T_9 and T_{10}, while the other end is connected to the midpoint of switches T_5, T_6, T_7, and T_8. Fig. 1(b) displays the output waveform of the PB 13-level inverter, illustrating the optimal switching angles produced by the ANN-based SHEPWM technique.

2.1. Various operating modes of the proposed topology

Fig. 2 illustrates the different operating modes of the proposed inverter. The input DC source voltage is divided into one-third using three capacitors, C_1, C_2, and C_3. The capacitor voltages are kept at one-third ($V_{DC}/3$) of the input voltage by sequentially activating the switches. Table 1 presents the states of the switches, with "1″ indicating the on state and "0″ indicating the off state, while the capacitor's charging and discharging states are represented as "C" and "D," respectively. The proposed topology achieves a twofold voltage gain, producing thirteen levels (0, $\pm V_{DC}/3$, $\pm 2V_{DC}/3$, $\pm V_{DC}$, $\pm 4V_{DC}/3$, $\pm 5V_{DC}/3$, and $\pm 2V_{DC}$) across the load, as illustrated in Fig. 2. The charging of the three capacitors is regulated by switches T_3 and T_4. Switches T_1 and T_2 are used to boost the output voltage from $\pm V_{DC}$ to $\pm 2V_{DC}$. The output polarity of the inverter is determined by switches T_9 and T_{10}. Table 1 outlines the various operating modes of the proposed system, along with their associated switching states and voltage levels.

Mode 0: During this stage, the load voltage is zero, and all three capacitors (C_1, C_2, and C_3) are charged to ($V_{DC}/3$) by connecting them in parallel to the input source through switches T_3 and T_4. Simultaneously, the energy stored in the inductive load is released by activating switches T_8 and T_{10}, as illustrated in Fig. 2(a).

Mode 1: When switches T_3, T_4, T_7, and T_{10} are activated, a potential of $V_{DC}/3$ is established across the load. The capacitors remain charged, and this $V_{DC}/3$ voltage is derived by subtracting the voltages V_{C1} and V_{C2} from V_{DC}.
Mode 2: By activating switches T_3, T_4, T_6, and T_{10}, a potential of $2V_{DC}/3$ is applied across the load. Switch T_6, which is connected in series with a pair of diodes, carries the load current.
Mode 3: A voltage of V_{DC} is applied across the load by turning on switches T_3, T_4, T_5, and T_{10}. The capacitors continue to be charged.
Mode 4: At this stage, the load voltage is $4V_{DC}/3$. Switches T_1, T_7, and T_{10} are activated, connecting the source and capacitor C_3 in series. As a result, C_3 discharges a potential of $V_{DC}/3$ combined with the source voltage V_{DC}, producing a total of $4V_{DC}/3$ across the load. The remaining capacitors, C_1 and C_2, stay unchanged.
Mode 5: The two capacitors of C_2 and C_3 discharges with input source to deliver the load voltage of $5V_{DC}/3$. During this state switches T_1, T_6 and T_{10} were turned on and the capacitor C_1 remains in ideal state.
Mode 6: At this stage, a maximum boosted voltage of $2V_{DC}$ is achieved across the load by connecting all three capacitors in series with the input source. Switches T_1, T_5, and T_{10} are turned on, with switch T_1 being the only one that must handle a peak blocking voltage of $2V_{DC}$. For the other modes, switches T_9 and T_2 substitute for T_{10} and T_1, respectively, while the rest of the setup remains the same.

Table 1
Switch and capacitor states for various modes.

Mode	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	C_1	C_2	C_3	V_{OUT}
1	0	0	1	1	0	0	1	0	0	1	C	C	D	$V_{DC}/3$
2	0	0	1	1	0	1	0	0	0	1	C	D	D	$2V_{DC}/3$
3	0	0	1	1	1	0	0	0	0	1	C	C	C	V_{DC}
4	1	0	0	0	0	0	1	0	0	1	D	–	–	$4V_{DC}/3$
5	1	0	0	0	0	1	0	0	0	1	D	D	–	$5V_{DC}/3$
6	1	0	0	0	1	0	0	0	0	1	D	D	D	$2V_{DC}$
7	0	0	1	1	1	0	0	0	1	0	C	C	C	0
8	0	0	1	1	0	1	0	0	1	0	C	C	D	$-V_{DC}/3$
9	0	0	1	1	0	0	1	0	1	0	C	D	D	$-2V_{DC}/3$
10	0	0	1	1	0	0	0	1	1	0	C	C	C	$-V_{DC}$
11	0	1	0	0	0	1	0	0	1	0	D	–	–	$-4V_{DC}/3$
12	0	1	0	0	0	0	1	0	1	0	D	D	–	$-5V_{DC}/3$
13	0	1	0	0	0	0	0	1	1	0	D	D	D	$-2V_{DC}$

Another significant advantage of the proposed topology is its reduced voltage stress. Fig. 3 shows the maximum peak voltages for the different switches, which are detailed as follows:

$$\begin{cases} V_{T3} = V_{T4} = V_{T5} = V_{T8} = V_{T9} = V_{T10} = V_{DC} \\ V_{T6} = V_{T7} = 3V_{DC}/2 \\ V_{T1} = V_{T2} = 2V_{DC} \end{cases} \tag{1}$$

Therefore, the Total Standing Voltage (TSV) of the proposed circuit can be calculated as,

$$TSV = \sum_{n=1}^{10} V_{Tn} = 6V_{DC} + 2V_{DC} + (3V_{DC}/2) \tag{2}$$

Thus, the per unit of the TSV can be calculated as,

$$TSV_{pu} = \frac{TSV}{V_{out(peak)}} = \frac{9.5V_{DC}}{2V_{DC}} = 4.25 \tag{3}$$

The Boosting Factor can be calculated as,

$$BF = \frac{V_{out(peak)}}{V_{DC}} = \frac{2V_{DC}}{V_{DC}} = 2 \tag{4}$$

This Fig. 3(b) illustrates the self-balancing mechanism of capacitors through their equivalent charging and discharging circuits. During both the charging and discharging phases, the circuit includes parasitic resistances from diodes (r_d), switches (r_{sw}) and the equivalent series resistance (ESR) of the capacitors (r_{ESR}). The input voltage (V_{dc}) is applied, and the capacitors charge to a voltage (V_c), factoring in the diode voltage drop (V_d).

The differential equation governing the capacitor voltage V_C during discharge is:

$$\frac{dV_C}{dt} = -\frac{1}{\tau}(V_C - (V_{dc} - V_d)) \quad where\ \tau = R_{total} * C \tag{5}$$

During the discharging phase, the time constant τ is larger due to the high load resistance R_L, which causes the capacitor to discharge more slowly. This slower discharge rate helps to minimize voltage ripple. Conversely, during the charging phase, τ is smaller because the resistance is lower, allowing the capacitor to charge more quickly. This rapid charging promotes effective self-balancing of the capacitor voltages and contributes to the capacitor's longevity.

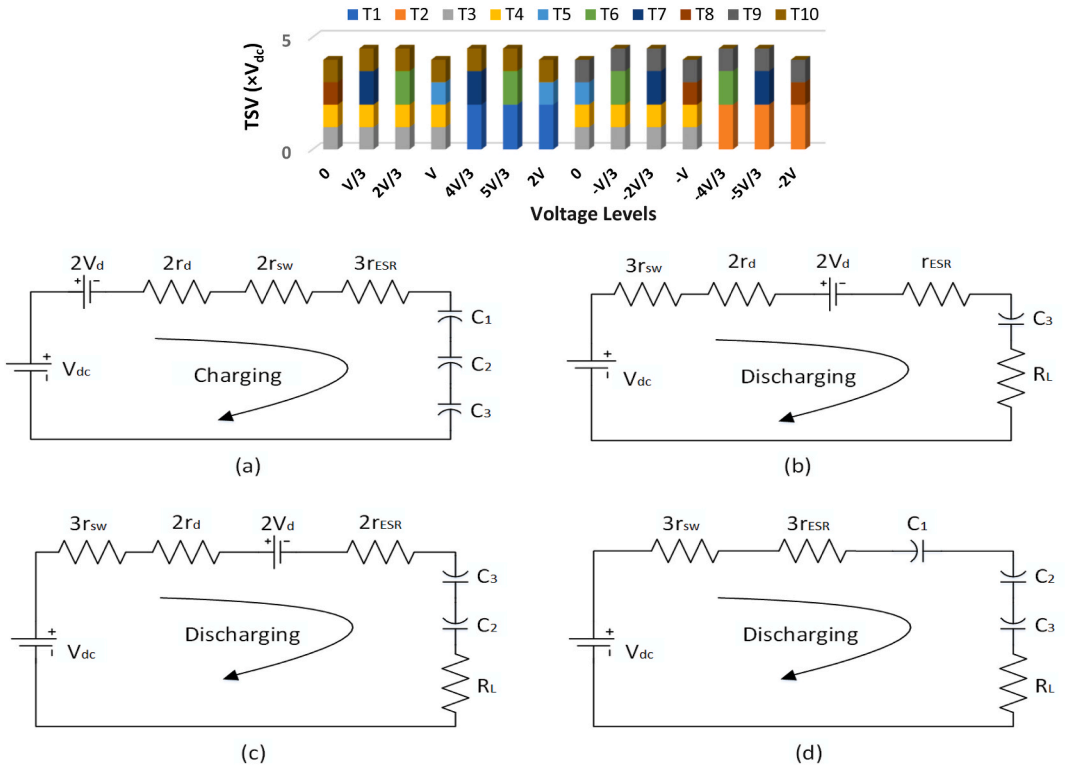


Fig. 3. (a) Total Standing Voltage (TSV) per level.Fig. 3. (b). Self-Balancing of capacitors with equivalent charging and discharging circuit

2.2. Extendable Version of the proposed model

Fig. 4 illustrates the extendable configuration of the PB model with a Capacitor Boosting Circuit (CBC). The PB_CBC model allows for an increase in levels to the desired extent by adding additional CBC units in parallel with the input source. By connecting N CBC units, the output voltage can be increased to (9N + 1) levels, as depicted in Fig. 4. The system needs (6N + 4) switches and 3N capacitor units to achieve the desired output voltage levels. Additionally, the use of a single DC source makes the proposed system highly suitable for renewable energy applications. The system provides symmetric voltage levels because the input source is common to all the switched capacitors. The output boosting factor of the proposed system increases by (NV_{DC}+1), with the constant 1 representing the base CBC unit. The proposed symmetric extendable topology achieves 19 levels by connecting two CBC units (CBC (1) and CBC (2)) in parallel with an input voltage of $3V_{DC}$. Table 2 details the various modes of the 19-level inverter and their respective switching states. It also includes two alternative switching states for reaching the same voltage levels. Table 2 illustrates only the positive half cycle of the 19-level inverter, with T_{10} replaced by T_9 during the negative half cycle. The calculations for the maximum peak voltage, TSV, TSV_{pu}, and BF of the proposed extendable PB_CBC model are as follows:

In each set of N CBC units, the switches T_{3n}, T_{4n}, T_{5n}, and T_{8n} each face a peak voltage of V_{DC}. Switches T_{6n} and T_{7n} each encounter a peak voltage of $3V_{DC}/3$ in every CBC unit. Consequently,

$$\sum (V_{T3n} + V_{T4n} + V_{T5n} + V_{T8n}) = 4N^{*}V_{DC} \text{ and } \sum (V_{T6n} + V_{T7n}) = (0.5N+1)^{*}V_{DC} \tag{6}$$

The voltage-boosting switches T_1 and T_2 are influenced by the peak magnitude of the load voltage and are determined by a multiplication factor of N, as follows:

$$\sum V_{T1} + V_{T2} = (N+1)V_{DC} \tag{7}$$

In the extendable topology, switches T_9 and T_{10} retain a peak voltage of V_{DC}, even with the addition of N CBC units. Thus, it can be calculated as:

$$\sum (V_{T9} + V_{T10}) = 2V_{DC} \tag{8}$$

Therefore, the Total Standing Voltage (TSV) can be calculated by summing the results from equations (5)–(8).

$$TSV = \sum_{N=1}^{\infty} V_{Tn} = (4N+2)V_{DC} + (N+1)V_{DC} + (0.5N+1)V_{DC}) = (5.5N+4)V_{DC} \tag{9}$$

Therefore, TSV_{pu} can be determined as:

$$TSV_{pu} = \frac{TSV}{V_{out(peak)}} = \frac{(5.5N+4)V_{DC}}{(N+1)V_{DC}} \tag{10}$$

The Boosting Factor can be computed as:

$$BF = \frac{V_{out(peak)}}{V_{DC}} = \frac{(N+1)V_{DC}}{V_{DC}} \tag{11}$$

2.3. Asymmetric configuration of the proposed model

The asymmetric circuit configuration, featuring two upturned PB models, is illustrated in Fig. 5. This design requires two voltage sources, V_{DC1} and V_{DC2}, with different magnitudes.

The circuit includes two CBC models connected in reverse configuration, with the load placed at the centre. The PB models are interconnected through complementary switches, T_9 and T_{9a}. This asymmetric design has the advantage of generating more voltage levels while requiring fewer components. The topology includes 18 switches in total, comprising 14 unidirectional and 4 bidirectional

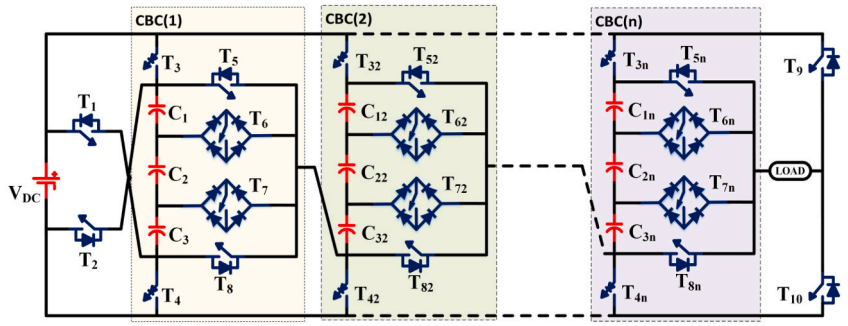


Fig. 4. Circuit diagram of extendable PB_CBC model.

Table 2
Switching states of the symmetric extendable 19-level CBC topology.

Mode	ON state switches		Level
0	T_3, T_4, T_8, T_{32}, T_{42}, T_{82}, T_{10}	T_3, T_4, T_5, T_{32}, T_{42}, T_{52}, T_9	0
1	T_3, T_4, T_7, T_{82}, T_{10}	T_3, T_4, T_{32}, T_{42}, T_{72}, T_{10}	$+V_{DC}$
2	T_3, T_4, T_6, T_{82}, T_{10}	T_3, T_4, T_{32}, T_{42}, T_{62}, T_{10}	$+2V_{DC}$
3	T_3, T_4, T_5, T_{82}, T_{10}	T_3, T_4, T_{32}, T_{42}, T_{52}, T_{10}	$+3V_{DC}$
4	T_1, T_7, T_{82}, T_{10}	T_1, T_8, T_{72}, T_{10}	$+4V_{DC}$
5	T_1, T_6, T_{82}, T_{10}	T_1, T_8, T_{62}, T_{10}	$+5V_{DC}$
6	T_1, T_5, T_{82}, T_{10}	T_1, T_8, T_{52}, T_{10}	$+6V_{DC}$
7	T_1, T_5, T_{72}, T_{10}	T_1, T_7, T_{52}, T_{10}	$+7V_{DC}$
8	T_1, T_5, T_{62}, T_{10}	T_1, T_6, T_{52}, T_{10}	$+8V_{DC}$
9	T_1, T_5, T_{52}, T_{10}	T_1, T_5, T_{52}, T_{10}	$+9V_{DC}$

switches, along with 6 capacitors. By setting the source magnitudes to $3V_{DC1}$ and $3/4V_{DC2}$ in the asymmetric model, the circuit produces 55 distinct voltage levels across the load. The switching states and their associated voltage levels for the 55-level PB model are detailed in Table 3.

2.4. Pulse generation technique for the proposed model

To minimize total harmonic distortion (THD) and enhance the quality of the output waveform, pulse width modulation (PWM) techniques are employed. PWM is classified into three categories based on switching frequency: PWM techniques are categorized based on switching frequency into high-frequency switching, low-frequency switching, and fundamental-frequency switching. The most commonly used methods include multicarrier PWM (for high frequency), sine PWM (for low frequency), and fundamental-frequency modulation techniques such as selective harmonic elimination (SHE) and nearest level control (NLC). While multicarrier PWM significantly reduces lower-order THD, it leads to increased switching losses due to its high switching frequency. Selective harmonic elimination (SHE) can also effectively remove low-order harmonics while minimizing switching losses. However, this approach requires solving a set of complex transcendental equations.

2.5. The nearest level control (NLC) PWM method

The Nearest Level Control (NLC) approach is straightforward and ideal for multi-level inverters (MLIs) with higher output voltage levels. It utilizes fundamental frequency modulation, which simplifies the process and is well-suited for MLIs with elevated output voltages. Consequently, in this proposed model, NLC-generated PWM is used to control the switches and achieve the desired output waveform. In the Nearest Level Control (NLC) approach, the reference sine signal is compared with the desired waveform to produce the necessary sample signal. This sample signal is then rounded to the nearest voltage level (NLC), which is used to generate gate signals for the switches according to Lookup Table 1. Fig. 6 illustrates the NLC method, showing the comparison between the reference signal and the desired output waveform [19].

2.6. Selective harmonic elimination approach

The Selective Harmonic Elimination (SHE) technique focuses on eliminating specific lower-order harmonics to improve the overall total harmonic distortion (THD) of the inverter. In the proposed inverter, SHEPWM is employed to target and remove lower-order harmonics such as the 3rd, 5th, 7th, 9th, and 11th, given that the output contains 13 levels. Higher-order harmonics can be effectively suppressed using small filters. The Fourier series is employed to derive the mathematical expressions for the output voltage

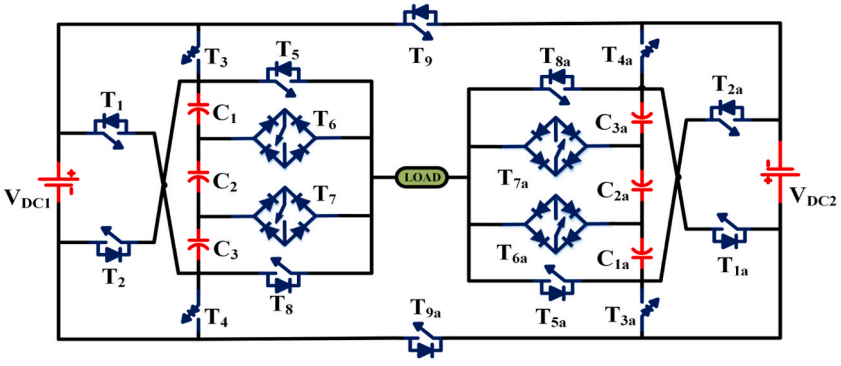


Fig. 5. Asymmetric configuration of the PB model.

Table 3
Asymmetric 55-level switching states.

Mode	Level	Switching states of asymmetric PB model (C1, C2, C3, C1a, C2a, C3a)
0	0	T_3, T_4, T_{3a}, T_{4a}, T_8, T_{5a}, T_{9a} (↑, ↑,↑,↑,↑,↑)
1	$V_{DC}/4$	T_{3a}, T_{9a}, T_4,T_8, T_{6a}, T_3, T_{4a} (↑,↑,↑,↓,↑,↑)
2	$V_{DC}/2$	T_{3a}, T_{9a}, T_4,T_8, T_{7a}, T_3, T_{4a} (↑,↑,↑,↓,↓,↑)
3	$3V_{DC}/4$	T_{3a}, T_{9a}, T_4,T_8, T_{8a}, T_3, T_{4a} (↑,↑,↑,↑,↑,↑)
4	V_{DC}	T_3, T_4, T_7, T_{5a}, T_{3a}, T_{9a}, T_{4a} (↑,↑,↓,↑,↑,↑)
5	$5V_{DC}/4$	T_3, T_4, T_7, T_{6a}, T_{3a}, T_{9a}, T_{4a} (↑,↑,↓,↓,↑,↑)
6	$6V_{DC}/4$	T_3, T_4, T_7, T_{7a}, T_{3a}, T_{9a}, T_{4a} (↑,↑,↓,↓,↓,↑)
7	$7V_{DC}/4$	T_3, T_4, T_7, T_{8a}, T_{3a}, T_{9a}, T_{4a} (↑,↑,↓,↑,↑,↑)
8	$2V_{DC}$	T_3, T_4, T_6, T_{5a}, T_{3a}, T_{9a}, T_{4a} (↑,↓,↓,↑,↑,↑)
9	$9V_{DC}/4$	T_3, T_4, T_6, T_{6a}, T_{3a}, T_{9a}, T_{4a} (↑,↓,↓,↓,↑,↑)
10	$10V_{DC}/4$	T_3, T_4, T_6, T_{7a}, T_{3a}, T_{9a}, T_{4a} (↑,↓,↓,↓,↓,↑)
11	$11V_{DC}/4$	T_3, T_4, T_6, T_{8a}, T_{3a}, T_{9a}, T_{4a} (↑,↓,↓,↑,↑,↑)
12	$3V_{DC}$	T_3, T_4, T_5, T_{5a}, T_{3a}, T_{9a}, T_{4a} (↑,↑,↑,↑,↑,↑)
13	$13V_{DC}/4$	T_3, T_4, T_5, T_{6a}, T_{3a}, T_{9a}, T_{4a} (↑,↑,↑,↓,↑,↑)
14	$14V_{DC}/4$	T_3, T_4, T_5, T_{7a}, T_{3a}, T_{9a}, T_{4a} (↑,↑,↑,↓,↓,↑)
15	$15V_{DC}/4$	T_3, T_4, T_8, T_{8a}, T_{3a}, T_{9a}, T_{4a} (↑,↑,↑,↓,↓,↓)
16	$4V_{DC}$	T_1, T_7, T_{5a}, T_{3a}, T_{9a}, T_{4a} (−,−,↓,↑,↑,↑)
17	$17V_{DC}/4$	T_1, T_7, T_{6a}, T_{3a}, T_{9a}, T_{4a} (−,−,↓,↓,↑,↑)
18	$18V_{DC}/4$	T_1, T_7, T_{7a}, T_{3a}, T_{9a}, T_{4a} (−,−,↓,↓,↓,↑)
19	$19V_{DC}/4$	T_1, T_7, T_{8a}, T_{3a}, T_{9a}, T_{4a} (−,−,↓,↑,↑,↑)
20	$5V_{DC}$	T_1, T_6, T_{5a}, T_{3a}, T_{9a}, T_{4a} (−,↓,↓,↑,↑,↑)
21	$21V_{DC}/4$	T_1, T_6, T_{6a}, T_{3a}, T_{9a}, T_{4a} (−,↓,↓,↓,↑,↑)
22	$22V_{DC}/4$	T_1, T_6, T_{7a}, T_{3a}, T_{9a}, T_{4a} (−,↓,↓,↓,↓,↑)
23	$23V_{DC}/4$	T_1, T_6, T_{8a}, T_{3a}, T_{9a}, T_{4a} (−,↓,↓,↑,↑,↑)
24	$6V_{DC}$	T_1, T_5, T_{5a}, T_{3a}, T_{9a}, T_{4a} (↓,↓,↓,↑,↑,↑)
25	$25V_{DC}/4$	T_1, T_5, T_{6a}, T_{3a}, T_{9a}, T_{4a} (↓,↓,↓,↓,↑,↑)
26	$26V_{DC}/4$	T_1, T_5, T_{7a}, T_{3a}, T_{9a}, T_{4a} (↓,↓,↓,↓,↓,↑)
27	$27V_{DC}/4$	T_1, T_5, T_{8a}, T_{3a}, T_{9a}, T_{4a} (↓,↓,↓,↑,↑,↑)

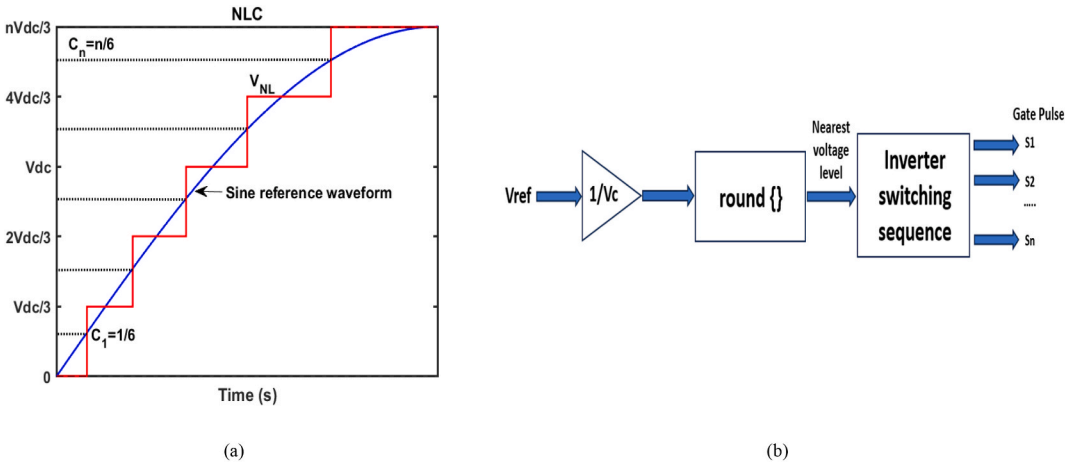


Fig. 6. (a) NLC waveform; (b) NLC Control logic.

waveforms. These expressions are given by the following equations:

$$f_n(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos n\omega t + V_n \sin n\omega t \tag{12}$$

Where a0 denotes the DC component, and an and V_n denote even and odd harmonics, respectively

$$\begin{cases} a_0 = \dfrac{1}{2\pi}\displaystyle\int_0^{2\pi} f(t) \\ a_n = \dfrac{1}{2\pi}\displaystyle\int_0^{2\pi} f(t)\sin n\omega t \\ V_n = \dfrac{1}{2\pi}\displaystyle\int_0^{2\pi} f(t)\sin n\omega t \end{cases} \tag{13}$$

Due to the quarter-cycle symmetry of the output waveform, the even-order harmonics ($a_0 = a_n = 0$) are canceled out, leaving only the odd harmonics (V_n). This is represented by Equation (12):

$$f_n(t) = \sum_{i=1,2,3\ldots}^{n} V_n \sin(n\alpha_i) \tag{14}$$

In Fig. 6(a), the odd notches occurring every quarter cycle are illustrated, with the staircase output voltage represented by V_n.

$$V_n = \frac{4V_{dc}}{\pi}\int_{\alpha_1}^{\alpha_2} \sin(n\omega t)dt + \int_{\alpha_2}^{\alpha_3} \sin(n\omega t)dt + \int_{\alpha_3}^{\alpha_4} \sin(n\omega t)dt + \int_{\alpha_4}^{\alpha_5} \sin(n\omega t)dt + \int_{\alpha_5}^{\alpha_6} \sin(n\omega t)dt + \int_{\alpha_6}^{\frac{\pi}{2}} \sin(n\omega t)dt \tag{15}$$

It is noted that where V_{dc} represents the magnitude of the input voltage source, Equation (15) can be simplified accordingly.

$$V_n = \frac{4V_{dc}}{\pi}\left[\sum_{i=0}^{j} (-1)^{i+1} \cos n\alpha_i\right] \tag{16}$$

Where j denotes the number of edges or notches per quarter cycle, the peak voltage of each nth harmonic component is given by

$$V_h = \frac{4V_{dc}}{n\pi}\left[\cos(n\alpha_1) + \cos(n\alpha_2) + \ldots + \cos(n\alpha_j)\right] \quad where\ n = odd \tag{17}$$

In this PB MLI, with 13 levels (N), (N−1)/2 switching angles are calculated to eliminate the lower-order harmonics of (V_3, V_5, V_7, V_9 and V_{11}) and the control angles for these harmonics are (α_1, α_2, α_3, α_4, α_5 and α_6). Additionally, Equation (17) can be used to compute both the fundamental peak voltage (V_1) and the values for the 3rd, 5th, 7th, 9th and 11th harmonic components.

$$\left.\begin{aligned} V_1 &= \frac{4V_{dc}}{\pi}[\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) + \cos(\alpha_5) + \cos(\alpha_6)], n = 1 \\ V_3 &= \frac{4V_{dc}}{3\pi}[\cos(3\alpha_1) + \cos(3\alpha_2) + \cos(3\alpha_3) + \cos(3\alpha_4) + \cos(3\alpha_5) + \cos(3\alpha_6)], n = 3 \\ V_5 &= \frac{4V_{dc}}{5\pi}[\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) + \cos(5\alpha_5) + \cos(5\alpha_6)], n = 5 \\ V_7 &= \frac{4V_{dc}}{7\pi}[\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) + \cos(7\alpha_5) + \cos(7\alpha_6)], n = 7 \\ V_9 &= \frac{4V_{dc}}{9\pi}[\cos(9\alpha_1) + \cos(9\alpha_2) + \cos(9\alpha_3) + \cos(9\alpha_4) + \cos(9\alpha_5) + \cos(9\alpha_6)], n = 9 \\ V_{11} &= \frac{4V_{dc}}{11\pi}[\cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cos(11\alpha_4) + \cos(11\alpha_5) + \cos(11\alpha_6)], n = 11 \end{aligned}\right\} \tag{18}$$

To eliminate the 3rd, 5th, 7th, 9th, and 11th order harmonics across the load, setting their respective voltage magnitudes to zero in Equation (18) is required.

$$V_1 = nM, V_3 = 0, V_5 = 0, V_7 = 0, V_9 = 0\ and\ V_{11} = 0 \tag{19}$$

The respective firing angle can be found with constraint that,

$$0 < \alpha_3 < \alpha_5 < \alpha_7 < \alpha_9 < \alpha_{11} < \frac{\pi}{2} \tag{20}$$

The inverter's modulation index (M) can be calculated by,

$$M = \frac{\pi V_1}{4n^* V_{dc}}, 0 \le M \le 1 \tag{21}$$

The primary objective of SHE PWM is to minimize the harmonic values as much as possible, and the firing angles are determined using the Newton-Raphson (NR) method. The fitness function is given by:

$$\text{Fitness Function} = \left(100\frac{V_1^* - V_1}{V_1^*}\right)^4 + \sum_{n=3,5,\ldots}^{2N_{Level}-1} \frac{1}{n}\left(50\frac{V_n}{V_1}\right)^2 \tag{22}$$

2.7. Newton raphson (NR) method

In the NR method, nonlinear equations are solved starting with an initial guess, which is a random value between 0 and 90°. Numeric iterations are denoted by j and e. The following steps are undertaken in the NR method.

1. Initial values are set in finding the firing angles

$$\alpha^0 = \left[\alpha_{1,}^0 \alpha_{2,}^0 \alpha_{3,}^0 \ldots \alpha_n^0\right] \tag{23}$$

2. Compute the values for nonlinear equation and dα using the Jacobian matrix for 'n' variables in the 'k' iterations.

$$J = \begin{bmatrix} \frac{\partial f_1}{\partial \alpha_1} & \cdots & \frac{\partial f_1}{\partial \alpha_n} \\ \vdots & \ddots & \vdots \\ \frac{\partial f_m}{\partial \alpha_1} & \cdots & \frac{\partial f_m}{\partial \alpha_m} \end{bmatrix} \tag{24}$$

$$\partial\alpha = J^* f\left(\alpha^k\right) \tag{25}$$

3. Repeat step 4 as long as the threshold is smaller than ∂α. Stop the process if the threshold is higher or equal to ∂α.
4. After updating αvalue by Equation (25), proceed to Step 2.

$$\alpha^{k+1} = \alpha^k + \partial\alpha \tag{26}$$

2.8. Artificial nueral network based SHE PWM for the proposed inverter

To eliminate selective lower-order harmonics, it is necessary to solve nonlinear transcendental equations. The Newton-Raphson method, combined with Artificial Neural Networks (ANN), is employed to find the optimized switching angles. ANN requires initial inputs for its training process. Fig. 7 illustrates the internal layers of the artificial neural networks used in this approach. It consist of a single input layer with a value of V_{dc} and two hidden layers (H_1 and H_2) positioned between the input and output layers to generate the optimal switching angles. To introduce nonlinearity into the model, a 'tanh' activation function, with a range between '-1′ and '1′, is employed. The computation of individual neurons (Y_i) is performed by adding a weight to all of their inputs. The number K ranges from 0 to the number of neurons in the previous layer. The tanh function is applied to scale the output values within the specified range. This is described as follows:

$$Y_i = \tanh\left(W_k X_k + B_i\right) \tag{27}$$

It is noted that W_k represents the weight of individual neurons, X_k denotes the output of the kth neuron, and B_i indicates the bias in the hidden layer. The mean squared error (MSE) loss is used to calculate the error metrics. To reduce error loss, the Back Propagation technique is applied, which involves adjusting the weights of each layer using the Adam optimizer.

$$MSE = \frac{1}{N}\sum_{i=1}^{N}\left(y_i - y_i'\right)^2 \tag{28}$$

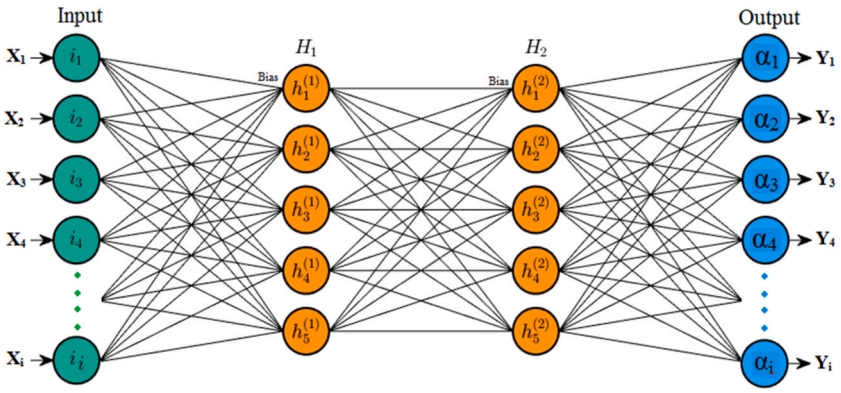


Fig. 7. Architecture of ANN for the proposed PB 13L inverter.

The optimization process for the hybrid ANN-NR algorithm is detailed in the flowchart in Fig. 8. In this method, an artificial neural network (ANN) is trained with optimal switching angle data calculated offline for a specific inverter setup. The data is divided into training, testing, and validation sets in a 60:20:20 ratio. The ANN provides initial estimates, which are then refined using the Newton-Raphson method. Because the ANN's estimates are close to the global optima, the method converges quickly and yields highly accurate switching angles. If perfect solutions are not possible, the ANN's estimates still provide sufficiently accurate angles, reducing harmonic

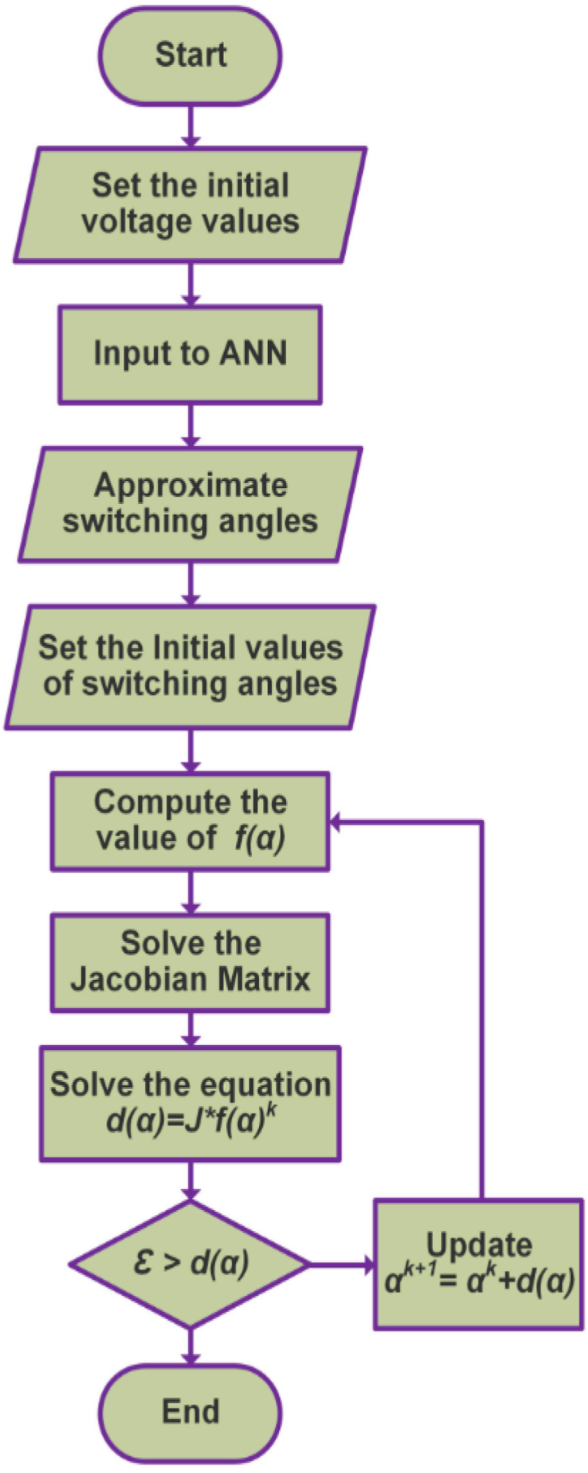


Fig. 8. Flowchart of ANN based SHE PWM for the proposed PB 13L inverter.

distortion.

Table 4 presents data on various parameters (α_1 to α_5) and specific measurements (5th, 7th, 11th, and 13th) across different values of MI. The values for MI range from 0.1 to 1.0. α_1 to α_5: These columns represent different quantitative measures related to MI, showing how each parameter changes as MI varies. 5th, 7th, 11th, and 13th. These values appear to represent specific measurements or characteristics associated with the MI values. They likely represent metrics such as specific frequencies, intensities, or other relevant data points. Fig. 9(a) illustrates the variations in switching angles relative to the modulation index, while Fig. 9(b) depicts the variations in harmonic order in relation to the modulation index.

3. Power loss calculation

3.1. Conduction loss of the switch and diode (P_{conl})

Conduction loss (P_{conl}) refers to the loss that occurs when a switch or diode is turned on, which is caused by the internal resistance of the switch (R_{IGBT}) or diode (R_{Diode}), along with the load current (I_L) and the constant(β). For a switch and a diode, P_{conl} can be calculated as follows [29]:

$$P_{conl.IGBT} = \left[V_{IGBT} + R_{IGBT} i^{\beta}\right] i(t) \tag{29}$$

$$P_{conl.Diode} = [V_{Diode} + R_{Diode} i(t)] i(t) \tag{30}$$

3.2. Switching loss of the switches (P_{sw_loss})

Switching losses occur due to the overlap of voltage and current on the switches during dynamic transitions between the ON (t_{on}) and OFF (t_{off}) states. The magnitude of these losses is influenced by the switch blocking voltage (V_{BV}) and the switching frequency (f_{sw}). The switching losses P_{sl} are calculated as follows:

$$\boldsymbol{P_{sw\_loss}} = \sum_{i=0}^{10} \frac{\mathbf{1}}{\mathbf{6}} \boldsymbol{f_{swi} V_{BVij} I_L \left(t_{on} + t_{off}\right)} \tag{31}$$

3.3. Capacitor ripple losses (P_{cap_rl})

Power loss occurs during the charging interval due to the equivalent series resistance (ESR) of capacitors. The voltage loss caused by ESR can be calculated using the ripple voltage across the capacitor (C).

$$P_{cap\_rl} = \frac{f_{sw}}{2} * C * V_{cvd} \tag{32}$$

The total power loss (P_{total}) of the proposed inverter is calculated as follows:

$$P_{total\_loss} = P_{con\_loss} + P_{sw\_loss} + P_{cap\_rl} \tag{33}$$

Inverter efficiency is determined by comparing the power output of the inverter to its power input.

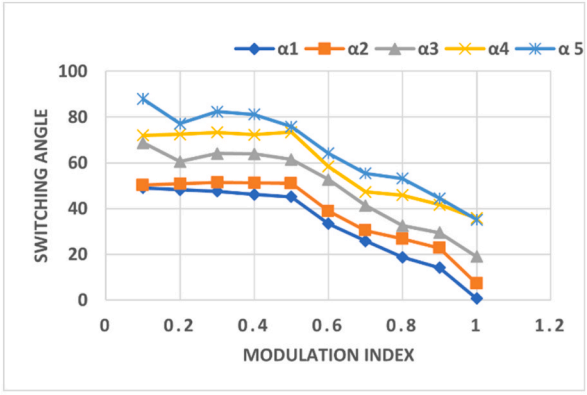
$$\eta = \frac{P_{output}}{P_{input}} * 100, where\ P_{input} = P_{ouput} + P_{total\_loss} \tag{34}$$

4. Comparative assessment

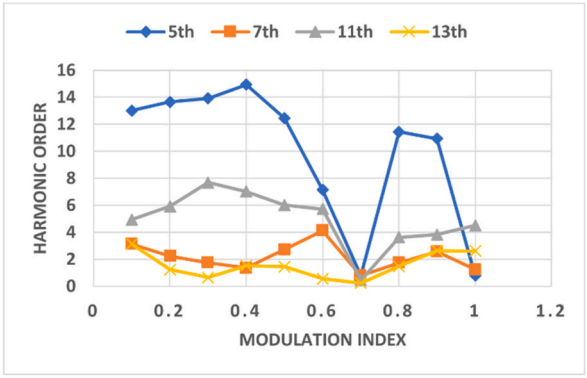
The performance of the PB 13-level inverter is evaluated against other relevant and traditional inverters. A comprehensive analysis has been conducted on the PB 13-level inverter, focusing on the total count of components such as levels (N_L), switches (N_{sw}), gate

Table 4
Analysis of harmonics against switching angle with various MI.

MI	α_1	α_2	α_3	α_4	α_5	5th	7th	11th	13th
0.1	49.1011	50.2313	68.7953	72.0123	87.9134	13.01	3.13	4.93	3.13
0.2	48.2501	50.7892	60.5634	72.4523	77.1457	13.65	2.23	5.91	1.23
0.3	47.5678	51.3465	64.1246	73.3057	82.3571	13.92	1.74	7.68	0.64
0.4	46.2014	51.2456	63.9126	72.3061	81.2038	14.94	1.35	7.01	1.53
0.5	45.1342	51.0234	61.4327	73.4129	75.8913	12.45	2.71	6.01	1.44
0.6	33.3568	38.9024	52.7150	58.3910	64.1482	7.13	4.12	5.72	0.55
0.7	25.7810	30.3451	41.3245	47.3274	55.3812	0.79	0.79	0.45	0.23
0.8	18.6743	26.7891	32.5102	45.9125	53.2014	11.43	1.74	3.62	1.48
0.9	14.1567	22.7564	29.4724	41.6734	44.5267	10.93	2.56	3.82	2.64
1	0.7135	7.2345	19.0135	35.8142	35.1820	0.79	1.23	4.5	2.6



(a)



(b)

Fig. 9. (a) Modulation Index against switching angle, (b) Modulation Index against harmonic order.

Table 5
Comparative analysis of PB 13-level inverter with other relevant topologies.

Topology	N_L	N_{sw}	N_{gd}	N_d	N_{cap}	N_{DC}	TSV_{pu}	η (%)	THD (%)	Voltage Boosting factor	CF	Polarity Reversal
DCMLI	13	24	24	132	–	1	8	–	–	Nil	14.85	Inherent
FCMLI	13	24	24	–	66	1	8	–	–	Nil	9.77	Inherent
CHBMLI	13	24	24	–	–	6	6	–	–	Nil	30.92	H-Bridge
Roy, Sadhu, and Panigrahi 2020 [4]	11	12	12	8	4	1	6.4	92.1	8.22	5	3.23	Inherent
(Padmanaban, Dhanamjayulu, and Khan 2021) [14]	13	24	24	–	–	6	6	89.3	9.1	1	24.92	H-Bridge
(Kumar, T.A. et al., 2023) [29]	7	11	10	–	2	1	6	–	19.62	3	2.23	H-Bridge
(Manickam et al., 2022) [19]	9	12	12	1	2	1	5	–	9.35	2	2.46	Inherent
(Samadaei, Kaviani, and Bertilsson 2019) [20]	13	14	11	–	2	2	5.3	95.3	3.9	2	4.97	Inherent
(Liu, Zhu, and Zeng 2020) [21]	13	20	16	–	6	2	5.3	–	23.8	1.5	7.27	Inherent
(Roy, and Sadhu 2021) [22]	13	14	14	2	4	2	6	91	7.45	3	6.25	Inherent
(Zeng et al., 2020) [23]	13	14	12	–	4	1	6	98.2	5.3	1.5	2.77	Inherent
(Panda, Bana, and Panda 2021) [24]	13	12	12	4	4	1	4.33	95.2	4.17	3	2.80	Inherent
(Ye et al., 2021) [25]	13	10	10	4	4	1	5.5	97.2	11	6	2.58	Inherent
(Shikai et al., 2021) [26]	13	14	12	–	4	1	4.33	96.3	7.5	3	2.65	Inherent
(Tayyab et al., 2021) [27]	13	12	11	3	3	1	7.3	97.2	4.9	3	2.79	Inherent
(Bhatnagar et al., 2022) [28]	13	13	13	1	3	1	17	–	7.2	3	3.62	Inherent
[32]	11	11	11	1	0	3	10.3	92.4	6.87	0	7.85	H-bridge
[33]	13	14	14	14	0	6	6	97.31	5.6	0	21.69	Inherent
Proposed	**13**	**10**	**10**	**8**	**3**	**1**	**4.2**	**96.9**	**6.9**	**2**	**2.71**	**Inherent**

drivers (N_{gd}), diodes (N_d), capacitors (N_{cap}), and input DC sources (N_{DC}). The proposed topology is compared to various MLIs in Table 5. The primary focus of the PB 13-level inverter is on reducing device count and optimizing the system's Total Semiconductor Volume (TSV). The proposed model utilizes only 10 power semiconductor switches and 10 gate drivers to produce 13 output voltage levels, which represents a significant reduction compared to [4][14][11][20–27]. Compared to the proposed model, the topology in Ref. [24] has a similar count of switches and drivers but a higher total semiconductor volume per unit (TSV_{pu}) of 5.5. In contrast to the design by Ref. [14], the proposed model incorporates an intrinsic polarity reverser and voltage booster. The SHEPWM technique utilizing APSO-GA results in a Total Harmonic Distortion (THD) of 18.12 % [30]. The PSO-based SHEPWM achieves a THD of 11 % [31], while the ANN-NR-based SHEPWM offers a THD of 9.1 % [14]. Notably, our proposed model achieves a THD of 6.9 %, demonstrating superior performance in harmonic reduction.

The main focus, as with the PB 13-level inverter, is on device count reduction as well as the system's TSV. Only 10 power semiconductor switches with 10 gate drivers are used in the proposed model to generate the 13-levels of output voltage, which is significantly less than [4,14,20–29]. In comparison to the proposed model, the topology in Ref. [24] has a similar switch and driver count, but a high TSV_{pu} value of 5.5. In comparison to Ref. [14], the suggested model has an intrinsic polarity reverser and voltage booster.

The CF is utilized to assess the cost efficiency per output voltage level, defined by [26]:

$$CF = \frac{(N_{sw} + N_{gd} + N_d + N_{cap} + TSV_{pu})^* N_{DC}}{13} \tag{35}$$

Unlike the topologies presented by Refs. [11,18,20], and [21,22], which require multiple DC input sources, the proposed design operates with just a single DC source to deliver equivalent output levels. Table 6 illustrates a comparative analysis of the proposed PB 13-level model and other relevant topologies, focusing on their cascaded extensions. The variables n and m indicate the number of cells or modules within the extendable configurations, with the topology's attributes determined by the count of DC sources (N_{DC}).

In comparison to Refs. [18–22], the proposed topology only requires a single DC input source to provide identical output levels. Table 6 compares the cascaded extension of the proposed PB 13-level model with the relevant topologies. The extendable topological configuration's features are represented in terms of the number of levels (N_L).

5. Simulation results

The effectiveness of the proposed 13-level inverter circuit is assessed by simulating it under different load conditions. The simulation results and analysis, conducted using MATLAB/SIMULINK, are presented in Fig. 10. The model was evaluated with two distinct loads: a resistive load of (R = 40Ω and RL = 50Ω + 100 mH). Fig. 10(a) presents the initial results for the resistive load with a resistance of R = 40Ω and an input voltage of 150V. The voltage and current waveforms are in alignment, resulting in a 300V output load voltage, as depicted in the same figure. Consequently, the proposed model achieves a voltage boost that is twice the input voltage. Power losses occur when the switches are in the ON and OFF states. Details on the power loss associated with the switching and diode conduction are provided in Section 4. When the input voltage is higher, the forward conduction voltage drop of the diodes has a minimal impact on the output, making it nearly negligible. Fig. 10(b) displays the output voltage and current waveforms for a resistive and inductive load (RL = 50Ω + 100 mH). Given that the load power factor is less than one, the current lags behind the input voltage. Fig. 10(c) illustrates the capacitor voltages V_{C1}, V_{C2}, and V_{C3} highlighting their ability to handle peak load conditions. Fig. 11 presents the voltage stress experienced by each switch. Switches T_1 and T_2 experience a maximum voltage stress of $2V_{DC}$. The voltage stress on switches T_3, T_4, T_5, T_8, T_9, and T_{10} equals the input source voltage (V_{DC}), while switches T_6 and T_7 have a lower voltage stress of ($2V_{DC}/3$).

Fig. 12(a) displays the FFT analysis of the proposed model using the NLC control technique, which resulted in a Total Harmonic Distortion (THD) of 6.67 %. Although the NLC technique achieves a lower overall THD percentage, the harmonic profile shows that the magnitudes of the 3rd, 5th, 7th, 9th, and 11th order harmonics are relatively high and prominent. When the ANN-based SHEPWM approach is applied, the dominant harmonic spectra are effectively eliminated, resulting in a reduced THD value of 6.07 %, as shown in Fig. 12(b). This approach achieves a lower THD and a higher fundamental value compared to the direct NLC method, as depicted in the

Table 6
Comparative analysis of PB 13-level inverter with other relevant topologies.

Topology	N_{sw}	N_{gd}	N_d	N_{cap}	N_L	Gain
(Padmanaban, Dhanamjayulu, and Khan 2021) [14]	$4N_{DC}$	$4N_{DC}$	–	–	$2N_{DC}$ +1	–
(Kumar, T.A. et al., 2023) [29]	$7N_{DC}$ + 4	$7N_{DC}$ + 3	–	$2N_{DC}$	$6N_{DC}$+1	$3N_{DC}$
(Samadaei, Kaviani, and Bertilsson 2019) [20]	$14N_{DC}$	9 N_{DC}	$14N_{DC}$	$2N_{DC}$	$12N_{DC}$+1	–
(Liu, Zhu, and Zeng 2020) [21]	$10N_{DC}$	$10N_{DC}$	–	$3N_{DC}$	$6N_{DC}$+1	$1.5N_{DC}$
(Roy, and Sadhu 2021) [22]	$14N_{DC}$	$14N_{DC}$	$2N_{DC}$	$4N_{DC}$	$6N_{DC}$+1	3
(Zeng et al., 2020) [23]	$4(N_{DC}+3)$	6 N_{DC}+5	–	2 (N_{DC}+1)	$(2^{n+2}-3)N_{DC}$	$(1/(2^{n-1}))N_{DC}$
(Shikai et al., 2021) [26]	$8N_{DC}$+6	$7N_{DC}$+5	–	2 (N_{DC}+1)	$4(2^{n+1}-1)+N_{DC}$	$(2^{n+1}-2^{-m})N_{DC}$
(Bhatnagar et al., 2022) [28]	$4N_{DC}$+13	$4N_{DC}$+12	1	3+ N_{DC}	–	–
[32]	$(6N_{DC}+12)/4$	$(2N_{DC}+9)/2$	$(2N_{DC}-4)/4$	–	$2N_{DC}$ + 1	–
[33]	$2N_{DC}$ + 10	$2N_{DC}$ + 10	–	–	$2N_{DC}$ + 9	–
Proposed	**$6N_{DC}$+4**	**$6N_{DC}$+4**	**$8N_{DC}$**	**$3N_{DC}$**	**N_{DC}+12n**	**N_{DC} + n**

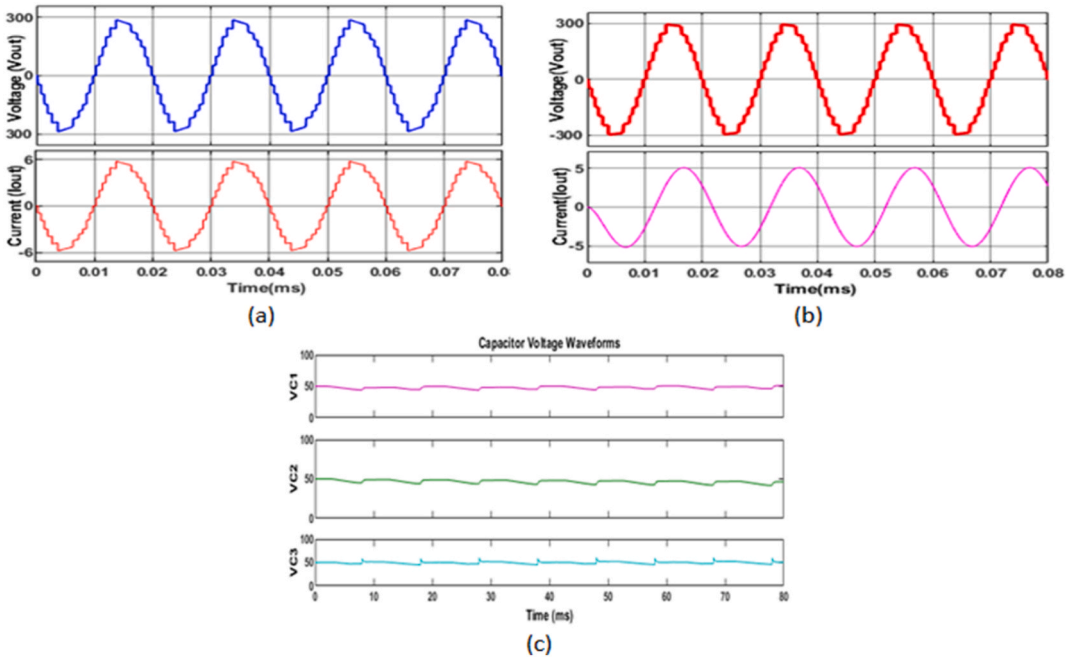


Fig. 10. Simulation results for the PB 13-level MLI (a) Output load voltage and current waveform of resistive load value 40Ω, (b) Output load voltage and current waveform of RL value 50Ω + 50 mH, and (c) Capacitor voltage waveforms of V_{C1}. V_{C2} and V_{C3}.

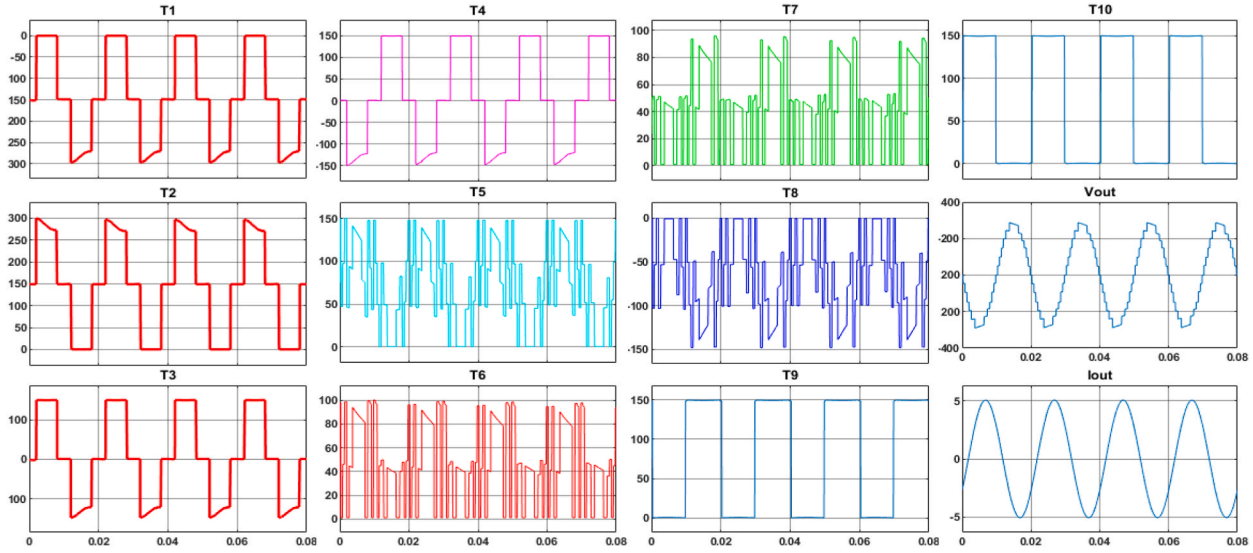


Fig. 11. Voltage stress on the individual switches with respective the load voltage and current waveform.

same figure.

The efficiency of the proposed MLI is calculated mathematically. The total loss in 32.3W for a total output power of 800W which displayed on Table 7. The proposed model provides efficiency of 95.96 %. The scales on the experimental results were displayed in Figs. 13 and 14 The efficiency curve of the proposed MLI has been shown in Fig. 15 and 16

6. Hardware results

The hardware performance of the proposed PB 13-level inverters is evaluated using a key sight digital storage oscilloscope (DSO). Gating signals are generated through MATLAB and are then processed by a DSP-based TMS320F2812 controller, utilizing the CCS compiler for integration. Fig. 13 illustrates the static performance of the model with a resistive load The input DC voltage of 150V is

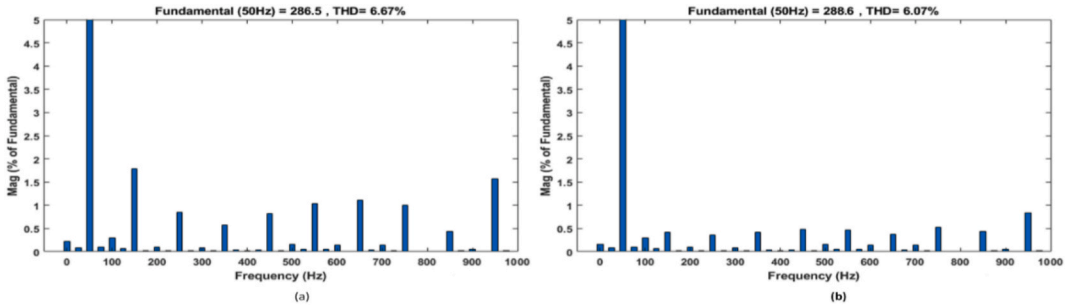


Fig. 12. THD values of the PB 13-level inverter using a) NLC, and b) ANN based SHEPWM.

Table 7
Power loss distribution of the proposed topology with Pout = 800W

Power Loss of	P_{sw_loss} (W)	P_{conl} (W)	P_{total_loss} (W)
Switch T_1	0.0380	4.8	4.8
Switch T_2	0.0380	4.8	4.8
Switch T_3	0.0037	1.18	1.18
Switch T_4	0.0037	1.18	1.18
Switch T_5	0.0011	0.018	0.018
Switch T_6	0.0015	3.568	3.568
Switch T_7	0.0004	3.568	3.568
Switch T_8	0.0011	0.018	0.018
Switch T_9	0.0110	1.62	1.62
Switch T_{10}	0.0082	1.62	1.62
Total Switch			22.372
Capacitor Loss (P_{cap_rl})		**C_1**	**3.35**
		C_2	**3.19**
		C_3	**3.39**
Total Losses (W)			**32.302**

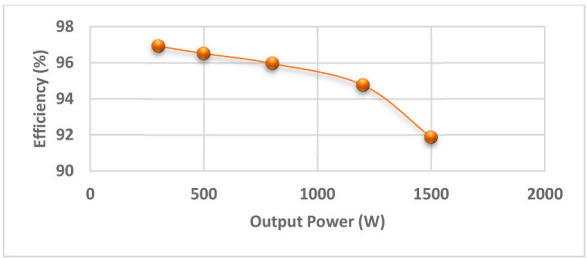


Fig. 13. Efficiency vs output power curve of the proposed topology.

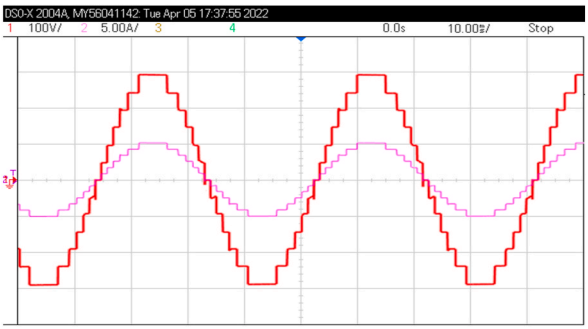


Fig. 14. Output load voltage and current waveform of the resistive load value of R = 50Ω.

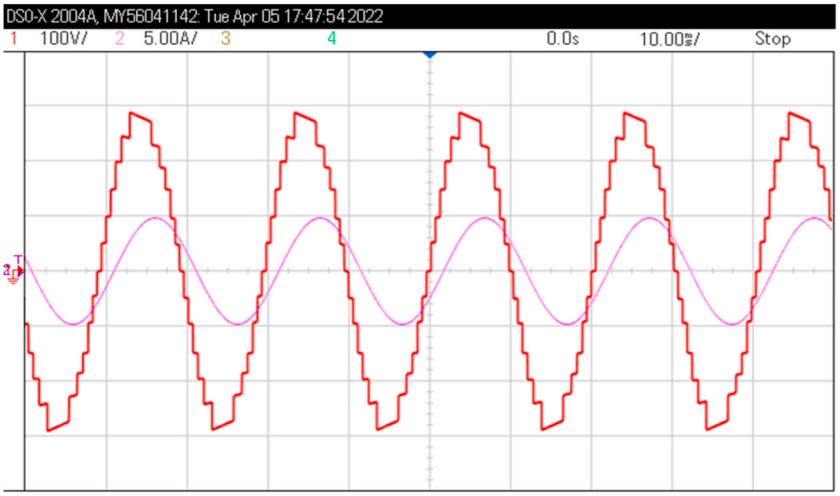


Fig. 15. Output load voltage and current waveform of the resistive load value of RL = 40Ω + 100 mH.

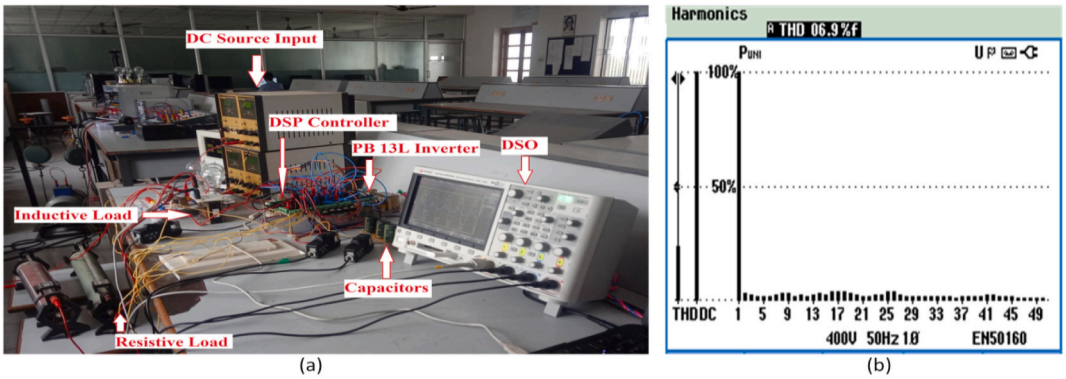


Fig. 16. (a) Prototypical model for PB 13-level inverter, and (b) FFT analysis with ANN based SHEPWM.

effectively Fig 17 and 18 doubled across the load (R = 50Ω). Furthermore, the figure shows that the output voltage reaches 300V with a current of 5A and a unity power factor. Table 8 summarize the components and their voltage/current ratings.

Fig. 13 displays the waveform resulting from a resistive and inductive load RL = 40Ω + 100 mH. When the load shifts from resistive to inductive, the output current waveform maintains a sinusoidal shape with a power factor of 0.8. The current through the load is 4.9A, and the voltage across the load is 298V. During peak load conditions, the output voltage Fig 19 and 20 curve shows a tilt, reflecting the reduction in capacitor voltages to their minimum levels. Fig. 14 showcases the prototype of the proposed PB 13-level

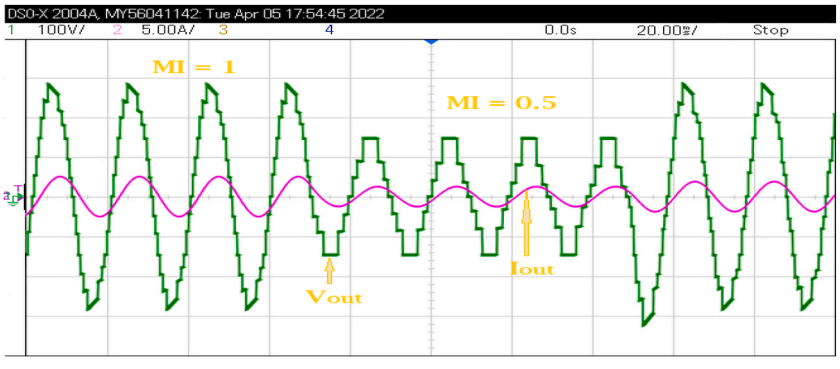


Fig. 17. Load voltage and current waveform of RL = 40Ω + 100 mH load with cyclic modulation index value of (MI = 1) during first four cycles later changed the MI value to 0.5 for next four cycles.

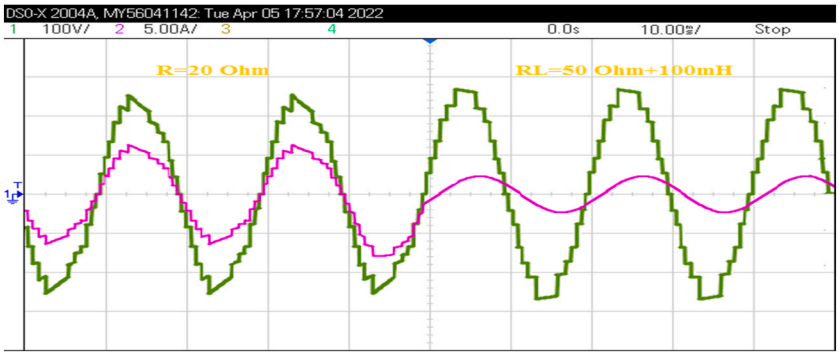


Fig. 18. Load voltage and current waveform of R = 20Ω load during first three cycles later changed the load value RL = 50Ω + 100 mH for next three cycles.

inverter along with the associated THD results. Fig. 15 demonstrates the dynamic performance of the model after the modulation index is adjusted from 1 to 0.5. Throughout these changes, the input voltage remains constant at 150V. As the modulation index decreases, the number of voltage levels steps down from 13 to 7. Additionally, during the transition from 7 to 13 levels, a minor voltage spike is observed, which can be reduced by fine-tuning the filter capacitance across the load.

Fig. 17 illustrates the voltage and current waveforms during dynamic load shifts. Initially, the load is maintained as resistive (R = 20Ω) for three cycles before switching to a combined resistive and inductive load (RL = 50Ω + 100 mH) for another three cycles. The figure highlights the smooth transition of current from the resistive load to the resistive-inductive load. These hardware results confirm that the PB 13-level inverter effectively manages both static and dynamic load conditions.

7. Conclusion

The proposed high-gain, single-source multilevel inverter (MLI) offers significant advancements for renewable energy applications. By utilizing a novel topology with a single DC source and incorporating switched capacitors, the design achieves a remarkable voltage boost without the need for additional DC-DC converters or transformers. The inverter efficiently produces thirteen voltage levels using just 10 power switches and three capacitors, resulting in a compact and cost-effective solution. The inclusion of a selective harmonic removal technique, powered by artificial neural networks (ANN), successfully reduces total harmonic distortion (THD) to 6.07 %, further enhancing output quality. The system's overall efficiency of 96.9 %, combined with its reduced component count and lower total standing voltage (TSV), underscores the design's practicality and superiority. The successful experimental validation of the system confirms its viability for real-world renewable energy applications, marking it as a promising solution for solar and wind power integration.

Data availability

The authors confirm that the data generated or analyzed during this study are included in this article. No additional data is available.

CRediT authorship contribution statement

Anand Kumar Thangapandi: Writing – review & editing, Writing – original draft, Validation, Supervision, Methodology, Formal analysis, Data curation, Conceptualization. **Amit Kumar:** Writing – review & editing, Writing – original draft, Supervision, Software, Methodology, Investigation, Formal analysis, Conceptualization. **Durgalakshmi Karthigeyan:** Writing – review & editing, Methodology, Investigation, Formal analysis, Data curation. **Suganthi Ramasamy:** Writing – review & editing, Validation, Software, Methodology, Investigation, Formal analysis, Data curation. **Venkatesh Arumugam:** Writing – review & editing, Validation, Investigation, Formal analysis. **Gianluca Gatto:** Writing – review & editing, Validation, Supervision, Resources, Project administration, Investigation, Funding acquisition.

Table 8
Experimental parameters.

Component	Part Number	Rating	Proposed
Switches	IRFP240	200V,20A	6
	IRFP350PBF	400 V,16A	2
	FIO 50-12BD	1200V,50A	2
Capacitor	B41231C9228M000	2200uF,100V	3

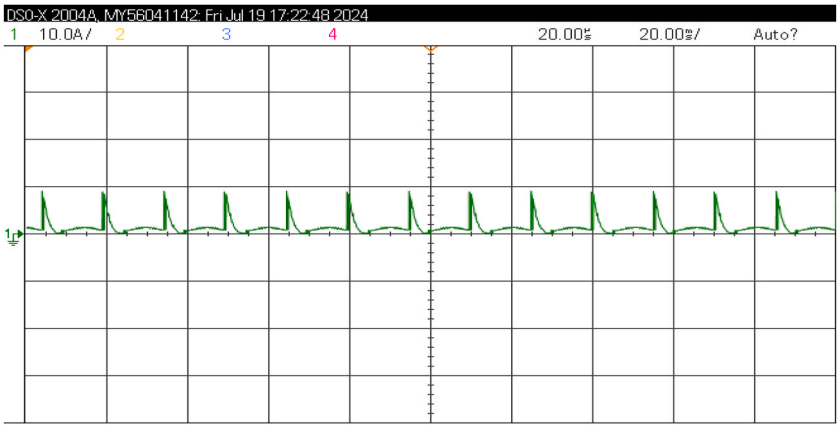


Fig. 19. Input current waveform of the proposed inverter during the load condition of R = 50Ω.

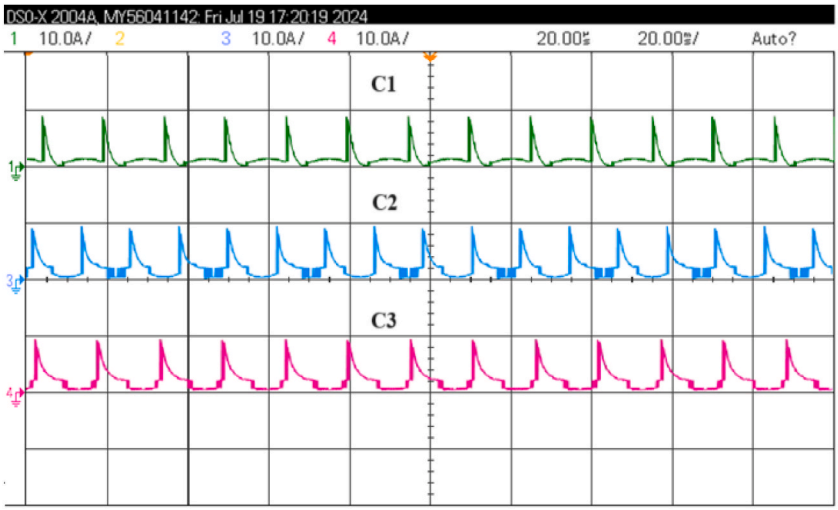


Fig. 20. Capacitor current (C1, C2 and C3) waveforms of the proposed inverter with R = 50Ω.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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