



Full Length Article



## Further characterisation of Digital Pixel Test Structures implemented in a 65 nm CMOS process

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## ARTICLE INFO

## Keywords:

Monolithic Active Pixel Sensors  
Solid state detectors

## ABSTRACT

The next generation of MAPS for future tracking detectors will have to meet stringent requirements placed on them. One such detector is the ALICE ITS3 that aims to be very light at 0.07 %  $X/X_0$  per layer and have a low power consumption in the active area of 40 mW/cm<sup>2</sup> by implementing wafer-scale MAPS bent into cylindrical

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Received 12 May 2025; Received in revised form 19 September 2025; Accepted 10 October 2025

Available online 14 October 2025

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half layers. To address these challenging requirements, the ALICE ITS3 project, in conjunction with the CERN EP R&D on monolithic pixel sensors, proposed the Tower Partners Semiconductor Co. 65 nm CMOS process as the starting point for the sensor. After the initial results confirmed the detection efficiency and radiation hardness, the choice of the technology was solidified by demonstrating the feasibility of operating MAPS in low-power consumption regimes,  $< 50 \text{ mW/cm}^2$ , while maintaining high-quality performance. This was shown through a detailed characterisation of the Digital Pixel Test Structure (DPTS) prototype exposed to X-rays and ionising beams, and the results are presented in this article. Additionally, the sensor was further investigated through studies of the fake-hit rate, the linearity of the front-end in the range 1.7–28 keV, the performance after ionising irradiation, and the detection efficiency of inclined tracks in the range 0–45°.

## 1. Introduction

Monolithic Active Pixel Sensors (MAPS) incorporate the charge-sensitive volume and the read-out circuitry in one piece of silicon and can be fabricated in standard CMOS processes. This allows for a sensor that has promising characteristics for tracking detectors, such as low capacitance, low mass and low power consumption. MAPS were intensively developed and used over the last decade [1]. MAPS have demonstrated their suitability for operation in high-energy physics experiment vertex and tracking detectors [2]. The most recent implementation of a large-area MAPS detector was the Inner Tracking System 2 (ITS2) for the ALICE experiment at CERN [3,4]. The ITS2 uses the ALPIDE chip [5,6], which was fabricated in the TowerJazz 180 nm CMOS process and showed excellent performance in terms of detection efficiency ( $\gg 99\%$ ) and spatial resolution (about  $5 \mu\text{m}$ ).

The ITS2 will undergo an upgrade called the ITS3, where the three innermost tracking layers will be replaced during the LHC Long Shutdown 3 (2026–2028) [7]. The ITS3 employs wafer-scale MAPSs with a length of 260 mm that are thinned to  $\leq 50 \mu\text{m}$  to reduce the material in the detector. These sensors are required to have power consumption below  $40 \text{ mW/cm}^2$  in the active area so that operation at temperatures achievable by air cooling  $O(+25 \text{ }^\circ\text{C})$  is possible [8]. Due to the challenging requirements imposed on the next generation of MAPS detectors, the Tower Partners Semiconductor Co. (TPSCO) 65 nm CMOS imaging process [9] was chosen as the starting point for sensor development. The first submission in the 65 nm CMOS process, in conjunction with the CERN EP R&D on monolithic pixel sensors [10], was called Multi-Layer Reticle 1 (MLR1). It contained many different test structures to fully explore the feasibility of using the CMOS process for use in future detectors [11].

With the first set of results from the MLR1 demonstrating the detection efficiency and radiation hardness of the 65 nm technology [12,13], further investigations into the performance of the technology were carried out. Therefore, a MAPS prototype called the Digital Pixel Test Structure (DPTS) was characterised by fluorescence X-rays and ionising particles from a beam, the results of which are presented in this paper.

Since one of the crucial requirements for the next generation of MAPS is reduced power usage, a particular focus was placed on the operation and performance of the sensor in low-power settings. Given that the active region of the final ITS3 stitched sensor will be a complex design with many components, and the DPTS is a simpler design, a comparison of the active region power consumption is not appropriate. Instead, because the two chip designs have similar pixel architectures, the pixel matrix power consumption will be used for a more representative comparison. The target for the pixel matrix power consumption of the ITS3 sensor is  $15 \text{ mW/cm}^2$  for a pixel pitch of  $20.8 \times 22.8 \mu\text{m}$  [8]. In addition, the performance after ionising irradiation, a study of the Fake-Hit Rate (FHR), the evaluation of the linearity of the front-end, and the response to inclined tracks were also examined.

## 2. The DPTS chip

The DPTS sensor measures  $1.5 \text{ mm} \times 1.5 \text{ mm}$ , features a  $32 \times 32$  pixel matrix with a pitch of  $15 \mu\text{m}$  and contains full-CMOS circuitry [12,14]. This allows a digital front-end in each pixel, including an amplifier,

shaper, and discriminator, as detailed in [12]. Furthermore, a test circuitry that injects an externally controlled test charge is also present in the pixel. The sensor can be configured by the shift register located on the periphery, allowing pixel masking and pixel selection for pulsing. The sensor is controlled by external reference currents and voltages and is read out via a Current-Mode Logic (CML) output [15]. All pixels are read out simultaneously via a differential digital output that encodes the pixel position and Time-over-Threshold (ToT).

The steady-state front-end power consumption of a pixel is given by the currents  $I_{bias}$ ,  $I_{biasn}$ ,  $I_{db}$ , and  $I_{reset}$  multiplied by the supply voltage (+1.2 V). Since the reset current is orders of magnitude lower than the other currents (pA compared to nA) and the  $I_{db}$  current in the discriminator branch flows only while the discriminator is active, the total current of the pixel is given by the main branch,  $I_{bias}$ . Thus, the lowest possible power consumption is  $12 \text{ nW}$  per pixel due to  $10 \text{ nA}$  being the lowest operational  $I_{bias}$  setting.

## 3. Laboratory measurements

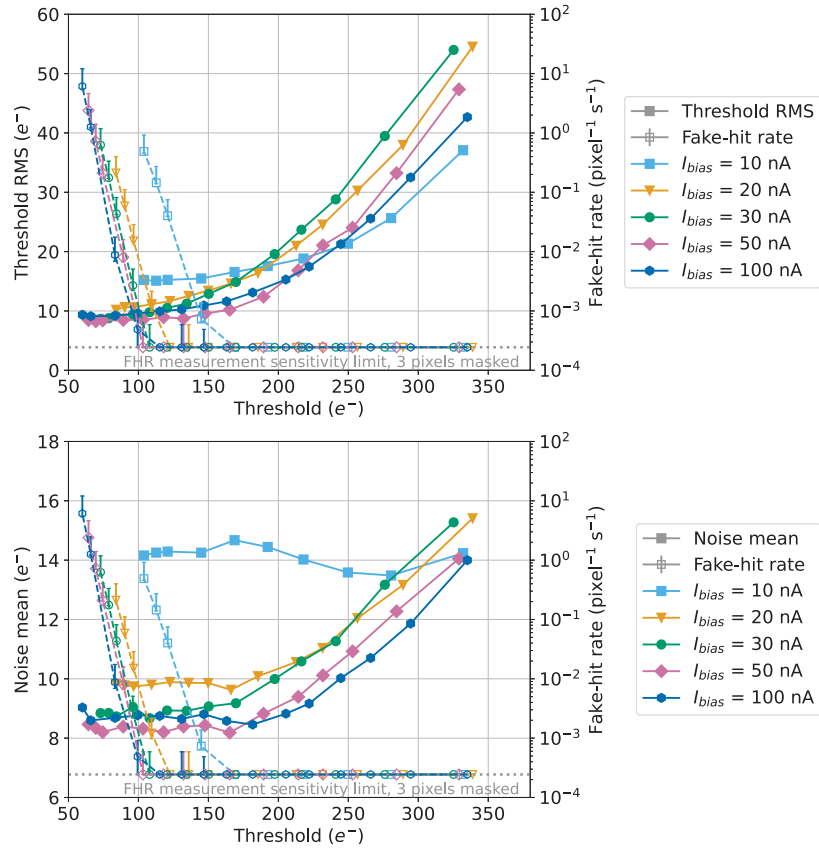
### 3.1. Data acquisition setup

The biases and control signals are supplied to the DPTS chip via a custom-made setup, allowing the control of the in-pixel front-end. The chip biases are set to the so-called “nominal” values defined by the design operating point, as described in Ref. [12], unless otherwise stated or varied in the measurement. For measurements that varied the reverse bias ( $V_{sub}$  and  $V_{puell}$ ), both chip bias voltages that control the amplifier ( $V_{casb}$  and  $V_{casn}$ ) were adjusted accordingly [12]. The digital signals from the chip are read out via a CML output and recorded on an oscilloscope with a sampling rate of 5 GS/s and a bandwidth of 500 MHz.

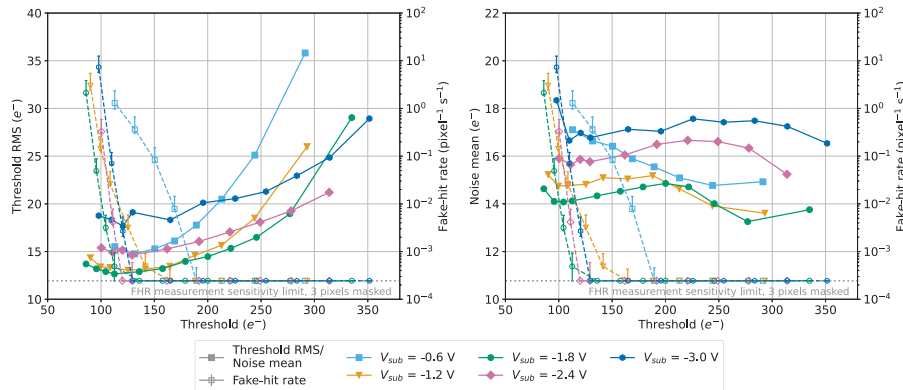
### 3.2. Performance at low power consumption

As mentioned in Section 2, the sole contributor to the DPTS pixel matrix power consumption is the chip current bias parameter called  $I_{bias}$ . Thus, the performance at low power consumption levels was investigated by measuring the pixel threshold spread (threshold RMS), pixel noise (width of the s-curve) and FHR (number of noise hits per pixel per second in the absence of external stimuli) at the  $I_{bias}$  values of 10, 20, 30, 50 and  $100 \text{ nA}$ . These values correspond to a pixel matrix power consumption of 5.3, 10.6, 15.9, 26.5 and  $53 \text{ mW/cm}^2$ , respectively. In contrast to the previous results [12], where  $I_{bias}$  was varied while keeping the other settings at their “nominal” values, in this study, the chip bias settings at each  $I_{bias}$  were optimised to obtain the best performance. The optimised chip biases were  $V_{casn}$ ,  $I_{reset}$  and  $I_{db}$ . For comparison, the measurements at  $I_{bias} = 100 \text{ nA}$  are left at the “nominal” settings.

Fig. 1 shows the chip’s performance as a function of the threshold for low  $I_{bias}$  values. It can be seen that there is a small difference between the results at the thresholds  $< 200 e^-$  for  $I_{bias} = 30\text{--}100 \text{ nA}$ . This indicates some margin for lowering the power consumption with only a minimal impact on the performance. Whereas, for  $I_{bias} = 20 \text{ nA}$ , the threshold RMS and the noise mean are slightly larger, and the onset



**Fig. 1.** The threshold RMS and fake-hit rate vs. threshold (top) and the noise mean and fake-hit rate vs. threshold (bottom) at different  $I_{bias}$  values. At each  $I_{bias}$ , the chip bias parameters were optimised, except  $I_{bias} = 100$  nA, which is left at the “nominal” settings for comparison.



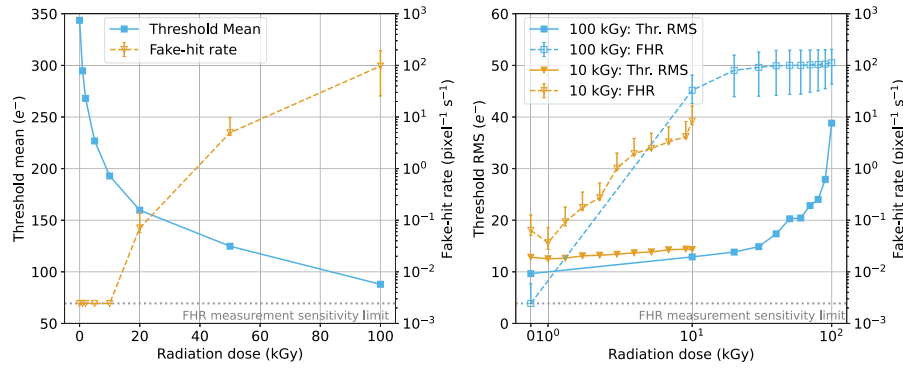
**Fig. 2.** The threshold RMS and fake-hit rate vs. threshold (left) and the noise mean and fake-hit rate vs. threshold (right) at varying  $V_{sub}$  values at  $I_{bias} = 10$  nA. At each  $V_{sub}$ , the chip bias parameters were optimised.

of the FHR happens at slightly larger thresholds. This performance reduction continues for  $I_{bias} = 10$  nA but is more prominent, particularly for the noise mean and the FHR.

An option to improve the performance at the very low power consumption operating points is to increase the reverse bias ( $V_{sub}$ ). This is shown in Fig. 2, which exhibits an improvement in terms of the onset of the FHR when increasing  $V_{sub}$  from  $-1.2$  V to  $-3$  V. However, in terms of threshold RMS and noise mean, only  $-1.8$  V has marginally lower values, whereas for  $-2.4$  V and  $-3$  V, the values are larger. These results indicate that at the lowest power setting, there are minimal improvements in the performance above  $V_{sub} = -1.2$  V.

### 3.3. Performance after ionising irradiation

The evolution of the chip performance, in terms of threshold and fake-hit rate, was measured during the irradiation of several sensors using 10 keV X-rays from a tungsten target at CERN. The impact of the radiation dose at constant chip bias parameters is shown in Fig. 3(left), demonstrating that the threshold mean decreases and the fake-hit rate increases. This suggests that the radiation changes the chip’s operating point, which can be accounted for by changing  $V_{casb}$ . To disentangle the effect of the changing threshold on the fake-hit rate, the performance was also measured while tuning the threshold to a constant value of



**Fig. 3.** Left: the threshold mean and fake-hit rate vs. ionising radiation dose at a constant  $V_{casb}$ . Right: the threshold RMS and fake-hit rate vs. ionising radiation dose at a threshold tuned to  $125 e^-$  for two chips irradiated to different dose levels, 10 kGy and 100 kGy, at different rates.

$125 e^-$  during the irradiation. The value of  $125 e^-$  was chosen so that the FHR would be visible at low doses, but not so high that the chip becomes inoperable at higher doses. The results for two chips irradiated to different dose levels, 10 kGy and 100 kGy, at different rates are shown in Fig. 3(right). It can be seen that the fake-hit rate at a constant threshold increases with radiation dose, increasing by approximately two orders of magnitude from 0–10 kGy. For the threshold RMS, a slight increase is seen from 0–10 kGy, but above this range, it increases rapidly.

The chip performance was also evaluated as a function of the time elapsed since the end of the irradiation. This annealing was performed at a constant temperature of  $21\text{--}22^\circ\text{C}$  as the irradiated chips were stored and tested in a temperature-controlled laboratory. Fig. 4(left) shows the annealing effect on a chip with a total dose of 500 kGy at constant chip bias parameters. After the irradiation, the fake-hit rate decreases by an order of magnitude within the first day. The sharp drop in the fake-hit rate is likely due to a power cycle of the chip that occurred during this time. The general trend of the threshold mean is that it increases with annealing time. Immediately after the irradiation, the points where the threshold is 0 indicate that the chip is inoperable. After this, the chip begins to recover and the threshold can be measured. Once again, the sharp fluctuations are likely caused by power cycles.

Fig. 4(right) shows the performance of a chip tuned to a threshold of  $125 e^-$  with a total dose of 100 kGy. The threshold tuning was performed before each threshold measurement on a subset of pixels. Here, the fake-hit rate remains constant until three days after the irradiation, at which point the fake-hit rate starts to decrease. The same trend is also seen in the threshold RMS. These measurements have been performed on several different chips at doses of 10, 100 and 500 kGy, and they all show similar trends.

Another way to evaluate the chip performance after ionising irradiation is to compare the  $^{55}\text{Fe}$  spectra. To perform this test, X-ray emissions from an  $^{55}\text{Fe}$  source illuminating the top side of the chip at a distance of approximately 12 mm were measured. Three selections were applied to the data: keeping only single pixel clusters, removing all the edge pixels and removing the pixels whose hit rates are five standard deviations above the mean. A ToT calibration for each pixel is then applied to account for the variation in the pixel-to-pixel response, and a charge calibration to convert the measured ToT in mV to  $e^-$  is applied individually for each chip [12]. Fig. 5 shows the spectra for a non-irradiated chip and chips irradiated to 10, 100, 500 kGy and 5 MGy, where it can be seen that there is a negligible difference in the position, height and width of the Mn- $K_\alpha$  peak. This indicates, as expected, that ionising radiation has no impact on the charge collection up to dose values of 5 MGy.

However, the influence of ionising irradiation on the front-end electronics is seen by comparing the measured  $^{55}\text{Fe}$  spectrum of the

**Table 1**

Measured charge calibration factors before and after irradiation of the same sensor for chips at different levels of ionising irradiation.

Dose (kGy)	Calibration before	Calibration after
10	$1.045 \pm 0.067$	$1.080 \pm 0.077$
100	$1.044 \pm 0.077$	$1.104 \pm 0.082$
500	$1.054 \pm 0.071$	$1.124 \pm 0.087$

same chip before and after irradiation tuned to the same threshold ( $200 e^-$ ), as shown in Fig. 6. A threshold of  $200 e^-$  was chosen to ensure that, after irradiation, the sensor's FHR would remain low enough not to contribute a significant number of noise hits. The irradiation causes a shift of the Mn- $K_\alpha$  peak to lower ToT values, which points to an influence of the irradiation on the ToT calibration. Further evidence of this change is shown in Table 1, where the charge calibration (conversion factor of the ToT from mV to  $e^-$ ) is given before and after irradiation for different dose levels with 81 days of annealing measured at the same conditions. As the dose level increases, so does the difference in the charge calibration.

### 3.4. Fake-hit rate

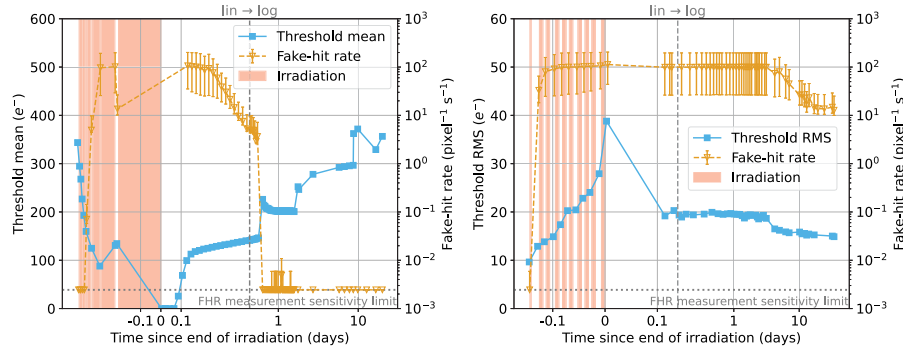
An important quantity for evaluating the sensor performance is the FHR, and how this quantity evolves with the chip biasing has already been measured [12]. The FHR is defined as the number of noise hits per pixel per second in the absence of external stimuli. For a MAPS, there are two main contributions to the total FHR: thermal noise and random telegraph noise (RTN). The contribution of thermal noise is random and can be modelled by a function that determines the probability that a pixel has a fake hit at a certain threshold. Assuming the thermal noise follows a zero-mean Gaussian distribution with standard deviation  $n_p$ ,  $\mathcal{N}(x|0, n_p)$ , the probability of a fake hit is given by

$$f(t_p, n_p) = \int_{t_p}^{\infty} \mathcal{N}(x|0, n_p) dx = \frac{1}{2} \operatorname{erfc} \left( \frac{t_p}{\sqrt{2}n_p} \right), \quad (1)$$

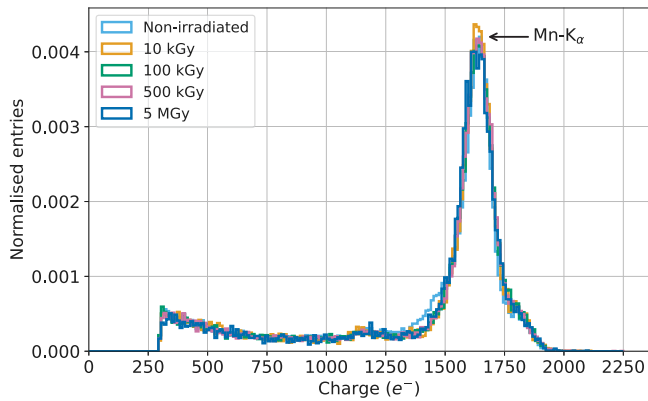
where  $t_p$  and  $n_p$  are the threshold and noise of the pixel given by an s-curve measurement. To account for the pixel-to-pixel change in threshold and noise, the average fake-hit rate over the whole matrix is given by the expectation value of  $f(t_p, n_p)$  [16]. Assuming the threshold and noise distributions are Gaussian, and partially solving gives:

$$\overline{\text{FHR}}(\mu_t, \sigma_t, \mu_n, \sigma_n) = \frac{1}{2} \int_0^{\infty} \operatorname{erfc} \left( \frac{\mu_t}{\sqrt{2}\sqrt{n^2 + \sigma_t^2}} \right) \mathcal{N}(n|\mu_n, \sigma_n) dn, \quad (2)$$

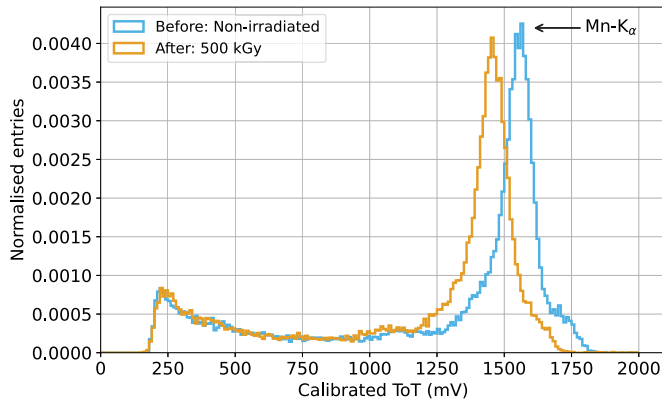
where  $\mu_t$  and  $\sigma_t$  are the mean chip threshold and threshold RMS,  $\mu_n$  and  $\sigma_n$  are the mean chip noise and noise RMS, and  $\mathcal{N}(n|\mu_n, \sigma_n)$  is a normal



**Fig. 4.** Left: the threshold mean and fake-hit rate vs. the time since the end of the irradiation at a constant  $V_{cass}$  for a chip with a total dose of 500 kGy. Right: the threshold RMS and fake-hit rate vs. the time since the end of the irradiation at a threshold tuned to  $125 e^-$  for a chip with a total dose of 100 kGy. The red boxes indicate the period during which the sensor underwent irradiation.



**Fig. 5.** Measured  $^{55}\text{Fe}$  spectra of single pixel clusters for different levels of ionising irradiation: non-irradiated, 10, 100, 500 kGy and 5 MGy.



**Fig. 6.** Measured  $^{55}\text{Fe}$  spectra of single pixel clusters of the same chip before and after an irradiation dose of 500 kGy tuned to the same threshold ( $200 e^-$ ).

distribution with mean  $\mu_n$  and standard deviation  $\sigma_n$ . The remaining integral in Eq. (2) has to be solved numerically. There is no simple model for the RTN noise contribution to the FHR, so it is not included in the FHR model.

Measurements of the FHR for non-irradiated DPTS chips at the ‘nominal’ settings were performed as a function of the threshold with  $5 \times 10^6$  triggers at a constant  $+20^\circ\text{C}$ . A comparison of the measured results with the thermal FHR model described in Eq. (2) is shown in Fig. 7. In total, three chips were measured and compared to the thermal model, and all show the same trends. To avoid selection bias and for visualisation purposes, the first chip that was measured was chosen

to be presented in the paper. For the non-masked results, there is a large difference between the thermal model and the measurements, indicating that the thermal contribution is not the dominant noise source.

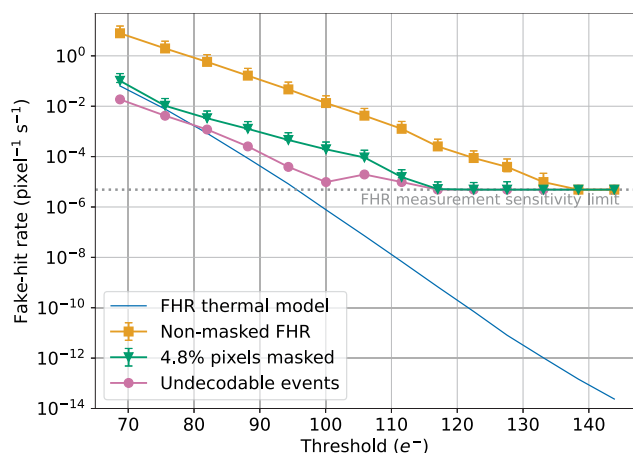
A mask was then applied to the results by cutting pixels with a hit frequency higher than ten times the matrix mean frequency, resulting in 4.8% pixels masked. This masking reduces the FHR by around 2 orders of magnitude, indicating a large contribution from pixels that systematically give a hit, the so-called hot pixels. A hot pixel may occur due to defects within the pixel, causing its threshold to deviate significantly from the mean or resulting in high s-curve noise. The masked FHR results show agreement with the thermal FHR model at low thresholds ( $70\text{--}80 e^-$ ), above which the measured values start to deviate from the model, signifying that other sources are significantly contributing to the masked FHR. One such contribution could be from the undecodable events (and thus unmaskable) that arise when hits clash on the CML output (cf. Section 2). Another source, particularly at higher thresholds, could be RTN.

Overall, the main source of noise for the DPTS comes from the hot pixels. After masking these pixels, the contributions to the FHR are thermal noise at low thresholds, and the undecodable events and RTN at larger thresholds. A further validation of the thermal FHR model described here is needed and will be performed with the next generation of chip. This chip will not suffer from undecodable hits due to its different readout architecture, enabling a more thorough investigation of the agreement between the model and the FHR at lower thresholds

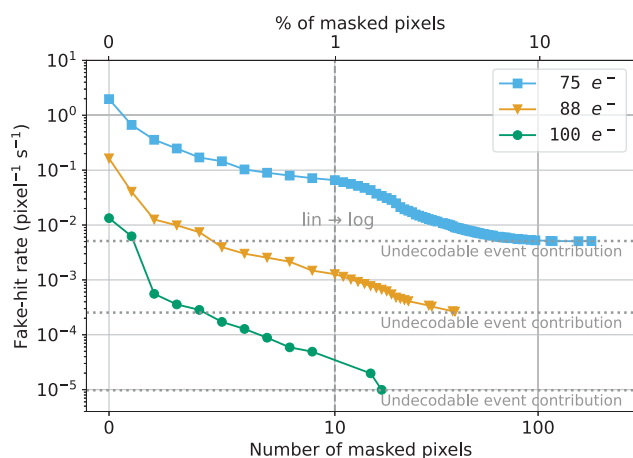
Another important aspect to understand about FHR is how it varies with the number of pixels masked, as shown in Fig. 8 for three threshold values: 75, 88 and  $100 e^-$ . By masking 10 pixels (less than 1%), the FHR reduces by more than an order of magnitude, demonstrating that the FHR for this sensor is dominated by a few pixels that are consistently registering a hit. As the threshold increases, the reduction in FHR from masking 10 pixels becomes more pronounced. Masking additional pixels further reduces the FHR, albeit to a lesser extent, and eventually the FHR plateaus. This plateau occurs because the contribution to the FHR from undecodable events cannot be masked, indicating a non-negligible contribution from such hits. If these hot pixels can be identified and are few, they can be masked online, allowing the FHR to be lower and reducing the likelihood of having undecodable events.

#### 4. Measurements of fluorescence X-rays emitted from a target

The DPTS sensor was characterised by fluorescence X-rays to evaluate the linearity of the front-end from 1.7 to 28.5 keV. The measurement campaign took place from May 2023 to June 2023 at the OptimaTo (Optimal Imaging and Tomography) laboratory [17], located at Elettra Sincrotrone Trieste (Italy) [18].



**Fig. 7.** The measured fake-hit rate (line and dot markers) with different levels of masking, the contribution from undecodable events (orange) and the FHR model (blue line) as a function of threshold. Data were taken with  $5 \times 10^6$  triggers at a constant temperature of  $+20^\circ\text{C}$ .



**Fig. 8.** The measured fake-hit rate as a function of the number of pixels masked at three threshold values: 75, 88 and  $100 e^-$ . The  $x$ -axis initially uses a linear scale, but after reaching 10, it switches to a logarithmic scale.

**Table 2**  
Energies of the characteristic peaks [19] of the primary beam.

Peak	Energy (keV)
Ga $K\alpha$	9.2
In $K\alpha$	24.2
Sn $K\alpha$	25.2

#### 4.1. Setup

A microfocus liquid metaljet X-ray source (Excillum D2+, 160 kV, Sweden) with a Galinstan alloy anode was used to produce the primary X-ray beam. A conical X-ray beam exits the source through a window with a 13-degree opening angle, and a copper collimator was used to further reduce the beam divergence. The energy spectrum of the beam was a continuum Bremsstrahlung, adjustable in the range 30–160 kV and contained characteristic lines of Gallium, Indium and Tin emissions (Table 2).

Manganese and tin foils were used as targets and placed in the beam with an angle of  $45^\circ$  relative to the beam direction. The characteristic emissions of manganese and tin are shown in Table 3. The DPTS was placed parallel to the target at approximately 10 cm, with the top side

**Table 3**  
Energies of the characteristic peaks [19] of the manganese and tin targets.

Peak	Energy (keV)
Mn $K\alpha$	5.9
Mn $K\beta$	6.5
Sn $K\alpha$	25.3
Sn $K\beta$	28.5
Sn $L\alpha$	3.4

facing the incoming fluorescence emissions. This position was chosen to remove the detector from the conical beam and reduce unwanted hits from the primary X-rays. However, hits from Compton scattering of the primary beam on the target are still possible. A picture of the setup is shown in Fig. 9.

The custom-made setup presented in Section 3.1 was used to operate the DPTS. The chip biases were set to the nominal values except for  $V_{casb}$ , which was set to 250 mV to tune the threshold to  $150 e^-$  to reduce the chance of a noise hit.

#### 4.2. Results

The data were analysed as described in Section 3.3 for the  $^{55}\text{Fe}$  spectrum. An additional selection that removes pixels with bad position encoding has been applied to the data.

Fig. 10 shows the measured spectrum of fluorescence X-rays emitted from a manganese target. Five emission peaks are resolved in the spectrum (Fig. 10): the Mn- $K_\alpha$  and Mn- $K_\beta$  characteristic emission peaks, the Mn- $K_{\alpha,\beta}$  escape peak, the argon characteristic emission peak Ar- $K_{\alpha,\beta}$  and the silicon fluorescence peak Si- $K_{\alpha,\beta}$ . The Mn- $K_\alpha$  and Mn- $K_\beta$  peaks are fitted with a sum of two Gaussians. The escape and the Ar- $K_{\alpha,\beta}$  peaks are fitted with a Gaussian and a linear fit is used to reproduce the background. The silicon fluorescence peak is fitted with a Gaussian and an exponential fit is used to reproduce the background.

Fig. 11 shows the measured spectrum of fluorescence X-rays emitted from a tin target. The emission peaks that are resolved in the spectrum (Fig. 11) are the Sn- $K_\alpha$ , Sn- $K_\beta$  and Sn- $L_\alpha$  characteristic emission peaks, the argon characteristic emission peak Ar- $K_{\alpha,\beta}$ , the silicon fluorescence peak Si- $K_{\alpha,\beta}$  and the peaks originating from scattered X-rays from the primary source. The Sn- $K_\alpha$  peak, the Sn- $K_\beta$  peak and the closest peak from scattered X-rays are fitted with a sum of three Gaussians and an exponential fit is used to reproduce the background. In Fig. 11 the fit function is shown only for the Sn- $K_\alpha$  and the Sn- $K_\beta$  peaks. The Ar- $K_{\alpha,\beta}$  and the Sn- $L_\alpha$  peaks are fitted with a sum of two Gaussians and a linear background fit. The silicon fluorescence peak is fitted with a Gaussian, and an exponential fit is used to reproduce the background.

The values of the peaks measured for both targets are shown in Fig. 12. The data from the tin target are fitted with a linear function. The linearity is preserved up to 28.5 keV, the energy of the tin  $K_\beta$  emission.

#### 5. Measurements with ionising particle beams

Following the laboratory results previously shown in Section 3, the DPTS performance was also measured with ionising particle beams to further investigate the behaviour at low-power consumption settings and after ionising irradiation. Additionally, an investigation into the performance with inclined tracks was carried out. These studies took place from July 2022 to May 2023 at two test beam facilities: CERN PS and DESY [20], providing 10 GeV/c positive hadrons and 5.4 GeV/c electrons, respectively.

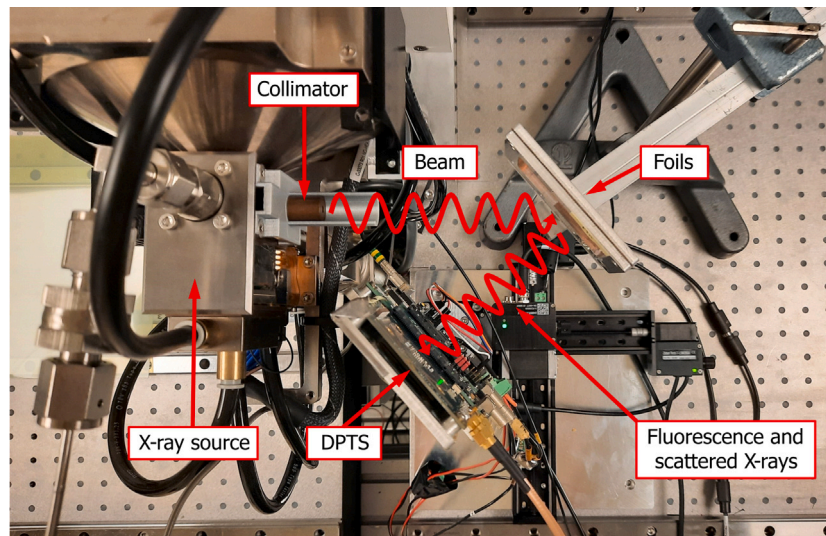


Fig. 9. A picture of the setup used to measure fluorescence X-rays emitted from either a Manganese or tin foil.

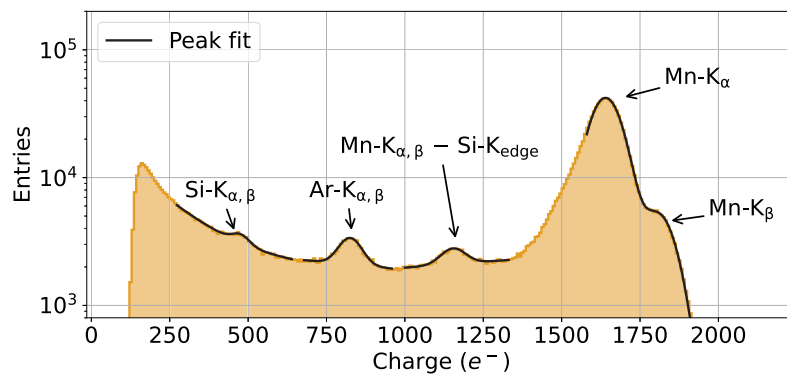


Fig. 10. Measured spectrum of fluorescence X-rays emitted from a manganese target. The sensor was able to resolve the manganese characteristic emission peaks ( $\text{Mn-K}_{\alpha}$  and  $\text{Mn-K}_{\beta}$ ), the  $\text{Mn-K}_{\alpha,\beta}$  escape peak ( $\text{Mn-K}_{\alpha,\beta} - \text{Si-K}_{\text{edge}}$ ), the argon characteristic emission peak ( $\text{Ar-K}_{\alpha,\beta}$ ) and the silicon fluorescence peak ( $\text{Si-K}_{\alpha,\beta}$ ).

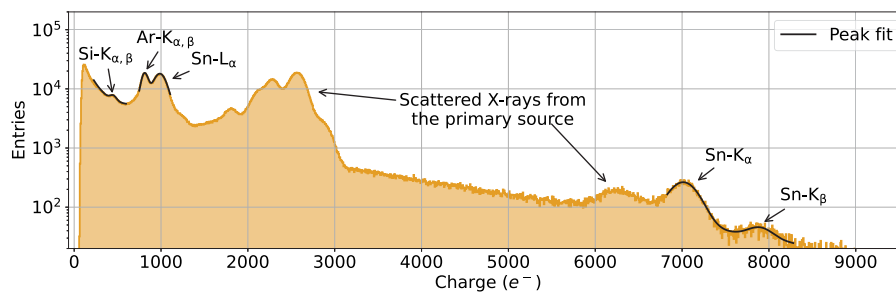


Fig. 11. Measured spectrum of fluorescence X-rays emitted from a tin target. The sensor was able to resolve the Sn characteristic emission peaks ( $\text{Sn-K}_{\alpha}$ ,  $\text{Sn-K}_{\beta}$ ,  $\text{Sn-L}_{\alpha}$ ), the argon characteristic emission peak ( $\text{Ar-K}_{\alpha,\beta}$ ) and the silicon fluorescence peak ( $\text{Si-K}_{\alpha,\beta}$ ).

### 5.1. Setup

The setup consists of a beam telescope with six reference planes, each equipped with an ALPIDE chip. These planes provide space points for track reconstruction for two DPTS sensors installed at the centre of the telescope with three reference planes on either side, Fig. 13. One of the DPTSs was the device under test (DUT), while the other was used as a trigger. This trigger DPTS was installed on a micro-positioning stage to control the  $x$  and  $y$  movement so that an overlap with the DUT was

made. The data acquisition was based on the EUDAQ2 framework [21]. During the measurements with inclined tracks, the DUT's rotation around the  $y$ -axis was controlled with a rotational stage with an angle of  $0^\circ$  being the “nominal” position, i.e. the DUT is perpendicular to the beam. To account for the rotational stage, the distances to the adjacent planes on either side of the DUT were increased. For the measurements performed during the power-consumption and ionising-radiation studies, an aluminium jig with a 1 mm hole aligned to the position of the chip was used to cool and keep the DUT at a constant temperature of  $+20^\circ\text{C}$ .

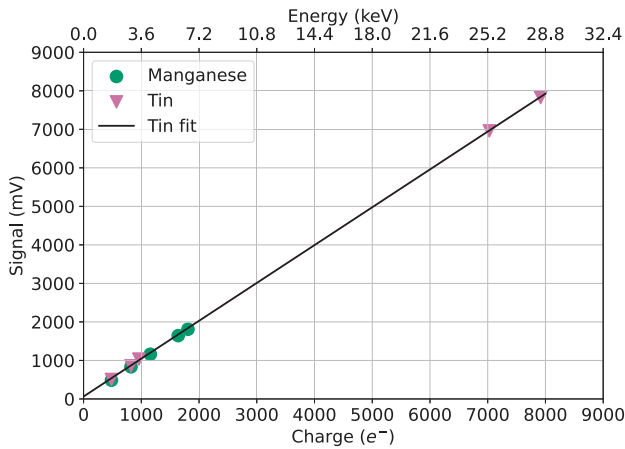


Fig. 12. The measured peak values as a function of the literature peak values for both the manganese and tin targets. A linear function is fit to the peaks of the tin target.

### 5.2. Analysis tools and methods

The Corryvreckan test beam data reconstruction framework [22] was used to process and analyse the data. This was done by reconstructing tracks from clusters on the reference planes with the General Broken Lines model [23] and interpolating the track position on the DUT(s). To ensure a high quality of the data sample, several track and event selection criteria were applied: only one track per event, a reduced track  $\chi^2 < 3$ , each track must have one hit on each reference plane, and tracks must not intersect the DUT within two pixel pitches from the sensor edge. Fake hits were kept to a minimum by masking pixels on the reference planes with too large a hit rate (more than 1000 times the average;  $< 1$  pixel per plane were affected). For the DUT, the probability of associating a fake (noise) hit to a track was minimised by requiring the response to be within  $3 \mu\text{s}$  of the trigger signal.

In the detection efficiency analysis, the non-decodable events arising from readout signal collisions on the CML lines were associated with the pixel (15, 15). These events are considered as real hits with an undetermined position due to the negligible likelihood that two fake hits coincide in time and result in a non-decodable event. As a result, a loose spatial selection is applied to ensure the efficiency is not underestimated by not including the non-decodable hits. This selection is a circular acceptance window of  $480 \mu\text{m}$  in radius used to associate clusters on the DUT to tracks.

In the timing resolution analysis, a spatial acceptance window selection with a radius of  $45 \mu\text{m}$  is used, but no timing selection is applied. Without an external trigger, the trigger DPTS was used as a timing reference and its chip biases were kept at the “nominal” settings throughout the measurements. Two corrections were applied to the measured DUT signal time accounting for the column delay and the time walk.<sup>1</sup> The time residuals between the DUT and the trigger DPTS were then fit with a Gaussian to obtain the standard deviation  $\sigma$ . To estimate the timing resolution of the trigger DPTS, three factors need to be considered: the trigger DPTS was used as a reference, the timing resolution does not depend on chip biases other than  $I_{bias}$ , and there is a similar timing resolution performance for the DUT and trigger DPTSs. Therefore, the trigger timing resolution at the “nominal”  $I_{bias} = 100 \text{ nA}$  was estimated to be  $\sigma/\sqrt{2}$ , resulting in a value of  $\sigma_{TRG} = 28.3 \text{ ns}$ . Finally, the DUT timing resolution for other  $I_{bias}$  values was calculated using  $\sigma_{DUT} = \sqrt{\sigma^2 - \sigma_{TRG}^2}$ .

<sup>1</sup> These corrections were not possible with the trigger DUT since it was used as a timing reference.

### 5.3. Performance at low power consumption

Although previous performance results of the DPTS sensor are reported at a comparably high conservative pixel current of  $I_{bias} = 100 \text{ nA}$  [12] and thus a high power consumption setting (cf. Section 2), the sensor performance at low power consumption is of special interest for air cooling solutions in a future application of the technology.

Fig. 14 shows the dependence of the detection efficiency and the fake-hit rate, measured in situ, on the mean chip threshold achieved by supplying different voltages for  $V_{cath}$  at various power consumption settings ranging from  $I_{bias} = 100 \text{ nA}$  to the lowest possible  $I_{bias} = 10 \text{ nA}$ . The nominal reverse bias voltage of  $-1.2 \text{ V}$  is supplied and the remaining biasing parameters are individually optimised for each  $I_{bias}$  setting. The three noisiest pixels, determined by their accumulated hit occupancy during data analysis, are masked. Starting at  $100 \text{ nA}$  and reducing  $I_{bias}$ , it appears that the threshold margin in which efficiency remains above 99% is reduced and the onset of the FHR occurs at higher thresholds. For the ITS3, a FHR below  $0.01 \text{ pixel}^{-1} \text{ s}^{-1}$  is required. Thus, an  $I_{bias}$  current of at least  $30 \text{ nA}$  is needed to be below this and reach 99% efficiency. This results in a pixel matrix power consumption of  $15.9 \text{ mW/cm}^2$  for the DPTS but for the ITS3 sensor, with a larger pitch of  $20.8 \times 22.8 \mu\text{m}$ , this reduces to  $7.6 \text{ mW/cm}^2$ , which is below the required target of  $15 \text{ mW/cm}^2$  [8]. As with the laboratory measurements in Section 3.2, the chip performance drops considerably once at  $20 \text{ nA}$  and particularly for  $10 \text{ nA}$  where an efficiency of 99% is not reached.

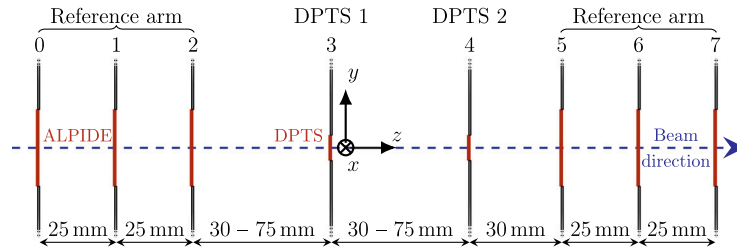
To study the effect of radiation, the results are shown in Fig. 15 for a proton irradiated sensor having received a combination of an ionising dose of  $10 \text{ kGy}$  and a non-ionising dose of  $10^{13} \text{ 1 MeV n}_{eq} \text{ cm}^{-2}$  (satisfying the requirements of ITS3 [8]). Despite the shift in operational range, the irradiated chip shows no performance degradation in terms of efficiency and FHR performance compared to that of the non-irradiated chip. The irradiated chip can reach an efficiency of 99% at  $I_{bias} = 10 \text{ nA}$ ; however, this is likely attributed more to chip-to-chip variations than the irradiation.

The influence of the reverse bias voltage at  $I_{bias} = 10 \text{ nA}$  was also investigated for the non-irradiated chip and found a marginal improvement in performance when increasing  $V_{sub}$ , but not significantly enough to justify having the chip operate in a very low-power consumption regime.

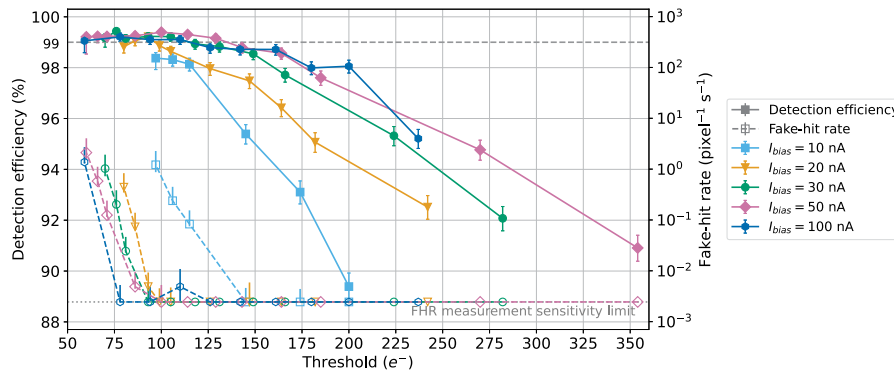
Further investigation of the chip performance at low power consumption was carried out by measuring the timing resolution. This is because  $I_{bias}$  directly influences the timing performance of the DPTS. The impact of varying  $I_{bias}$  on the timing resolution at a constant threshold is shown in Fig. 16 where it can be seen that decreasing  $I_{bias}$  from the “nominal” value of  $100 \text{ nA}$  increases the timing resolution.<sup>2</sup> This trend becomes more significant once the  $I_{bias}$  value drops below  $40 \text{ nA}$ , at which point, the time resolution increases more rapidly. For the three threshold values measured ( $110 e^-$ ,  $125 e^-$  and  $150 e^-$ ), there is a negligible influence of the threshold on the timing resolution.

Measurements of timing resolution were also carried out at chip bias settings that were optimised for each  $I_{bias}$  to obtain the best performance. A comparison of the timing resolution as a function of the threshold between a non-irradiated chip and a chip irradiated to the expected ITS3 levels ( $10 \text{ kGy}$  and  $10^{13} \text{ 1 MeV n}_{eq} \text{ cm}^{-2}$ ) is shown in Fig. 17. The influence of  $I_{bias}$  is evident in both chips. The effect of the threshold on the timing resolution is negligible for  $I_{bias}$  values  $> 30 \text{ nA}$ . For lower values of  $I_{bias}$ , the timing resolution increases for lower thresholds. The cause of this trend could be that, at the lower values of  $I_{bias}$ , the operating point of the chip becomes less stable and affects the chip’s performance. At the same threshold and  $I_{bias}$  values, the non-irradiated chip and the irradiated chip show the same timing resolution, indicating that this level of irradiation has no impact on the timing performance.

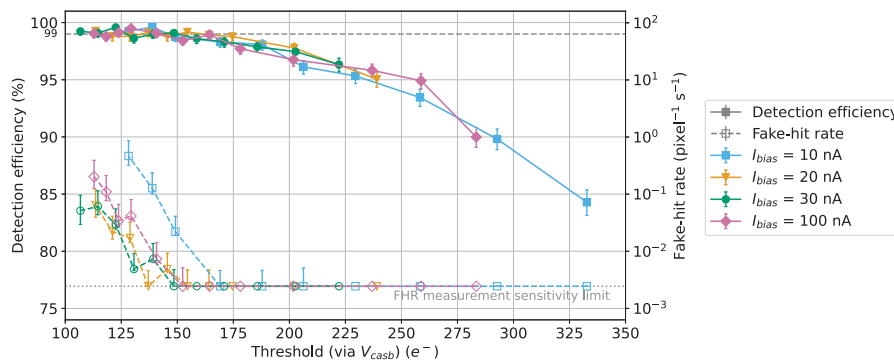
<sup>2</sup> The previous result of  $6.3 \text{ ns}$  [12] was not replicated due to the different trigger system and no timewalk correction applied to the trigger DPTS.



**Fig. 13.** A sketch of the beam telescope (not to scale) used to perform measurements with ionising particle beams. The setup consists of 6 ALPIDE reference planes and two DPTS sensors in the centre. The distances on either side of the DUT were increased to 75 mm to accommodate the rotational stage for the inclined track measurements.



**Fig. 14.** Detection efficiency (filled symbols, solid lines) and fake-hit rate (open symbols, dashed lines) as a function of the average threshold for a non-irradiated chip at different power consumption settings ( $I_{bias}$ ).



**Fig. 15.** Detection efficiency (filled symbols, solid lines) and fake-hit rate (open symbols, dashed lines) as a function of the average threshold for a proton irradiated chip at different power consumption settings ( $I_{bias}$ ) at  $V_{sub} = -1.2$  V. Three noisy pixels have been masked.

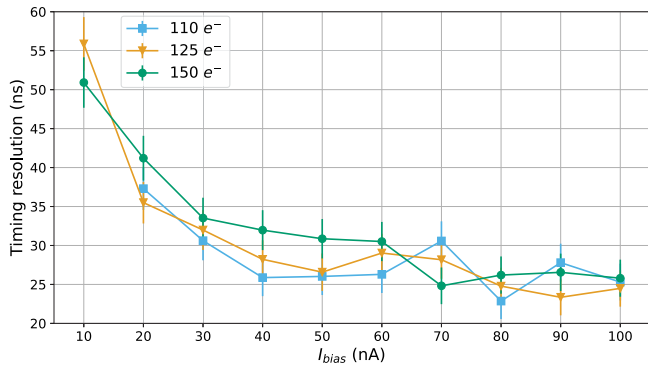


Fig. 16. The timing resolution as a function of  $I_{bias}$  at constant threshold values for a non-irradiated chip.

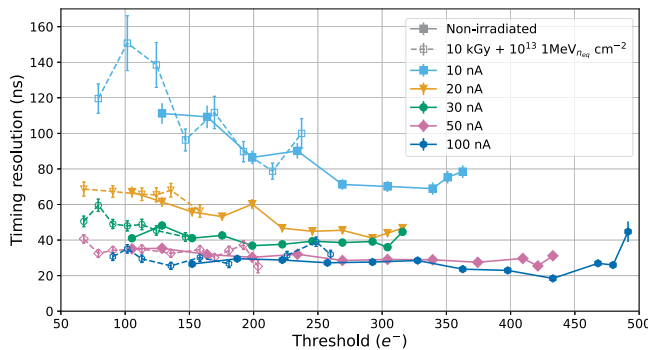


Fig. 17. The timing resolution as a function of the threshold at varying  $I_{bias}$  values for a non-irradiated chip (filled symbols, solid lines) and a proton irradiated chip (open symbols, dashed lines).

#### 5.4. Performance after ionising irradiation at nominal power consumption

Previously, it was shown that the DPTS sensor is radiation hard up to ionising doses of 100 kGy [12]. This radiation hardness was further tested by first irradiating the chips at CERN (cf. Section 3.3) at dose levels up to 5 MGy, then measuring the performance. Results of these irradiated chips are shown in Fig. 18, where the detection efficiency and fake-hit rate are shown as functions of the average threshold at “nominal” setting, except for  $V_{sub} = -3.0$  V where the best performance in terms of efficiency and FHR is seen [12]. It can be seen that a detection efficiency of 99% is reachable for all dose levels and that with increasing dose, the onset of the FHR occurs at higher thresholds. For the chip irradiated to 500 kGy, the impact of annealing on the chip is also seen, showing that the onset of the FHR occurs at lower thresholds when the chip is annealed for four months compared to 4 days. This means there is a larger operational region where the detection efficiency is above 99% and the FHR is below  $0.01 \text{ pixel}^{-1} \text{ s}^{-1}$ .

#### 5.5. Inclined tracks

In addition to the results taken with tracks at perpendicular incidence shown in [12], measurements were also taken in the angular range 0–45° at the “nominal” settings. Fig. 19 shows the detection efficiency as a function of the threshold for several track incident angles. For all angles, the detection efficiency increases with decreasing threshold. As the track angle increases, so does the detection efficiency and the range of threshold values in which the detection efficiency is above 99%. This is further demonstrated in Fig. 20.

The effect of the track incident angle on the cluster size at different threshold values was also investigated and is shown in Fig. 21. As expected, as the angle increases, so does the average cluster size, but

the cluster size only changes by <1 pixel over the whole angular range. Another important quantity to monitor is the number of undecodable events, which increases with angle, as shown in Fig. 21. This is because, with the larger cluster size, there is a greater chance of the hits clashing on the readout line. The change in the number of undecodable events is negligible for angles up to 20°, after which there is an increase of approximately 2%.

## 6. Conclusions

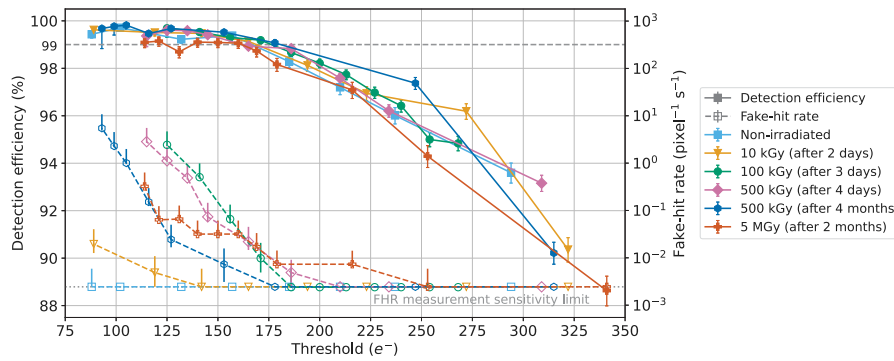
Additional measurements of the Digital Pixel Test Structure MAPS prototype to those previously presented [12] have been performed with a focus on the impact of operating the chip in low-power-consumption regimes as this is a key requirement of the ALICE ITS3 detector.

Laboratory measurements of the chip performance demonstrate that with a pixel matrix power consumption as low as  $15.9 \text{ mW/cm}^2$ , there is minimal impact on the threshold RMS, noise mean and fake-hit rate compared to the “nominal” value of  $53 \text{ mW/cm}^2$ . However, the performance degrades at lower pixel matrix power consumption values, particularly at the lowest value,  $5.3 \text{ mW/cm}^2$ . There is a marginal improvement by increasing the reverse bias to  $-1.8$  V. These trends are also seen in testbeam measurements where an excellent efficiency of above 99% is maintained down to  $10.6 \text{ mW/cm}^2$  and a timing resolution of below 100 ns is achieved even for the lowest pixel matrix power consumption settings. However, the DPTS is not able to maintain an efficiency of 99% at a FHR of below  $0.01 \text{ pixel}^{-1} \text{ s}^{-1}$  while having a pixel matrix power consumption of less than  $15 \text{ mW/cm}^2$ . This is expected to be improved in the final ITS3 sensor design, where, among design improvements, the pixel pitch will be larger, and thus the power density will be lower. The impact of larger pixel sizes on the performance has been studied in [8,13] and found to be within the ITS3 requirements in terms of detection efficiency and spatial resolution.

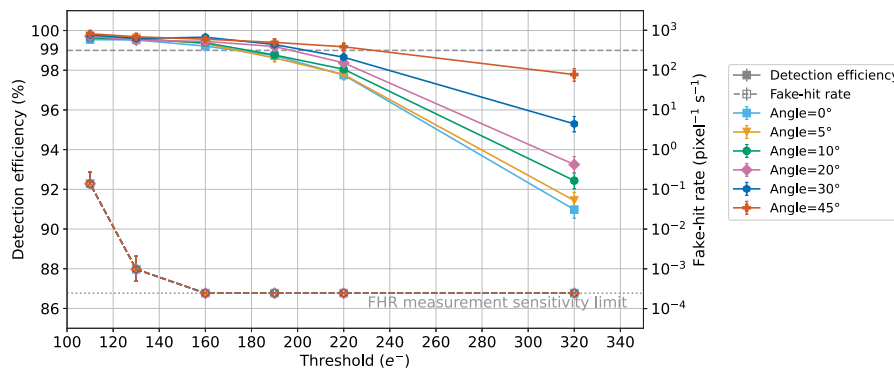
The impact of ionising radiation was measured, showing that the operating point of the chip is affected and the performance, in terms of threshold RMS and FHR, deteriorates. These impacts on performance can be reduced through annealing, with the largest improvement occurring after 3 days. X-ray emissions from an  $^{55}\text{Fe}$  source show that ionising radiation has a minimal impact on the charge collection but does impact the front-end electronics by reducing the measured ToT value of the Mn- $K_{\alpha}$  peak. In-beam measurements of the efficiency for sensors with accumulated dose up to 5 MGy further demonstrate the negligible impact of ionising radiation on the charge collection and the reduction in the fake-hit rate with annealing time.

Further measurements investigating the sources of the FHR for the DPTS showed that the dominant contributor was the hot pixels. Applying a mask to 5% of the pixels revealed that, below a threshold of  $80 e^{-}$ , the contribution from the thermal noise dominates, and above this threshold, the contribution from random telegraph noise and undecodable events dominates. Fluorescence X-rays from manganese and tin targets were used to demonstrate the linearity of the front-end for an energy range of 1.7 to 28.5 keV. Finally, measurements of inclined tracks showed that increasing the track angle up to 45° increases the detection efficiency and average cluster size. However, the number of undecodable events also increases but remains below 2%.

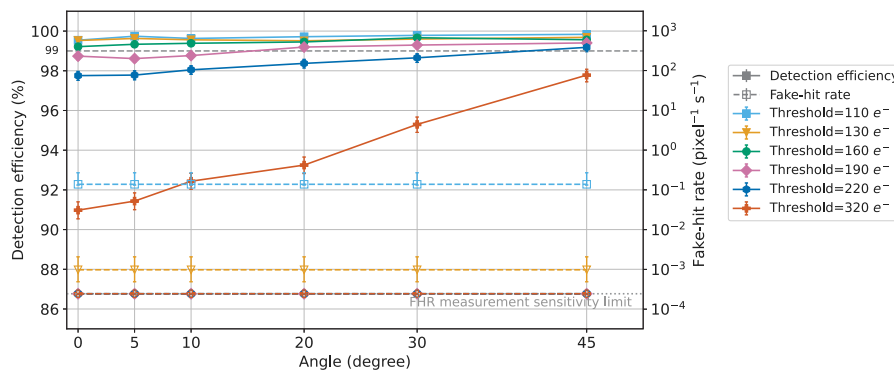
Along with the previous DPTS results and the results from the Analog Pixel Test Structures [13], a more complete picture of the performance and capabilities of the Tower Partners Semiconductor Co. 65 nm CMOS process is now available. From this, insights into the operation and design of current and future sensors in this technology can be taken advantage of. These include the second submission in the 65 nm process, designated ER1, containing the first full-scale stitched sensor prototypes along with future submissions working towards the goal of a waferscale bent sensor and a fully cylindrical detector for the ALICE ITS3.



**Fig. 18.** Detection efficiency (filled symbols, solid lines) and fake-hit rate (open symbols, dashed lines) as a function of the average threshold for chips irradiated to various ionising doses and annealing times. The chips were measured at “nominal” setting except for  $V_{sub} = -3.0\text{V}$ . Four pixels have been masked only for the 5 MGy chip.



**Fig. 19.** Detection efficiency (filled symbols, solid lines) and fake-hit rate (open symbols, dashed lines) as a function of the average threshold for chips with different track incident angles.



**Fig. 20.** Detection efficiency (filled symbols, solid lines) and fake-hit rate (open symbols, dashed lines) as a function of the track incident angles for different average thresholds.

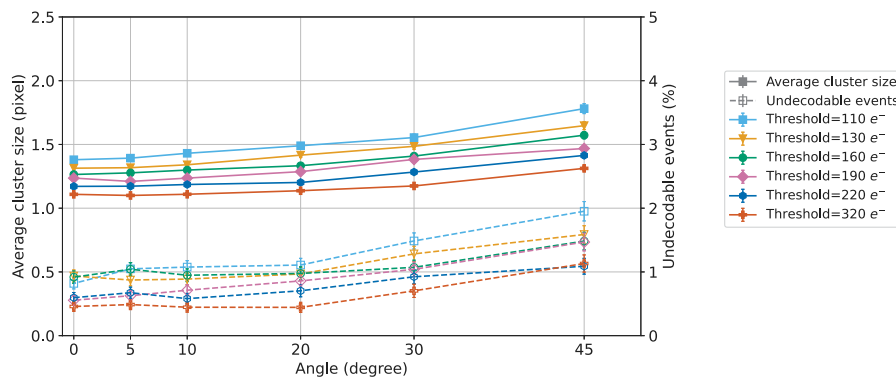


Fig. 21. Average cluster size (filled symbols, solid lines) and the percentage of un-decodable hits (open symbols, dashed lines) as a function of the track incident angles for different average thresholds.

### CRedit authorship contribution statement

**Matthew Daniel Buckland:** Writing – review & editing, Writing – original draft.

### Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

### Acknowledgements

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF). We would like to thank the coordinators at DESY for their valuable support of this test beam measurement and for the excellent test beam environment.

The authors thank the Optimato team at the Elettra Sincrotrone for providing their facility and expert support in conducting the X-ray fluorescence measurements.

ITS3 R&D and construction is supported by several ITS3 project grants including LM2023040 of the Ministry of Education, Youth, and Sports of the Czech Republic and Suranaree University of Technology, the National Science and Technology Development Agency, Thailand (JRA-CO-2563-12905-TH, P-2050706), and the NSRF via the Program Management Unit for Human Resources & Institutional Development, Research and Innovation (PMU-B B47G670091) of Thailand.

M. Buckland acknowledges the UKRI Science and Technology Facilities Council (STFC) (grant no. ST/W00450X/1) for supporting this work.

P. Becht acknowledges the support by the HighRR research training group [GRK 2058] and funding by the German Federal Ministry of Education and Research/BMBF (project number 05H21VHRD1) within the High-D consortium.

W. Deng acknowledges the support by the National Key Research and Development Program of China (2022YFA1602103).

This work has been sponsored by the Wolfgang Gentner Programme of the German Federal Ministry of Education and Research (grant no. 13E18CHA). The irradiation of sensors by protons was carried out at the CANAM infrastructure of the NPI CAS Rez.

### Data availability

Data will be made available on request.

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