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Photogating in Suspended InAs Nanowire Field Effect Transistors for Neuromorphic Applications

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Received: 31 July 2025 | **Revised:** 20 October 2025 | **Accepted:** 13 November 2025

Keywords: gate-all-around | InAs nanowire | neuromorphic | photogating effect | synaptic plasticity

ABSTRACT

Suspended indium arsenide (InAs) nanowires offer a unique platform for studying surface-driven transport phenomena due to their high surface-to-volume ratio and the absence of dielectric interfaces. In this work, we investigate the role of surface states in InAs nanowire field-effect transistors. Electrical characterization reveals a high electron mobility of ≈1500 $cm^2V^{-1}s^{-1}$, alongside a subthreshold swing of 1.49 V dec^{-1}, indicating a reduced gate efficiency caused by surface traps. Temperature-dependent analysis yields activation energies of ~100 meV, confirming the dominant influence of shallow trap states on both threshold voltage and subthreshold slope. Under pulsed optical excitation, the devices exhibit persistent negative photoconductivity and gate-tunable hysteresis. The on/off current ratio exceeds 10^5 at 200 K. These effects are attributed to a photogating mechanism controlled by the interplay between gate voltage and photoinduced trap occupation. The demonstrated ability to modulate long and short-term memory behavior through optical and electrical stimuli highlights the potential of these nanowire devices for neuromorphic applications.

1 | Introduction

1D materials, such as nanowires and nanotubes, offer distinct structural advantages over their 2D and bulk counterparts. Their inherently high surface-to-volume ratio enhances interactions with the environment, making them ideal for sensing and surface-dominated transport applications [1–3]. Strong quantum confinement along the axial and radial directions leads to unique electronic and optical properties [4], while their high aspect ratio geometry is well suited for gate-all-around (GAA) device architectures, enabling superior electrostatic control compared to planar 2D channels and making them highly scalable for advanced logic technologies [5]. Moreover, 1D materials exhibit quasi-ballistic transport [6, 7] and mechanical flexibility [8, 9], opening opportunities in flexible electronics [10], photonics [11, 12], and neuromorphic devices [13, 14]. The ability to engineer axial and radial heterostructures, often without the constraints of lattice matching, further expands their potential for tailored band structure design and multifunctional device integration, beyond what is achievable with layered 2D materials [15, 16].

Indium arsenide (InAs) nanowires (NWs), as a class of 1DIII-V semiconductors, have garnered significant interest for next-generation nanoelectronic and optoelectronic devices due to their unique combination of material and structural properties. InAs features a narrow bandgap (0.35–0.48 eV depending on crystal phase) and an intrinsically high electron mobility exceeding 40 000 $cm^2V^{-1}s^{-1}$at room temperature, far surpassing that of con-

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ventional materials, such as silicon or gallium arsenide [17–21]. These features render InAs NWs particularly promising for applications in high-speed electronics, mid-infrared photodetection, light-emitting diodes, and flexible optoelectronic systems [22–26].

However, despite their theoretical potential, the actual performance of InAs NW-based devices often falls short, particularly in field-effect transistors (FETs). Reported issues include high off-state leakage currents, suboptimal carrier mobility, and anomalous photoresponse behaviors such as negative photoconductivity [27, 28]. These limitations are widely attributed to the high surface-to-volume ratio of NWs, which makes their electrical properties particularly sensitive to surface states and native oxide formation [29]. The spontaneous oxidation of InAs in ambient conditions results in a defective surface rich in trap states, which severely impacts charge transport, gate modulation efficiency, and long-term device stability [30, 31].

In this context, surface defects become the dominant factor controlling device behavior, especially in architectures where the NW is suspended and thus devoid of substrate-induced or interfacial artifacts. Suspended InAs NW-FETs provide an ideal platform for isolating the contribution of surface states to transport phenomena. Without dielectric interfaces, the influence of surface traps can be probed directly through electrical characterization, offering insights into mobility degradation, threshold voltage instability, and subthreshold slope deterioration.

Beyond their role in limiting performance, surface states can also be leveraged for novel device functionalities. Recently, increasing attention has been devoted to nanoscale electronic systems for neuromorphic computing, where devices mimic the analog and adaptive behavior of synapses in the mammalian brain [32–35]. In this context, InAs nanowires offer a unique opportunity: their surface traps, inherently present due to their large surface area and interface roughness, can be used to modulate the device conductance over time [36, 37].

In this work, we investigate the role of surface states in suspended InAs nanowire transistors through a combination of electrical and optoelectronic characterization techniques. Standard field-effect measurements are used to evaluate the baseline transport properties and assess the influence of surface effects on mobility and gate control, while temperature-dependent analysis provides quantitative insight into the energetics of charge trapping, allowing the extraction of activation energies associated with shallow trap states. The dynamics of these traps are further explored through pulsed optical excitation, which reveals persistent photoresponse and memory effects indicative of slow detrapping processes.

Compared to previous studies on substrate-supported or oxide-embedded InAs nanowires, the suspended architecture employed here eliminates substrate-induced effects and allows the direct observation of surface-state-mediated photogating. This configuration provides unambiguous evidence that shallow traps at the nanowire surface are responsible for the observed negative photoconductivity and memory behavior, thereby extending the current understanding of photogating mechanisms in III–V

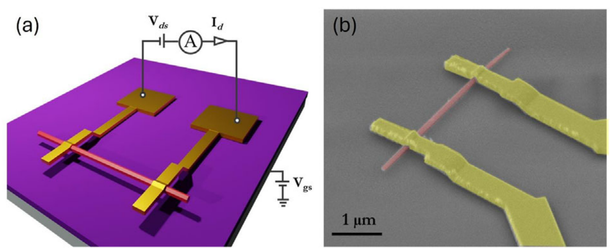

FIGURE 1 | (a) Schematic and (b) SEM image of the device under study, shown in pseudocolors. The InAs nanostructure is highlighted in red color. Gold-yellow color is used for the metallic electrodes implementing ohmic contacts. The equivalent circuit used to voltage-polarize the nanowire and to apply a back-gate voltage is depicted in overlay.

nanostructures and establishing a direct link between surface-state physics and neuromorphic functionality.

By modulating the gate potential, it is possible to control the occupation and relaxation of surface traps, enabling transitions between short-term and long-term synaptic plasticity. This comprehensive approach not only clarifies the mechanisms by which surface states influence device performance but also demonstrates their potential as active elements in neuromorphic architectures. In this framework, we focus on the inhibitory effect of light on the device conductance. While numerous studies have reported excitatory photoresponses, where illumination increases the photocurrent through photogenerated carriers [38–40], here we present a distinct perspective in which light induces current inhibition, and the transition from short- to long-term memory is governed by the applied gate voltage.

2 | Results and Discussion

Suspended InAs nanowire devices were fabricated starting from gold-catalyzed, n-doped InAs nanowires grown by chemical beam epitaxy [41]. The nanowires had a length of 2 µm and a diameter of 80 nm. A 300 nm-thick polymethyl methacrylate PMMA layer, serving as a sacrificial spacer, was spin-coated onto a substrate consisting of 280 nm (τ_{ox}) of thermally grown SiO_2 on 0.5 mm-thick p-doped silicon. Nanowires, were drop-cast onto the PMMA layer, which was subsequently patterned and crosslinked by electron beam lithography (EBL) to define the suspension area. Unexposed PMMA was removed in acetone, and contact electrodes (Ti/Au, 10/100 nm) were defined by a second EBL step followed by thermal evaporation. Prior to metal deposition, the nanowire contact regions were passivated using a $(NH_4)_2S_X$ solution to ensure low resistance Ohmic contacts. The final suspension was achieved by oxygen plasma etching of the sacrificial layer, yielding electrically contacted suspended nanowires [42]. Figure 1a shows a schematic of the device under investigation. The metal contacts serve as the drain and source terminals of the transistor, while a gate terminal is accessible on the back side of the device. Scanning Electron Microscopy (SEM) was used to characterize the structure, and the resulting false-colour SEM image is shown in Figure 1b. The channel length, defined as the portion of the nanowire between the contacts, is estimated to be L = 1.6 µm.

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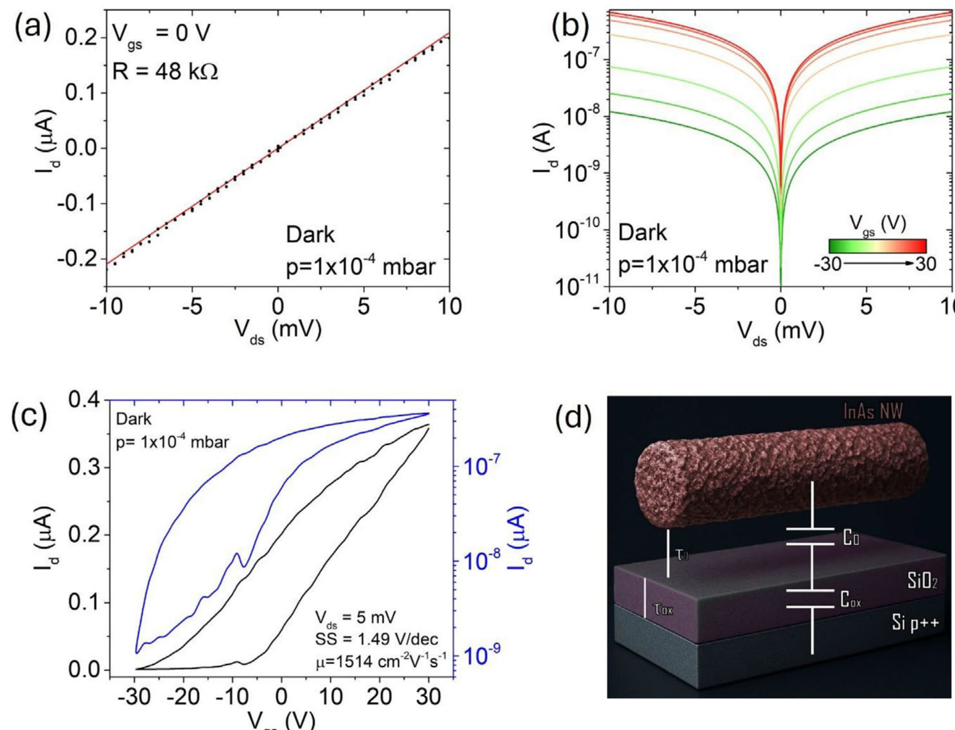

FIGURE 2 | *I–V* characteristic in dark conditions (a) at $V_{gs} = 0$ V and (b) at different applied V_{gs}. (c) Transfer characteristic in linear (black line) and logarithmic scale (blue line) in dark conditions. (d) Schematic of the capacitance model.

Electrical characterization was performed under high vacuum conditions ($p = 1\times10^{-4}$ mbar). The current–voltage (*I–V*) characteristics, measured in the dark and at room temperature, are shown in Figure 2a. The *I–V* curve exhibits a linear behavior, confirming the presence of smooth Ohmic contacts at the drain and source terminals. Output characteristics of the transistor, i.e., *I–V* curves at different gate-source voltages (V_{gs}), are presented in Figure 2b. The data indicate that the gate-source voltage bias modulates the current flowing through the nanowire, demonstrating a field-effect control of charge carrier transport in the channel. Furthermore, the current increases with increasing gate voltage, suggesting that the dominant charge carriers are electrons.

Consequently, the device operates as an n-type field-effect transistor (FET), as confirmed by the transfer characteristics shown in Figure 2c. In this measurement, the drain current (I_d) was recorded while sweeping V_{gs} from −30 V to +30 V, under a fixed drain-source bias $V_{ds} = 5$ mV. From the black curve, which represents the transfer characteristic in linear scale, the field effect electron mobility μ_n can be extracted using the following expression:

$$\mu_n = g_{m,max} \frac{L}{C \cdot V_{ds}} \quad (1)$$

where $g_{m,max}$ is the maximum transconductance, i.e. the maximum value of $\frac{dI_d}{dV_{gs}}$, and C is the total gate-channel capacitance per unit length. The total capacitance C is given by the series combination of the oxide capacitance C_{ox} and the vacuum capacitance C_0, as illustrated in Figure 2d.

The evaluation of C_{ox} and C_0 is made by the "metallic cylinder on an infinite metal plate" approximation [43]. Within this approach, $C_{ox} = \frac{2\pi\varepsilon_0\varepsilon}{\cosh^{-1}(\frac{\tau_{ox}+r}{r})}$ and $C_0 = \frac{2\pi\varepsilon_0}{\cosh^{-1}(\frac{\tau_0+r}{r})}$, where $\varepsilon = 3.6$ is the SiO_2 dielectric constant, ε_0 is the vacuum permittivity, $\tau_0 = 100$ nm is the distance between the nanowire and the substrate, and $r = 40$ nm is the nanowire radius. The total capacitance C is then obtained from the series combination of C_{ox} and C_0:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_0} \Rightarrow C = \frac{2\pi\varepsilon\varepsilon_0}{\left(\cosh^{-1}\left(\frac{\tau_{ox}+r}{r}\right) + \varepsilon\cosh^{-1}\left(\frac{\tau_0+r}{r}\right)\right)} = 20.67\,pF/m \quad (2)$$

The extracted field effect electron mobility $\mu_n = 1510$ cm^{-2}V^{-1}s^{-1} at 300 °C is consistent with the highest values reported in the literature for similar devices [44, 45]. However, the device exhibits a relatively high subthreshold swing (SS = 1.49 V dec^{-1}), which is defined as the inverse of the subthreshold slope, obtained from the linear fit of the current in the subthreshold region.

This apparent inconsistency, i.e. high field effect electron mobility but poor subthreshold behavior, indicates that, despite efficient charge transport in the on-state, gate control over the channel in the subthreshold regime is limited. A primary contributing factor is the suspended architecture of the nanowire, which results in weak electrostatic coupling due to the physical separation from the gate electrode and the low effective dielectric constant of the surrounding environment. Additionally, structural non-uniformities or unintentional doping fluctuations along the

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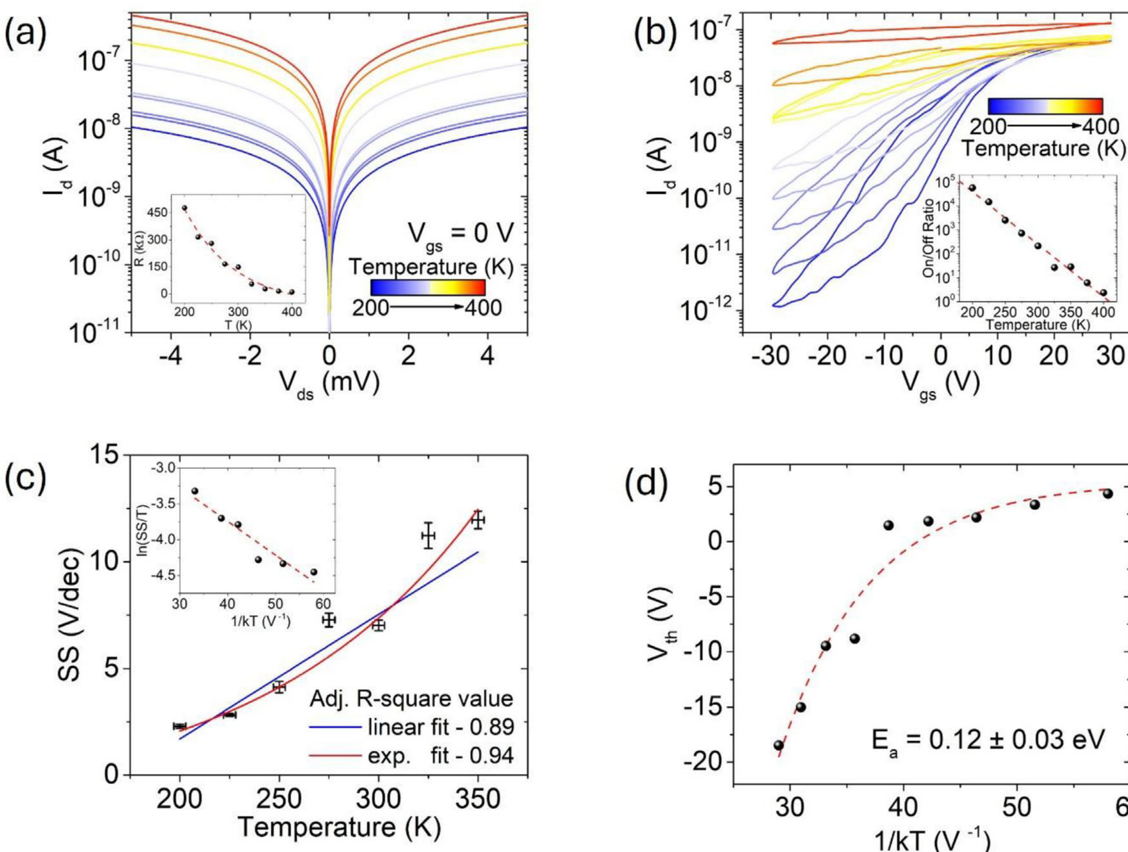

FIGURE 3 | (a) *I–V* at different temperatures. Extracted resistance vs temperature curve in the inset. (b) Transfer characteristics at different temperatures. On/off ratio in the inset. (c) Subthreshold swing versus temperature and (d) threshold voltage as a function of the reverse temperature.

nanowire, possibly caused by extended defects, locally enhance conduction bringing the chemical potential in the conduction band, thus impeding current suppression in the off-state.

Moreover, a high density of localized surface trap states (D_{it}), arising from intrinsic point defects or structural disorder, can dynamically trap and release charge carriers, effectively screening the gate electric field. This dynamic behavior degrades the switching efficiency and contributes to the increased subthreshold swing. In this context, the role of D_{it} becomes crucial for a comprehensive understanding of the device's electronic behavior. The role of these trap states is also reflected in the hysteretic behavior [46–48] observed between the forward and reverse gate voltage sweeps in the transfer characteristic shown in Figure 2c.

Therefore, to further investigate the presence of localized surface trap states, we conducted a comprehensive characterization over a temperature range from 200 to 400 K. The output characteristics at various temperatures are shown in Figure 3a. The drain current increases with the increasing temperature. The inset of Figure 3a shows the channel resistance plotted as a function of temperature, confirming the expected semiconducting behavior of the InAs nanowire. Figure 3b presents the transfer characteristics at different temperatures. Gate modulation improves, and the on/off current ratio increases exponentially with decreasing temperature, reaching nearly five orders of magnitude at 200 K.

The subthreshold swing (SS) of a transistor depends on temperature, as described by the following equation [49]:

$$\mathrm{SS} = \left(\frac{\mathrm{kT}}{\mathrm{q}}\ln 10\right)\left(1 + \frac{\mathrm{q}^2\mathrm{D}_{\mathrm{it}}}{\mathrm{C}}\right) \tag{3}$$

where $\mathrm{C}_{\mathrm{it}} = \mathrm{q}^2\mathrm{D}_{\mathrm{it}}$ represents the surface trap capacitance, and C is the channel-to-gate capacitance as previously defined. Equation (3) assumes that both D_{it} and C are temperature-independent, which may not hold true in our experimental conditions.

Indeed, the extracted SS values reveal a non-linear dependence on temperature (Figure 3c), indicating that Equation (3), with capacitances independent of temperature, does not fully capture the underlying physical mechanisms. This suggests the presence of an energy distribution of trap states within the nanowire bandgap that become active at different temperatures [50, 51].

Assuming that the trap activation follows an Arrhenius-type behaviour [52, 53]

$$D_{it} \propto \exp\left(-\frac{E_a}{kT}\right) \tag{4}$$

where E_a is the activation energy, then

$$SS \sim \left(\frac{kT}{q}ln10\right)\exp\left(-\frac{E_a}{kT}\right) \tag{5}$$

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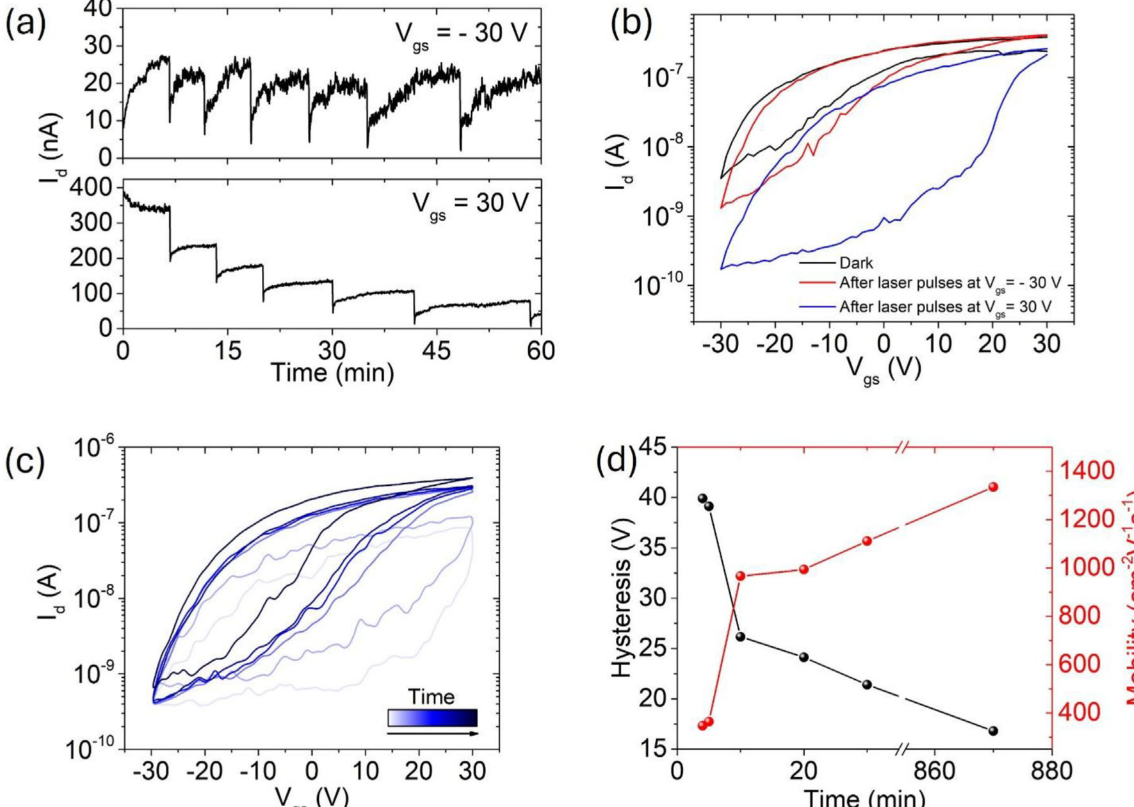

FIGURE 4 | (a) Current versus time while applying 2 s laser pulses at fixed V_{ds} and V_{gs}. (b) Transfer characteristics measured after laser pulses reported in (a). (c) Transfer characteristics measured during the recovery of the device. (d) Hysteresis width and field effect electron mobility versus time during the recovery of the device.

here, the assumption that $q^2D_{it}/C \gg 1$ was made considering the geometry of the device. The linear dependence of $ln\ (SS/T)$ versus $1/kT$, shown in the inset of Figure 3c, supports the validity of Equation (5) and the estimated value of $E_a \approx 0.09\ eV$ indicates shallow traps below the conduction band edge with low band tail extension.

A similar analysis can be carried out for the temperature dependence of the threshold voltage (V_{th}), as shown in Figure 3d. Assuming that the variation of V_{th} is primarily governed by thermally activated shallow trap states, we can express this dependence as:

$$V_{th} \propto \exp\left(-\frac{E_a}{kT}\right) \tag{6}$$

From the linear fit reported in Figure 3d, we estimated the activation energy $E_a \approx 0.12$ eV consistent with the activation energy extracted from the subthreshold swing analysis. This supports the hypothesis that thermally activated shallow traps (conduction-band or acceptor-like states) are the dominant mechanism influencing both V_{th} and SS in this temperature range.

To complete the analysis of surface defects in the nanowire, we examined the filling and emptying dynamics of shallow trap states. To this end, we excited carriers by irradiating the device with 2-seconds white laser pulses under fixed bias conditions. Figure 4a shows the drain current (I_d) as a function of time during laser irradiation, with $V_{ds} = 1$ mV and gate voltage $V_{gs} = \pm 30$ V. Negative photoconductivity (NPC) is observed at both gate voltages. However, while the current quickly recovers after the laser pulse at negative gate voltage, a persistent cumulative decrease in current is observed at positive gate voltage. This behavior is also reflected in the transfer characteristics measured immediately after the laser pulses, as shown in Figure 4b. An increased hysteresis is evident, indicating enhanced electron trapping, which appears to be more pronounced under positive V_{gs} conditions. To further investigate the de-trapping process, we recorded a series of transfer characteristics in the dark during the recovery phase, as illustrated in Figure 4c. The device required ≈15 h to nearly return to its original state. Electron field effect mobility and hysteresis width, defined as the voltage width at I_d = 10 nA, are estimated from the transfer characteristics and reported in Figure 4d. The electron mobility is affected by the electron trapping, as it is proportional to the carrier concentration, and thus changes accordingly with the hysteresis width.

To gain further insight into the effects of laser irradiation, we measured a series of transfer characteristics after exposing the sample to laser pulses of varying durations. The resulting data are shown in Figure 5a. As the duration of the pulses increases, the transfer characteristics widen, leading to an enhanced hysteresis. The hysteresis, defined here as the gate voltage difference at I_d = 20 nA, is plotted as a function of pulse duration in Figure 5b.

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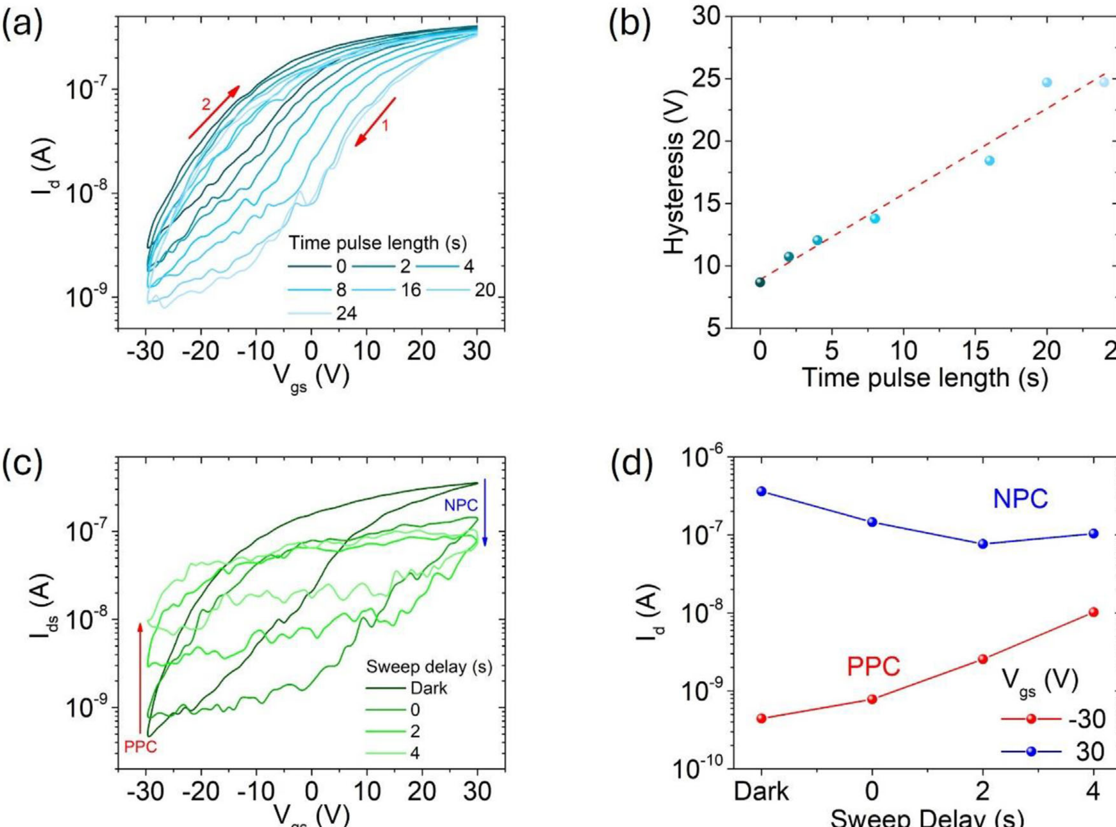

FIGURE 5 | (a) Transfer characteristics and (b) hysteresis measured after different time laser pulses. (c) Transfer characteristics during laser irradiation measured using different sweep delay time. (d) Current extracted from (c) at different V_{gs}.

The observed linear trend indicates that the filling of trap states is proportional to the pulse duration, i.e., to the photogenerated carrier density.

In a complementary experiment, we measured the transfer characteristics during laser irradiation. By varying the sweep delay time of the acquisition system, we effectively modulated the duration of laser exposure during the measurement (Figure 5c). Both negative and positive photoconductivity (NPC and PPC, respectively) are observed at different gate voltages. Specifically, Figure 5d shows the drain current values extracted at $V_{gs} = \pm 30\ V$. The mechanism responsible for NPC at $V_{gs} = 30\ V$ appears to be largely independent of the measurement duration (i.e., laser exposure time), whereas PPC at $V_{gs} = -30$ V increases with longer sweep delay times.

The observed behaviour of the NW FET can be explained using the band diagram model illustrated in Figure 6. Figure 6a,b show the band structure at the NW surface, where the density of defect states is the highest. We assume that under dark, equilibrium conditions, the Fermi level is pinned in the conduction band of InAs [54] and a portion of these acceptor-like traps is filled with electrons. Since the NW is n-type, conduction is dominated by electrons. When a positive V_{gs} = 30 V is applied, a high density of electrons is present in the channel, resulting in a high drain current. Conversely, at V_{gs} = -30 V, an energy barrier forms at the interface with contacts, suppressing electron injection and effectively turning the transistor off.

Upon laser irradiation, electron-hole (e–h) pairs are photogenerated within the NW. The electrons are readily captured by surface trap states, which become negatively charged, effectively reducing the local n-type doping and leading to the sharp current drop observed in Figure 4a. The gate voltage plays a critical role in determining the recombination dynamics of the photogenerated carriers. At positive gate bias, photogenerated holes are pushed away from the channel to metal contacts (Figure 6c), reducing their spatial overlap with photogenerated electrons and thereby suppressing recombination. This leads to accumulation of negative charge and to the persistent NPC observed in Figure 4a. In contrast, under negative gate bias, holes are kept in the channel (Figure 6d), facilitating recombination with photogenerated electrons and enabling partial current recovery within minutes.

An alternative, electrostatic explanation, independent of energy band considerations, leads to the same conclusion. Assuming a higher trap state density near the NW surface, a positive gate voltage (Figure 6e) pulls the electrons toward the gate dielectric, effectively increasing their probability of capture in surface trap states and reducing their probability of recombination. Conversely, a negative gate voltage pushes the photogenerated electrons into the NW core, where they can more easily recombine with photogenerated holes. This light-induced modulation of the channel via charge trapping is known as the photogating effect. Notably, this phenomenon has been scarcely reported in cylindrical systems such as NW FETs, where the gate field envelops the entire channel in an all-around configuration.

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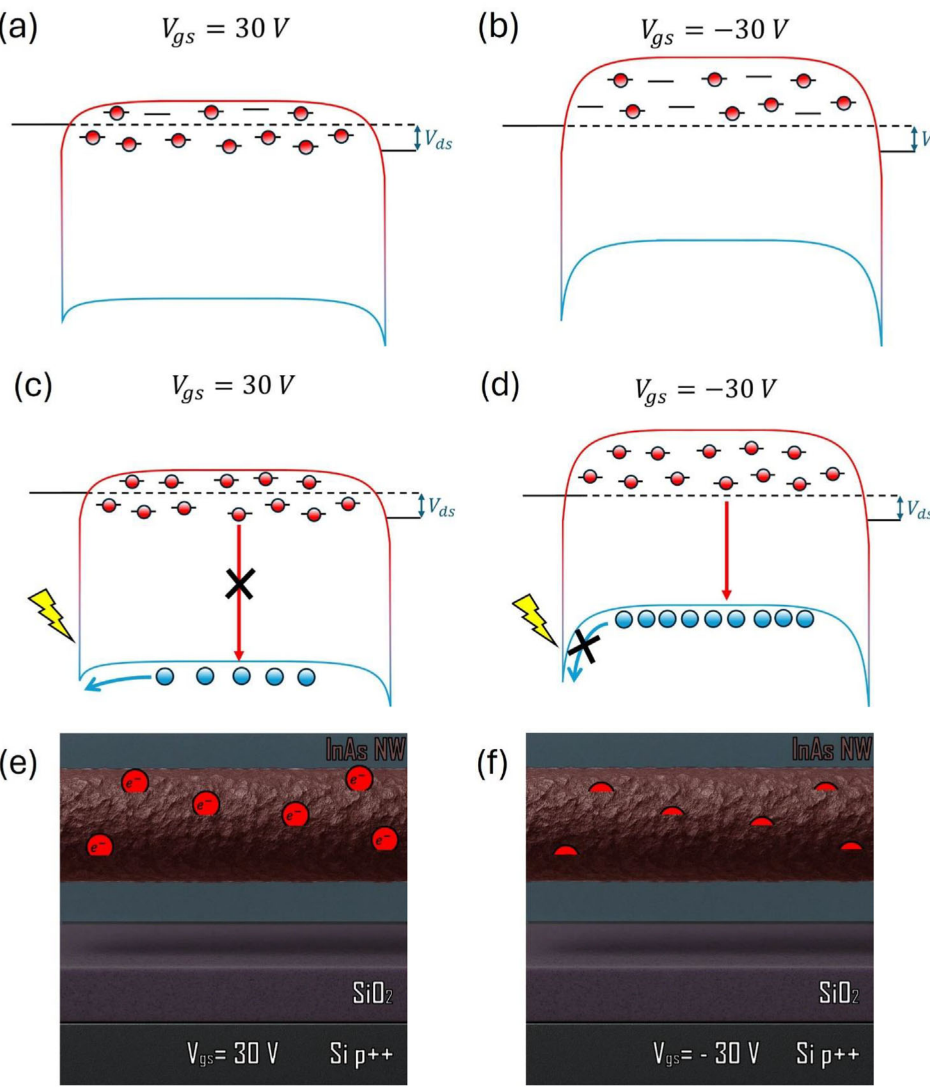

FIGURE 6 | Band diagram schematic of the NW surface in (a,b) dark and (c,d) under laser irradiation. Red and blue circles indicate electrons and holes, respectively. Red arrows describe recombination mechanisms. (e,f) All-Around photogating effect: trapped electrons are attracted or rejected by the applied gate electric field.

This model also accounts for the transfer characteristics observed after laser pulses in Figures 4b and 5a. When a positive gate voltage is applied, trap states are filled with electrons, which do not recombine because of the reduced cross section with holes, resulting in an effective n-type doping reduction. During the subsequent reverse sweep, this excess trapped charge shifts the transfer curve toward positive voltages. In contrast, during the forward sweep at negative gate voltage, detrapping is promoted, increasing the n-doping and shifting the curve to the left. The rightward shift is more pronounced with increasing laser pulse duration, consistent with a higher density of photogenerated electrons available for trapping.

Finally, the model also explains the behavior observed in Figure 5c. The trapping and recombination processes occur on different timescales, with trapping being significantly faster. As the sweep delay time increases, effectively prolonging laser exposure, the slower recombination process becomes more relevant. This leads to an exponential increase in current at $V_{gs} = -30$ V due to enhanced hole accumulation and recombination. The observation of PPC under negative gate bias supports the notion that, under dark conditions, surface trap states are already partially filled with electrons. The current increase thus corresponds to detrapping followed by rapid recombination. Conversely, the nearly flat NPC trend at $V_{gs} = +30$ V, confirms that the trapping process is fast and that the trap states become fully occupied quickly.

The primary mechanisms by which the device under investigation converts optical stimuli into electrical signals are photoconduction and the photogating effect. In particular, the application of gate bias enables control over the persistence of negative photoconductivity. This behavior arises from the interaction with surface trap states, which become populated by photogenerated electrons during illumination. This controllable and persistent photoresponse makes the mechanism highly suitable for the implementation of optoelectronic artificial synapses (OEAS) [55].

Synapses are the fundamental elements that connect neurons in the brain, acting as dynamic junctions that mediate

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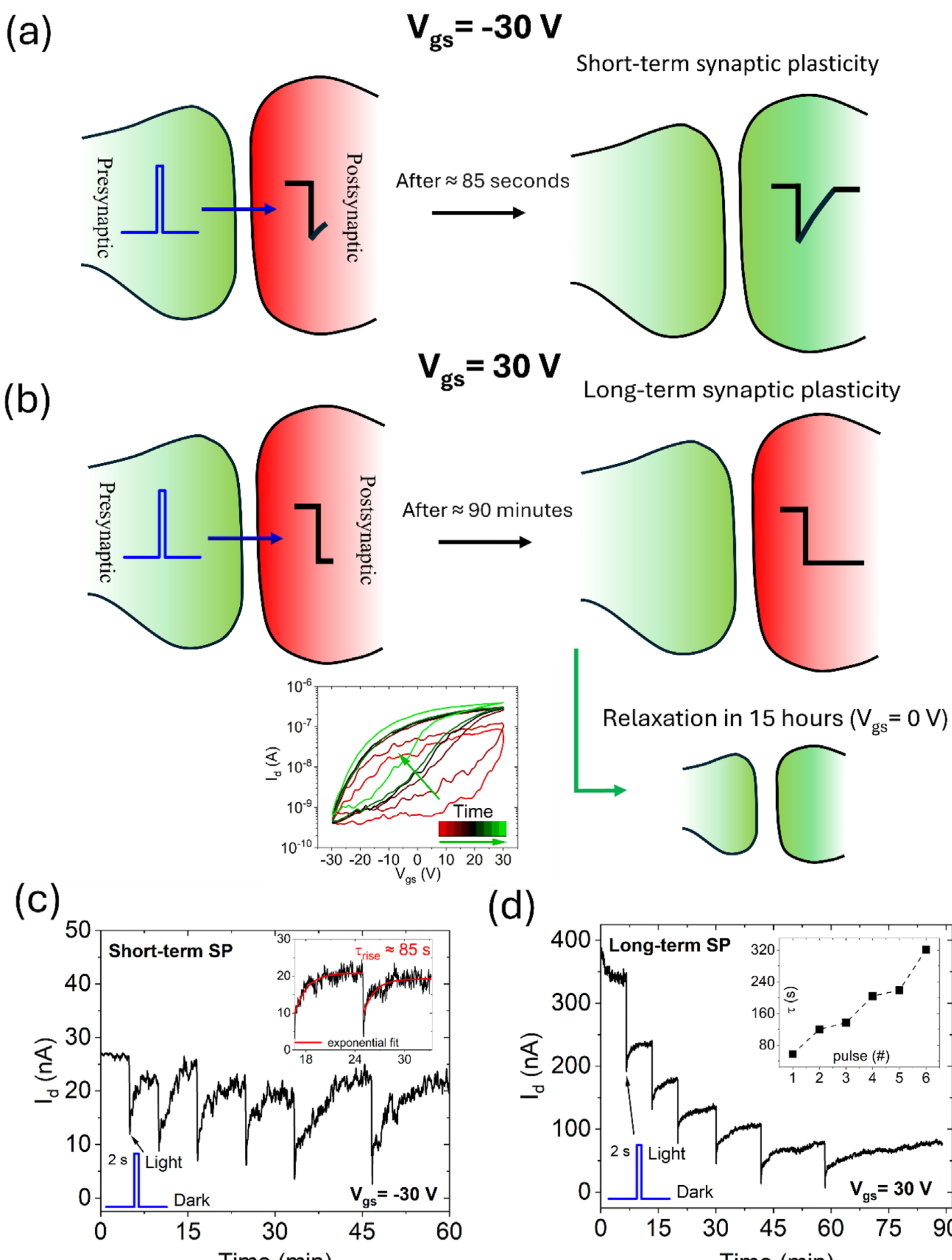

FIGURE 7 | Short-term (a) and long-term (b) synaptic plasticity modulate by gate voltage. (c) Short-term plasticity is emulated by repeated 2-second light pulses applied at V_{gs} = -30 V, resulting in a synaptic relaxation time of ≈85 s, as estimated from the exponential fit shown in the inset. (d) Long-term synaptic plasticity observed under positive gate voltage, with the inset showing the relaxation time increasing with the number of pulses.

communication between them [56, 57]. Neural signals propagate via intracellular action potentials and are transmitted across synapses through neurotransmitter release or, in some cases, electrical coupling, with the strength of transmission modulated by the synaptic weight [58]. One of the most remarkable features of the mammalian brain is its plasticity, which refers to the capacity of neural activity shaped by experience to rewire functional connections within neural circuits, thereby shaping future cognition, emotion, and behavior. Synaptic plasticity (SP) refers specifically to the activity-dependent modulation of the strength or efficacy of synaptic transmission at existing synapses. For over a century, it has been proposed as a fundamental mechanism by which transient experiences are encoded into long-lasting memory traces [49]. Synaptic transmission can be either excitatory or inhibitory, depending on the type of neurotransmitter released and the nature of the postsynaptic receptors. Excitatory synapses have positive synaptic weights, increasing the postsynaptic response, whereas inhibitory synapses have negative synaptic weights, reducing or counteracting it. These modifications span a wide range of timescales, from milliseconds to hours, days, or even longer. Accordingly, synaptic plasticity is generally classified into short-term synaptic plasticity (STSP) and long-term synaptic plasticity (LTSP), depending on the duration of the induced changes in synaptic weight. STSP typically lasts for several minutes or less [59], whereas LTSP can persist for several hours or more [60].

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In this framework, both excitation and inhibition of the postsynaptic current can arise from the intrinsic hysteretic behavior of the device under appropriate gate modulation, as already reported in literature both for other nanowires [61–63] and other materials in general [64–66]. The light-induced negative photoconductivity reported here thus represents one of the possible operation modes enabling controllable inhibitory response in neuromorphic systems. In our experiment, an inhibitory postsynaptic current (IPSC) is triggered by a 2-second pulse of white light illumination, because of the negative photoconductivity phenomenon associated with the photogating effect. For the implementation of an OEAS, the drain current I_d is used as the IPSC [67]. By tuning the gate voltage, the timescale of synaptic plasticity can be modulated from short-term to long-term regimes. Specifically, applying a gate voltage of $V_{gs} = -30$ V results in STSP, as shown in Figure 7a, while $V_{gs} = +30$ V induces LTSP, as seen in Figure 7b. Under STSP conditions, the IPSC recovery lasts ≈85 s, and this relaxation time remains nearly constant regardless of the number of light pulses applied. This behavior is confirmed by fitting the rising edge of the IPSC recovery (following the light pulse) with an exponential function, as shown in the inset of Figure 7c. The duration over which the system retains the inhibitory effect before returning to baseline can be interpreted as a form of short-term memory. Conversely, under positive gate bias conditions (Figure 7c), repeated inhibitory stimuli lead to an cumulative response due to the enhanced persistence of NPC. As the number of light pulses increases, the IPSC decreases progressively. After six pulses, the IPSC is reduced by ≈40% relative to its initial value, indicating a significant and lasting modification of the synaptic state. Recovery to the initial condition requires both a return to zero gate bias and an extended relaxation time of ≈15 h, as evidenced by the time evolution of the transfer curves in Figure 7b. This behavior is indicative of long-term synaptic plasticity.

To quantitatively characterize this transition, the rise of the IPSC after illumination was fitted with an exponential function, allowing extraction of the characteristic time constant τ, associated with the stabilization of the current to a new steady-state value under positive gate voltage. This timescale reflects the underlying trapping/detrapping dynamics, as previously described in the model presented in Figure 6. Notably, τ increases linearly with the number of applied light pulses, ranging from 58 to 321 s. This dependence suggests that the stabilization process is hindered by an increased density of trapped electrons, which accumulate as more photons are absorbed. The presence of positive gate bias further promotes electron trapping by attracting photogenerated electrons toward the nanowire surface, thereby slowing recombination and extending the response time. In contrast, when a negative gate bias is applied, electrons are repelled from the surface, which facilitates recombination and results in a τ value that is effectively independent of the number of light pulses.

3 | Conclusion

We have demonstrated that suspended InAs nanowire FETs exhibit strong photogating effects governed by the trapping and release of photogenerated carriers at surface states. The devices show high field effect electron mobility (~1500 $cm^2V^{-1}s^{-1}$), but also a significant subthreshold swing (1.49 V dec^{-1}), revealing the impact of shallow surface traps on gate control. Through temperature-dependent measurements, we extracted activation energies of ≈100 meV, confirming the presence of thermally activated shallow traps that dominate subthreshold and threshold behavior. Under laser irradiation, the devices exhibit persistent photoconductivity and pronounced hysteresis, with memory effects modulated by gate bias and optical pulse duration. These findings demonstrate that surface states, often seen as a limitation, can be repurposed to emulate synaptic behavior, paving the way for the use of InAs nanowire-based FETs in neuromorphic applications. InAs nanowire FETs with controllable hysteresis and light-induced inhibitory behavior can serve as synaptic elements in hybrid neuromorphic circuits, including self-organizing nanowire networks [68, 69]. Their conductance can be potentiated or depressed via gate or optical pulses, enabling short- and long-term plasticity, and supporting both excitatory and inhibitory connections for applications such as pattern recognition and temporal signal processing [70].

Funding

ADB acknowledges the support from the Università degli Studi di Salerno with grant n. ORSA254881. FR acknowledges the support from FAR 2024 Progetti interdisciplinari - Linea UNIMORE "NT-ROBOT" (CUP E93C24001920005), INFN project "MANIFOLD", and National Recovery and Resilience Plan (PNRR), Mission 04, Component 2, Investment 1.5 NextGenerationEU, Call for tender No. 3277 dated December 30, 2021 (Award Number: 0001052 dated June 23, 2022).

Conflicts of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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