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Federico Parenti, Riccardo Sargeni, Elisabetta Dimaggio, Francesco Pieri, Filippo Fabbri, Tommaso Losi, Fabrizio Antonio Viola, Arindam Bala, Zhenyu Wang, Andras Kis, Mario Caironi, Gianluca Fiori*; **Ultrathin Transistors and Circuits for Conformable Electronics**, **ACS Nano Letters**, vol. 24, issue 49, 2024, pages 15870-15877

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Ultra-thin transistors and circuits for conformable electronics

Federico Parenti,[1] Riccardo Sargeni,[1] Elisabetta Dimaggio,[1] Francesco Pieri,[1] Filippo Fabbri,[2] Tommaso Losi,[3] Fabrizio Antonio Viola,[3] Arindam Bala,[4] Zhenyu Wang,[4] Andras Kis,[4] Mario Caironi,[3] and Gianluca Fiori[1,*]

[1]*Dipartimento di Ingegneria dell' Informazione, Università di Pisa, Pisa, Italy*

[2]*NEST Laboratory, Istituto Nanoscienze-CNR and Scuola Normale Superiore, Pisa, Italy*

[3]*Center for Nano Science and Technology, Istituto Italiano di Tecnologia (IIT), Milano, Italy*

[4]*Institute of Electrical and Microengineering, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland*

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Abstract

Adapting electronics to perfectly conform to non-planar and rough surfaces, such as human skin, is a very challenging task which, if solved, could open up new applications in fields of high economic and scientific interest ranging from health to robotics, wearable electronics, human-machine interface and Internet of Things. The key to success lies in defining a technology that can lead to the fabrication of ultra-thin devices while exploiting materials that are ultimately thin, with high mechanical flexibility and excellent electrical properties. Here, we report a hybrid approach for the definition of high-performance, ultra-thin and conformable electronic devices and circuits, based on the integration of ultimately thin semiconducting transition metal dichalcogenides (TMDC), i.e., MoS_2, with organic gate dielectric material, i.e., polyvinyl formal (PVF) combined with the ink-jet printing of conductive PEDOT:PSS ink for electrodes definition. Through this cost-effective, fully bottom-up and solution-based approach, transistors and simple digital and analogue circuits are fabricated by a sequential stacking of ultrathin (nanometer) layers on a few micron thick polyimide substrate, which guarantees the high flexibility mandatory for the targeted applications.

* gianluca.fiori@unipi.it

INTRODUCTION

The development of electronic circuits capable of bending and conforming to non-planar and irregular surfaces, such as human skin, is becoming essential in several applications, ranging from Internet of Things (IoT) to e-textile architectures, wearable electronics and healthcare [1–6]. This radical change can only be made possible by conformal field-effect transistors (FETs), which in turn can become a reality through the selection of suitable materials with excellent electrical and mechanical properties, coupled with the development of frontier technologies for device fabrication beyond standard integrated circuit processes on rigid substrates.

Mechanical flexibility and conformability of materials depend not only on their intrinsic properties, i.e., bending stiffness [7], but also on the definition of novel methods of material film fabrication. As stiffness scales with the cube of material thickness, the possibility of employing the thinnest possible materials represents a breakthrough in conformable applications. The requirement for reduced thickness has to also match the good electrical properties of the materials as insulator (or dielectric), semiconductor, and conductors, which are the main ingredients for FET devices.

Carbon-based materials, especially organic polymers, are the current standard for flexible electronic technologies, thanks to their intrinsic mechanical flexibility and the availability of dielectric, conductive, and semiconducting organic compounds [8, 9]. In addition, they can usually be processed using low temperature, large area and cost-effective methods, e.g., solution based, making them suitable for a wide range of applications [10, 11]. However, there are limitations to the use of these materials for the fabrication of high-performance flexible FETs and circuits, mainly related to the properties of organic semiconductors (OSCs). The latter usually exhibit poor operational stability in ambient conditions over time [12, 13] and mobility values below 100 $cm^2V^{-1}s^{-1}$ [14–16]. Two-dimensional materials (2DMs), instead, such as transition metal dichalcogenides (TMDCs), with their wide range of electronic properties, from insulating to metallic or semiconducting [17], are the thinnest materials yet synthesized, consisting of layers just a few atoms thick, and can be easily transferred on flexible substrates. In particular, semi-conducting 2DMs, such as MoS_2, exhibit exceptional electrical properties, with extremely high mobility values [18], eventually exceeding 100 $cm^2V^{-1}s^{-1}$ on FETs fabricated with standard lithographic processes [19], and significantly reduced stiff-

ness (of the order of 10^{-10} N/m), allowing large-scale integration capabilities, with a number of integrated transistors up to $10^3 - 10^4$ cm^{-2} [20].

Following the FET stack, a good and as thin as possible dielectric is also required. Organic polymers are good candidates [21] due to their mechanical properties and solution processability, which can reduce the thermal budget of the process and the fabrication costs, compared to vacuum deposition (e.g., CVD, ALD and sputtering) or oxidation techniques. However, many of these polymers have a low relative dielectric constant [22], which limits their use in low-voltage applications. In general, they tend to exhibit electrical losses [23], forcing an increase in film thickness up to the micron range, and therefore operating voltages from tens to hundreds of volts: this limits their use in portable and wearable electronics, where voltages smaller than 5 V are required [24]. However, among the various organic polymers, poly(vinyl formal) (PVF) is a solution-processable polymer with great potential. Nanometer-scale PVF films have shown excellent insulating and mechanical properties, as well as the ability to conform to irregular and dynamic surfaces [25–27].

The missing element in this ambitious design is the development of a process that enables the integration of the thinnest and highest-quality materials into an ultrathin stack, completed with conductive electrodes, with the extraordinary ability to be shaped by the final application surface.

Here, we report a hybrid fabrication approach for the definition of ultrathin and high-performance conformable FETs and circuits. We integrate 2DMs and organic compounds on a flexible polyimide (PI) substrate using a combination of solution-based methods and high-quality material deposition techniques. We select a MOCVD grown monolayer of MoS_2 as the semiconducting 2DM and transfer it to PI films because it is the most promising in terms of electrical and mechanical properties. In particular, the field-effect carrier mobility of MoS_2 allows the definition of high-performance electronic devices [28–30].

Nanometre thick PVF films were chosen as the gate dielectric material to limit the overall thickness of the device while increasing the integration density and reducing the operating voltages.

To define the source, drain and gate electrodes and interconnections, we chose inkjet printing due to its high customisation and versatility at room temperature [31–37]. It provides precise control over the volume of each droplet during the printing process, ensuring accuracy and consistency and minimising waste [38–42]. In addition, it is a scalable pat-

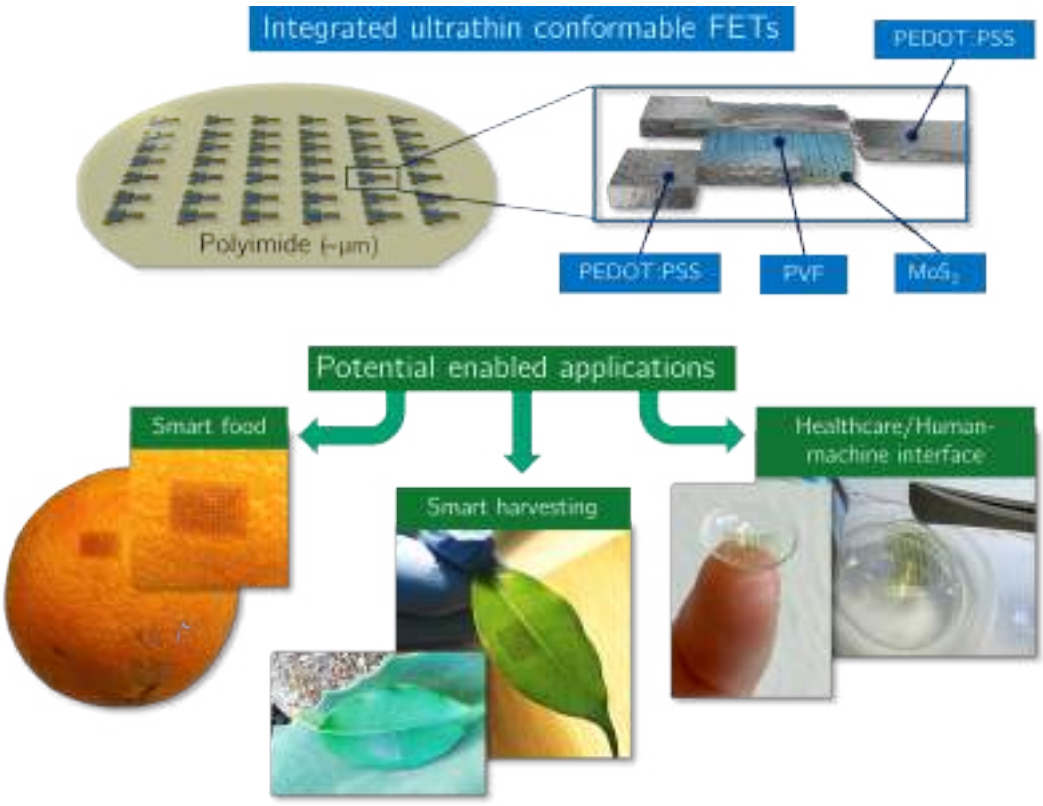

Figure 1. A schematic view of an array of transistors and a sketch of a single device in the inset. At the bottom some potential applications enabled by our technology. An array of more than one hundred transistors fabricated on a polyimide flexible substrate, adhering to the surfaces of an orange (bottom left) and a leaf (in the middle), showing examples of implementation for smart agriculture. A flexible circuit (bottom right), fabricated on a polyimide substrate, conforming to an eye contact lens (dynamic surface) as an example of wearable electronic application.

terning method that provides a viable alternative to lithography in this application, where a low-temperature process is required to maintain the quality of the PVF layers. In terms of electrically conductive materials, we chose the water-based PEDOT:PSS ink, which guarantees the definition of feature with thicknesses at the nanoscale, typically in the range of tens of nanometers. This order of thickness is comparable to that achieved with thermally evaporated materials. Moreover, it does not require any post-deposition baking or sintering steps, making it fully compatible with a low-temperature process.

This hybrid approach allowed us to define ultrathin (< 200 nm) FETs on PI films (3.8 μm thick), with high integration density (around 100 cm^{-2}) and extremely good electrical properties. Figure 1 illustrates a schematic view of a single FET, in the inset, and an array of

transistors defined with our process, which have been transferred to several surfaces with a high degree of roughness, and which can open new applications, spanning from smart agriculture to wearable electronics. Based on these small devices, we have developed analog and digital circuits to showcase the potentials achievable with our technology.

FABRICATION OF ULTRA-THIN FETS

Ultra-thin FETs are fabricated following a bottom-up solution-based strategy, combining inkjet printing and advanced material deposition techniques, on a flexible substrate. Figure 2 illustrates the main steps of the fabrication process. A monolayer film of MoS_2, grown through MOCVD [30], is mechanically patterned on its native sapphire (Al_2O_3) substrate. This patterning is achieved by precisely controlling the micrometer-scale movements of a metal tip using a custom scribing system developed in-house [43]. By placing the tip in contact with the target surface, it can selectively remove the 2D material in localized areas. The patterned MoS_2 film is then transferred, using a thermal release tape, onto a few microns thick polyimide (PI) substrate, previously deposited on top of a silicon Si wafer. During the transfer process, a sacrificial layer of poly(methyl methacrylate) (PMMA) is spun onto the MoS_2 film to provide mechanical stability and facilitate processing. After the transfer, the PMMA layer is removed, leaving a matrix of isolated MoS_2 areas on PI.

Each FET is defined within an isolated semiconductor region to reduce the occurrence of high dispersion current phenomena when multiple devices are biased simultaneously (similar to a shallow trench isolation). On top of MoS_2, transistors source and drain electrodes are printed with a water-based poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) conductive ink, defining the region of the transistor channel with typical dimensions of $W \times L = 400 \times 70\ \mu m^2$, where L and W are its length and width, respectively. Two 25 nm thick PVF films, delaminated from a silicon wafer carrier and suspended in water, are collected directly with the PI substrate, with the FETs areas on top, following the procedure previously reported by Viola *et al.* [25]. Finally, a top-gate electrode is printed on top of the PVF using the same PEDOT:PSS conductive ink, aligned to the bottom channel areas. Based on the morphological analysis conducted using an Atomic Force Microscope (AFM) in the FET region, as detailed in Section 5 (Fig S5) of the Supporting Information, a comprehensive thickness assessment was achieved. This analysis revealed a total thickness of

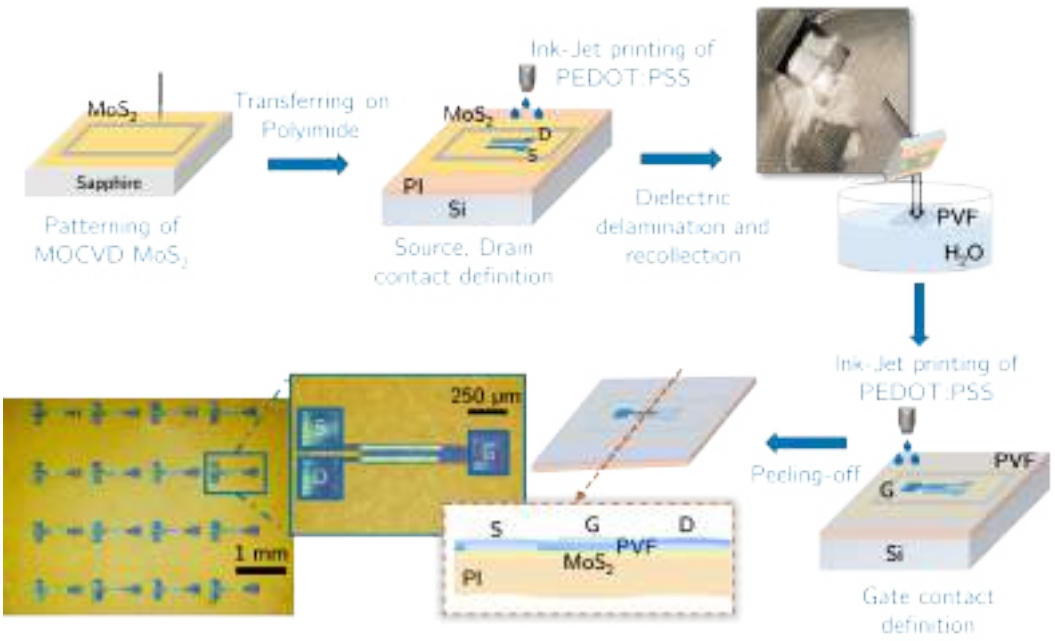

Figure 2. Schematic representation of the main fabrication process steps: from the semiconductor film patterning on sapphire, to the transfer of the flexible PI substrate with the whole devices stack on top. A sketch of the final cross section is shown in the inset. In the optical micrographs, a matrix of ultra-thin FETs fabricated on flexible PI substrate is shown.

120 nm for the drain stack and 90 nm for the gate stack, which is a remarkable achievement for a non-lithography-based process for conformable electronics. The optical micrographs in Figure 2 show a single ultrathin FET and a dense matrix of FETs on the PI substrate fabricated through this process. Further details of the process and the materials used can be found in Methods section. For circuit fabrication, transistors can be interconnected by defining inkjet-printed gold vias through the insulating layer. Finally, the full stack can be delicately peeled from the initial substrate and transferred to different surfaces because of their exceptional conformability.

ELECTRICAL CHARACTERIZATION OF CONFORMABLE FETS

The typical transfer and output characteristic curves, reported in Figure 3a and Figure 3b, demonstrate the low operation voltage range (< 5 V) of our FETs. Moreover, the ohmic response in the low drain voltage region (Figure 3 c) suggests good electrical contact between PEDOT:PSS electrodes and MoS_2. The curves also show that the gate leakage current is

negligible compared to the drain/source currents, proving the excellent quality of PVF as a gate dielectric material. To be noted that the transfer characteristic gives evidence of the typical hysteresis of 2DM based FETs, which strongly depends on the presence of charge traps at the interfaces and causes a shift in the threshold voltage from forward to backward sweep. The phenomenon is reduced in the output characteristics, which are a function of the drain-source voltage.

As shown in Figure 3d, the performance metrics for an array of 85 working transistors on the same chip were evaluated, showing an average threshold voltage (V_{TH}) of 1.76 V, a current ratio I_{max}/I_{min} typically ranging from 10^2 to 10^3, calculated according to the procedure reported by Cheng *et al.* [44], a subthreshold swing of 1.58 V/dec and a mobility of 2.44 $cm^2V^{-1}s^{-1}$, for devices with a channel width and length of 400 μm and 70 μm, respectively. These parameters were extracted following the procedure reported in Section 6 of the Supporting Information, and the related descriptive statistics are summarized in Table 2 of the same Section.

The field-effect mobility (μ_{FE}), a crucial factor in assessing the electric performance of a FET, was evaluated according to the bias condition of the devices, such as linear regime or saturation regime, employing the expressions derived for an ideal long-channel MOSFET for $V_{GS} > V_{TH}$:

$$\mu_{FE} = \begin{cases} \frac{L}{W}\frac{1}{C_i}\frac{1}{V_{DS}}\frac{\partial I_D}{\partial V_{GS}}, \mathrm{V}_{DS} < V_{GS} - V_{TH} \\ 2\frac{L}{W}\frac{1}{C_i}(\frac{\partial \sqrt{I_D}}{\partial V_{GS}})^2, \mathrm{V}_{DS} > V_{GS} - V_{TH} \end{cases}$$

where C_i is the insulator film capacitance per unit area, V_{GS} is the gate to source voltage and V_{DS} is the drain to source voltage.

To guarantee a precise mobility estimation, the capacitance value was calculated on a PVF-based parallel plate capacitor structure, fabricated on PI. Following the classical expression:

$$C_i = \frac{\epsilon_r \epsilon_0}{t}$$

where ϵ_r is the relative permittivity of the insulator, ϵ_0 is the permittivity of free space and t is the insulator film thickness.

By measuring the capacitance per unit area, using an insulator thickness of 50 nm common to all fabricated devices, it was found that the average relative permittivity value was 3.8. This result is in agreement with other characterizations of the material reported in previous studies [25, 26]. More details and data about capacitance measurements can be found

in Section 7 of the Supporting Information. Taking into account this value of capacitance per unit area, an average field-effect mobility of 2.44 $cm^2V^{-1}s^{-1}$ was estimated.

The good mobility and narrow operating voltage range achieved with our devices demonstrate the robust competitiveness in terms of electrical performances, which can lead to a low power consumption, crucial for portable applications.

In Figure 3e, the average field-effect mobility (μ_{FE}), expressed as a function of the operating voltage of our FETs, is compared with the values reported by other groups for transistors defined on flexible substrates. Only devices with a FET stack thickness below < 1 μm have been considered. Most of the reported values are referenced to organic semiconductor-based FETs, indicated with blue spheres, as representative of the current standard technology for flexible electronics. Entries for TMDC-based flexible FETs, indicated with blue stars, are also included. Following the color gradient, the top left area indicates the low-voltage (< 10 V) and high-mobility (> 1 $cm^2V^{-1}s^{-1}$) region, where our work is located. The green dashed line is described by the expression $\mu = k \cdot V$, where μ, V and k represent mobility, operation voltage, and ratio between our mobility and operation voltage values, respectively. The entries positioned above this line, following the color gradient, denote instances where the ratio μ to V exceeds our own. It is worth noting that, differently to our case, these instances involve lithographic-based fabrication processes and vacuum-based advanced deposition techniques, which inherently imply higher fabrication costs and higher thermal budgets, the latter preventing device fabrication on top of substrates of interest for recyclable and responsible electronics as the paper.

To demonstrate the pliability and conformability of our devices, we performed an electromechanical characterization. This involved assessing their electrical response when subjected to static bending conditions with various curvature radii, thereby demonstrating their ability to maintain functionality even when conformed to different shapes. Figure 3f shows multiple transfer characteristics for bending radii of 14 mm and 11 mm, confirming that the electrical response of the devices remains unaffected by the bending condition, as no significant changes are observed in the drain and gate currents. In Figure 3g, a picture of our setup for electromechanical characterization is reported. Finally, devices must be able to function optimally even when conformed to nonplanar dynamic surfaces, such as human skin, which may subject them to repeated bending cycles. Hence, we conducted an investigation into the longevity of our devices, observing negligible alterations in their electrical behavior even

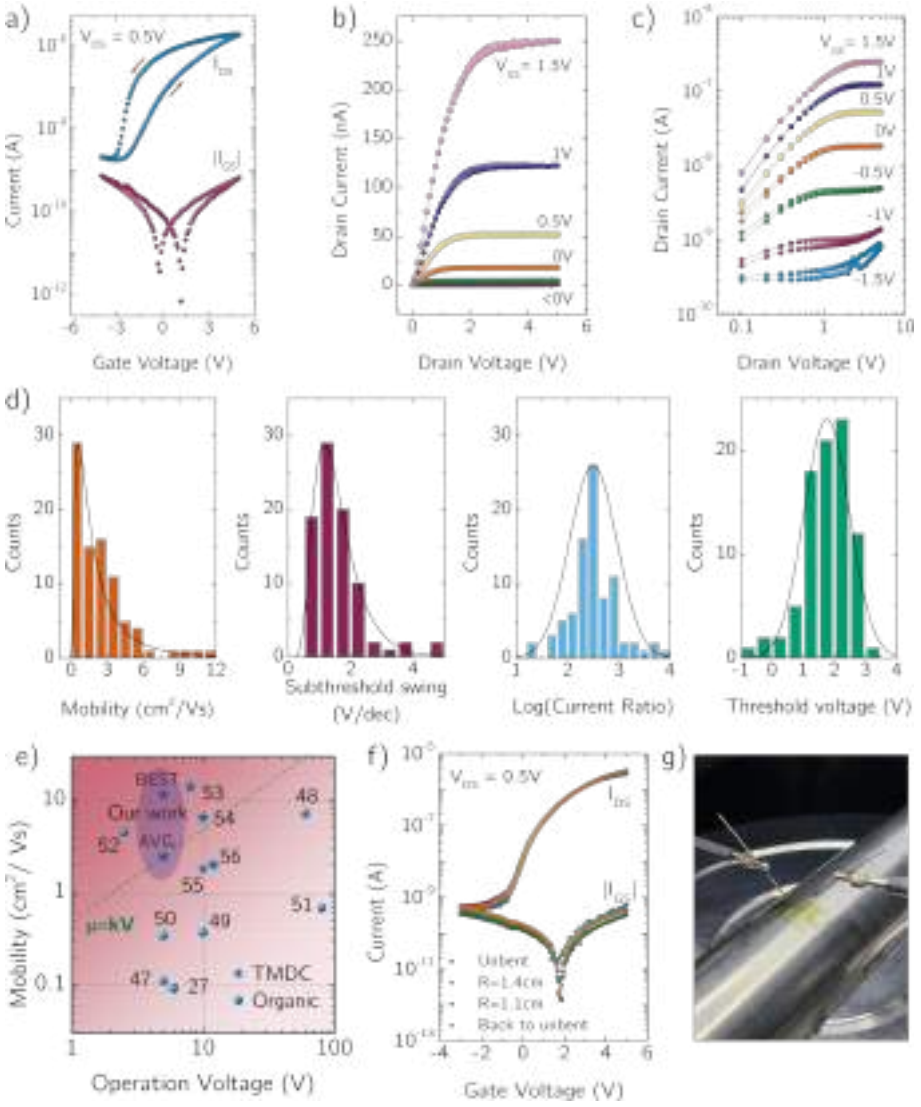

Figure 3. a) Typical transfer characteristic curve of our FETs, measured for a V_{DS} of 0.5 V (scan-rate of 100 mV/s). b) Output characteristic curves of our FETs, measured for diverse V_{GS} values, and log-log curves of the output characteristics (c). d) Histograms showing mobility, threshold voltage, subthreshold swing, and I_{max} over I_{min} current ratio distributions, for an array of 85 transistors on the same chip. e) Field-effect mobility related to operation voltage for transistors on flexible substrates, based on OSCs [25, 45–50] and on TMDCs ([51–54]), corresponding to blue spheres and blue stars, respectively. Entries have been chosen among the ones reported in Table 3 of Section 9 of the Supporting Information. f) Transfer characteristics for different bending radii and a V_{DS} of 0.5 V. g) Picture of the measurement setup for the bending characterization.

after subjecting them to numerous bending cycles (up to 500), underscoring their robustness and durability. Results and more details can be found in Section 8 of the Supporting Information. Similarly, a parallel study was conducted on PEDOT:PSS-PVF parallel plate capacitors, giving results consistent with the ones derived from the FETs analysis. This parallel investigation reinforces the conclusions on the performance and durability of our devices and confirms the robustness of our technology across different device architectures.

CONFORMABLE ELECTRONIC CIRCUITS

Several circuits have been fabricated using the proposed technology and the previously described FETs as elementary building blocks. Figure 4a shows the optical micrograph and the electrical schematic of an inverter logic gate composed of two transistors, $M1$ and $M2$, following the depletion-load nMOS-like logic, where the transistor $M2$ acts as a pull-up resistor. The aspect ratio (W/L) is about 17 for $M1$ and 19 for $M2$.

Figures 4b and c show the input-output characteristics measured for a single value of the supply voltage (V_{DD}) of 5 V and for several values (5 V down to 1 V), respectively. The gain (G), defined as the slope of the transfer curve (dV_{OUT}/dV_{IN}), where V_{IN} and V_{OUT} are the input and output voltages, is also shown (right axis). The inverter has a high gain value of 25 when the circuit is biased with a voltage of 5 V, and it maintains almost full output swing even when biased with smaller values of V_{DD}, down to 1 V. The inversion voltage decreases as V_{DD} is reduced, along with the gain.

Another interesting digital circuit is the NAND gate, which is essential in combinational logic as it can be used to implement all the other logic functions. Hence, defining a conformable NAND enables all boolean operations for any conformable application. Figure 4d shows the schematic and optical micrograph of a depletion-load nMOS-like NAND gate, where transistors $M1$ and $M2$ act as a pull-down network, and $M3$ as pull-up resistor. The aspect ratio is about 7.5 for $M1$ and $M2$, and 25 for $M3$. Figure 4e shows the circuit output voltage as a function of the input sequence (V_{IN_1},V_{IN_2}). The input high-logic value corresponds to 3 V, while the low level to 0 V. The power supply V_{DD} is set to 3 V. Accordingly to the truth table of a NAND gate, the output voltage is in low state (0) only when both input signals, represented by V_{IN_1} and V_{IN_2}, are in high state $(1, 1)$. Otherwise, output voltage results to be in high state (1). The output voltage plot confirms that this condition is sat-

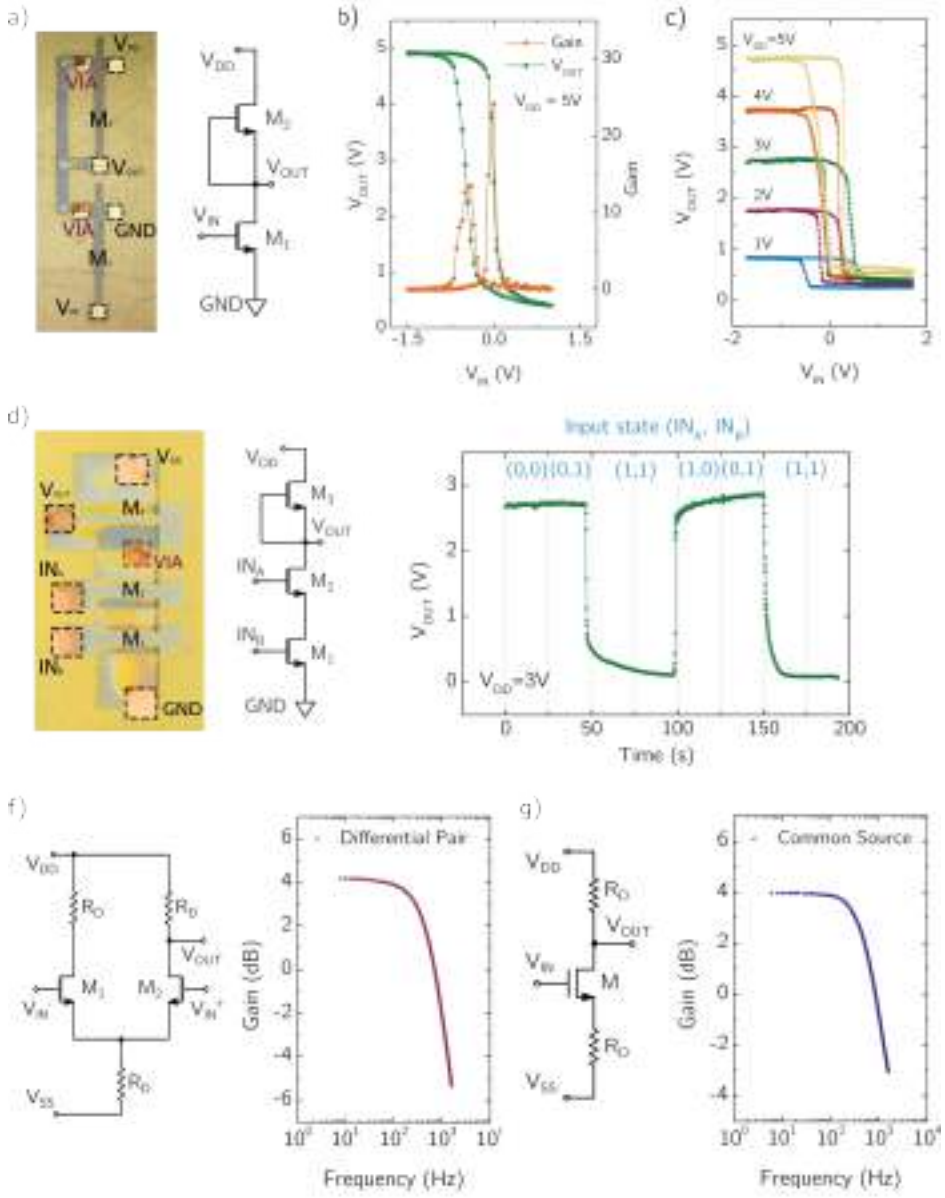

Figure 4. a) Optical micrograph and electrical schematic of a depletion-load inverter. b) Transfer characteristic (left axis) and voltage gain modulus (right axis) of a depletion-load inverter gate as a function of the input voltage, for a supply voltage of 5 V, and for diverse values of supply voltage, down to 1 V (c) d) Optical micrograph and electrical schematic of a depletion-load NAND gate. e) Output voltage of the NAND gate as a function of the input sequence (V_{IN_1},V_{IN_2}), with a supply voltage of 3 V. f) Electric schematic of a differential pair (left) and its frequency response (right). g) Electric schematic of a degenerated common source stage (left) and its frequency response (right).

isfied by our device. Moreover, the output state transitions are steep and the output swing is almost full. To demonstrate the versatility of our technology, we have also defined analog circuits. The schematics of a fabricated differential pair and a degenerated common-source stage [55] are presented in Figure 4f and g, respectively. Transistors M_1, M_B and M are all fabricated with an aspect ratio of about 7, the supply voltages applied are ± 10 V, and the values of resistances R_D and R_S are 8.2 MΩ and 1 MΩ, respectively. In addition, the corresponding frequency responses, illustrating gain as a function of frequency, are provided for both circuits. This characterization demonstrates the capability of our technology in the realization of analog circuits with desirable performance.

CONCLUSIONS

In this study, we have successfully defined ultra-thin and highly conformable field-effect transistors (FETs) using a low-cost and low-temperature fabrication process, which combines high-quality MOCVD-grown monolayer MoS_2 with solution-processable organic materials such as PI, PVF and PEDOT:PSS. Our approach involves the sequential stacking of nanometer-scale layers of flexible materials, resulting in a gate-stack structure with a total thickness of 90 nm. Notably, this achievement surpasses results obtained by processes that do not include lithographic steps. The fabricated FETs exhibited exceptional performance characteristics, facilitating their integration into more complex electronic circuits for both digital (e.g., depletion load inverter and NAND gates) and analog (e.g., differential pairs and degenerated common source amplifiers) applications. Furthermore, our investigation demonstrated that these devices maintain satisfactory operation under bending stress and repeated bending cycles, with minimal impact on their characteristics. This resilience is crucial for applications in conformable electronics, affirming the validity of our approach.

METHODS

Field-effect transistors were fabricated with a top-gate/top-contact configuration on MoS_2 films transferred onto polyimide (PI) substrates. PI substrates were defined starting from solution (PI2611, purchased from HD Microsystems) deposited on top of silicon chips, with a film thickness of 3.8 μm, following the procedure described in Section 1 of the Supporting

Information. MOCVD-grown MoS_2 films were grown following the procedure reported by Cun *et al.* [30].

Molybdenum disulfide patterning

Isolated rectangular regions of MoS_2 films on the native sapphire substrate were defined by mechanically scratching the surface with a high-precision materials printer equipped with a scratching lithography tool. This step ensured insulation between neighbouring devices on the same substrate, reducing leakage current during biasing. Then, the MoS_2 films were transferred on the PI substrates following the procedure described in Section 3 of the Supporting Information. Raman analysis of MoS_2 before and after the transfer process has been performed to prove the high quality of this semiconducting layer. The complete analysis has been reported in Section 4 (Fig S3) of the Supporting Information.

Inkjet printing

Inkjet printing was used for the definition of source, drain, gate electrodes and interconnections. A Fujifilm Dimatix DMP2850 equipped with 2.4 pL Samba nozzle cartridges was used to print patterns with a PEDOT:PSS conductive ink (RD CleviosTM P Jet X N, purchased from Heraeus). The conductivity of PEDOT:PSS and the dispersion viscosity were enhanced by incorporating anhydrous ethylene glycol (99.8% by Sigma Aldrich) at a 5% *wt.* concentration. Then, a non-ionic polyoxyethylene surfactant solution (TritonTM X-100 by Sigma Aldrich) was added to improve the wettability of the ink at a 1% *wt.* concentration. All electrodes and patterns were printed in one layer with a drop spacing of 25 μm, with the printer platen temperature heated at 40 °C. No annealing or post-treatment processes were performed after any of the printing steps.

Polyvinyl formal deposition

Once defined the bottom source and drain electrodes on top of the MoS_2 areas, the PVF nanosheets were recollected following the procedure described in Section 2 of the Supporting Information. The procedure was repeated twice to build a double layer stack of PVF

nanosheets, with a final thickness of 50 nm, with the purpose of improving the dielectric reliability, i.e., reducing the leakage current of the final transistors. Raman analysis of the structure with PI/MoS_2/PVF has also been performed and reported in Section 4 (Fig S4) of the Supporting Information.

Circuits Fabrication

For interconnecting transistors, PEDOT:PSS and a commercial water-based gold ink (DryCure Au-J purchased from C-INK Co., Ltd.) were used to create vias through the insulating layer. These vias enabled the connection of top gate electrodes to bottom source and drain electrodes. To test the device properties under different bending conditions, the PI films with the integrated devices on top were peeled from the initial rigid substrates and transferred on cylindrical surfaces with different curvature radii.

Measurements

All electrical measurements were conducted under ambient conditions. DC characterization of transistors and circuits was performed using a Keithley 4200 SCS parameter analyzer, multiple Keithley 2450 source meter units, a Tektronix MSO2014B oscilloscope, a HP 33120A function/arbitrary waveform generator and an ONO SOKKY CF-9400 FFT analyzer. Capacitance measurements were carried out with a Keysight E4989A LCR meter.

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ULTRA-THIN TRANSISTORS AND CIRCUITS FOR CONFORMABLE ELECTRONICS – SUPPORTING INFORMATION

Polyimide films deposition and morphological characterization

Polyimide films were deposited on SiO_2/Si substrates of approximately 1 cm^2 area. The chips were first cleaned in acetone and isopropyl alcohol (IPA), then treated with 15 minutes UV/ozone (UVO) to enhance surface hydrophilicity, followed by dehydration for 15 minutes at 135 $°C$ on a hotplate. The polyimide solution (PI2611, purchased from HD Microsystems) was spun at 3000 rpm for 40 seconds on top of the cleaned chips, achieving a film thickness of 3.8 μm. A two-step soft baking process (65 °C for 3 minutes, then 135 °C for 3 minutes) was performed to remove excess solvent. Finally, a two-step curing treatment was performed in a quartz tube furnace in N_2 atmosphere (1000 sccm): 200 °C for 1 hour, then 300 °C for 2 hours, allowing polymerization and cross-linking. The curing temperature sets the maximum processing temperature that the PI film can withstand, with the glass transition occurring at 380 °C. A ramp rate of 2 °C per minute ensured low residual mechanical stress, producing high-quality films. The deposited PI films showed complete compatibility with solution-based methods and low-temperature (below the curing set point) processes.

Figure 5a shows an image of a typical PI film spun over SiO_2, which was used as a substrate for our process. A morphological analysis of a 230×175 μm^2 scratched area of the PI film, reported in Figure 5b, was performed with a microprofilometer (Bruker DektakXT) operated in the 3D Map mode. The analysis revealed an average thickness of 3.8 μm with minimum fluctuations on the PI surface. Figure 5d illustrates the thickness of the PI film as it varies with the measurement direction (Y), obtained from the morphological map represented in Figure 5c by averaging in the transversal direction (X) of the profiles. The error bars depict thickness fluctuations, approximately 1.5 nm for the SiO_2 surface and 20 nm for the PI surface.

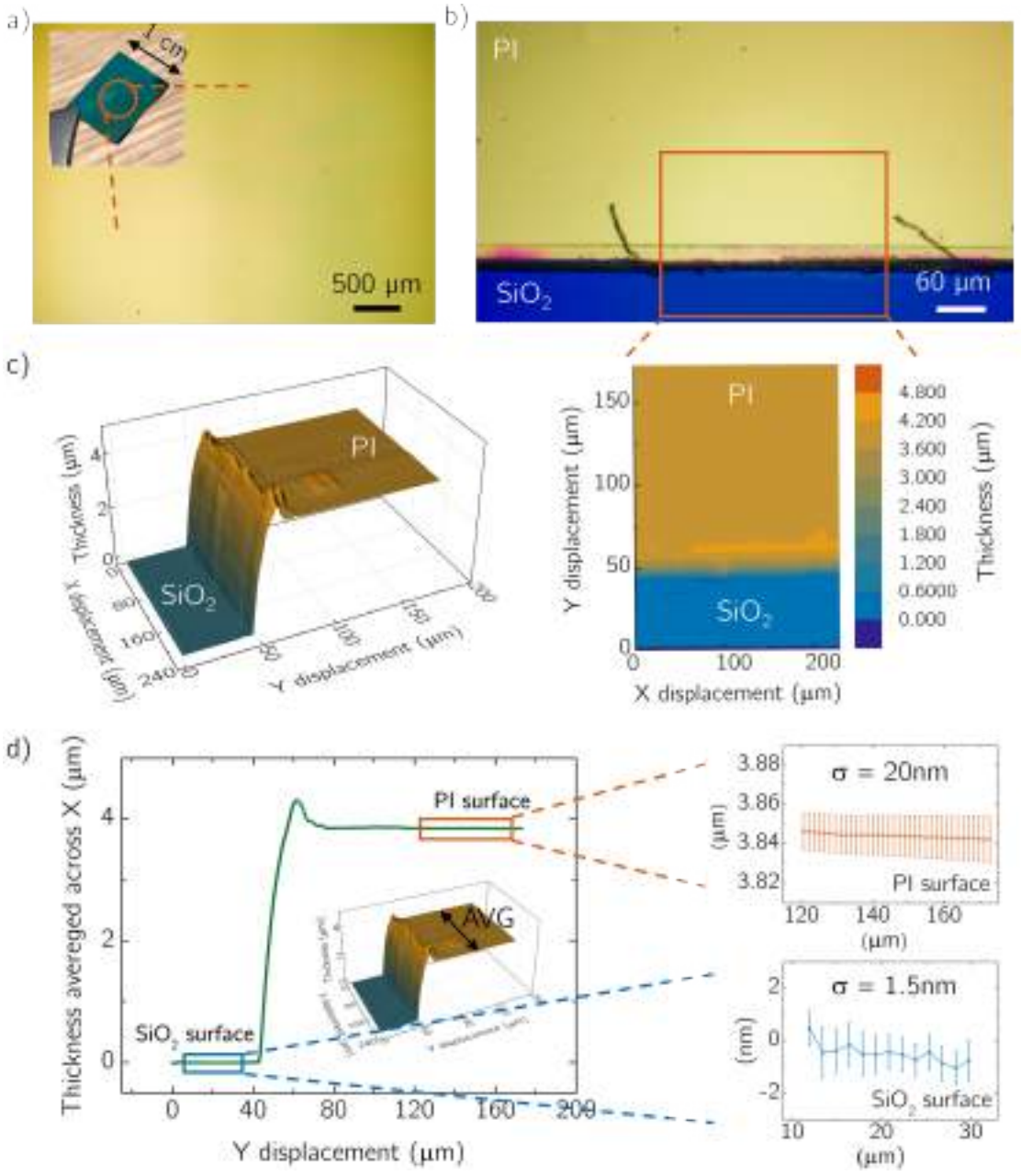

Figure 5. a) Micrograph of a PI film surface in its central region. In the inset, a picture of the sample, handled with tweezers. b) Micrograph of the scratch made with a surgery blade on the PI film for the morphological analysis. c) Morphological map of a 230×175 μm^2 area as a result of the microprofilometer measurements. The thickening of the PI film at its edge is attributed to the formation of wrinkles due to the stress caused by the blade. d) PI film profile along the Y direction, derived from the map averaging in the X direction. On the right, detailed views of the regions of PI and SiO_2. The error bars represent the standard deviation (σ) of the thickness.

Polyvinyl formal films deposition and transfer

Poly(vinyl formal) (PVF) nanometric films fabrication was performed adapting the processes previously reported by Viola *et al.* [25] and Baxamusa *et al.* [56].

For the preparation of the dielectric layer, two solutions were needed: one for the PVF layer, purchasing the starting powder from SPI Supplies as Vinylec E Polyvinyl Formal Resin, and a second for the poly(diallyldimethyl ammonium chloride) (PDAC) layer (purchased in solution, 20% *wt.* in deionized water, from Sigma Aldrich). A 0.5% *wt.* PDAC solution was obtained by dilution in deionized water and then stirred for 15 minutes. A 1% *wt.* PVF solution was prepared dissolving the PVF powder in ethyl lactate (EL) by stirring at 650 rpm and 50 °C for 3 hours. Before use, the PVF solution was heated to 50°C and stirred, again at 650 rpm, for 15 minutes to prevent polymer aggregates.

A Si wafer, used as substrate, was initially cleaned with acetone, followed by IPA, then treated with 15 UVO to improve the wettability of its surface. Immediately after, the PDAC solution was spun on its top at 4000 rpm for 15 seconds, followed by 10 seconds of baking on a hot plate at 100 °C, resulting in a subnanometric layer. The PVF solution was spun over the PDAC layer in a two-step process: 5 seconds at 300 rpm and 5 seconds at 3000 rpm. The PVF and PDAC layers were then baked on a hot plate at 50 °C for 60 seconds to remove the excess solvent, achieving a thickness of 25 nm. The PVF/PDAC layers were then cut in squares and transferred from the carrier to the receiver substrates, taking advantage of the hydrosolubility of the PDAC interlayers. The carrier wafer was slowly dipped in deionized water at an angle of approximately 45°, inducing the complete dissolution of the PDAC interlayer. Finally, the PVF nanosheets, floating on the water surface due to their hydrophobicity, were drawn directly with the final substrates.

Figure 6a and b show the schematic representation of the process and some pictures taken during the delamination and recollection phases.

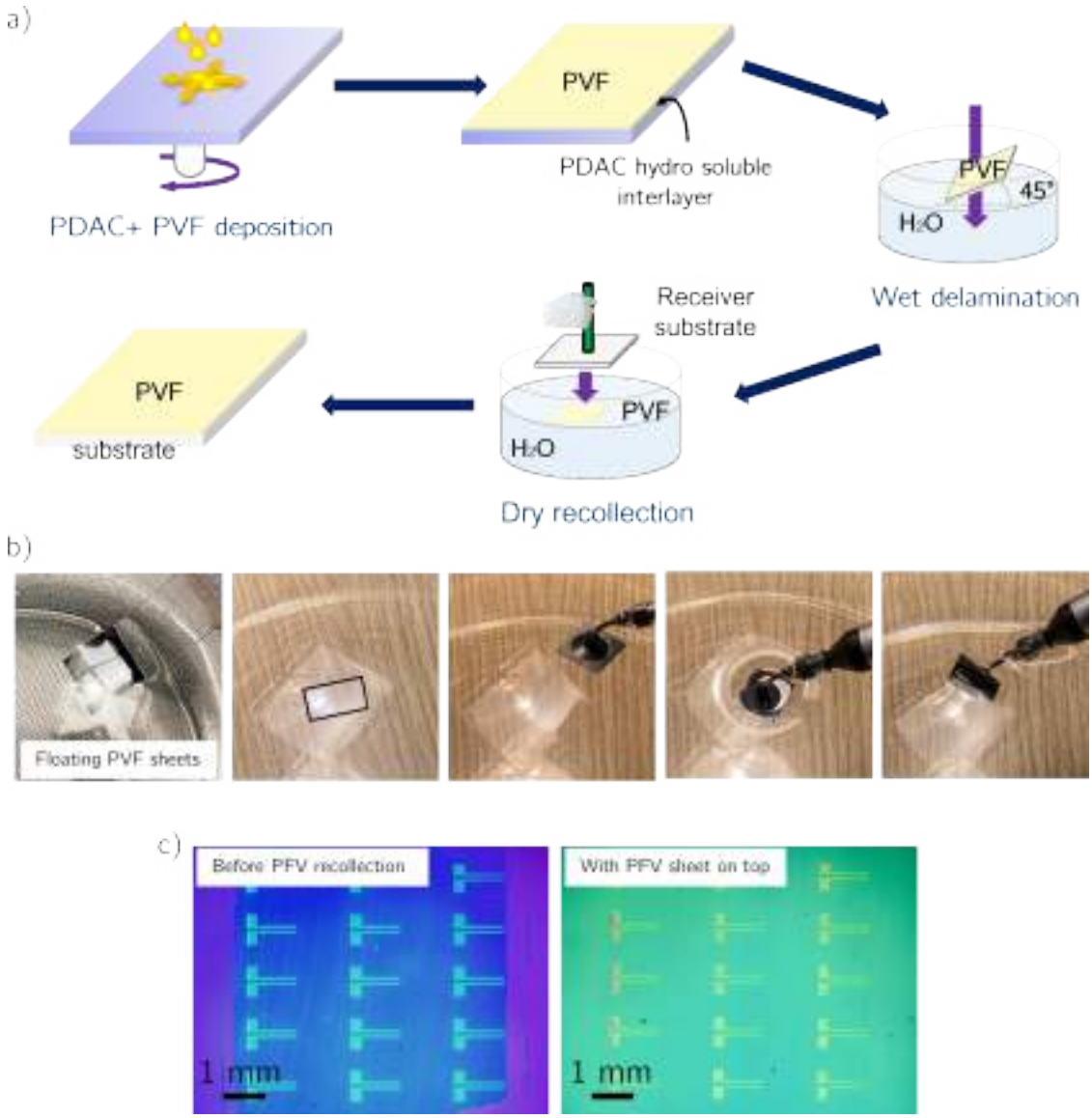

Figure 6. a) Schematic representation of the PVF deposition and transferring process. b) Pictures taken during the PVF nanosheets transfer process. From the PVF sheets floating on the deionized water surface, after the delamination from their carrier Si wafer (on the left), to the single PVF sheet (marked with a black dotted rectangle) recollection, once in close contact with the receiver substrate (on the right). c) Micrographs showing an example of a PVF film transfer on a Si/SiO_2 substrate with MoS_2 and PEDOT:PSS electrodes on top (left).

Molybdenum disulfide films transfer

For the transfer process, a layer of poly(methyl methacrylate) (PMMA) was spun over MoS_2 grown on sapphire substrates, to provide mechanical stability and preserve the quality

of the 2DM layer and to ease its detachment. A piece of commercial thermal-release tape (3195MS purchased from REVALPHA) was attached to the substrate and immersed in deionized water for 10 minutes. The stack composed by the thermal tape with PMMA and the embedded MoS_2 was then peeled off from the sapphire and placed on the PI/Si substrate on a hotplate at 50 °C, for 30 minutes. The thermal tape was then released, raising the temperature to 130 °C. Finally, the sacrificial layer of PMMA was removed with a bath in hot acetone (50 °C) for 1 hour and a rinsing in IPA.

The schematic representation of the process together with some pictures taken during its progress are reported in Figures 7a and 7b, respectively. In Figure 7c, the MoS_2 film transferred on top of SiO_2 (left) and of PI (right) substrates is shown.

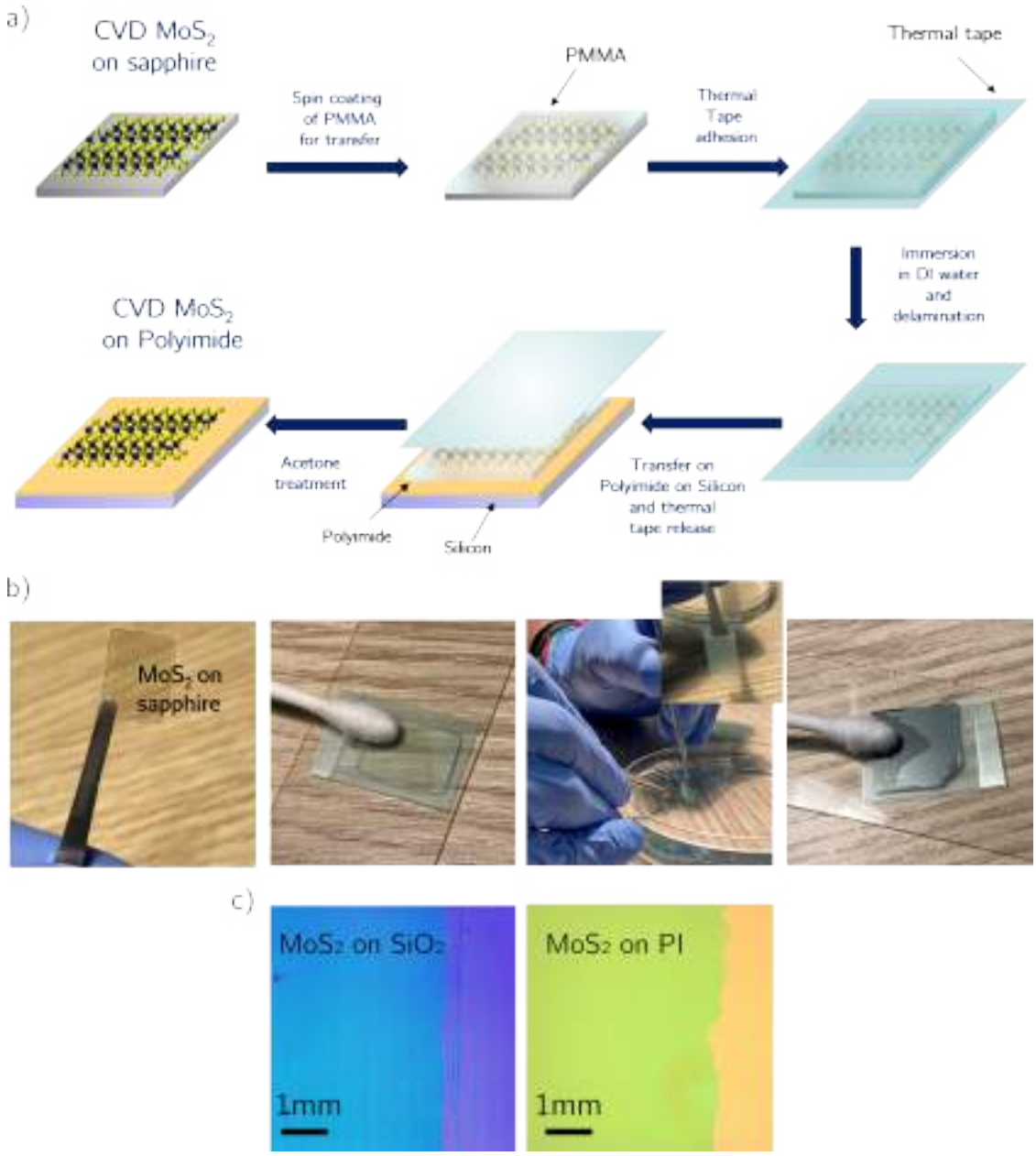

Figure 7. a) Schematic representation of a MoS_2 film transferring process. b) Pictures taken during the process. From left to right: Sapphire substrate with MoS_2 on top, first thermal release tape adhesion on PMMA/MoS_2/sapphire stack (a cotton swab helps to avoid formation of bubbles), peeling of the tape/PMMA/MoS_2 stack from sapphire, and its transfer on PI through the second adhesion (a cotton swab is used again with the same purpose). c) A MoS_2 film transferred on top of SiO_2 (left) and on PI (right) substrates.

Raman analysis

Scanning Raman spectroscopy was carried out with a Renishaw InVia system, equipped with a confocal microscope, a 532 nm excitation laser and a 2400 line/mm grating (spectral resolution < 1 cm^{-1}). All analysis were performed with a 100X objective ($NA = 0.85$), an excitation laser with a power of 500 μW and an acquisition time of 3 seconds. The Raman modes were fitted with a Lorentzian peak.

Figure 8 presents the Raman characterization of the monolayer MoS_2. The representative Raman spectra (Figure 8a), of MoS_2 on the sapphire growth substrate (black line) and of MoS_2 transferred to polyimide with PVF on top (red line), present the standard Raman modes, E_{2g}, at 385.1 cm^{-1} and A_{1g}, at 405.2 cm^{-1}. The A_{1g} mode corresponds to the sulfur atoms oscillating in anti-phase out-of-plane and the E_{2g} mode is related to the sulfur and molybdenum atoms oscillating in anti-phase parallel to the crystal plane [57].

To quantify strain and doping after the transfer process, we employed the MoS_2 correlation plot of the Raman shifts of modes E_{2g} and A_{1g}, also known as the $\epsilon - n$ system [58, 59]. This method allows to disentangle and to quantify the strain and doping variations and it is normally employed for studying the effect of different growth substrates [60] or in transferred MoS_2 for the development of Van der Waals heterostructures [61]. The full lines represent the zero strain and zero doping lines, while the dashed lines correspond to iso-strain and the iso-doping lines, calculated following the insights from previous works [57, 62].

The origin of the system $\epsilon - n$ is the zero strain and charge neutrality phonon frequencies, which are set at 385 cm^{-1} for the E_{2g} mode and at 405 cm^{-1} for the A_{1g} mode, evaluated in the case of CVD-grown MoS_2 suspended monolayer membrane [57]. Data on the MoS_2 monolayer grown on the sapphire substrate present a round distribution revealing a strain-free monolayer and an average positive charge concentration of $(2.24 \pm 0.05) \cdot 10^{12}$ cm^{-2}. While, in the case of the MoS_2 transferred on polyimide, the data distribution is horizontally dispersed. Tensile strain varies between strain-free and to a maximum value of 0.05%. The charge concentration increases, showing a variation between $2.3 \cdot 10^{12}$ cm^{-2} and $3.4 \cdot 10^{12}$ cm^{-2}. The increase of the tensile strain is probably due to the morphology of the polyimide layer, which has a larger roughness compared to sapphire. The increase in electron concentration is related to a possible charge transfer from the polymeric insulators, as reported in the supporting information of reference [58].

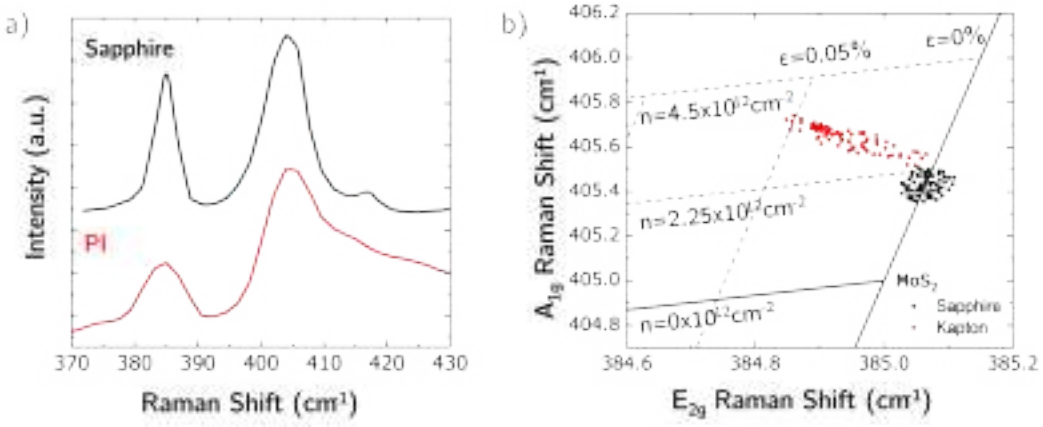

Figure 8. Comparison of the Raman data of MoS_2 monolayer on sapphire and on PI. a) Representative Raman spectra, on sapphire (black line) and on PI (red line). b) MoS_2 $\epsilon - n$ correlation plot for the evaluation of the strain and carrier concentration in case of the MoS_2 grown on sapphire (black dots) and transferred on PI (red dots).

Figure 9 presents the Raman spectrum of a PI/MoS_2/PVF structure, fabricated on a SiO_2/Si substrate in order to have a more intense Raman signal. The sharp mode at 520 cm^{-1} is assigned to the silicon transverse optical vibrational mode. In addition, the Raman spectrum presents several vibrational modes above 1000 cm^{-1}, attributed to PVF and PI. The accurate attribution of the different vibrational modes is reported in Table SI. The inset presents an enlargement of the range of the MoS_2 Raman modes, where the E_{2g} and A_{1g} peaks appear at 385 cm^{-1} and 405.3 cm^{-1}, respectively. The Raman modes of the MoS_2 are superimposed to a broad band at 450 cm^{-1} assigned to the PVF.

Peak Raman Shift (cm^{-1})	Material	Attribution	Reference
1106	PI	C–N–C transverse vibration	[63, 64]
1253	PVF/PI	C–O stretching	[63–65]
1305	PVF	CH bending vibration	[63–65]
1383	PVF/PI	C–C stretching	[63–65]
1439	PVF/PI	C–N stretching	[63–65]
1505	PI	C=C stretching	[63, 64]
1616	PI	C=C stretching	[63, 64]

Table I. The table STT presents a resume of the attribution of the Raman modes.

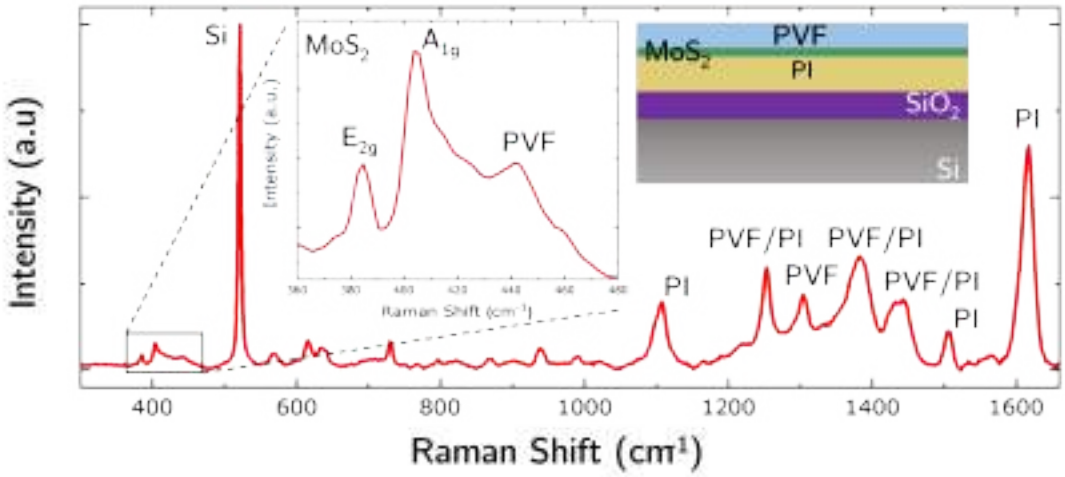

Figure 9. Raman analysis of the structure PI/MoS_2/PVF, attached on a SiO_2/Si substrate. The insets present: a sketch of the structure in analysis and an enlargement of the range of the MoS_2 Raman modes.

AFM measurements on FET stacks

AFM topography and phase maps were collected using a Bruker AFM operated in the Scan assist mode. The AFM measurements were performed by scratching the surface of a dedicated device fabricated on a SiO_2/Si substrate, employing a custom in-house developed scribing system [43].

The AFM morphological analysis allowed an accurate evaluation of the thicknesses of both the drain stack and gate stack. Figure 10a reports the morphological map of the drain stack consisting of MoS_2, PEDOT:PSS drain electrode and PVF, and the line profile obtained by AFM measurements, revealing a thickness of 120 nm. A similar analysis was conducted for the gate stack (Figure 10b), composed of MoS_2, PVF, and PEDOT:PSS gate-electrode, where the line profile reveals a total thickness of 90 nm.

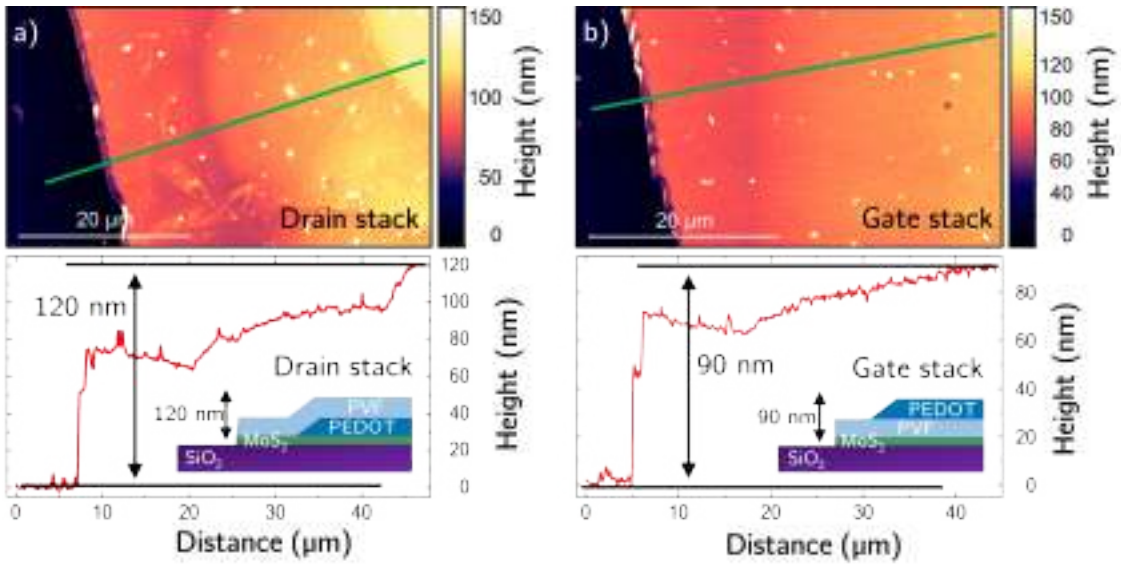

Figure 10. AFM morphological maps of the drain stack (a) and the gate stack (b). The related line profiles, indicated on the map by a green dashed line, are reported below each corresponding map, with a schematic representation of the measured device stack as inset.

Electrical characterization and descriptive statistics

The statistics of electrical parameters were derived employing a customized Python script. An ensemble of 85 transistors, sharing identical nominal dimensions of $L = 65$ μm and $W = 420$ μm, was characterized. For each transistor, both a forward and a backward I_D - V_{GS} curve, with V_{GS} ranging from -4 V to 5 V, and V_{DS} set to 0.5 V, were measured. Gate leakage (I_G) and source (I_S) currents were simultaneously measured too.

The script processed raw data from individual devices within the dataset, excluding any defective units (e.g., those exhibiting short circuits between electrode pairs or open circuits between source and drain) from analysis. For every acceptable device, the I_D - V_{GS} curves were further processed. To reduce the impact of noise, each curve was smoothed with a least-squares polynomial fitting. Two separate sets of parameters (from the forward and backward curve) were extracted for each device.

Threshold voltages (V_{TH}) were determined as the V_{GS} value where the tangent line to the I_D - V_{GS} curve, at its maximum slope intersects the V_{GS} axis (i.e., with the maximum transconductance method). A graphical representation of the procedure can be found in Figure S11a.

The values of V_{TH} were subsequently used for the evaluation of the field-effect mobility (μ_{FE}) values. To this purpose, we used the expressions derived for both the linear and the saturation regime of an ideal long-channel MOSFET for $V_{GS} > V_{TH}$:

$$\mu_{FE} = \begin{cases} \frac{L}{W}\frac{1}{C_i}\frac{1}{V_{DS}}\frac{\partial I_D}{\partial V_{GS}}, \mathrm{V}_{DS} < V_{GS} - V_{TH} \\ 2\frac{L}{W}\frac{1}{C_i}(\frac{\partial\sqrt{I_D}}{\partial V_{GS}})^2, \mathrm{V}_{DS} > V_{GS} - V_{TH} \end{cases}$$

where C_i is the insulator film capacitance per unit area. An example of mobility value extraction can be found in Figure S11c.

Regarding the on-off current ratios, Cheng *et al.* [44] proposed an alternative metric to the traditional I_{on}/I_{off} ratios, due to the ambiguity in the choice of the gate voltages corresponding to the ON and OFF states. We thus adopted their methodology and computed the I_{max}/I_{min} ratios, evaluated within the linear regime, as a more robust indicator of FET performance for digital applications.

Finally, the subthreshold slope (SS) values were computed as the minimum change in ΔV_{GS} required to achieve a tenfold increase in I_{DS}, specifically within the exponential regime of the transfer curves (i.e., in the subthreshold regions, where $V_{GS} < V_{TH}$). Figure S11b illustrates the procedure.

Statistical distributions and complete descriptive statistics of the forward and backward parameters, extracted with the above procedures, can be found in Figure S12 and in Table SII. Values of mobility (μ_{FE}), threshold voltage (V_{TH}), subthreshold swing (SS) and current ratio (I_{max}/I_{min}) are reported.

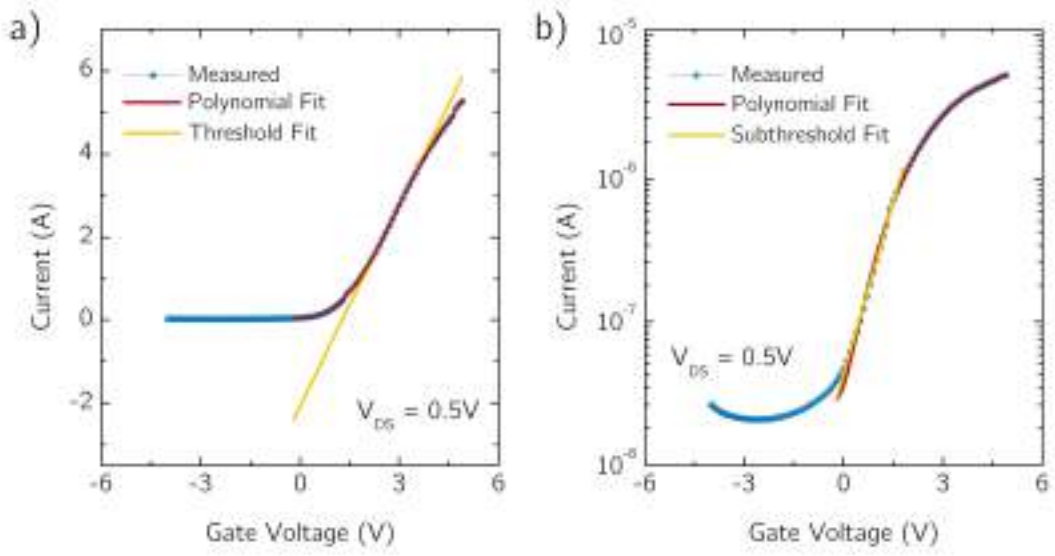

Figure 11. Graphical representation of the parameters extraction process. a) Polynomial fitting (red line) of a target transistor's transfer characteristic curve (blue line). The threshold voltage value is determined by the intercept point where the tangent to the transfer curve (yellow line), at its maximum slope, intersects the V_{GS} axis. b) Polynomial fitting (red line) of the same transfer characteristic curve (blue line), depicted in semi-logarithmic scale. The subthreshold fit line (yellow) is utilized to determine the boundaries of the V_{GS} interval within which the transfer curve experiences a tenfold increase in I_{DS}, specifically within the subthreshold region ($V_{GS} < V_{TH}$). Additionally, I_{max} and I_{min} are indicated on the transfer curve. c) Representation of field effect mobility (yellow line) as a function of the gate voltage, calculated from the same transfer characteristic (blue line). The target mobility value is extracted in its maximum.

Ultra-thin capacitors fabrication and characterization

Parallel plate capacitors featuring inkjet-printed PEDOT:PSS as top/bottom electrodes and PVF as insulator were fabricated on PI substrates to assess the electrical properties of PVF thin films, as illustrated in Figure 13a. The fabrication process replicates that of FETs, with the omission of the step involving MoS_2 transferring.

A set of 24 working capacitors fabricated on the same PI substrate was characterized by modeling the capacitors with an R_P–C_P parallel model, wherein R_P accounts for leakage through the dielectric film phenomena. The impact of series resistance was disregarded, given the high conductivity of the PEDOT:PSS electrodes. C_P and R_P were estimated by

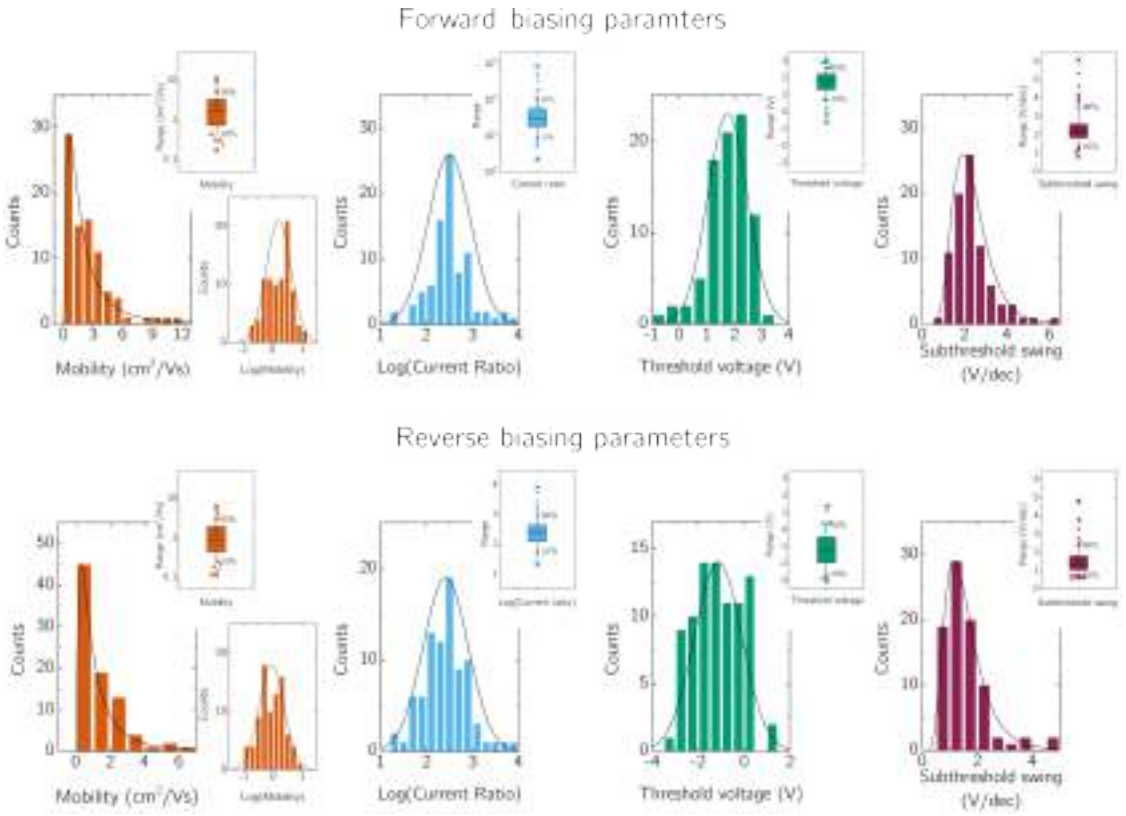

Figure 12. Hystograms reporting the statistical distributions of the forward biasing (a) and backward biasing (b) electrical parameters, calculated for the characterized set of 85 working transistors fabricated on the same chip. Mobility and subthreshold swing are fitted against a log-normal distribution, while threshold voltage and logarithm of current ratio against a normal distribution. Box representations, featured in the insets, show the mean and median values. The error boxes span from the 25^{th} to the 75^{th} percentiles. Additionally, mobility is shown logarithmically transformed in the insets and fitted against a normal distribution.

evaluating the capacitor performance across a frequency range, from the DC to the high-frequency regime. The measurements were conducted using a four-probe configuration while applying a 1 V amplitude sinusoidal signal. An open circuit calibration was performed before data acquisition to evaluate the system's parasitic capacitance, considered as an offset in the capacitance measurements.

Figure 13b reports the average values of the capacitance per unit area C_P, the conductance per unit area G_P, the admittance ratio $\omega C_P/G_P$ between the capacitive susceptance and the parallel parasitic conductance, and the relative permittivity ϵ_r, for the characterized set

	Bias	Mean	Std dev	L 95% CI	U 95% CI	Min	Med	Max
μ_{FE} (cm^2/Vs)	fw	2.44	2.30	1.94	2.93	0.172	1.68	11.5
	bw	1.35	1.27	1.08	1.63	0.112	0.865	6.45
V_{TH} (V)	fw	1.76	0.734	1.60	1.92	-0.575	1.89	3.10
	bw	-1.13	1.04	-1.36	-0.909	-3.02	-1.17	1.41
SS (V/dec)	fw	2.36	0.930	2.16	2.56	0.817	2.21	6.12
	bw	1.58	0.823	1.41	1.76	0.584	1.41	4.86
I_{max} (μA)	fw	1.92	1.85	1.52	2.32	0.111	1.24	9.64
	bw	2.01	1.93	1.59	2.427	0.121	1.31	10.1
I_{min} (nA)	fw	9.18	13.8	6.20	12.2	0.239	5.06	95.3
	bw	12.8	21.2	8.18	17.3	0.311	6.20	123
I_{max}/I_{min}	fw	631	1217	369	894	21.7	302	8523
	bw	554	1165	303	806	21.2	272	8744

Table II. Descriptive statistics for the characterized array of 85 working transistors fabricated on the same chip. Mean, standard deviation, upper and lower 95% confidence intervals, minimum, maximum and median values are reported for extracted mobility (μ_{FE}), threshold voltage (V_{TH}), subthreshold swing (SS), maximum (I_{max}) and minimum (I_{min}) drain currents and their ratio (I_{max}/I_{min}). Values are extracted from the set of measured transfer characteristics. Entries labeled as "fw" and "bw" refer to the forward (rising V_{GS}) and backward (falling V_{GS}) biasing, respectively.

of capacitors, with error bars representing the standard deviation. The $\omega C_P/G_P$ ratio is a crucial figure of merit for real capacitors, indicating their quality in terms both of material properties and fabrication reliability. A higher value signifies a device closer to its ideality, where the leakage phenomena through the insulating layer can be neglected. Our capacitors exhibit exceptional reliability with a constant value of ϵ_r up to frequencies on the order of tens of kilohertz, enabling their application in a wide range of digital and analog electronics.

The dielectric constant was derived from the measured capacitance values according to

the parallel plate capacitor model:

$$\epsilon_r = \frac{C_P t}{A \epsilon_0}$$

where A is the area of the capacitor (designed to be a square with a side of 400 μm), ϵ_0 is the vacuum permittivity value ($8.85 \cdot 10^{-12}$ $\mathrm{AsV^{-1}m^{-1}}$, while an average thickness (t) equal to 50 nm of the PVF insulating layer was considered.

A representation of the mean admittance $Y = G_P + j\omega C_P$, in terms of both amplitude ($|Y|$) and phase (Φ_Y), as a function of frequency is depicted in Figure S13c for the same set of capacitors, with error bars representing the standard deviation of values. Consistent with the conclusions regarding the $\omega C_P/G_P$ ratio, the graph illustrates that the phase of the admittance maintains a value close to $\pi/2$ for frequencies up to 10^4 Hz, indicating its nearly ideal capacitive behavior with negligible parasitic effects.

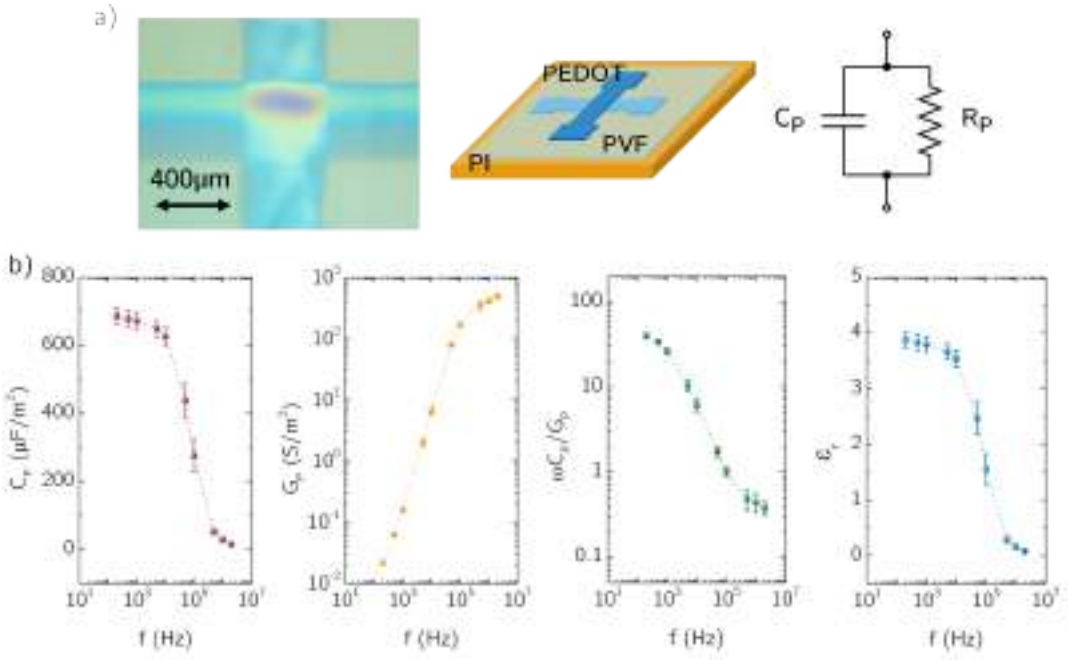

Figure 13. a) Optical micrograph, sketch and equivalent electric schematic of a parallel plates capacitor fabricated on PI, with top/bottom electrodes made of PEDOT:PSS, and 50 nm thick PVF as dielectric material. b) Dynamic electrical characterization of an array of 24 working capacitors fabricated on the same PI substrate. The capacitance per unit area C_P, the conductance per unit area G_P, the admittance ratio $\omega C_P/G_P$, and the relative permittivity ϵ_r are reported as functions of the applied voltage frequency, spanning from 200 Hz to 2 MHz. Mean values are reported and error bars represent the standard deviation. C) Amplitude ($|Y|$) and phase (Φ_Y) representation of the mean admittance $Y = G_P + j\omega C_P$ as a function of frequency, for the same set of capacitors. The standard deviation is represented by error bars.

Electromechanical characterization

The pliability and conformability of PEDOT:PSS-PVF parallel plate capacitors and MoS_2-PEDOT:PSS-PVF transistors were evaluated under both static and dynamic bending conditions.

Static characterization involved examining their electrical response under varying static bending conditions with curvature radii of 14 mm and 11 mm. Dynamic characterization aimed to demonstrate their functionality during repeated bending cycles, with up to 500 cycles performed. The results of this investigation are depicted in Figure 14.

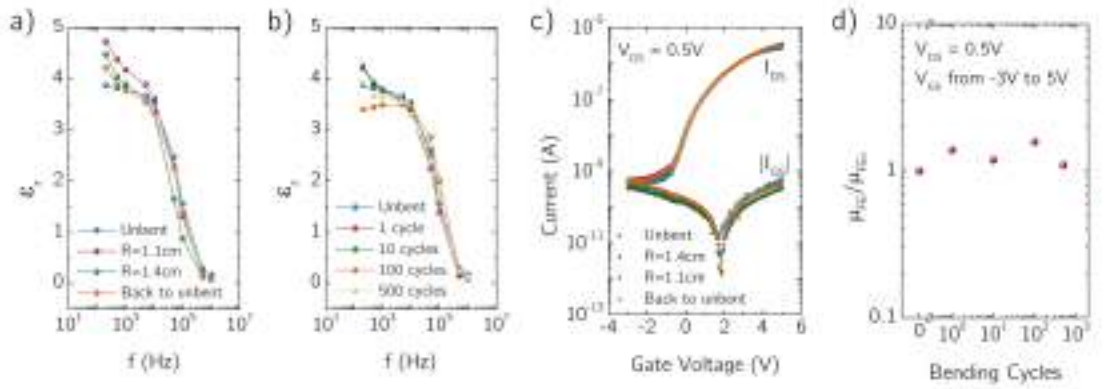

Figure 14. Dynamic characterization of our devices under bending conditions. a) Relative permittivity of PVF (ϵ_r) measured for different bending radii, and before and after a sequence of bending cycles (up to 500) (b), as functions of the applied voltage frequency, spanning from 200 Hz to 2 MHz. c) Transcharacteristic curve measured for a drain voltage of 0.5 V and for different bending radii. d) Field-effect mobility μ_{FE} measured after several bending cycles (up to 500) and normalized to its starting value μ_{FE_0} (before undergoing mechanical stress).

Capacitors were characterized by determining the average relative permittivity (ϵ_r) as a function of the applied voltage frequency, ranging from 200 Hz to 2 MHz. Transistors were characterized by measuring their transfer characteristic (I_D as a function of V_{GS}) at a fixed V_{DS} value of 0.5 V, while concurrently extracting their average mobility (μ_{FE}) as a control parameter. Negligible alterations in their electrical behavior were observed during both static and dynamic characterizations. Any minor variations can be attributed to the measurement conditions themselves, as applying the probes becomes more challenging when the device is bent, potentially compromising the measurement accuracy.

Table of comparison

A comparative analysis of various studies on flexible and conformable transistors and circuits reported in the recent literature, focusing on parameters such as transistor film thickness, utilized materials, fabrication techniques and electrical performance (e.g., mobility, operating voltage, and threshold voltage), is reported in Table SIII.

	Gate stack (nm)	Substrate (μm)	S, D electrodes (nm)	G electrode (nm)	Semiconductor (nm)	Dielectric (nm)	Technology	Op. voltage (V)	Mobility (cm^2/Vs)	Th. voltage (V)	Strengths
Our work	110	PI, 3.8	PEDOT, 60	PEDOT, 60	s.l. MoS_2, < 1	PVF, 50	Sol., MOCVD	5	2.44	1.89	Op. voltage, Mobility
[51]	60	PET, 300	Ti/Au, 2/30	Au, 30	s.l. MoS_2, < 1	HfO_2, 30	Sol., CVD, ALD, Litho	8	13.9	N.A.	Mobility, Op. volt.
[45]	120	Parylene, 0.06	Au, 30	Au, 30	DNTT, 30 *or* PDI-8CN2, 30	Parylene, 60	Sol., CVD, Th. dep.	5	0.11	1	Volt., CMOS
[25]	130	Freestanding	PEDOT, 20	PEDOT, 60	DPP-TVT, 20	PVF, 50	Sol.	6	0.092	0.9	Fully sol. based, Op. volt.
[66]	560	Freestanding	Au, 30	Au, 30	PTCDI-C1, 30	PMMA/PVA, 500	Sol., Th. dep.	60	0.52	N.A.	
[46]	360	Freestanding	Au, 20	Au, 20	C8-BTBT, 20	C-PVA, 320	Th. dep.	60	7.22	-15	Mobility
[47]	350	Freestanding	Au, 50	Au, 50	DNTT, 50	Parylene-SR, 250	Sol., Th. dep., PVD	10	0.37	-0.55	Op. volt.
[67]	465	Freestanding	Au, 35	Au, 20	Pentacene, 30	PVDF-TrFE, 415	Sol., EBD, Th. dep.	30	N.A.	N.A.	
[48]	124	Parylene, 0.060	Au, 30	Au, 30	DNTT, 30	Parylene, 64	Sol., CVD, Th. dep.	5	0.34	-1.72	Op. volt.
[68]	> 220	Parylene, 2	PEDOT, 40	PEDOT, 40	DPP-TT *and* P(NDI2OD-T2), N.A.	PMMA, 20 & Parylene, 160	Sol., CVD	10	0.1	N.A.	CMOS, Op. volt.,
[69]	> 250	Parylene-C, 0.7	PEDOT, N.A.	PEDOT, N.A.	TIPS Pentacene, N.A.	Parylene-C, 250	Sol., Th. Dep., CVD	7	0.13	0	Op. volt.
[70]	> 190	Parylene, 0.4	Au, 40	Al, 40	TIPS Pentacene & ActiveInk, N.A.	Al2O3/Parylene-C, 20/130	Sol., Th. dep., Litho, CVD	6	0.14	0.65	Op. volt, CMOS, High freq
[49]	795	PDMS, N.A.	Au, 30	Au, 30	DNTT, 50	PVA/DC1–2577, 285/430	Litho, Sol., Plasma	80	0.68	-0.51	High density
[50]	120	Parylene, 4	MoO_3/Au, 30/40	Al, 45	Ph–BTBT–10, 30	pV3D3, 45	Th. Dep., CVD, Sol.	2.5	4.5	0	Op. volt.
[71]	450	PVA, 0.35	Au, 30	Au, 30	PTCDI–C_{13}, 40	PMMA, 380	Sol., Th. Dep., Litho	70	0.58	N.A.	Op. volt.
[72]	110	Parylene, 1	Ti/Au, 10/75	Cr, 35	IGZO, 50 *or* NiO, 50	Al_2O_3, 25	Th. Dep., EBD, Sput., Litho	5	11	0.4	Mobility, Op. volt., CMOS
[52]	63	PI, 1.5	Cr/Au, 3/30	Cr/Au, 3/30	sl. MoS_2, < 1	Al_2O_3, 30	CVD, ALD, Th. dep	10	6.5	3.8	Mobility, Op. volt.
[73]	> 400	PET,	Graphene, N.A.	Graphene, N.A.	exf. m.l. MoS_2, N.A.	c-PVP, 400	Sol., CVD, RIE, Litho	20	0.7	27.1	
[53]	170	PI, 8	Ni, 50	Al/Ti, 100/35	s.l. MoS_2/h-BN, < 2	Al_2O_3, 35	MOCVD, Sol., Litho, ALD, RIE, Sput.	10	1.8	-4.4	
[74]	> 1380	SEBS	CNT, N.A.	CNT, N.A.	29-DPP-SVS-(2), 130	SEBS-X-azide, 1250	Sol., Th. dep., Litho	30	1.37	-1	High density
[54]	130	PI, 4.8	Au, 50	Ti, 100	s.l. WS_2, < 1	Al_2O_3, 30	Sol., CVD, Th dep., ALD, Sput., Litho	12	2	N.A.	Mobility, Op. volt.

Table III.