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Fabrication of Flexible Double-Gate Organic Thin Film Transistor For Tactile Applications

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In this work, the development of a flexible Double-Gate (DG) organic thin film transistor (DG-OTFT), and its employment is reported for the realization of multimodal tactile sensors. Due to the self-encapsulation of the stacked DG architecture, highly stable organic transistors are obtained that show almost negligible degradation after 6 months. Moreover, such configuration is also very useful for the development of sensing devices. In the case, one of the two gates is used to bias and set the working point of the devices, whereas the second one is connected to a polyvinylidene fluoride(PVDF)-capacitor, a pyro/piezoelectric material. It is demonstrated that the charge displacement induced by the PVDF capacitor due to an applied external pressure or due to a temperature variation led to a reproducible variation of the device's output current. Using this approach high-performing multimodal tactile sensors are obtained with sensitivity to up to 241 nA N^{-1} and 442 nA $°C^{-1}$ respectively.

1. Introduction

Organic thin film transistors (OTFTs) have gained remarkable attention over the past decades as a valid alternative to inorganic TFTs[1] for the fabrication of highly flexible electronic systems.[2–9] In fact, this class of materials offers a wide range of attractive characteristics, such as mechanical flexibility, easy processing, and low-temperature fabrication techniques over large areas and with cost-efficient technologies.[10–15] Therefore, they have been intensively employed for different applications going from flexible and ultra-thin circuits[16–18] to the development of transistors-based flexible sensing systems for wearable electronics applications,[19,20] biosensing,[21] robotics,[22] haptic,[23–25] and artificial skin systems.[26,27]

Over the years many different OTFT architectures have been reported with the aim to improve the transistor electrical performances, stability, and sensing capabilities. Recently, the so-called Double-Gate configuration is gaining a new life, as the employment of a second gate, could lead to a tuning of the transistor threshold voltage, thus allowing for the fabrication of flexible circuits with high performances.[28]

The easiest and more known Double-Gate architecture, as depicted in **Figure 1A**, is generally characterized by the integration of a bottom gate and a top gate TFT, sharing the same active layer. Generally, once the first bottom gate transistor is fabricated, it is possible to deposit at the top of it a second dielectric layer and a further top gate electrode. In this case, the charge carrier accumulation into the device channel can be modulated by the two gates. According to what is already reported in the literature, such devices can be operated in different regimes.[29] Considering a p-type active layer, when both gates electrodes are referred to the same common ground, the device is operated in the so-called symmetric regime. When a negative gate bias is applied from both gates, the devices operate in the double accumulation mode, whereas, by applying a positive bias, it is operated in the double depletion mode. If the polarities of the two gates are different, the transistor is operated in the mixed mode. In other words, if one of the two gate voltages, for instance the bottom one, is kept constant, the transistor threshold voltage can still be modulated by the employment of the second gate. This effect has been successfully employed for the development of organic transistor-based logic circuits, where the top gate was exploited to properly control the threshold voltage or to tune the device performances, such as the operation voltages.[30–32] Moreover, Kwon et al. improved the integration in organic complementary circuits, where n-type and p-type devices were vertically stacked to achieve a 3D monolithic integration.[33]

More than this, the employment of a dual-gate architecture could be exploited for the development of different kind of sensing devices.[34] In fact, by properly functionalizing the second gate electrode, it could be possible to create very efficient charge sensing devices, as inducing charge on the second gate, by any sort of interaction with an external medium, can lead to a reliable threshold voltage shift in the final devices, and, therefore, a detectable output current variation. There are, indeed, several recent reports where such an approach has been

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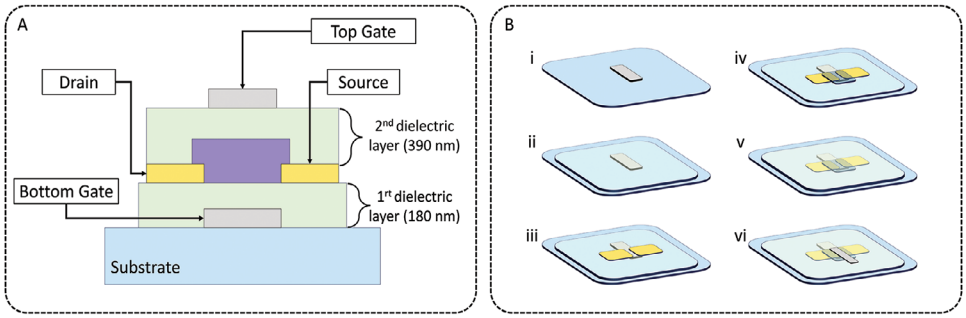

Figure 1. Fabrication process of the proposed Double-Gate organic thin film transistor (DB-OTFT). A) Cross-section of the Double-Gate architecture, with the four terminals and dielectric thicknesses highlighted. B) The device fabrication process started with the deposition of the bottom gate (i) followed by the deposition of the first Parylene C dielectric layer (ii). Afterward, the gold contacts were deposited and patterned (iii) and on the channel area the tips-pentacene was deposited by drop casting (iv). Finally, the second Parylene C dielectric layer (iv) and the deposition of the top gate (vi) ended the fabrication process.

efficiently employed for the fabrication of high performing charge sensing devices. For instance, S. Wu et al. developed a dual-gate electrochemical transistor for monitoring of oxygenation changes, arising from the photosynthesis cycles of saltwater micro-algae.[35] M. Nikolka et al. demonstrated the possibility to develop a platform for electrostatic biosensing applications,[36] whereas R. Pfattner et al. developed a flexible dual-gate structure for pH sensing.[37]

A different approach in the use of the DG-TFT structure is proposed in a recent paper by Jain et al.; their dielectric-modulated Double-Gate presented an innovative structure, based on air gaps between the gates and the active region. In this case, the dielectric is made of two materials, allowing molecules to be trapped within these air gaps. When this happens, a modification of the dielectric constant occurs, leading to a current variation; the sensitivity here depends on how the dielectric constant varies, with greater sensitivity for greater dielectric constant values.[38]

In this paper, the focus is on the optimization of a flexible, low-voltage, Double-Gate organic TFT (DG-OTFT) based on solution-processable organic semiconductor. Interestingly, the Double-Gate transistors show a highly reproducible behavior with similar threshold voltages and relatively high mobilities, and, most importantly, have been characterized for several months without showing any significant device degradation due to the fact that the top dielectric/gate structures dramatically improved its stability against oxygen and moisture. Moreover, by coupling the proposed Double-Gate organic transistor with a pyro/piezoelectric element, namely a commercial film of poly-vinylene difluoride (PVDF), a tactile sensor able to successfully detect temperature and force stimuli for artificial skin applications was developed.

2. Device Fabrication

Two sets of devices were fabricated, each set with 5 transistors. The first set is a common bottom gate-bottom contact organic thin film transistor based on Tips-pentacene, whereas the second set is a Double-Gate organic transistor based on the same semiconductor.

The fabrication process workflow is summarized in Figure 1B. All the devices in this work were fabricated on a 175 µm thick poly(ethylene terephthalate) (PET) substrate. A first Aluminum deposition through a shadow mask was performed to realize the bottom gate of the transistor Figure 1B(i). Both dielectric layers have been realized by using Parylene C. This material was chosen because it can be deposited in pinhole free thin films, forming a conformal coating even on rough surfaces, and it is biocompatible, therefore suitable for the envisioned application.[39,40] A first dielectric layer made by Parylene C was deposited by Chemical Vapor Deposition (CVD) with a thickness of 180 nm and on top of it, gold source and drain contacts were deposited by thermal evaporation and patterned by a standard photolithography process Figure 1B(ii,iii). As an active layer, TIPS-Pentacene (1% in Anisole) was deposited directly on the transistor channel area by drop casting followed by a thermal annealing on a hot plate at 60 °C to ensure the complete evaporation of the residual solvent Figure 1B(iv). The fabrication process workflow for the first set of devices is finished at this step. For the development of the Double-Gate organic transistor, a second Parylene C dielectric layer was then deposited with a thickness of ≈400 nm Figure 1B(v). To complete the device, the aluminum top gate electrode was finally deposited on top of the device through thermal evaporation using a shadow mask Figure 1B(vi). It has been decided to use a thicker second dielectric layer because of the very rough morphology of the drop-casted TIPS-Pentacene film, in order to avoid vertical leakage paths with the top electrode. The cross-section of the proposed device is represented in Figure 1A, where the four terminals of the Double-Gate Organic Transistor are highlighted.

In this work, for the fabrication of the pyro/piezoelectric capacitors, an already stretched and poled 110 µm-thick Poly(vinylidene fluoride) (PVDF) film from Measurement Specialties Inc.-MEAS was employed. Two thermal evaporated aluminum electrodes were realized on both sides of the film through

Table 1. Mean values for Vth, µ and leakage current for the two sets of samples measured at day 0.

	Not Encapsulated	Encapsulated
V_{th} [V]	$(7,1 \pm 1,1) \cdot 10^{-1}$	$(7,5 \pm 3,2) \cdot 10^{-1}$
µ [$cm^2V^{-1}s^{-1}$]	$(1,9 \pm 0,4) \cdot 10^{-1}$	$(2,3 \pm 0,5) \cdot 10^{-1}$
I_{GS} [A]	$(5,1 \pm 4,0) \cdot 10^{-11}$	$(8,7 \pm 3,9) \cdot 10^{-10}$

a shadow mask. Specifically, we developed a set of three different capacitor dimensions, namely 25, 9, and 1 mm^2.

3. Results and Discussions

3.1. Ageing Analysis

At first, we have characterized two sets of samples. The average results are reported in **Table 1** and the typical output and transfer curves are reported in **Figure 2A** for what concerns the single-gated devices and Figure 2B for the finished double-gated devices. As clearly noticeable from the reported data, the average electrical performances are very similar in the two sets of devices, moreover, it can be also noticed, as expected, as reported in Figure 2C, the electrical performances of the Double-Gate devices can be finely modulated by the employment of the second gate.

Due to the asymmetric structure of the double-gated devices, it has been decided to use the bottom gate to bias the transistor while the top gate is used to set the working point by applying different voltages or use it as sensing electrode.

As described in the device fabrication section, all the devices analyzed in this work have been fabricated using TIPS-Pentacene, deposited by drop-casting, as organic active layer. As TIPS-Pentacene, when interfaced with gold electrodes, is a very good hole transport layer, all the fabricated devices behave as unipolar p-type organic transistors. When a negative voltage is applied by the bottom gate, the charges injected from the source can be collected at the interface with the bottom gate dielectric, forming the transistor channel. In the double gated devices, applying a negative (positive) voltage with the top gate, leads to the formation of a second channel at the top gate dielectric/semiconductor interface thus leading to an increase (decrease) of the overall holes concentration, meaning that a shift of the threshold voltage towards more positive (negative) values can be clearly observed.

In other words, when both gates voltages are negative, two channels are present at the two semiconductor/dielectric interfaces, and the transistor behaves in a double accumulation mode. When two positive voltages are applied, the transistor behaves in a double depletion mode. When the two gate voltages have different polarity, the transistors behave in a mixed regime. As a matter of fact, as expected, it is therefore possible to finely tune the transistors threshold voltage by the employment of the second gate. It is worth noting that a modulation of carrier concentration, by means of the top gate, leads also to a modulation of charge carrier mobility; these two effects are clearly shown in Figure 2C. In particular, it can be noticed that by increasing the carriers' density in the channel, leads to twofold effect: first, the threshold voltage shifts towards more positive values, moreover, also the transistor carrier mobility slightly increases. This effect is not surprising as it has already been observed in the majority of organic semiconductor-based transistor, in which the mobility generally increases when increasing the over-threshold conditions, that is, increasing carriers' concentrations.[41]

Once all the samples have been measured, immediately after their fabrication, they have been stored in air, at a constant temperature of 23 °C and in the dark. Both sets of devices have been periodically characterized, in order to evaluate the evolution of their electrical performances over time. In fact, it is well reported in the literature that the interaction of moisture and oxygen with the organic active material, typically leads to significant degradation effects and therefore to an early degradation of the transistor performances.[42–48]

As expected, all the devices from set 1 of Bottom-Gate transistors, being not encapsulated, are characterized by a visible and continuous decay of the mobility, which generally tends to become more pronounced after the first 30 days, reaching more than 60% degradation after 200 days.

Interestingly enough, on the contrary, all the top-gated transistor are characterized by a much better stability over time, showing that the presence of the combination of an organic/inorganic layer over the organic semiconductor, allowed dramatically reducing oxygen and moisture interdiffusion into the device channel. In fact, as can be clearly noticed, even after 6 months, charge mobility is comparable to the one extrapolated right after their fabrication (**Figure 3**).

3.2. Tactile Sensor Characterization

After the optimization and characterization of the Double-Gate transistors (DGTs), a multimodal tactile sensor based on the same architecture has been developed. In this case, DGTs were coupled with a PVDF capacitor. In all these measurements, a constant bottom gate voltage is applied to the devices, whereas one plate of the PVDF capacitor is connected to the top gate and the second to the source. In this way, the voltage induced by the piezoelectric or pyroelectric effect, see Figure S1 (Supporting Information) reported in the Supporting Information, create a variation of the voltage between the top gate and the source, thus modulating the charge carriers concentration (i.e., the threshold voltage and the output current) in the sensor.

Specifically, the top gate of such devices was connected to one plate of the capacitor, while the other capacitor plate was connected to the source of the transistor as shown in **Figure 4A**. This solution allowed to mechanically decouple the sensing element, that is, the PVDF capacitor, to the device channel, thus making the characterization of the sensor's response more efficient. The working principle of the fabricated sensor is very simple. A variation of temperature and/or an applied external force to the PVDF capacitor, leads to a variation of the dipole moment in such film. This will be reflected in a charge displacement in the connected electrodes. Therefore, the charge induced on the top gate electrode, will be able to apply a vertical field on the transistor channel, thus leading to a variation of its output current.

3.2.1. Temperature Characterization

At first, the transistor was characterized as temperature sensor, using the same set-up reported in A. Mascia et al. work.[49] The PVDF capacitor was placed on the top of a Peltier cell, which was powered by a benchtop voltage power supply. In this way, only the PVDF capacitor was exposed to the temperature stimuli. The overall temperature was controlled by means of an infrared Temperature Sensor (PyroCouple Calex PC21MT-1, Calex Electronics

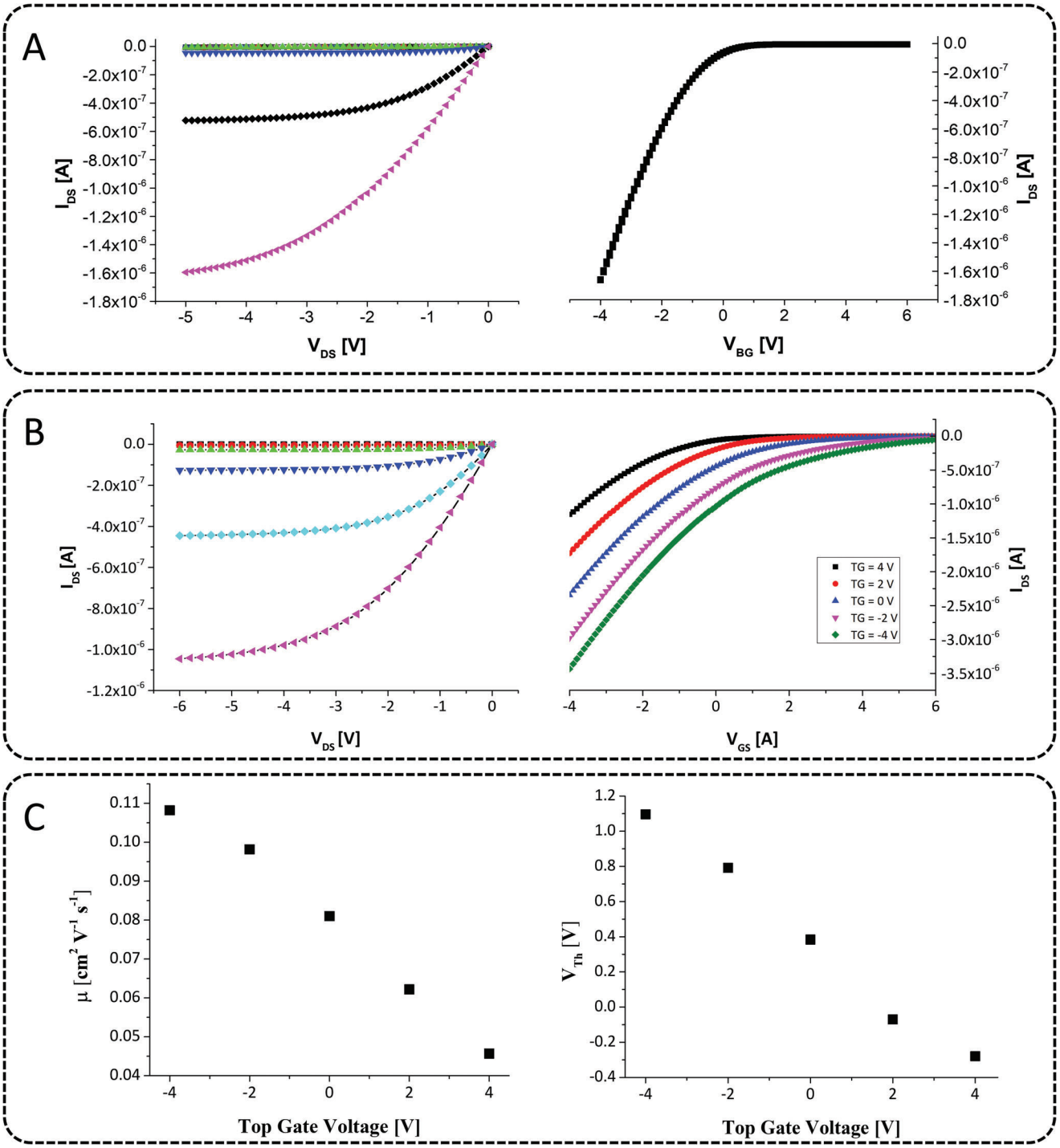

Figure 2. A) Output (left) and transfer (right) characteristics of a typical bottom gate-bottom contact organic TFT. B) Output (left) and transfer (right) characteristics of a proposed device biased through the bottom gate. In both cases, the top gate was grounded. C) Mobility (left) and threshold voltage (right) shift depending on the voltage applied on the top gate.

Limited). The output response of the single PVDF capacitor is reported in Figure S1 (Supporting Information), showing that such film is capable of inducing voltage variations in the range of ≈2 V that could be enough to properly modulate the transistor threshold voltage. In fact, as it is shown in Figure 4B, where the output current of the device is reported, by increasing the temperature an increase of the output current was induced. This effect is due to the pyroelectricity that creates a charge separation in the PVDF film that perturbates the charge on the top gate of the device, leading to a shift of the device threshold voltage towards more

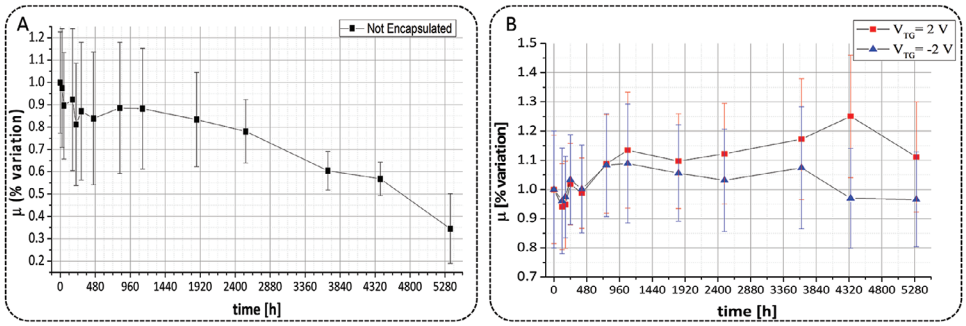

Figure 3. Mean mobility variation over time, shown in percentage from day 0 (right after fabrication) for the not encapsulated devices A) and the encapsulated devices (Double-Gate transistor) B).

positive values. Interestingly, by switching the capacitor plates connected to the top gate of the transistor a decrease of the current was observed when the temperature was increased, as reported in Figure 4C.

This phenomenon is consistent with the fact that in such case opposite charges were induced into the top gate, thus shifting the device threshold voltage towards more negative values and leading to a reduction of the carrier concentration in the channel. These flipping tests demonstrate that the current variations are actually induced by the pyroelectric effect of the PVDF capacitor and not by some random undesired effect. For this reason, the sensor was characterized with both configurations, in order to investigate which of the two leads to better response.

Since the transistor response to the stimuli given by the PVDF capacitor, depends on which side of it is connected to the top gate, whenever there will be an increase in the absolute value of the current, will be referred as ***switch-on mode***; on the contrary, ***switch-off mode***.

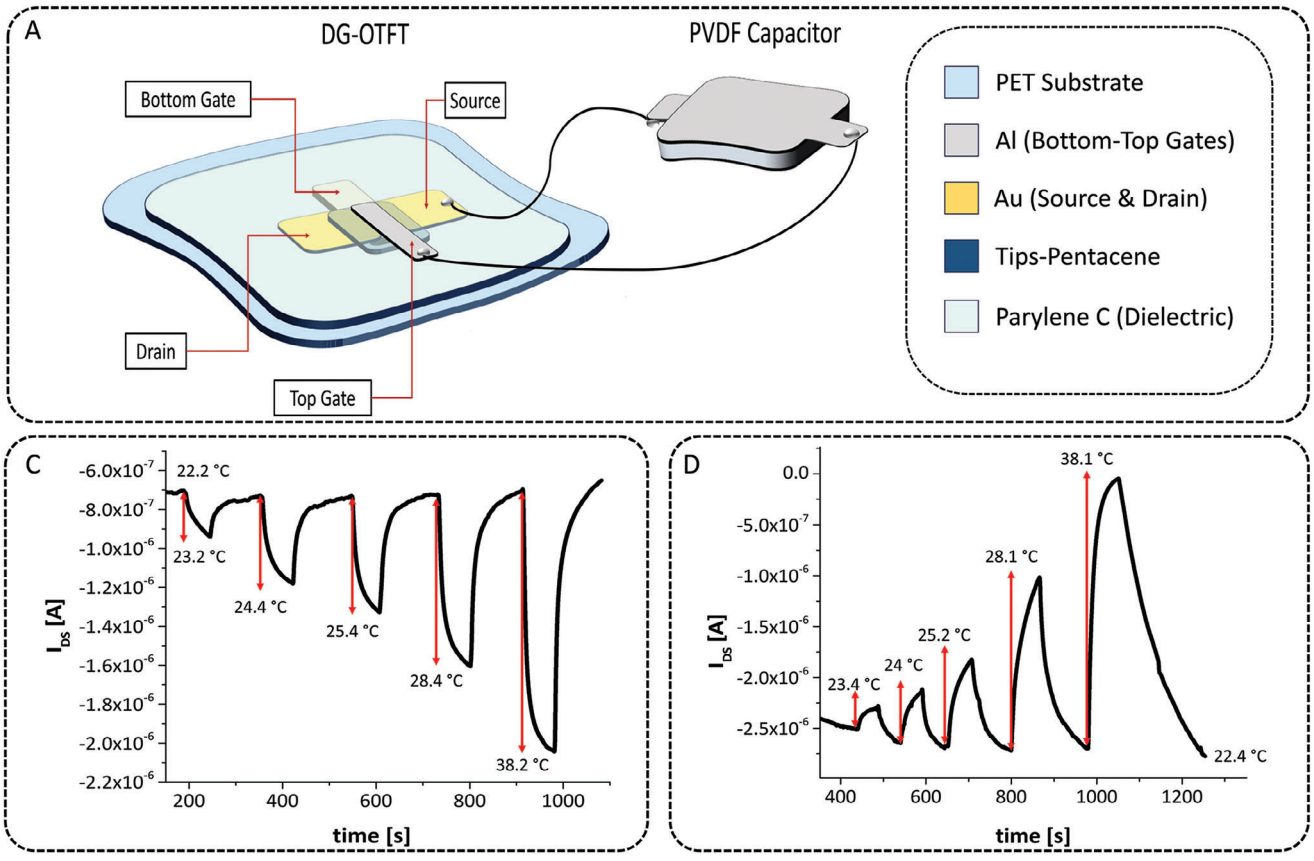

Figure 4. Measurement set-up and flipping test of the Double-Gate Organic Transistor as temperature sensor. A) Sketch of the proposed device, with the Bottom gate, Drain, Source and Top gate contacts highlighted, coupled with the PVDF capacitor (not in scale); B) The sensor output current increases (in absolute value) as the temperature increases; C) the opposite sensor response (decrease of the output current) as the temperature is increased, was obtained by flipping the connection of the PVDF capacitor between the top gate and the source of the transistor.

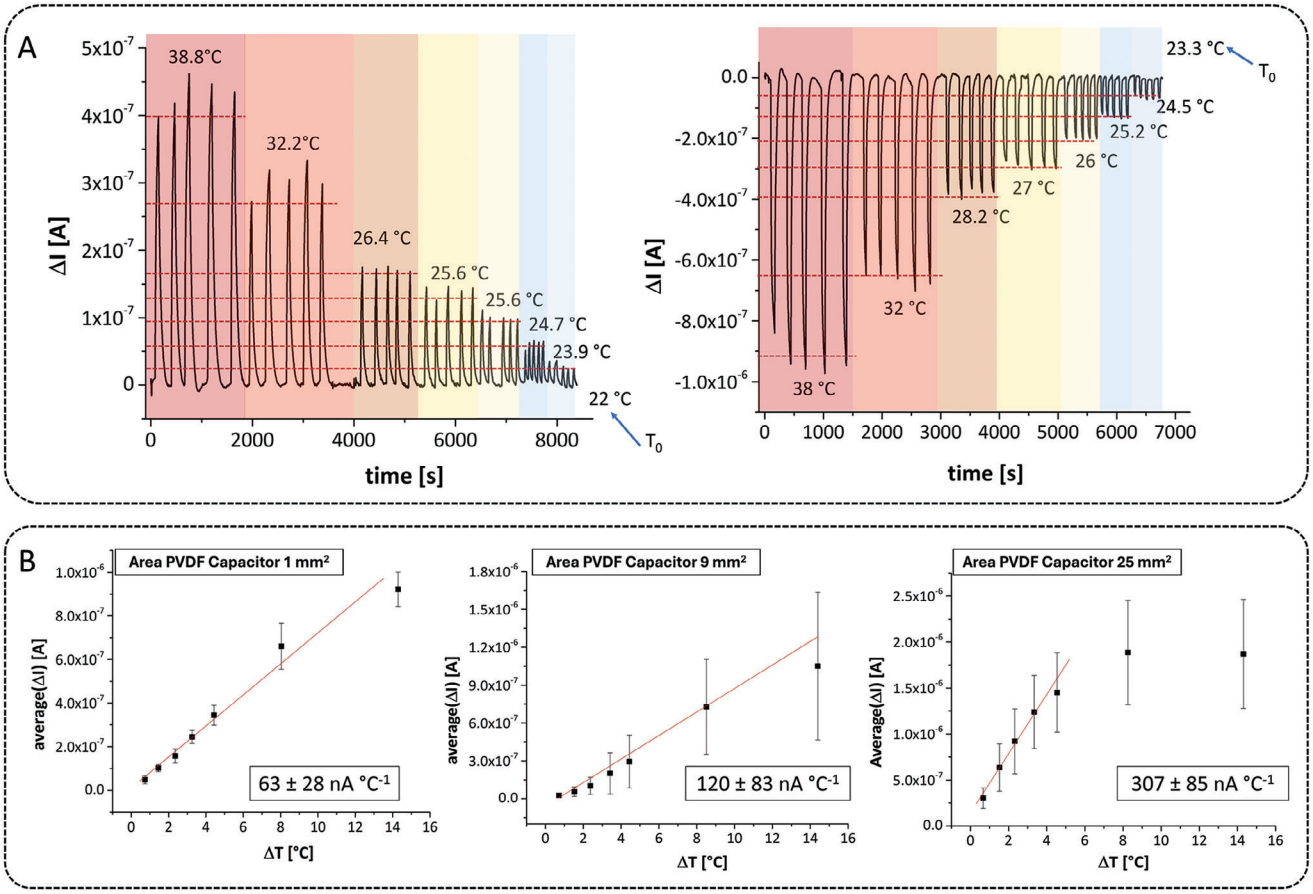

Figure 5. Temperature measurement for the Double-Gate organic transistor. A) Dynamic response of the device for different temperature stimuli, each one exerted 5 time, for both configurations. In this example the PVDF capacitor has an area equal to 9 mm^2; B) Average (over 5 devices) calibration curves and corresponding sensitivity (calculated as the slope of the linear part of the curve) for the three different PVDF capacitors employed in this work, namely 1, 9 and 25 mm^2 respectively.

In addition, we performed the hysteresis test to characterize the sensor response for both temperature and force increasing and decreasing the external stimuli. The results, reported in Figure S2 (Supporting Information) in the SI, clearly demonstrate that the measurement hysteresis is almost negligible.

To deeply investigate the Double-Gate transistor as temperature sensor, a set of 5 different device was measured exerting 5 repetitions for each temperature value. In addition, three different PVDF capacitors with an area of 25, 9, and 1 mm^2 were employed. From **Figure** 5A it is possible to notice the quick response of the device to the temperature variations, for both configurations employed. The devices reported an average sensitivity over 5 devices of ≈307 ± 85 nA °C^{-1} for the capacitor with an area of 25 mm^2 with a notable maximum value of 442 nA °C^{-1}. Moreover, it is possible to tune both the temperature range of response and the device sensitivity, depending on the capacitor dimension, which is particularly interesting depending on the application for which such device is developed. In fact, the reduction of the area led to an increase of the detection range (see Figure 5B) where the three average calibration curves are reported for the switching-off mode), while the sensitivity scales with the PVDF capacitor area, as reported in **Table** 2.

3.2.2. Force Characterization

A similar approach with the aim to physically decouple the Double-Gate transistor and the PVDF capacitor was employed for the characterization as force sensor. The PVDF capacitor was placed onto a load cell, and a commercial dynamometer (FCA-DS2-50N by IMADA, Northbrook, IL, USA) mounted on a vertical motorized stand (MX2 by IMADA, Northbrook, IL, USA) was employed to exercise the mechanical stimuli onto the capacitor. Also in this case, by changing the connected plate of the PVDF capacitor between the top gate and the source electrode gave rise to a flipping of the sensor response, as it is shown in **Figure** 6A,

Table 2. Average sensitivity values calculated on a set of 5 devices for the three different PVDF capacitors areas employed.

Capacitor Area[mm^2]	Average sensitivity switch-off [nA °C^{-1}]	Average sensitivity switch-on [nA °C^{-1}]
25	307 ± 85	200 ± 36
9	120 ± 83	68 ± 53
1	63 ± 28	22 ± 8

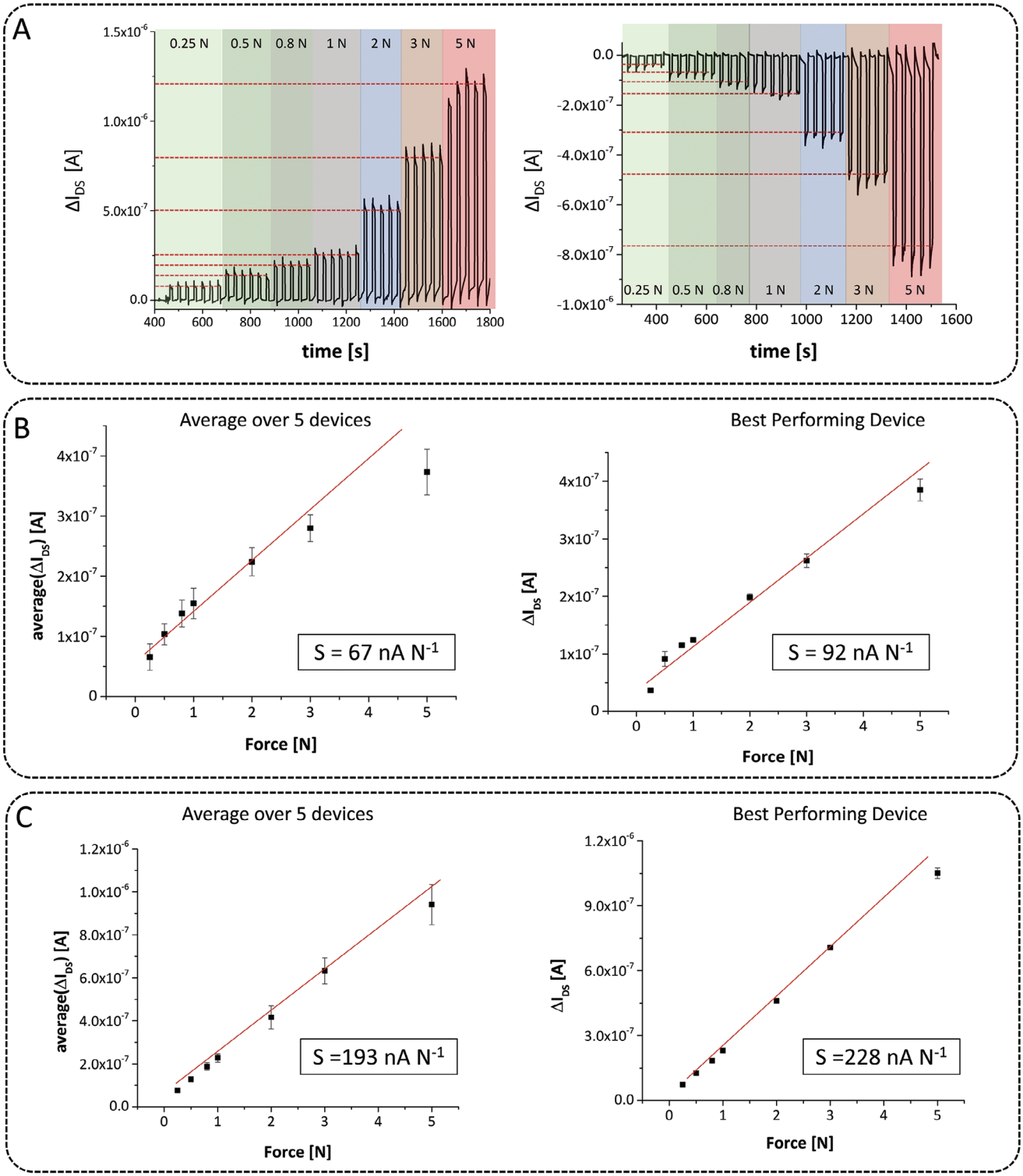

Figure 6. Force characterization for the proposed device. A) Dynamic response of the device, measured in both configurations, for different applied forces (0.25 – 5 N). In this example, a PVDF capacitor with an area of ≈25 mm^2 was employed; average (over 5 devices) calibration curve and best-performing device measured in the switch-off mode for the DG-organic transistor coupled with the 9 mm^2 PVDF Capacitor B), and with the 25 mm^2 PVDF Capacitor C). The sensitivity scales with the capacitor area and we obtained an average sensitivity of 67 and 193 nA N^{-1} for the 9 and 25 mm^2 PVDF capacitor respectively.

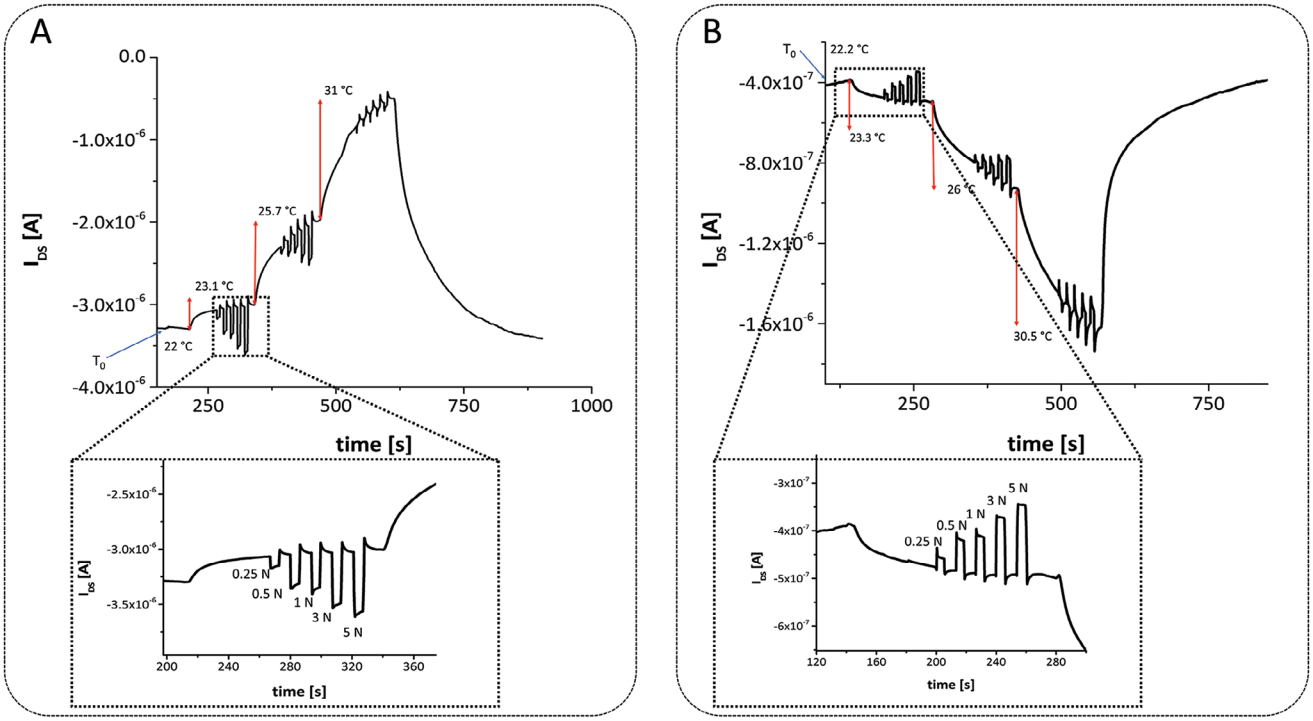

Figure 7. Multimodal characterization for the proposed device, where simultaneously temperature and force stimuli are applied, for the temperature-driven switch-off A) and switch-on B) current variations.

where the dynamic response of the device to different forces is reported. Therefore, both configurations were employed to characterize the device as force sensor. A set of 5 devices was characterized and, in this case, two different capacitor area were employed, namely 25 and 9 mm^2, since the commercial indenter used does not allow to exert a force on smaller areas in a reproducible manner. Each force value was exerted 5 times, and the sensor was able to detect forces from 0.25 up to 5 N, which is the typical range of response for tactile applications.[50] Interestingly, the sensor's response is highly reproducible, while at the same time being fully recoverable. Figure 6B shows the average calibration curve in the switch-off mode characterization for the capacitor with an area of 9 mm^2 while Figure 6C reports the same data for the capacitor of 25 mm^2.

In **Table 3** are reported the average sensitivities for the two capacitor areas employed, calculated from the average curve, (from a set of 5 devices) for both measurement configuration reported above. In addition, a maximum value of 241 and 92 nA N^{-1} was obtained for the 25 mm^2 and 9 mm^2 PVDF capacitor, respectively.

Table 3. Average sensitivity values calculated on a set of 5 devices for the two different PVDF capacitors areas employed.

Capacitor Area[mm^2]	Average sensitivity switch-off [nA N^{-1}]	Average sensitivity switch-on [nA N^{-1}]
25	193 ± 30	181 ± 50
9	67 ± 29	46 ± 17

3.2.3. Multimodal Characterization

Finally, both measurement setups were combined to achieve a multimodal characterization. The 9 mm^2 capacitor used for these measurements was put on top of the Peltier cell, beneath the dynamometer. Following the same protocol, both sides of the capacitor were connected, alternatively, to the top gate and source of the device. Afterward, the device was measured as a multimodal tactile sensor by exerting simultaneously force and temperature stimuli. The sensor was capable to clearly detecting different applied forces for all the different temperatures employed. Moreover, it is interesting to note that the opposite variation of the current induced by the two stimuli allows a straightforward discrimination of the two (**Figure 7**).

4. Conclusion

In conclusion, we have optimized the procedure for fabricating flexible Double-Gate organic TFTs based on TIPS-Pentacene. The fabricated devices can be operated at voltages below 5 V and are characterized by small threshold voltage, ranging ≈1 V and relatively high mobility, ≈0.2 $cm^2V^{-1}s^{-1}$. It has been demonstrated that the top gate allows a fine control of the transistor performances, and that this approach can be employed for finely tuning, after device fabrication, its final working conditions, thus eliminating the generally low reproducibility of solution processed organic transistors. Moreover, thanks to the self-encapsulation of the top dielectric/metal, it has been demonstrated that such devices can be stored for months in ambient conditions without observing any mobility degradation or

significant threshold voltage shift. Afterward, by exploiting the possibility to modulate the threshold voltage, we have developed a multimodal tactile sensor capable to detect force and temperature variations by connecting a pyro/piezoelectric capacitor between the top gate and the source contact of the transistor. This approach provides an easy, and low-cost solution for the fabrication of tactile sensor onto flexible substrates with remarkable characteristics and stable performances over time.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

Double-gate, flexible, multimodal, organic, tactile sensor

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