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The Evolution of Semiconductor Devices: From Transistors to Quantum and Neuromorphic Computing

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ABSTRACT

This review traces the development of semiconductor equipment, from bipolar junction transistors (BJTs) to advanced architectures such as fin field-effect transistors (FinFETs), nanowire transistors, and carbon nanotube FETs. We highlight major developments that have enabled improvements in performance, energy efficiency, and integration density. Special attention is paid to detailed bandgap materials (SiC, GaN), two-dimensional materials, and van der Waals (VdW) heterostructures, which are ready to shape the next generation of power and high-frequency electronics. Next-generation trends beyond CMOS, such as neuromorphic engineering and quantum computing, are identified, with a focus on operating methodology and recent hardware realizations. The application ground is linked to industry-specific needs in healthcare, energy, and AI hardware. Comparative data tables and combined figures are presented to further the performance benchmark. We consider existing challenges, fabrication intricacies, quantum decoherence, and the integration of materials and emphasize future paths, among them quantum–neuromorphic hybrid systems, green fabrication methods, and artificial intelligence-based design approaches. Furthermore, 2026 predictions, in-depth industrial applications, quantitative comparisons, and opportunities for further research efforts are critically reviewed.

1 | Introduction

Semiconductor technologies have witnessed transformative changes since the invention of the transistor in 1947 and enabled revolutionary advancements in computing, communications, healthcare, transportation, space systems, and other fields [1, 2]. The continuous shrinkage of transistor dimensions, governed by Moore's Law [3, 4], has led to advances in computing power, integration levels, and power efficiency. However, the conventional complementary metal oxide semiconductor (CMOS) scaling technologies face fundamental physical limits and the increasing fabrication costs, driving the development of advanced CMOS architectures and beyond-CMOS technologies to sustain future semiconductor scaling [5].

Modern advances in computing, communications, medicine, transportation, and artificial intelligence (AI) all depend on the availability and capability of semiconductor technology. The research field is pursuing two synergistic lines of investigation to allow future improvements in the performance of these electronic devices. These lines are based on, first, the exploitation of continued improvement in silicon (Si)-based technology

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through what is known as "advanced CMOS" technology: from fin field-effect transistors (FinFETs) to the latest development in gate-all-around (GAA) transistors (also called nanosheet field-effect transistors (FETs) and complementary FET (CFETs) in different contexts). Second, the exploitation of what is described as "beyond-CMOS" technologies: namely, tunnel field-effect transistors (TFETs), spintronics based devices, memristors, neuromorphic processors, and quantum hardware for computation. In the rest of the paper, this distinction is rigorously followed.

1.1 | The Birth of the Transistor

Semiconductor technology history is an example of constant human progress and desire for perfection. The history of semiconductor evolution is presented in Figure 1. It all began back in 1947 when the point-contact transistor was invented by John Bardeen and Walter Brattain from Bell Labs [6]. This discovery outstripped unpredictable vacuum tubes and gave way to the era of the solid state of things. The evolution of Si intensified in the late 1950s because its purification became better, thus making it the best semiconducting material for mass production [7]. Some other discoveries, such as bipolar junction transistor (BJT), were made in 1949 [8]. During the 1950s and 1960s, BJTs were dominating among semiconductor devices and helped create the first integrated circuits (ICs) [9]. The invention of the IC came about by Jack Kilby from Texas Instruments in the year 1958. This was a revolutionary development in the industry owing to the fact that the entire circuit was placed on one single chip [10]. The invention of the metal oxide semiconductor field-effect transistor (MOSFET) was pioneered in the year 1959 when Atalla and Kahng developed the MOSFET [11]. MOSFET had various advantages compared to BJT such as low power consumption and higher integration density [12]. The 1970s marked the emergence of MOSFET as the prevailing device type.

1.2 | The CMOS Technology Era

CMOS, first conceived in the early 1960s, was a ground breaking innovation by Frank Wanlass in 1963. In 1967, a demonstration of CMOS with complementary enhancement-type n- and p-channel MOSFETs showed the possibility of designing very high-input resistance circuits that had almost no power consumption when they were idle; this contrasted sharply with the transistor logic circuit families previously in use. CMOS has also shown advantages such as higher speed, lower heat dissipation per gate compared to PMOS and N-MOS, and potentially high integration density and higher yield of transistors [13, 14]. CMOS had become the default technology for digital ICs by the 1980s [15]. Semiconductor technology has evolved from classical BJTs and MOSFETs to advanced CMOS architectures, including FinFETs, GAA transistors, nanosheet FETs, and CFETs, followed by beyond-CMOS technologies such as TFETs, spintronic devices, memristors, neuromorphic hardware, and quantum computing. In contrast to conventional scaling-driven evolution, quantum computing, neuromorphic computing, spintronic devices, and memristive systems are computing paradigms that can be realized by advances in materials science, device physics, and system architectures. Future ICs are expected to integrate advanced CMOS technologies with beyond-CMOS accelerators through heterogeneous computing architectures [16].

1.3 | Scaling and Moore's Law

Most of the advancements in semiconductor technology over the past several decades have occurred as a result of constant scaling down of CMOS devices by following the pace set by Moore's Law. Coined in 1965 by Gordon Moore and later updated to about doubling every 2 years in 1975 [17], Moore's Law predicted the exponential increase in the number of

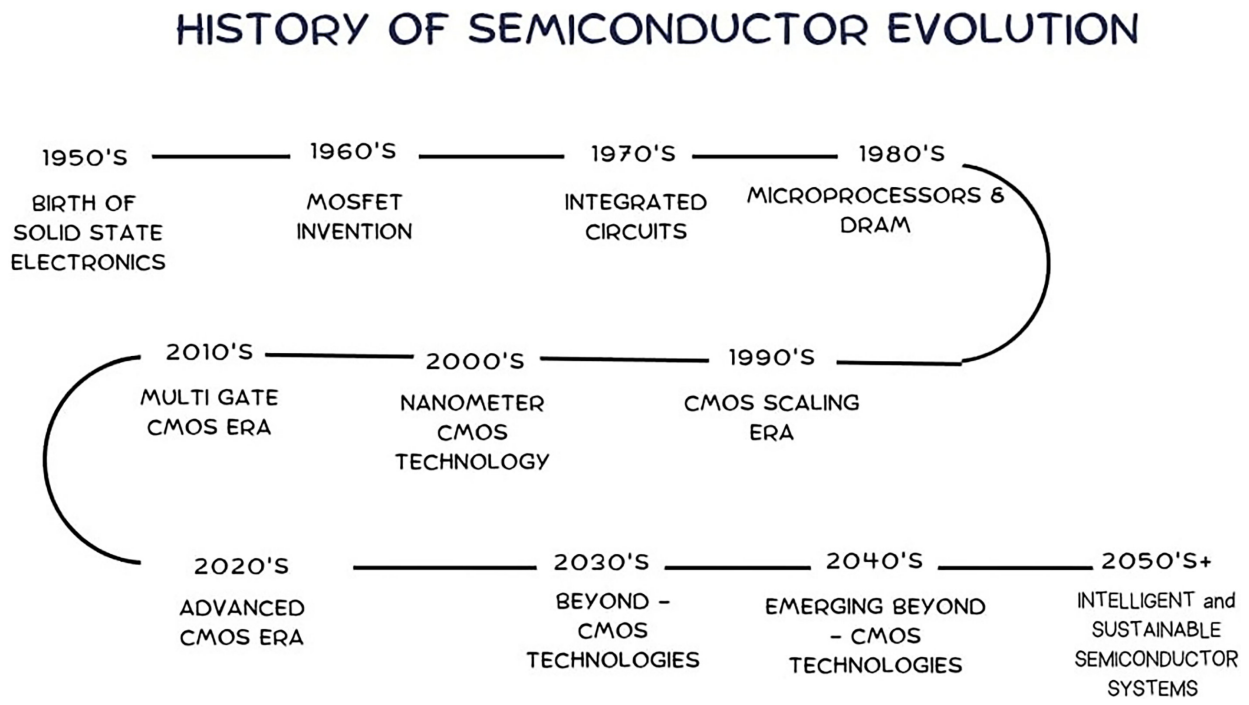

FIGURE 1 | Historical evolution of semiconductor devices across decades highlighting key milestones from the birth of solid-state electronics to future intelligent semiconductor systems.

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components on an IC over time. From the micrometer-scale technologies in the 1970s, shrinking of the transistor size into nanometer scale has led to spectacular improvement in semiconductor integration, performance, and energy efficiency. Microprocessor age or programmable computers began in 1971 with the advent of Intel 4004 microprocessor [18]. Due to extremely large-scale integration (VLSI) enabled by advances in manufacturing technology during the 1980s, millions of transistors were packed onto a single chip. With advancements in manufacturing and design, system-on-chip (SoC) technology evolved during the 1990s, integrating computation, input/output devices, and memory into a single component, leading to innovations in mobile and embedded systems [19, 20]. Figure 2 depicts the evolution of semiconductor devices from BJTs to prospective beyond-CMOS technologies.

2 | Advanced Semiconductor Materials

2.1 | Silicon-Germanium (SiGe) Alloys

In the 1980s, IBM developed the first generation of the SiGe heterojunction bipolar transistor (SiGe HBT). This transistor used SiGe as a base material, with a power consumption of 0.1 W, a speed of 50 GHz, and a size of 250 nm. The transistor integration density reached ≈100 000 transistors per mm^2. SiGe alloys, emerging in the 1990s, offered higher carrier mobility than Si and enabled RF/analog high-speed transistors. SiGe technology has found its way into wireless communication devices [21].

2.2 | III–V Compound Semiconductors

III–V compound semiconductors such as gallium arsenide (GaAs) and indium phosphide (InP) have been used for high-frequency and optoelectronic applications since the 1980s. Semiconductors such as the III–V compounds exhibit high electron mobility and direct bandgaps, making them excellent candidates for high-speed transistors and light-emitting diodes (LEDs); III–V compounds are thus a special type of semiconductor. Recently, III–V semiconductors have been integrated with Si to create hybrid devices for next-generation electronics [22].

2.3 | Wide-Bandgap Semiconductors

Silicon carbide (SiC) and gallium nitride (GaN) are examples of wide-bandgap semiconductors that have enabled a new generation of power electronics. These materials can sustain higher breakdown voltages and higher thermal conductivity than Si, enabling the creation of high-power, high-temperature devices. SiC and GaN devices are primarily used in electric cars, renewable energy systems, and 5G facilities [23].

2.3.1 | SiC

SiC has attracted considerable attention for its superior material properties, which distinguish it from conventional semiconductors such as Si. Its high breakdown field, high thermal conductivity, and wide bandgap make SiC a suitable material for power electronic applications, especially in high-power, high-temperature environments [24].

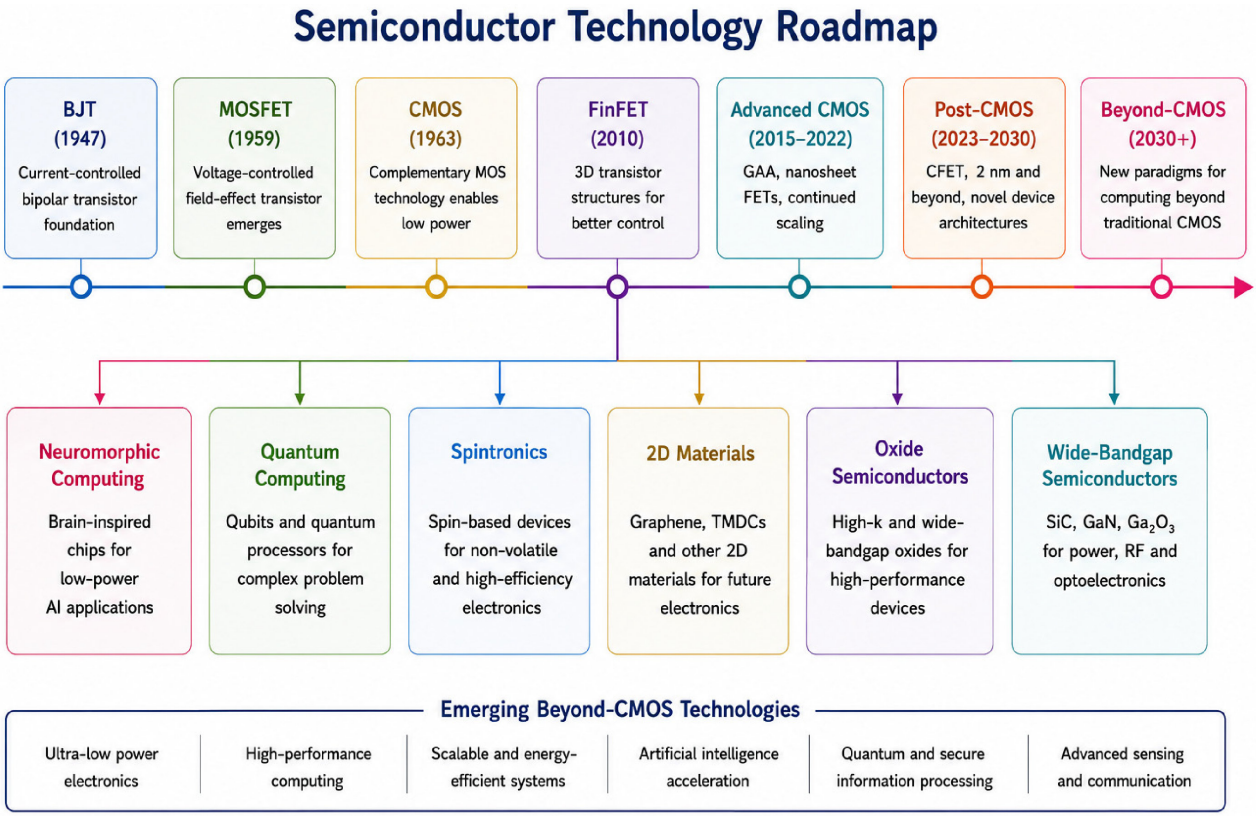

FIGURE 2 | Semiconductor technology roadmap from bipolar transistors to advanced CMOS and beyond-CMOS technologies.

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2.3.1.1 | *Material Properties and Structure.* SiC semiconductor properties were first reported in early 20th-century research. SiC is more radiation-resistant than Si. Therefore, it is a top candidate for high-energy and space-based applications. SiC contains three polymorphs: 6H-SiC, 4H-SiC, and 3C-SiC. The 4H-SiC structure is the predominantly used material for next-generation power device applications owing to its improved electron mobility and field stability [25].

2.3.1.2 | *Applications in Power Electronics.* SiC is transforming industries by enhancing efficiency, reducing losses, and enabling compact designs. In electric vehicles (EVs), SiC MOSFETs and diodes improve traction inverters, DC–DC converters, and onboard chargers. Their high efficiency extends the driving range, speeds up charging, and reduces the size and weight of power electronics [26]. Renewable power systems, such as wind turbines and solar inverters, benefit from reduced switching losses and greater efficiency enabled by SiC, improving energy harvesting and minimizing operational costs. Its resistance to harsh operating conditions guarantees optimal performance. SiC is also used in industrial motor drives to achieve greater power density and efficiency, enabling lower weight, smaller motors, and improved performance in applications such as pumps, compressors, and robotics. Additionally, SiC is revolutionizing power supplies and data centers by replacing Si, leading to higher efficiency, lower cooling requirements, and lower energy consumption [27].

2.3.1.3 | *Challenges and Advances.* SiC provides high efficiency but remains challenging. It is hindered by high material and fabrication costs, difficult fabrication, material synthesis defects, and reliability issues. Wafer quality improvements, defect reduction, and low-cost fabrication techniques are being used to solve these problems [28].

2.3.2 | *GaN*

Due to its wide bandgap and ability to operate at higher temperatures, GaN is widely used in high frequency and high-power devices worldwide. GaN is a high-speed, high-frequency material due to its higher electron mobility and the highest saturation velocity [29].

2.3.2.1 | *Material Properties and Performance.* The electron mobility of GaN is significantly improved compared to other semiconducting materials (i.e., SiC). For high-frequency, high-power-density operation, the material has an electron mobility of $\sim 2000\,cm^2/Vs$. Because of this characteristic, it is extremely suitable for RF devices and microwave power amplifiers, and GaN is widely used because it facilitates efficient heat dissipation and offers a high breakdown voltage [30, 31].

2.3.2.2 | *GaN in Power Electronics.* GaN transistors are widely used in power switching circuits due to their ability to support high-frequency switching. Due to their superior efficiency, GaN-based devices produce less heat than Si-based devices. GaN power devices have widespread applications in wireless communication systems, radar equipment, and power supplies, where they play a key role in state-of-the-art electronics [32, 33].

2.3.2.3 | *Challenges and Current Research.* Despite its promising attributes, GaN faces challenges related to cost-effective manufacturing, material defects, wafer bonding, crystal quality, and device reliability. Advances in the growth of high-quality GaN crystals on large-area substrates such as Si could significantly reduce manufacturing costs and improve the yield of GaN devices [34].

2.3.3 | *Comparative Studies of SiC and GaN*

Increasingly, research has compared the performance of SiC and GaN across various electronic applications. The studies highlight the strengths and weaknesses of the two materials across parameters such as efficiency, thermal conductivity, breakdown voltage, and operating frequency.

SiC and GaN are the materials that possess a wide bandgap (SiC, 3.2 eV; GaN, 3.4 eV), enabling them to support higher breakdown voltages, a critical factor for high-power applications. Nevertheless, SiC has a much higher breakdown voltage (up to 10 kV) than GaN (1.2 kV) and thus is the preferred choice for applications requiring higher voltages, e.g., power grids and EVs. Thermal management is also one of the most important differentiators between the two materials. SiC has a higher thermal conductivity ($5\,W\,cm^{-1}\,K^{-1}$) than GaN ($1.3\,W\,cm^{-1}\,K^{-1}$), making it more suitable for heat dissipation. This renders SiC the material of choice for high-power applications with high heat and power losses, including industrial motor drives and power inverters for renewable energy systems. Switching speed and efficiency are also essential in their applications. GaN has a much higher electron mobility ($2000\,cm^2/[V\,s]$) compared to SiC ($900\,cm^2/[V\,s]$), resulting in faster switching speeds. This makes GaN a better candidate for high-frequency operating conditions, such as RF communication systems, radar, and small power supplies. GaN also benefits from a higher electron saturation velocity (2.5×10^7 cm/s compared to 2.2×10^7 cm/s for SiC), further enabling its high-frequency applications. Cost is also an important factor when deciding between GaN and SiC. Although GaN offers superior frequency response and efficiency, device fabrication in GaN is costly owing to the difficulty of growing GaN crystals and the need for GaN substrates. SiC, although initially expensive, is eventually more cost-efficient due to its strength and ability to withstand harsh conditions and, therefore, is suitable for high-power applications. In spite of the differences, both materials possess some advantages. SiC is best suited for high-power, high-temperature conditions, whereas GaN is suited for high-speed, high-frequency applications. Their distinct properties dictate their application in power electronics, enabling optimized performance tailored to specific operating requirements. Table 1 gives an overview of the major technical parameters of SiC and GaN [35–37].

2.4 | Oxide Semiconductor Materials

The optical transparency, tunable conductivity, large area processability, and compatibility with flexible substrates have made oxide semiconductors a promising class of electronic materials. Compared to traditional Si-based semiconductors, oxide semiconductors are synthesized at comparatively low temperatures while retaining good electronic properties. The unique combination of electronic, optical, and mechanical properties makes them widely used in displays, UV photodetectors, power electronic devices, and neuromorphic computers. The most studied oxide semiconductor materials are amorphous indium gallium

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TABLE 1 | Overview of the major technical parameters of SiC and GaN.

Parameter	SiC	GaN
Bandgap	3.2 eV	3.4 eV
Critical electric field	3.0×10^6 V/cm	3.5×10^6 V/cm
Electron mobility	900 cm^2/[V s]	2000 cm^2/[V s]
Electron saturation velocity	2.5×10^7 cm/s	1.5×10^7 cm/s
Thermal conductivity	4.9 W/[cm K]	1.7 W/[cm K]
Breakdown voltage	Up to 10 kV	Up to 1.2 kV
Operating temperature	Up to 600 °C	Up to 200 °C

zinc oxide (a-IGZO), zinc oxide (ZnO), and ultra-wide-bandgap gallium oxide (β-Ga_2O_3) [38].

2.4.1 | a-IGZO

Today, a-IGZO is becoming a mainstream semiconductor material in advanced high resolution thin-film transistors (TFTs) for displays. The electron mobility of IGZO is at least 10–20 cm^2/V s, which means that displays with IGZO transistors can refresh at higher frequencies and with shorter delay times than those with amorphous Si. IGZO is an amorphous material and therefore can be deposited evenly over a wide substrate area, making it suitable for OLEDs, foldable devices, or wearable displays. The current study also shows that IGZO-based transistors possess high reliability, low power consumption, and good flexibility [39].

2.4.2 | ZnO

ZnO is a direct wide-bandgap semiconductor. It has a bandgap of 3.37 eV and a large exciton binding energy of 60 meV. All these factors lead to high interest in the use of ZnO as ultraviolet photodetectors, transparent electronics, gas sensors, and piezoelectric devices. The formation of ZnO nanostructures, such as nanowires, nanorods, and thin films, provides a larger surface area and improved carrier transport. ZnO-based heterostructures have also shown promising results for low-cost optoelectronic devices and flexible sensing platforms [40].

2.4.3 | β-Ga_2O_3 Ultra-Wide-Bandgap Semiconductors

Among the developing oxide semiconductors, β-Ga_2O_3 has attracted considerable interest due to its ultra-wide bandgap (~4.7–4.9 eV) and very high breakdown electric field, which suggests operation in high-voltage power devices far beyond that of SiC and GaN devices [41]. Schottky diodes, MOSFETs, and FETs fabricated in β-Ga_2O_3 exhibit encouraging characteristics and performance in high-voltage power conversion applications. While challenges in crystal growth and thermal conductivity remain to be explored, β-Ga_2O_3 is considered a candidate for future power electronics [42].

2.4.4 | Application of Oxide Semiconductors

Among oxide semiconductors, a-IGZO, ZnO, and β-Ga_2O_3 have attracted considerable attention for display electronics, sensing, and ultra-wide-bandgap power devices [43]. Furthermore, transition metal oxides including HfO_x, TiO_x, and TaO_x exhibit stable resistive switching behavior and are widely investigated as active layers for memristive devices and artificial synapses in neuromorphic computing [44].

3 | Emerging Semiconductor Devices

3.1 | Overview of Advanced Transistor Architectures

Over the last five decades, continuous transistor scaling has driven exponential improvements in computing performance. As Si CMOS approaches fundamental scaling limits, shrinking planar MOSFETs has led to short-channel effects, leakage, threshold voltage variation, and power density constraints, motivating advanced device architectures such as FinFETs, GAA nanosheet FETs, and CFETs. These challenges motivated the development of advanced transistor architectures that improve device performance, energy efficiency, and manufacturability while extending CMOS scaling [45]. The evolution of semiconductor devices now follows two complementary directions. The first extends conventional Si technology through advanced CMOS architectures, whereas the second explores beyond-CMOS technologies based on fundamentally different device physics and computing paradigms. The advanced CMOS technologies, represented by FinFETs, GAA transistors, nanosheet FETs, and CFETs, aim to improve performance at small scales through stronger electrostatic control on conventional CMOS structures based on charge switching [46], and beyond-CMOS technologies, including TFETs, spintronic devices, memristive systems, and neuromorphic architectures, explore nontraditional switching or state variables to reduce the energy and scaling limits of classical CMOS [47]. The following sections review the recent advances in advanced CMOS transistor architectures and subsequently introduce beyond-CMOS devices which will form core building blocks for the low-power and intelligent computing and for future quantum computer systems.

3.2 | FinFET Technology

FinFETs represent an evolutionary advanced CMOS technology rather than a beyond-CMOS device. Their three-dimensional (3D) fin-shaped channel improves electrostatic gate control, suppresses short-channel effects, reduces leakage current, and enables continued CMOS scaling below the 22-nm technology node. Commercialized by Intel at the 22-nm node in 2011, FinFETs have become the dominant transistor architecture for advanced ICs. Although they remain widely deployed in current semiconductor manufacturing, technology roadmaps indicate a gradual transition toward GAA nanosheet transistors for sub-3-nm process technologies [48–50].

3.2.1 | Working Principle and Structure

The FinFET is a 3D device in which the gate wraps around the vertical fin, improving control over the channel. This structure reduces short-channel effects, enabling use at smaller nodes. Industry adoption continues at sub-5-nm nodes due to scalability and a mature process [51]

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3.2.2 | *Electric Performance and Benefits*

FinFETs provide enhanced performance compared to conventional planar CMOS devices by offering higher drive current, lower leakage, and faster switching speeds. FinFETs provide significantly higher drive current, lower leakage current, improved electrostatic control, and reduced power consumption than conventional planar CMOS transistors, particularly at technology nodes below 22 nm [52, 53].

3.2.3 | *Fabrication Issues*

Even though FinFETs yield significant performance improvements over planar transistors, they also present multiple fabrication and integration challenges. Precise control over the dimensions of the fins—fin height, width, and pitch—has to be exercised in order to obtain a uniform electrical performance and reduce device variation. On top of this, the 3D geometry of the device complicates its processing; it contributes to the additional capacitance and resistance parasitic effects that would affect high-frequency performance. Gate-first and gate-last (replacement metal gate, RMG) technologies were engineered to mitigate these effects, enhancing performance and reliability while keeping CMOS process integration possible [54].

3.2.4 | *Recent Developments*

It has been proven by recently published articles that the integration of high-k gate dielectrics and channel materials like InGaAs has an ability to promote the FinFET performance by means of better electrostatic control, overcoming short channel effects, lowering leakage current, and boosting carrier mobility. All of these materials and device design techniques lead to a more suitable switching behavior and better power consumption in high-end FinFET applications [55].

3.3 | GAA and Nanosheet FETs

The GAA device surrounds the entire conducting channel with the gate for improved electrostatic control and reduced leakage, enabling better drive current, switching performance, and energy efficiency. Commercial implementations by Samsung, Intel, and TSMC confirm GAA technology as the natural successor to FinFETs and a key enabling architecture for continued transistor scaling within the advanced CMOS roadmap [56].

3.3.1 | *Working Principle*

The conducting channel is formed using with either vertical nanowires or horizontal stacked nanosheets, and the gate entirely covers the channel, greatly increasing the gate capacitance while drastically reducing electrostatic losses. Subthreshold swing (SS) and power consumption are decreased.

3.3.2 | *Nanosheet FETs*

The most mature commercial version of the GAA transistor architecture is the nanosheet FET. The principle of the nanosheet FET consists of stacking several horizontally arranged Si nanosheets in a vertical structure in order to increase channel width, drive current, and improve the electrostatic control. Its overall channel width is larger than that of nanowire transistors, leading to a higher current, and the process is more manufacturable [57].

3.3.3 | *Industrial Adoption*

Samsung became the first semiconductor manufacturer to commercialize 3-nm GAA technology based on multi-bridge channel FET (MBCFET) architecture. Intel has adopted RibbonFET technology for its 20 and 18 A process nodes, while TSMC has announced nanosheet GAA transistors for its 2 nm (N2) technology, confirming GAA as the successor to FinFETs in advanced CMOS manufacturing [58].

3.3.4 | *Future Directions and Challenges*

Despite their advantages, GAA transistor fabrication remains highly complex, requiring precise selective epitaxial growth, nanosheet release, advanced etching techniques, and high-resolution lithography. Future transistor technologies are expected to evolve toward CFET architectures, backside power delivery networks (BSPDNs), and monolithic 3D integration, enabling continued transistor scaling beyond the 2-nm technology node while improving energy efficiency, integration density, and computational performance [59].

3.4 | Nanowire Transistors

Nanowire transistors provide superior electrostatic integrity through GAA control and represent a highly scalable platform for future CMOS-compatible technologies. Their one-dimensional (1D) channel geometry enables excellent suppression of short-channel effects, making them attractive candidates for continued transistor scaling beyond conventional FinFET architectures. However, challenges exist in terms of fabricating uniformity, contact resistance, variance, and industrial scale-up processes. The following subsections cover these topics with basic principles of how they work as well as the merit of their performance with problems and challenges during fabrication.

3.4.1 | *Working Structure and Principle*

Nanowire transistors consist of a single semiconductor wire as the channel, with the gate encircling the wire on all sides. The 1D geometry enables better electrostatic control, which significantly reducing short-channel effects, and thus, nanowires are suitable for sub-5-nm nodes [60]. Nanowire transistors may be realized with Si, III–V compounds (such as InAs), or 2D materials (such as graphene).

3.4.2 | *Electrical Performance and Benefits*

Compared to the conventional FinFET, nanowire transistors possess various advantages owing to the GAA topology which have a strong electrostatic controlling of the channel, thus leading to a higher driving current, a steeper subthreshold slope, a reduced leakage current, and an improved switching performance. Numerous researches show that the GAA nanowire FET demonstrates a lower power consumption and a better switching

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characteristic in comparison with the FinFET. GAA nanowire FET has been shown to be a feasible choice for the future technologies below 5 nm [61].

3.4.3 | Fabrication Challenges

The fabrication of nanowire transistors is very challenging. These challenges involve controlling the nanowire diameter and alignment, which becomes increasingly important as device size is reduced. The growth of nanowires typically employs methods such as chemical vapor deposition (CVD), which requires strict control of deposition conditions. Emerging methods, such as selective area growth (SAG), have demonstrated promise in controlling nanowire diameter and alignment, as well as in addressing some fabrication challenges [62, 63]. Furthermore, graphene nanowires with high carrier mobility and enhanced switching performance reduce power consumption.

3.5 | TFETs

TFETs are considered beyond-CMOS because carrier conduction is mediated by the band-to-band tunneling effect, not through the thermionic emission phenomenon that dominates in traditional MOSFETs. The potential to obtain below-the-theoretical-limit 60 mV/decade SS makes TFETs highly attractive for the realization of ultra-low-power electronic circuits capable of operating at significantly lower power supply levels than current technology. TFETs could therefore play an important role in those application areas where power consumption is critically limited, e.g., portable electronics, the Internet of Things (IoT), and edge-computing AI processors.

Researchers have successfully achieved substantially enhanced tunnel efficiency and ON current in the past few years by extensively using III–V semiconductors, two-dimensional (2D) materials, and graphene-based heterostructures. Nevertheless, relatively poor ON current levels and difficulties in manufacturing and process integration still remain key obstacles for mass production of TFETs. Active research in areas such as heterojunction engineering, strain engineering, and novel channel materials is thus very actively pursued [64, 65].

3.6 | Spintronic Semiconductor Devices

Spintronic devices and memristive devices are two main categories of the beyond-CMOS technologies that use new principles for information processing unlike charge-based electronic devices in the mainstream CMOS technologies. Spintronic devices exploit the spin of the electron for information processing, while memristive devices hold the information based on different resistance states programmatically. Both technologies have been considered promising candidates for hardware implementation of neuromorphic computing and in-memory computing as well as future energy-efficient AI systems. The principles, advantages, and upcoming applications of both technologies are briefly reviewed in the subsections that follow.

The information processing and data storage functionalities can be realized with spintronic devices by exploiting the fundamental electron's intrinsic spin property along with the electron's charge. Besides the potential of overcoming limitations of charge-based electronics like volatility, these spintronic devices possess low-power, high-speed switching and improved endurance. Successful commercial applications based on magnetic tunnel junctions (MTJs), spin valves, and spin-transfer torque magnetic random-access memory (STT-MRAM) have already been reported, while more applications such as low-power computing, AI accelerators, or integration in next-generation memory systems with CMOS are enabled by recent research on spin–orbit torques, topological materials, and magnetic skyrmions [66].

3.7 | Memristive Devices

The memristor is a type of beyond-CMOS electronic device where information is stored within variable resistance states controlled by voltage programming. The intrinsic resemblance between a memristor and a biological synapse is beneficial for designing nonvolatile memory, neuromorphic, and in-memory computing systems. The resistive switching mechanism involves ionic migration, filament formation, or charge trapping at material interface for device conduction. Stable resistive switching has been reported in materials such as HfO_x, TiO_x, TaO_x, and IGZO, which are widely used for memory and neuromorphic devices.

Computational functions performed within memory enable reduced data movement between CPU and memory, thereby enhancing computation efficiency and decreasing power consumption [67].

3.8 | Industrial Perspective

Recent commercial adoption demonstrates a progressive transition from FinFET to GAA nanosheet technologies, while beyond-CMOS research is increasingly focused on neuromorphic accelerators, quantum processors, and heterogeneous integration for next-generation computing systems [68].

3.9 | Carbon Nanotube Field-Effect Transistors (CNT-FETs)

CNT-FETs are one of the earliest devices proposed as alternatives for continuing the scaled device limit with beyond-Si CMOS as back in the 1990s. Since then, remarkable advances in CNT synthesis, device fabrication, contact engineering, and scale integration have been made from late 1990s to the 2020s. Due to high carrier mobility and carrier transport via near-ballistic process and good electro-static control, CNTFETs showed great prospect in developing future high-speed, ultra-low-power, nanoscale electronics [69, 70]. Recent research on 1D semiconductor nanowires indicates a potential target for replacing the easy route using Si, but the greatest issues remain due to the material used.

CNT transistors are among the best alternatives beyond-CMOS technology can offer. Their carrier mobility and the material's conductivity are very high, resulting in a high thermal conductivity [69, 70]. This shows that not only are these devices powerful, but they also do not require much energy to operate.

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In 2024, the manufacturing of ICs of CNT-FET developed successfully by improvement of high-purity semiconducting CNT production technology, large-scale and low-cost fabrication process, and integration of large-scale circuits [71]. There are a few recent studies that have already operated CNT complex cell phones, both CPUs and ROM chips. Even though CNT devices are not yet mature, their processing is still a potential alternative to Si-based electronic devices. Table 2 shows the performance metrics of CNT transistors [72–78].

3.10 | Comparison of FinFETs, Nanowire Transistors, and CNT-FET

Figure 3 illustrates a comparative architectural overview of FinFET, nanowire TFET, and CNT-MOSFET devices.

Figures 3 and 4 provide a comparative perspective on the state-of-the-art FET designs: Fin-FETs, nanowire TFETs, and CNT-MOSFET devices. Figure 3 shows a 3D architectural view that first presents the various geometrical and material features—flexible stacked fins in FinFET, vertical nanowire structures in nanowire TFET, and CNT channels in CNT-MOSFET. Figure 4 adds a vertical schematic cross-section showing all branching, along with source, drain, and gate placements, as well as the actual paths for charge transport in each device. Table 3 shows the comparison of FinFETs, nanowire transistors, and CNT-FETs.

FinFETs, nanowire transistors, and CNT-FETs are sequential transistor technologies. They address the issues raised by their predecessors and pose new challenges. FinFET employs a 3D multi-gate architecture in which the fin-shaped channel is surrounded by a gate that provides far better electrostatic control than in traditional planar CMOS devices [79]. Nanowire transistors do one better than FinFETs, with a more complex design in which the gate entirely engulfs the channel, while maintaining the 1D cylindrical structure in a GAA geometry [80, 81]. Nanowire architecture enables even greater electrostatic control, reduced leakage, and enhanced performance. Scalability is another major differentiator among these

TABLE 2 | The performance metrics of carbon nanotube (CNT) transistors.

Performance metric	Description	Typical value for CNT transistors	Reference
On/off current ratio	The ratio of current when the transistor is "on" to the current when it is "off." High ratios are desirable for better device switching	10^6–10^8	[72, 73]
SS	Measures how sharply the current increases with gate voltage. A lower value indicates lower energy loss in switching	~60 mV/decade (close to theoretical limit)	[72, 73]
Carrier mobility (μ)	Measures the speed of charge carriers within the transistor. High mobility indicates fast switching times	10^4–10^5 $cm^2/V s$	[72, 74]
Scalability	The ability to scale the device size down while maintaining performance	Sub-10 nm, potential for atomic scale	[72, 73, 75]
Contact resistance	The resistance at the interface between the CNT and the metal electrode. Lower resistance is critical for performance	10^{-6}–10^{-3} Ω cm (low resistance achieved in some studies)	[72, 73]
Gate control	The ability of the gate to modulate the current flow in the transistor	Excellent electrostatic control	[72, 75]
Threshold voltage (Vth)	The minimum gate voltage required to turn on the transistor. It influences power consumption	~0.2–0.3 V	[76–78]
Power consumption	The amount of energy consumed during device operation, important for energy-efficient designs	Lower than silicon-based counterparts	[75]
Reliability	The ability of the CNT transistor to maintain performance over time under operating conditions	High stability, especially under mechanical stress	[72, 73]

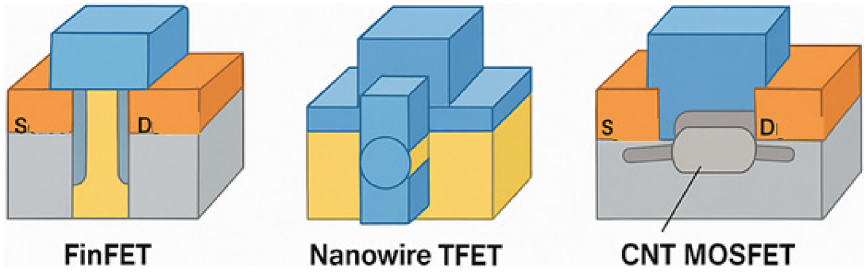

FIGURE 3 | Comparative architectural analysis of FinFET, nanowire TFET, and CNT-MOSFET, illustrating the transition from 3D fin structures to gate-all-around and carbon-based channel geometries.

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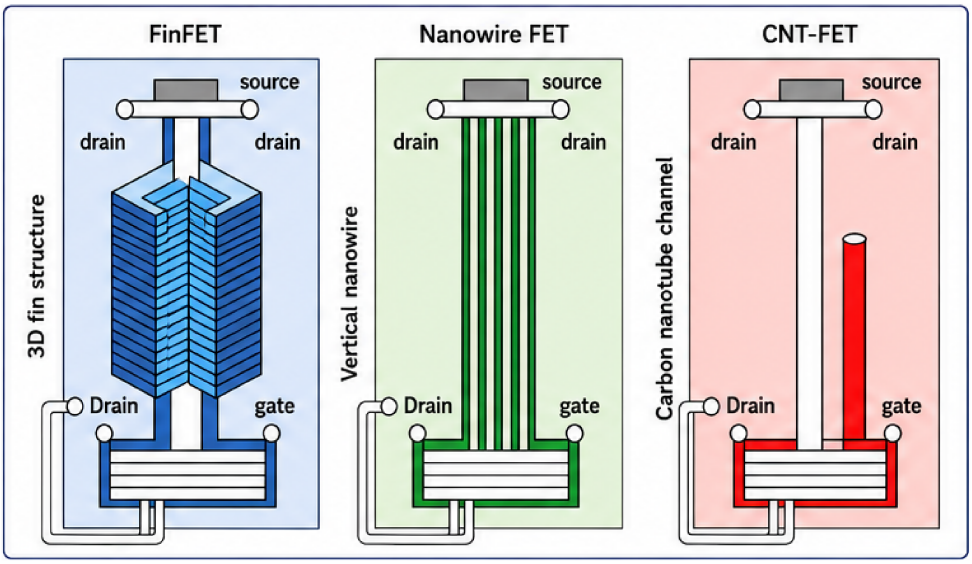

FIGURE 4 | Cross-sectional schematic comparison of FinFET, nanowire FET, and CNT-FET, highlighting the differences in gate control, channel dimensionality, and charge transport paths.

technologies. FinFETs perform well down to 5 nm, but below 3-nm nodes, limitations arise due to short-channel effects [82]. Nanowire transistors, by virtue of improved electrostatics and gate control, scale better at extreme nodes and are stronger contenders for future semiconductor technologies. FinFETs and nanowire transistors already perform better in terms of drive current than planar CMOS technologies; however, beyond the 5-nm technology node, nanowire transistors exhibit higher drive current due to higher carrier mobility [83]. Moreover, compared to FinFETs, nanowire transistors exhibit an ultra-low SS, enabling faster switching, reduced power consumption, and improved electrostatic control. Due to their GAA nature, leakage is reduced, thereby improving efficiency. Yet, this comes at the cost of a more complex fabrication technique [84]. While FinFETs, despite their complex structures, can be manufactured through state-of-the-art CMOS fabrication processes, nanowire transistors require regulated growth and nanowire alignment, thereby increasing the difficulty of large-scale manufacturing. The integration of modern semiconductor processing is simpler for FinFETs, whereas nanowire transistors require new fabrication approaches due to the alignment requirements of CMOS technology. CNT-FETs, the next giant leap for semiconductors, will push transistor performance to even greater heights. These might use CNTs to achieve near-zero leakage current, be ultra-scalable to the atomic limit, and offer ballistic transport for improved switching speeds [85]. The integration density and efficiency promised by CNT-FETs exceed 100 million FETs per mm^2; however, ongoing challenges with reliable fabrication, affecting both placement accuracy and variability control, along with poor compatibility with conventional CMOS processes, pose serious obstacles to the wide acceptance of CNT-FETs [86]. Notably, FinFETs are at the forefront of semiconductor applications in CPUs, GPUs, and AI processors. However, subpar performance at sub-3-nm nodes creates an opening for the next generation of nanowire transistors. Nanowire transistors offer the potential for enhanced performance for both AI and high-speed computing, if only certain manufacturing constraints can be overcome. While CNT-FETs have the greatest promise for performance and efficiency, at present, these devices are long-term solutions due to unresolved integration and manufacturing issues [87]. As the world advances toward smaller, better transistors, nanowire transistors will replace FinFETs, making CNT-FETs the focus of the next decade for ultra-low-power and high-speed computing.

4 | 2D Materials and Van der Waals (VdW) Heterostructures

In recent years, the rise of 2D materials like graphene and transition metal dichalcogenides (TMDs) opens up unprecedented opportunities to revolutionize next-generation semiconductor devices. They possess outstanding electronic properties including high carrier mobilities, tunable bandgaps, and atomic layer thickness, while combining various 2D materials into VdW heterostructures can provide new device opportunities that may outperform the current generation semiconductor devices [88, 89].

The representative fabrication workflows shown in Figure 5 compare the major process steps involved in SiC, GaN and two-dimensional semiconductor heterostructures. Similar basic process steps (micro-machining techniques) exist for all process flow, however with distinct steps concerning growth of materials, pattern definition of each layers, device structures and integration. Progress in fabrication technology has already supported successful demonstration of many high-speed and high-power electronic devices and has continued to drive on with developing advanced nanodevices.

4.1 | Emergence of 2D Materials

2D materials are materials synthesized in a single or a few atomic layers with nanometer thickness. 2D materials differ substantially from bulk materials because their reduced dimensionality confers peculiar electronic and optical properties [90]. 2D materials can

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TABLE 3 | Comparison of FinFETs, nanowire transistors, and carbon nanotube field-effect transistor.

Parameter	FinFETs	Nanowire transistors	CNT-FETs
Structure	3D multi-gate structure with the gate wrapped around the channel (Fin)	1D structure with a gate wrapped around the semiconductor wire	1D carbon nanotube channel
Gate control	Good electrostatic control due to 3D gate structure	Excellent electrostatic control due to 1D geometry	Outstanding (best electrostatic control with ballistic transport)
Drive current	Higher drive current compared to planar CMOS at smaller nodes	Higher drive current, especially at smaller technology nodes (sub-5 nm)	Best (high mobility and ballistic transport)
SS	Low SS due to improved gate control	Very low SS due to superior gate control	Near-zero (most efficient switching)
Leakage current	Reduced leakage current compared to planar CMOS	Very low leakage current due to superior electrostatic control	Near-zero (best power efficiency)
Fabrication complexity	Complex but achievable with existing CMOS processes	More complex due to precise control of nanowire growth and alignment	Very high (CNT synthesis and placement challenges)
Integration with CMOS	Easily integrable with current extremely difficult (poor compatibility with CMOS processes) CMOS processes	Integration with CMOS processes is challenging; requires new techniques	Extremely difficult (poor compatibility with CMOS processes)
Power consumption	Low (50% lower than planar CMOS)	Very low (better electrostatic control)	Extremely low (near-zero leakage current)
Integration density	~10 million transistors/mm^2	~20–30 million transistors/mm^2	>100 million transistors/mm^2 (potential for extreme scaling)
Electrostatic control	Good (better than planar MOSFETs)	Excellent (GAA structure)	Excellent (1D channel with ballistic transport)
Switching speed	Fast	Faster than FinFETs	Fastest (high carrier mobility, ballistic transport)
Material used	Silicon	Silicon, III–V compounds	Carbon nanotubes
Scalability (future nodes)	Good (used in 5 nm and below)	Excellent (can scale to 3 nm and beyond)	Outstanding (atomic-scale transistors possible)
Manufacturing maturity	Mature (used by Intel, TSMC, Samsung)	In development (adopted in research labs)	Early-stage (still experimental for large-scale production)
Industry adoption	Widely used in commercial semiconductor chips	Limited commercial adoption	Very limited (still in research phase)
Applications	CPUs, GPUs, AI chips	Future AI, high-speed computing	Next-gen energy-efficient computing, AI hardware

thus be classified into four groups: metals, semiconductors, insulators, and superconductors. Their different electronic properties confer strengths in photonics, electronics, and sensors for each group [91].

4.1.1 | *Graphene*

The most popular material is a thin, crystalline form of programmable carbon with a honeycomb structure. It is of great interest to researchers due to its excellent electrical characteristics. It has a very high electrical conductivity, with a charge-carrier mobility of 200 000 cm^2/Vs at low temperatures, and is one of the most conductive materials known [92]. There is also a phenomenon called ballistic transport in graphene, where electrons can move freely without scattering through the material, thereby improving its performance in high-speed electronic and optoelectronic applications. Although these properties are not undesirable, the absence of the so-called intrinsic bandgap in graphene is the main limiting factor for digital logic circuits and electronic switching, where a well-defined bandgap is required for efficient transistor operation. Experts are pursuing different approaches, including chemical doping, strain engineering, and heterostructure formation, which can compensate for the bandgap deficiency [93].

4.1.2 | *TMDs*

These semiconductor materials, such as MoS_2, WS_2, and $MoSe_2$, possess an indirect bandgap in bulk form, which changes to a direct bandgap once they are made into a single layer. This unique property makes them subjects of interest for optoelectronics and nanoelectronics devices [94].

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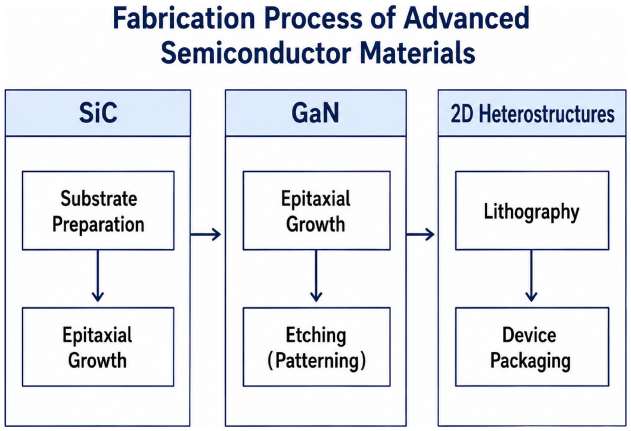

FIGURE 5 | Representative fabrication workflows for SiC, GaN, and two-dimensional semiconductor heterostructures.

4.1.3 | *Hexagonal Boron Nitride (hBN)*

Often referred to as the "white graphene," hBN is an insulator with high thermal stability and mechanical properties. Providing a high-quality interface for devices, it is often used as a substrate for graphene and TMDs [95].

4.1.4 | *Black Phosphorus (BP)*

A semiconductor with an adjustable direct bandgap, BP is well-suited for optoelectronic equipment such as photodetectors and LEDs. By varying the number of layers, one can change its characteristics [96].

4.1.5 | *Topologically Insulated Insulators (TIs) and Superconductors*

These materials have topologically protected surface states. These states are impervious to disorder and impurity scattering, making them excellent candidates for quantum computing and spintronic applications [97].

Although promising, 2D materials face many challenges, notably scalability, stability, and device integration [98]. One of the key challenges is the fabrication of high-quality monolayers over large areas. Another challenge is that 2D materials may be unstable in air, particularly for materials such as BP, which can quickly degrade in air [99].

4.2 | VdW Heterostructures

VdW heterostructures, formed by the vertical stacking of different 2D materials, allow for combining materials with mismatched lattice constants and distinct electronic and optical properties, unlike conventional heterostructures that requires strict lattice matching. The structure is held together by weak VdW forces between atomic layers. This feature has been utilized to develop tailored material systems with interesting phenomena [100].

VdW heterostructures are used for applications in electronics, optoelectronics, and quantum devices, owing to atomic sharp interfaces that ensure good charge transfer, low defect density, and excellent optical absorption. This makes VdW heterostructures suitable for devices like transistors, photodetectors, and photovoltaic devices [65]. Moreover, VdW heterostructures made of various combinations of 2D materials show great promise in devices such as superconducting magnetic hybrid systems and spintronic devices [101].

Recent studies have demonstrated that VdW heterostructures provide unprecedented control over the electronic properties at the atomic scale by judiciously stacking different 2D materials, achieving Type I, Type II, or Type III band offsets. Efficient charge transfer across interfaces, due to different band offsets, can be achieved, and this has been applied in transistors, photodetectors, and solar energy devices.

4.2.1 | *Fabrication Techniques for VdW Heterostructures*

The fabrication of VdW heterostructures involves several methods, including mechanical exfoliation, CVD, and molecular beam epitaxy (MBE) [102].

4.2.1.1 | *Mechanical Exfoliation.* This process involves mechanically peeling layers from a bulk material, typically used to prepare high-quality monolayers of materials such as graphene and TMDs.

4.2.1.2 | *CVD.* CVD is a widely used technique for synthesizing large-area 2D materials, including graphene, TMDs, and hBN. In this process, gaseous precursors are deposited onto a substrate to produce high-quality thin films for VdW heterostructure fabrication.

4.2.1.3 | *MBE.* Often used for producing extremely ordered heterostructures, MBE allows precise control over thin-film growth. However, this approach is more costly and complex than CVD.

4.2.2 | *Characteristics of VdW Heterostructures*

VdW heterostructures arise from the interaction of different materials. Proper alignment of the layers, especially the twist angle between them, is one of the most crucial factors to consider. Due to this, twist misalignment can lead to significant modifications in the electronic characteristics of the heterostructure, which can also result in effects such as flat bands and correlated insulating phases in graphene–TMD heterostructures [103].

Another crucial feature is interlayer coupling, which controls the electronic band structure and regulates charge transfer between layers. This phenomenon allows for bandgap engineering and the creation of new quantum states in VdW heterostructures. Additionally, these materials can be engineered to exploit quantum-mechanical effects, enabling new applications in quantum computing and optoelectronics [104].

4.3 | Applications of 2D Materials and Van der Waals Heterostructures

4.3.1 | *Electronics and Transistors*

2D materials, such as TMDs and graphene, are particularly researched for FET applications. Graphene-based FETs have high carrier mobility; however, their lack of a bandgap limits their

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use in digital logic circuits. In contrast, TMDs exhibit a tunable bandgap, making them better suited for transistor applications. Combining graphene and TMDs in VdW heterostructures appears to yield devices with improved performance [105, 106].

4.3.2 | Optoelectronics

In addition to their electronic uses, TMDs are ideal for optoelectronic devices such as lasers, LEDs, and photodetectors, as they exhibit a direct bandgap in monolayer form. Mixing different 2D materials allows scientists to create heterostructures that enhance charge transport, light emission, and light absorption. As a result, graphene–TMD heterostructures are being extensively explored for ultrafast photonic devices and high-performance photodetectors [107, 108].

4.3.3 | Spintronic Devices

Spintronics, which utilizes the spin and charge of the electron in electronic devices for information processing and storage, is a promising technology due to its low power consumption, high-speed processing, and nonvolatile features. 2D materials and VdW heterostructures have shown promise as platforms for spintronic devices due to their long spin diffusion lengths, adjustable spin–orbit coupling strengths, and atomically flat interfaces. The superior spin transport properties of graphene can be utilized, whereas TMDs, TI, and 2D magnetic materials can facilitate the manipulation of spin currents via proximity effect and interlayer coupling. Recently developed graphene–TMD and magnetic VdW heterostructures have been successfully demonstrated for spin injection, spin filtering, and spin current generation, which open up opportunities for constructing spintronic devices such as MTJs, spin valves, and MRAM. Graphene combined with spintronic device structures could promise the future generation of low-power electronic devices, nonvolatile storage systems, and quantum information technologies [109].

4.3.4 | Energy Harvesting and Storage

Moreover, they have great uses for energy storage and collection. Estimates for supercapacitors, batteries, and solar cells using other materials, such as TMDs and graphene, have been developed. 2D materials are ideal for energy storage applications, given their high surface area and conductivity; their optical properties may be utilized in next-generation solar cells [110, 111].

5 | Quantum Computing Hardware

Quantum computing utilizes quantum effects like superposition and entanglement to tackle computation tasks beyond the reach of classical computers. Leading hardware technologies include superconducting qubits, trapped ion systems, neutral atoms, Si spin qubits, photonic quantum processors, and topological qubits. Efforts have recently shifted toward the implementation of reliable and scalable, well-connected quantum information processing devices, via higher fidelity qubits, quantum error correction, and advances in quantum interconnects [112, 113].

5.1 | Superconducting Qubits

Superconducting qubits are the most mature among the technologies developed to build quantum computer processors, the first quantum computers being built on this technology by IBM, Google, and Rigetti. Superconducting qubits consist of a superconducting circuit that uses Josephson junctions to form a pair of states. This type of qubit is easy to scale since it uses processes similar to semiconductor fabrication and allows extremely fast quantum gate operations. Some processors have already been shown to contain more than 100 qubits. Despite these advantages, decoherence times, the number of required gates to perform an error-corrected calculation, and low-temperature operation are limitations to scalable quantum computing [114].

5.2 | Trapped-Ion Quantum Systems

Trapped-ion quantum computers use electrically trapped ions as qubits, whose states are manipulated with targeted laser pulses to implement quantum gates. Trapped-ion quantum computing features high-fidelity gates and very long coherence times, making it a promising architecture for fault-tolerant quantum computation [115]. This architecture offers higher gate fidelity, but scaling it is difficult due to the complexity of laser manipulation, ion trapping, and related techniques.

5.3 | Topological Qubits and Quantum Materials

Topological qubits use peculiar quantum states that are naturally protected from external interference, making them less susceptible to decoherence. Topological materials such as Bi_2Se_3 and Sb_2Te_3, as well as topological superconductors, could offer viable platforms for realizing Majorana-based qubits. The local perturbation immunity they possess could pave the way toward fault-tolerant quantum computing. While still an experimental topic, the potential of topological quantum systems is being pursued in the long term for scalable quantum architectures [116].

5.4 | Quantum Sensing Technologies

Quantum sensing employs quantum effects, such as superposition or entanglement, to achieve ultra-high detection precision. Technologies that use nitrogen vacancy (NV) centers in diamond, superconducting quantum interference devices (SQUIDs), and quantum magnetometers enable the detection of electric, magnetic, and thermal fields with nanoscopic precision [117]. This technology is used for material characterization, medical diagnostics, navigation, and energy storage research, providing superior measurement resolution and accuracy.

5.5 | Challenges and Future Prospects

Despite considerable progress, several issues must be resolved to achieve quantum computation: decoherence, error propagation,

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limited scalability, and the need to operate at cryogenic temperatures. For future heterogeneous platforms, there is foreseeable integration of advanced CMOS technologies with beyond-CMOS accelerators by incorporating conventional processor units, neuromorphic accelerators, and quantum co-processors into one heterogeneous computing platform. AI-supported electronic design automation, 3D heterogeneously integrated technology, and advanced package technology are all going to enable such convergence [118–120].

6 | Neuromorphic Computing

Most traditional digital computers have their architecture based on the von Neumann model, in which processing units and memories are physically separated. That model allowed decades of advances in semiconductor devices, but the constant movement of information back and forth between memory and processing requires data transfer time and energy consumption, known as the von Neumann bottleneck. Data intensive and AI applications are increasingly demanding computers capable of putting those components together [121, 122].

6.1 | Fundamentals of Neuromorphic Computing

Neuromorphic computing is a new computing paradigm that draws inspiration from the structure and functioning of the human brain, comprising a vast network of artificial neurons and artificial synapses. The computational and memory components in a neuromorphic hardware system are closely intertwined and placed on the same platform instead of being separate as in the typical von Neumann computer architecture, thus eliminating the communication latency caused by the movement of data between memory and processing units and dramatically enhancing energy efficiency [123]. Hence, these systems offer significant advantages in AI, edge AI, robotics, and intelligent control. The ability of the human brain to perform these tremendously complex functions at a small energy expenditure (20 W in comparison to conventional AI processors, which may have an output wattage in the tens or hundreds of Watts for less capability) drives most of the interest in neuromorphic computing, focusing on event-based information representation and transmission, massively parallel processing of information, and biologic-learning principles through such constructs as spiking neural networks (SNNs) [124].

The development of new semiconducting devices, such as memristive and other nonvolatile memories, continues to propel development in physical neuromorphic computing hardware platforms.

6.2 | SNNs

SNNs constitute the computational foundation of neuromorphic hardware. Information is encoded as discrete spikes rather than continuous numerical values, enabling sparse event-driven computation with substantially lower energy consumption. SNN accelerators implemented using CMOS circuits, memristive synapses, and mixed-signal architectures have demonstrated considerable promise for real-time intelligent sensing and autonomous systems [125, 126].

6.3 | Memristive Neuromorphic Hardware

Oxide-based memristors such as those utilizing HfO_x, TiO_x, and TaO_x offer nonvolatile tunable conductance modulation, making them appealing devices for implementation of artificial synapses. The use of low programming power consumption, large integration densities, and feasibility in crossbar arrangements drives the development of in-memory computing and neuromorphic processors utilizing memristors. Nevertheless, large device variability, limited programming cycles, and low endurance can pose significant challenges [127].

6.3.1 | Electrically Controlled Memristors

An electrically controlled memristor is one whose conductance (the reciprocal of resistance) is tuned by an external electrical signal, such as voltage or current. The switching mechanism is attributed to several effects, including ion migration within the device, filamentary conduction (driven by the formation or breaking of a conducting path), trapping/de-trapping of charges, and interfacial redox reactions in oxide structures such as TiO_x, TaO_x, HfO_x, and IGZO [128].

During operation, an externally applied potential induces the redistribution of defects, such as oxygen vacancies, or the accumulation/depletion of ions, resulting in a reversible transition between high- and low-resistance states. As the resistance can be modulated analogously to a biological synapse, it is more effective to achieve weight plasticity, such as long-term potentiation (LTP) and long-term depression (LTD), via spike timing-dependent plasticity. Electrically controlled memristors have proven to possess good endurance, scale to smaller sizes, and consume minimal energy during switching, making them an excellent choice for neuromorphic processors or in-memory computing structures [129].

6.3.2 | Optically Controlled Memristors

An optically controlled memristor is one whose conductance state is modulated by an external optical stimulus, such as light. Optically controlled memristors combine the functionality of optical detection and resistive memory, with various materials such as oxide semiconductors (ZnO, IGZO, TiO_2), 2D materials (MoS_2, WS_2), and perovskites that demonstrate photoinduced memristive effects. The generation of photogenerated carriers upon illumination influences the internal charge distribution and structural properties of the device, thereby switching conductance [130].

The combination of optical sensing and electrical resistive-state control paves the way for new hardware architectures, such as image sensors and even artificial visual systems. It is extremely useful for applications such as machine vision systems, autonomous navigation, and AI, which require sensing, perception, learning, and computing functionalities to be implemented directly onto a single chip [131]. Table 4 summarizes the key differences between electrically and optically controlled

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TABLE 4 | Comparison of electrically and optically controlled memristors.

Parameter	Electrically controlled memristors	Optically controlled memristors
Stimulus	Electrical voltage/current	Optical illumination
Switching mechanism	Ionic migration/filament formation	Photo-induced carrier generation
Response speed	Nanoseconds–microseconds	Nanoseconds–microseconds
Synaptic emulation	Excellent	Excellent
Artificial vision capability	Limited	High
Integration complexity	Moderate	Higher
Primary applications	In-memory computing, AI accelerators	Artificial vision, neuromorphic sensors

memristors, demonstrating their complementary roles in neuromorphic computing systems.

Electrically controlled memristors excel in speed and computational efficiency, making them suitable for in-memory AI accelerators, whereas optically controlled memristors offer enhanced sensory and artificial vision functionalities at the expense of higher integration complexity and slower response times [132–137].

6.4 | Neuromorphic Hardware Platforms

Significant efforts have been made to build hardware accelerators for neuromorphic computing. These hardware platforms are designed to mimic the massively parallel and event-driven structure of the biological brain, with power consumption orders of magnitude lower than that of contemporary GPUs [138].

6.4.1 | Industrial Implementations

IBM TrueNorth demonstrated large-scale neuromorphic computing using one million programmable neurons with extremely low power consumption, while Intel Loihi and Loihi 2 introduced on-chip learning capabilities and improved scalability. These hardware platforms represent significant milestones toward practical neuromorphic computing for robotics, edge intelligence, and autonomous systems [139, 140].

6.5 | Applications of Neuromorphic Computing

Neuromorphic computing finds application in a wide range of fields [141–144].

6.5.1 | AI and Edge Computing

The significant power savings achieved by neuromorphic processors in event-driven computation make them well-suited for always-on, low-power AI systems, including sensing and inference on constrained devices such as smartphones and smart wearables.

6.5.2 | Robotics and Autonomous Systems

The high parallelism and low latency processing enabled by neuromorphic hardware can revolutionize the way autonomous systems perceive and interact with their environment. This leads to improved robotic control, object recognition, adaptive learning, and decision-making abilities in dynamic and complex environments.

6.5.3 | Brain–Computer Interfaces

Neuromorphic systems enable us to interact directly between biological brains and machines. The capabilities could range from assistive applications, such as robotic prosthetic devices, to helping people with neural disabilities regain motor control.

6.5.4 | Intelligent Sensing and Machine Vision

Integrated sensing and processing in optically controlled memristor-based hardware can revolutionize machine vision, which requires massive amounts of parallel processing in real time, as in autonomous cars and surveillance systems.

6.6 | Challenges and Future Outlook

Despite promising developments, several challenges exist for the mass adoption of neuromorphic systems. These are mostly related to the variability of the devices used (e.g., memristors), the endurance of devices under prolonged operation, the difficulty of large-scale integration, the uniform production of desired device properties during fabrication, and the optimization of neuromorphic algorithms with hardware. Future semiconductor research will increasingly combine advanced CMOS technologies with beyond-CMOS accelerators through heterogeneous integration, chiplet-based architectures, backside power delivery, 3D integration, and AI-assisted electronic design automation. Emerging materials, advanced packaging, and co-optimization across devices, circuits, and systems will be essential to sustain improvements in performance, energy efficiency, and reliability beyond the limits of conventional scaling [145, 146].

7 | Conclusion and Perspectives

In this review, we summarize the progression from early, classical CMOS technology to more advanced CMOS architectures and ultimately to exciting, next-generation beyond-CMOS technologies. By providing a distinct set of characteristics for what constitutes advanced CMOS—that is, the modern transistor designs

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based on FinFET, GAA transistor, nano-sheet FET, and CFET structures—and what will constitute a true departure to beyond-CMOS paradigms such as TFETs, spintronics, memristive logic, neuromorphic computing hardware, and quantum computing, this work has constructed a unified technical foundation from which the development of future Si devices can be analyzed. Modern efforts in wide-bandgap, oxides, 2D, and heterogeneous materials confirm that the future of computing relies upon a convergence of materials, devices, and intelligent systems. Fabrication capabilities, reliability, quantum error correction, AI for automated design, and environmentally sustainable methods of production will continue to define future trends in semiconductor technologies.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

Data sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

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