Printed, Low Voltage, All-Organic Transistors and Complementary Circuits on Paper Substrate

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Paper is drawing considerable attention as a possible alternative to plastic for the development of flexible electronics. Indeed, in order to reduce excessive plastic consumption and waste, paper is attractive thanks to its renewable nature, low cost, ubiquity and flexibility. Here, a simple, cost-effective and low temperature approach, based on inkjet-printing, is presented for the development of low voltage, all-organic field effect transistors on commercial paper. Both n- and p-type transistors are developed with reproducible electrical performances, such as low operating voltages (not exceeding 5 V) and quasi-zero threshold voltages. Moreover, fabricated devices are characterized by a remarkable mechanical stability, as they can be deformed even at small bending radii without any significant degradation of their

performances. Finally, as proof-of-concept for this technology, complementary electronic circuits are fabricated and tested, as basic building blocks for future development of complex flexible electronics on paper.

1. Introduction

In the Internet of Things (IoT) era, the demand for smaller, smarter and flexible electronics has never been greater. In the past few years, flexible technology has been extensively investigated both in industries and in research institutions as an attractive candidate for next-generation consumer electronics. As a result, research and development on flexible plastic electronics have witnessed huge advances and it is expected to enable a wide range of applications.[1-4] However, despite the significant technological progress and advantages of plastic as substrate for flexible electronics, some intrinsic problems must be considered. Indeed, rapid innovation and costs reduction have dramatically increased access and consumption of electronics products,[5] which are continuously updated and released on market in few months. This evolution generates technological challenges and poses a growing ecological problem: plastic consumption and waste are a major concern in the modern world.[6] Therefore, a considerable amount of plastic electronics waste would exacerbate the already serious environmental contamination. On these bases, the development of flexible electronics consisting of biodegradable, renewable and biocompatible materials is highly desirable.[7,8]

The employment of paper or paper-like substrates is attracting considerable attention as a possible alternative to plastic in next-generation flexible electronics.[9-12] Paper is by far the most employed and cost-effective material in our daily life, with an average price close to 0.1 cent·dm^{-2}, which is substantially lower than that of plastic substrates such as polyethylene therephtalate (PET, ≈2 cent·dm^{-2}) and polyimide (PI, ≈30 cent·dm^{-2}). Moreover, compared to conventional flexible substrates, paper integrates flexibility and bendability with peculiar

features such as ubiquity, low costs and eco-sustainability. These attractive properties make paper a promising material for the development of flexible electronics for different applications, such as Point-of-Care devices,[13] disposable sensors,[14,15] solar cells,[16] paper displays,[17] energy storage,[18] smart packaging and RFID tags.[19] Among different technologies, organic electronics has gained a rising interest for the development of low-cost paper electronics.[20-24] In particular, an intensive research has focused on the development of Organic Thin-Film Transistors (OTFTs) on paper substrates, since transistors are fundamental building blocks of most electronic systems. Indeed, compared to inorganic or metal-oxide-based transistors, OTFTs have some important technical advantages, such as the possibility of being produced by means of large-area, cost-effective techniques, which exploit at an industrial size solution-based and low-temperature processes. To date, different researchers have contributed to the development of OTFTs on paper-like substrates, typically employing conventional fabrication techniques, such as sputtering and evaporation.[25-29] It is noteworthy that, in any case, performances are generally inferior to those of devices on plastic substrates, and, except few recent works,[30-31] operation voltages of OTFTs on paper are generally in the order of tens of volts. In addition, in order to take advantage of the low cost of paper substrates and really push flexible paper electronics into the market, inexpensive, highly efficient and low temperature fabrication methods are necessary. Printing techniques have gained interest for depositing functional materials rapidly, precisely, and reproducibly through a mask-less approach. In particular, thanks to scalability and manufacture costs, inkjet printing on paper is more competitive than other approaches. Until now, great effort has been devoted to the development of different printed electronics devices and systems including transistors,[32] solar cells,[33] memory elements and RFID tags.[34,35] However, most of these advances have been made for printed device on plastic substrates, while little progress has been obtained for printed electronics on paper. Indeed, significant challenges remain and the number of printed OFETs on paper is still limited. [36-38]

In this article, an all-organic field effect transistor (OFET) fabricated on a commercially available paper substrate is presented. With respect to the state-of-the-art, proposed OFETs are fabricated by means of large-area, cost-effective and low-temperature techniques, namely inkjet printing and chemical vapour deposition, easily up-scalable to industrial size. Moreover, the all-organic structure can be operated at low voltages (less than 5 V) for both n- and p-channel transistors. This is an unprecedented result for OFET fabrication on paper substrates by means of large area fabrication techniques. Process reliability and reproducibility of electrical performances are demonstrated in statistically-relevant sets of devices. Mechanical stability of fabricated devices is also proved, as a fundamental feature for their future employment in different application fields including bioengineering and smart packaging. Thanks to the successful fabrication of both p-type and n-type devices, complementary electronic circuits, such as inverters and logic gates, are fabricated and tested.

2. Results and Discussion

2.1. Structure, materials and fabrication process

Bottom-gate bottom-contact OFETs with the structure shown in **Figure 1**a were fabricated on *p_e:smart paper type 1* from Felix Schoeller. This is a 185 ± 10 µm thick flexible paper substrate with a specific weight of 190 ± 10 $g \cdot m^{-2}$ and a surface coated with a hydrophilic nonporous primer layer. Atomic Force Microscopy (AFM) was employed to collect information about the paper surface morphology. In particular, AFM images reveal a root mean square (rms) roughness of about 0.5 nm (**Figure S1**, Supporting Information). For the fabrication of the basic transistor structure, two large-area techniques were effectively combined: inkjet printing and Chemical Vapor Deposition (CVD). Inkjet printing was employed for patterning all electrodes in the transistor structure, i.e. gate, source and drain contacts, employing a poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS)-based commercial ink. Specifically, source and drain contacts were designed

with an interdigitated structure, comprising 10 channels with single channel length of about 200 μm. CVD was employed for the deposition of the gate insulator layer, namely a Parylene C film with a capacitance of 9 $nF \cdot cm^{-2}$. It is worth noting that inkjet printing and CVD are compatible techniques in terms of throughput and working area. Moreover, CVD processes are also compatible with other printing techniques with larger throughput, such as roll-to-roll processes.[39] In order to fabricate p-channel OFETs (p-OFETs), a home-made 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS pentacene)-based ink was deposited by inkjet printing, while ActivInk™ N1400 was deposited through spin coating in the case of n-channel OFETs (n-OFETs). Interestingly, the fabrication process was carried out at low temperatures, i.e. maximum 60°C for the inkjet printing and ambient temperature for CVD.

Focussed-ion beam scanning electron microscopy (FIB-SEM) (Helios 650 and Helios 600i, FEI) was performed to verify OFETs structure at the nanoscale. A device cross-section is shown Figure 1b, where the gold layer deposited on top of the OFET architecture as part of FIB-SEM process is also visible. The stacking of different layers composing the device structure (PEDOT:PSS gate electrode, Parylene C dielectric layer, PEDOT:PSS source/drain electrodes) is clearly distinguishable from the image, thus proving that deposited materials do not penetrate the substrate, thus forming a continuous and close layer, which is fundamental for the development of printed electronics. FIB/SEM analysis also allowed a quantitative evaluation of different layers thicknesses: a thickness of about 250 nm, 300 nm and 200 nm were measured for gate, dielectric and source/drain contacts, respectively.

2.2. OFETs electrical characterization

2.2.1. p-type OFETs

At first, p-type OFETs have been fabricated and tested. **Figure 2**a and 2c shows representative output and transfer characteristics of such devices, respectively. It is possible to highlight that all the fabricated devices can be operated at low voltages, specifically at gate-

to-source (V_{GS}) and drain-to-source (V_{DS}) voltages not exceeding 5 V in absolute value, with a quasi-zero threshold voltage (V_{TH}). The output curves (Figure 2a) are characterized by a very good linear behaviour at small V_{DS} and a good saturation, as well as a significant field-effect current modulation for larger V_{DS}, exceeding ($V_{GS}-V_{th}$). These results, together with the negligible hysteresis shown in the transfer characteristic curves (Figure 2c), allow inferring a good quality of charge carrier injection and insulator-semiconductor interface. Moreover, from transfer characteristic curves, an average threshold voltage of (-0.4±0.2) V, a subthreshold slope of (0.5±0.2) V·decade^{-1} and a field-effect mobility in saturation regime of (0.2±0.1) $cm^2 \cdot V^{-1}s^{-1}$ are extrapolated. An on/off current ratio of p-OFETs is $(6\pm4)\cdot10^3$ is obtained, while the gate-to-source current (I_G, leakage current) is in the range of 10^{-10} A. This last result indicates that the Parylene C layer allows a perfect insulation of the gate contact, even if it is thin enough to ensure a low voltage operation. All the average data, related to a total of 50 p-OFETs, are reported in **Table 1**. **Figure S4** in Supporting Information reports threshold voltage and mobility stability over time, and for devices subjected to bias stress. Although these results must be considered preliminary, it is possible to observe that threshold voltage variation is limited to a few hundreds of millivolts, when devices are subjected to 500, consecutive, double-sweep transfer characteristic acquisitions. A similar threshold voltage variation has been recorded for devices stored at free air, and un-controlled ambient conditions, over a period of time of approximatively 20 days. As regards charge carrier mobility, a maximum percentage variation of 15% has been recorded in bias stress tests, while the maximum variation is of about 30% in aging tests. In the latter case, the not-controlled ambient conditions during storing and measurements have to be taken into account: as a matter of fact, nor threshold voltage, nor mobility show an actual aging trend. It is noteworthy that these results are substantially equivalent to what is obtained on plastic substrates to not encapsulated, bottom-gate bottom-contact, TIPS pentacene-based OFETs.[40]

2.2.2. n-type OFETs

The availability of a reliable fabrication process for both p-type and n-type organic transistors is nowadays of utmost importance to develop complex organic circuits. Indeed, complementary organic technologies would have great advantages in low-power consumption, high integration density, and implementation in a wide variety of complex (analog/digital) circuits, fundamental for several applications in the IoT era. Therefore, in order to fabricate organic complementary circuits, both p- and n-type organic semiconductor are required. However, the performances of organic CMOS-like circuits are so far limited by the typical poor performances and air stability of the most of n-type organic semiconductors. In particular, good performance of n-type OFETs are generally observed only in inert atmosphere. In this work, a commercially available, environmentally stable, n-type organic semiconductor, namely ActivInk^{TM} N1400, is employed for the development of n-OFETs for organic complementary circuits. N1400 is a perylene derivative, which can be deposited by thermal evaporation but also from liquid phase since it is soluble in chlorinated solvents. Interestingly, N1400 stability in air has been previously demonstrated,[41] as well as the possibility of fabricating N1400-based devices by means of inkjet printing.[34] With the aim of obtaining complementary logic circuits, this molecule has been employed in order to fabricate solution processed n-type OFETs on paper. Typical output and transfer characteristics of N1400-based n-OFETs are reported in Figure 2b and 2d, respectively. It is noteworthy that also in this case all the fabricated devices can be operated at low-voltages, not exceeding 5V. Again, a good current stability in saturation and field-effect current modulation can be observed from output characteristic curve (Figure 2b), even if the maximum output current (for the same device geometry) is lower than the one obtained in the previously reported p-OFETs. This is related to the lower charge carrier mobility obtained using N1400, which is $(1.0\pm0.5)\cdot10^{-2}$ $cm^2\cdot V^{-1}s^{-1}$ in saturation regime, as extrapolated by transfer characteristic curves (Figure 2d). An average threshold voltage of (0.5±0.3) V, a subthreshold slope of

(0.6±0.4) V·decade^{-1} and an on/off current ratio of (4±3)·10^{2} are obtained. Finally, a negligible hysteresis and a leakage current in the order of 10^{-10} A can be noticed, demonstrating once more that Parylene C is able to form a very good thin and pin-hole free insulating layer, able, at the same time, to give rise to a good interface with the most of the organic semiconductors. All the average data, related to a set of 50 n-OFETs, are reported in Table 1. **Figure S5** in Supporting Information reports the threshold voltage and mobility variations for devices subjected to bias stress test, and in aging tests. The experimental conditions are the same of TIPS pentacene devices reported in Figure S4. In this case, a more significant trend of threshold voltage and mobility variations can be noticed. In bias stress test, threshold voltage variation approaches 1 V after 500, consecutive transfer characteristic acquisition, while mobility changes of about 10%. Nonetheless, a substantial plateau is reached after 400 cycles. Similarly, in more than 20 days, threshold voltage and mobility show a significant variation only in the 4 days (0.5 V of threshold voltage variation, 40% of percentage mobility variation): afterwards, threshold voltage and mobility are substantially stabilized.

2.3. OFETs electromechanical characterization

In order to be really able to integrate paper electronics into common object of daily use, stability upon mechanical deformation is fundamental. Indeed, flexibility and bendability are key requirements for several applications of printed electronic systems on paper. The ultimate goal is the development of electronic systems that can be bent (into a bending radius of a few centimeters or a few millimeters) without degradation of the electronic functionality. For these reasons, the mechanical robustness of proposed OFETs on paper was investigated under bending. At first, both p- and n-OFETs were bent several times at different bending radii (R = 45, 25, 10, 7.5 and 5 mm) in order to identify their eventual failure point. To this aim, transistors electrical parameters were extrapolated before, during and after each bending step.

Figure 3a and 3c show the evolution of the saturation mobility under bending for p- and n-OFETs, respectively. Interestingly, no significant degradation upon bending can be noticed even when devices are bent at a radius of 5 mm. Moreover, mechanical stress tests have been performed by bending devices at a radius R = 7.5 mm. As shown in Figure 3b and 3d, both p- and n-OFETs saturation mobility reveals a good stability even after 200 bending cycles, confirming that these transistors are quite robust to bending. Interestingly, similar transistor structures, with the same organic semiconductors as active layer and fabricated on plastic substrates of similar thickness, are characterized by a more significant variation of the electrical characteristics as a response to mechanical deformations.[42,43] In order to explain such a difference, an accommodation of most of the mechanical stress in the cellulose fibers composing the paper substrates can be hypothesized. In this way, only a small part of this stress is actually applied directly onto the organic active layers, thus justifying the improved mechanical stability of devices fabricated on paper. These results attest the suitability of the proposed technology for the development of flexible printed organic electronics on paper substrates.

2.4. Organic complementary circuits

2.4.1. Logic inverter

Results presented so far highlight that it is possible to fabricate n- and p-OFETs with the same materials/substrate, large area fabrication techniques, and same processing conditions. Thanks to this powerful combination, the most obvious next step is the development of complementary logic circuits, which need both n- and p-type transistors. Indeed, compared to unipolar logic, complementary logic benefits from reduced power dissipation, faster switching speed, and good immunity to signal variations. As previously mentioned, recently, there has been an increasing interest in the use of OTFT technology in next-generation thin film electronics, because the performance enhancements enable its employment in applications

like flexible displays, large area sensors and RFID. In particular, a significant attention has been paid to the employment of OTFTs in practical wearable devices and RFID tags. A complementary logic configuration is more desirable for such devices because of its low power consumption compared with the unipolar p- or n-OTFT circuit configuration. A complementary organic technology allows the implementation of complex mixed analog/digital circuits to be achieved with high yield and lower current consumption, as well as high reliability. In this work, low-voltage organic complementary circuits on paper substrate are proposed, thus demonstrating an actual possibility of accomplishing the challenge of developing low cost, flexible, portable, and easy recyclable products.

The simplest complementary circuit is the logic inverter. **Figure 4**a schematically shows an inverter with complementary p- and n-type transistors, which both act as driving transistors, i.e. both actively pull the output node. The p-OFETs is the pull-up transistor, which pulls the voltage of output node V_{out} to bias V_{DD} when the input voltage V_{in} is low (0), while the n-OFET is off. The pull-down transistor is the n-OFET, which pulls the output node to 0 when V_{in} is high (V_{DD}), while the p-OFET is switched off.

The organic complementary inverters here presented have been fabricated with the same process described in previous paragraphs, by integrating n- and p-OFETs on the same paper substrate. As schematically depicted in Figure 4b, the inverter structure is obtained by driving the transistors with the same gate electrode in order to provide the V_{in} and by making them share the drain electrode, which is also the output node. A static characterization was performed by sweeping the logic state of V_{in} from “0” to “1” at voltages ranging from 0 to 5 V. Figure 4c shows a typical voltage transfer characteristic, which allows extrapolating essential electrical parameters such us rail-to-rail behaviour, logic threshold voltage, gain and noise margin. First of all, the transfer characteristic curves are characterized by an almost complete rail-to rail behaviour, since the output voltage swing goes from 0 to V_{DD}. In general, the switching point or the logic threshold voltage V_M is defined as the input voltage for which

$V_{out} = V_{in}$, which should be $V_{DD}/2$ for an ideal inverter. The value of the logic threshold voltage can be extracted graphically from the intersection of the voltage transfer curve with the $V_{out} = V_{in}$ curve (Figure 4c), obtaining $V_M \sim 3$ V (slightly more than $0.5 \cdot V_{DD}$). In order to realize an integrated circuit, the output of an inverter has to be able to act as input of a subsequent stage. This means that the inverter needs to have a gain, i.e. a region with a slope larger than unity in the transfer curve. A maximum gain of 14 V/V has been recorded as derivative of the transfer curve at the logic threshold, proving the suitability of the proposed technology to develop complementary logic circuits.

Finally, the noise margin must be considered as a further figure of merit for an inverter. This parameter gives an estimation of the inverter immunity against input signal variations (noise), which cannot be avoided in practical applications. According to the "maximum equal criterion", the noise margin can be obtained by mirroring input and output voltages in the transfer curve and by determining the size of the maximum square that fits in the area between the original and the mirrored transfer curve. As shown in Figure 4d, the noise margin results to be 1,4 V which is about 50% of $0.5 \cdot V_{DD}$, a value generally considered suitable for correct operation of organic logic circuits.

2.4.2. Logic gates

Starting from basic inverters, logic gates can be obtained. Indeed, an inverter is the simplest form of logic gates, i.e. the logic NOT. As proof of concept of the proposed technology, complementary NOR, OR, NAND and AND logic gates are developed. **Figure 5**a and 5b show circuit configurations, circuit symbols and truth tables for NAND, AND, NOR and AND gates. A NAND gate is fabricated by connecting two p-OFETs in parallel (pull-up network) and two n-OFETs in series (pull-down network), as shown in Figure 5a. A complementary AND gate is obtained by connecting the output of the NAND ($F = \overline{A \cdot B}$) to the input of an inverter. Similarly, in a NOR gate the pull-up network consists of two p-OFETs in series and the pull-down networks of two n-OFETs in parallel, while the

complementary OR gate is obtained by connecting the output of the NOR ($F = \overline{A + B}$) to the input of an inverter (Figure 5b). Typical output versus two inputs voltage characteristics of the different logic gates are reported in Figure 5c. The operating voltage is V_{DD} = 5 V, while the two input voltages, A and B, are 5 V for logical 1 and 0 V for logical 0. These characteristics have been obtained by considering the voltage levels reached by the circuit in the steady state: no information about the dynamic response was derived, as the experimental setup didn't allow the dynamic variations of A and B signals, which were actually imposed in separated measurements (i.e., removing each time the bias to the circuit). It is clearly evident that the output of the NAND gate is high (1) if at least one input is low (0); the output of the NOR gate is low (0) if any of the inputs is high (1); the AND gate has a low (0) output if at least one input is low (0); the OR gate gives a high output (1) if one or more of the inputs are high (1). In an ideal case the output voltage of each logic gate should be as close as possible to the input voltage, i.e. $V_{out} \approx V_{DD}$.

It is noteworthy that for the developed organic logic gates, a value close to zero (in the range (0.009;0.4) V) is actually recorded corresponding to a logical 0, while a value very close to V_{DD} (in the range (4;4.97) V) is recorded corresponding to a logical 1, according to the desired truth tables. These results demonstrate the real possibility of developing complex low voltage electronic organic circuits on flexible paper substrate.

3. Conclusions

In conclusion, a low voltage, all-organic OFET structure fabricated on a commercially available paper substrate has been developed. Large-area, cost-effective fabrication techniques, namely inkjet printing and chemical vapor deposition, have been employed. Both n- and p-type OFETs have been developed. A complete statistical analysis of electrical performances is provided for a relevant set of devices. Both n- and p-channels OFETs can be operated at low-voltages, not exceeding 5 V in absolute value, with significant reproducible

electrical parameters such as a quasi-zero threshold voltage, a carrier mobility of (0.2±0.1) $cm^2 \cdot V^{-1}s^{-1}$ for p-OFETs and of $(1.0\pm0.5)\cdot10^{-2}$ $cm^2 \cdot V^{-1}s^{-1}$ for n-OFETs. Moreover, their mechanical stability has been demonstrated. Both p- and n-OFETs were bent several times at different bending radii: no significant degradation of the saturation mobility can be noticed even when devices are bent at a radius of 5 mm. Moreover, both p- and n-OFETs saturation mobility reveals a good stability even after 200 bending cycles at a radius R = 7.5 mm. Finally, low voltage organic complementary electronic circuits, such as inverters and NAND, AND, NOR and OR logic gates, have been developed, in order to exhaustively proof the possibility to develop low cost, flexible, portable, and easy recyclable electronic products.

4. Experimental Section

Device Fabrication: All organic transistors have been fabricated on a commercially available paper substrate, namely *p_e:smart paper type 1* from Felix Schoeller. This is a white opaque paper substrate with a nonporous surface coating and a hydrophilic primer layer. It has a thickness of 185 ± 10 μm and a specific weight of 190 ± 10 $g \cdot m^{-2}$. The front side of the paper has a surface energy of 55 ± 10 $mN \cdot m^{-1}$, a surface electrical resistance bigger than 10^4 Ohm and a temperature resistance of about 100 °C. Both p- and n-type OFETs have the same bottom-gate bottom-contact structure. A commercially available, Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS)-based ink (PJET HC from Heraeus) was employed for patterning gate, source and drain contacts, employing a Dimatix Materials Printer DMP2831 (Fujifilm Dimatix). In particular, a 16-nozzle cartridge with single drop volume of 1 pL (DMC11601, Fujifilm Dimatix) was filled. Gate electrodes were inkjet-printed directly on the paper surface: three nozzles, biased with a firing voltage of 25V, were employed for printing gate electrode of 10x2 mm^2, defined by the overlap of two subsequently printed layers. A drop spacing of 20 μm was set, and the printer platen was maintained at a fixed temperature of 60°C. The gate insulator is a 250 nm-thick Parylene C

film, deposited using a PDS 2010 Labcoater 2 (Specialty Coating System). An adhesion promoter (A-174 Silane, Specialty Coating Systems) was also inserted in the deposition chamber to improve the quality of the film. Source and drain electrodes were inkjet-printed using the same PJET HC-filled cartridge and the same printing conditions described for gate electrodes (with the exception of the employment of a single nozzle). In particular, source and drain contacts were designed with an interdigitated structure, comprising 10 channels with single channel length L of about 200 μm and W = 2 mm, obtaining a final W/L = 100. Source and drain electrodes were post-processed with a curing step over a hot plate (90°C for 15 minutes) and a subsequent deposition of ethylene glycol (EG, Sigma Aldrich) by inkjet printing. Specifically, a cartridge with a single drop volume of 10 pL (DMC11601, Fujifilm Dimatix), two nozzles with a firing voltage of 40 V and a drop spacing of 80 μm were employed. EG was left drying for 30 minutes over the printer platen at a temperature of 60°C. In the case of p-OFETs, the organic semiconductor is the 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS pentacene, Sigma Aldrich). It was inkjet-printed from a 1.5wt% solution in anisole (Sigma-Aldrich), employing a cartridge with a single drop volume of 10 pL (DMC11601, Fujifilm Dimatix), three nozzles biased at 40 V, a drop spacing of 30 μm and leaving the platen at room temperature. In the case of n-OFETs, the semiconductor is the ActivInk^{TM} N1400 (Polyera). In particular, a 0.5%wt solution in anisole (Sigma-Aldrich) was deposited through spin coating without any further patterning, and then left drying for 5 minutes over a hot plate at a temperature of about 100°C.

All organic complementary circuits have been fabricated simply integrating n- and p-OFETs. All circuits connections have been inkjet-printed employing the PJET HC ink with the same printing parameters of gate, source and drain electrodes.

AFM characterization: Atomic Force Microscopy (AFM) measurements were obtained by means of a SPM SOLVER PRO by NT-MDT in semi-contact mode, using NSG01 tips.

FIB/SEM characterization: Scanning electron microscopy coupled with focused ion beam sectioning (SEM/FIB) was operated for measuring the thickness of the OTFTs' layers. First, a 10 nm thick layer of gold was deposited on the structures via sputter coating (Agar Scientific). Afterwards, samples were loaded in to a dual beam machine (Helios 650 and Helios 600i, Thermo Fisher Scientific) and a region of interest was identified by scanning the surface with the electron beam at a voltage of 3-5 kV. Cross sections were realized by first trenching out part of the material via selective etching carried out with the ion beam operating at a voltage of 30 kV and current at 0.25 – 9.3 nA and then by polishing the interface fixing the ion beam current at 1.4 pA – 0.25 nA.[44] Imaging of the cross section was performed in "immersion" mode and backscattered acquisition, fixing dwell time at 30 μs and beam parameters to 2.0 kV as voltage and 86 pA – 2.8 nA current.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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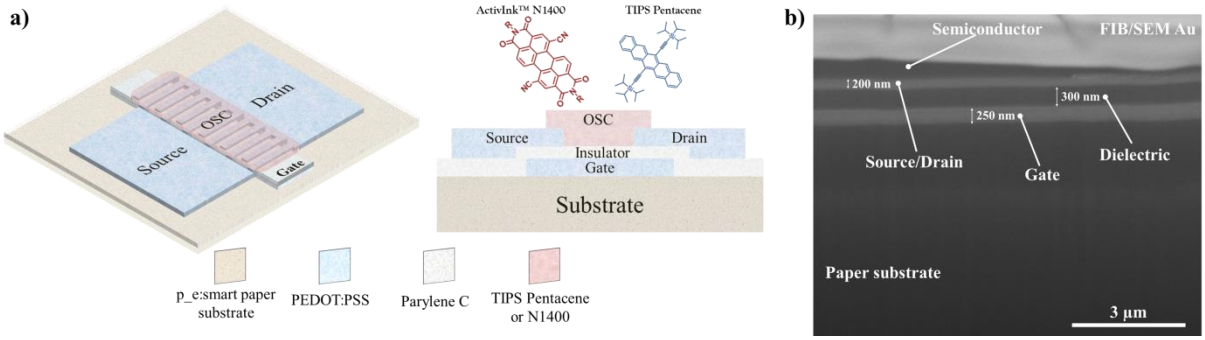


Figure 1. a) 3D cartoon and schematic cross-section of the bottom-gate bottom-contact structure with the indication of all employed materials. All films were printed except for the Parylene C dielectric layer. b) FIB/SEM image showing a cross-section through device. From the bottom to the top of the image: paper substrate, gate electrode of about 250 nm, 300 nm thick dielectric layer, source/drain electrode of about 200 nm, semiconductor layer and finally gold sputtered on the top of the device as part of the FIB/SEM process.

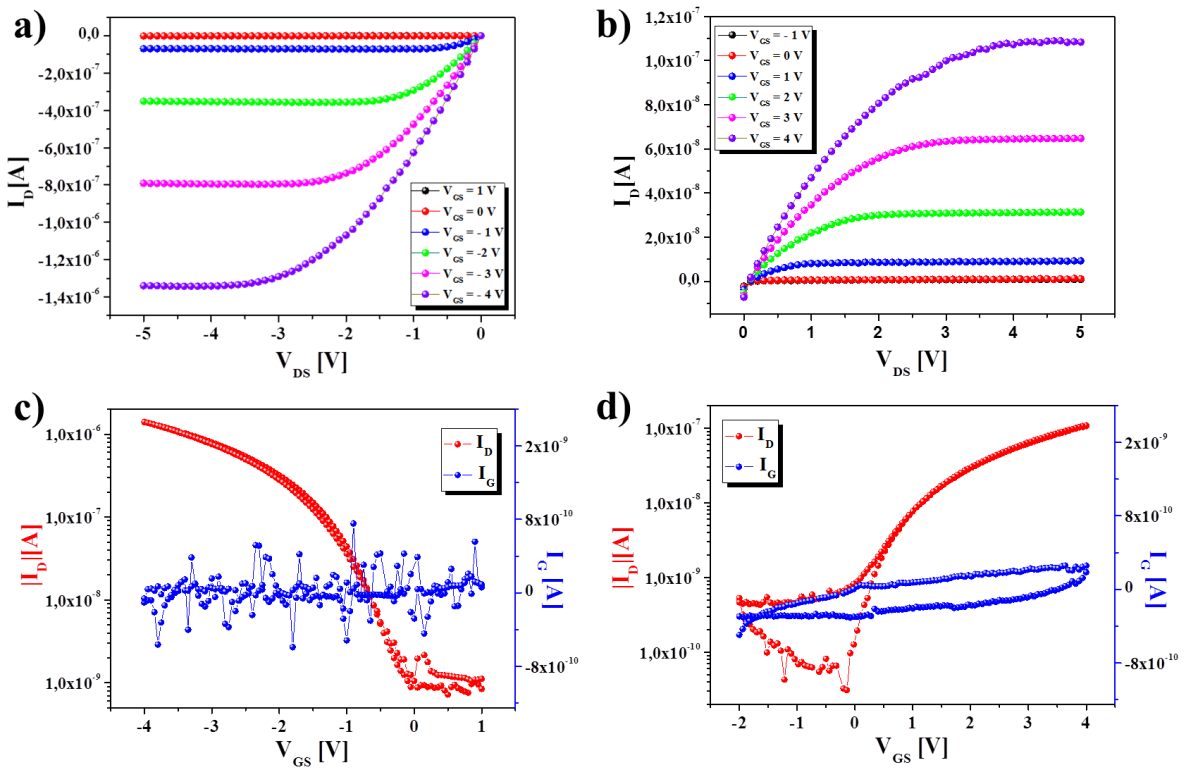


Figure 2. Typical output (a-b) and transfer characteristic curves (c-d) of p-OFETs (a-c) and n-OFETs (b-d) with channel length L=200 µm and weight W = 20 mm (W/L = 100). Transfer characteristics were measured with V_{DS} = -5 V for p-type OFETs, and V_{DS} = 5 V for n-type OFETs. In (c-d), leakage current (I_G) measured contemporary to I_D is also reported.

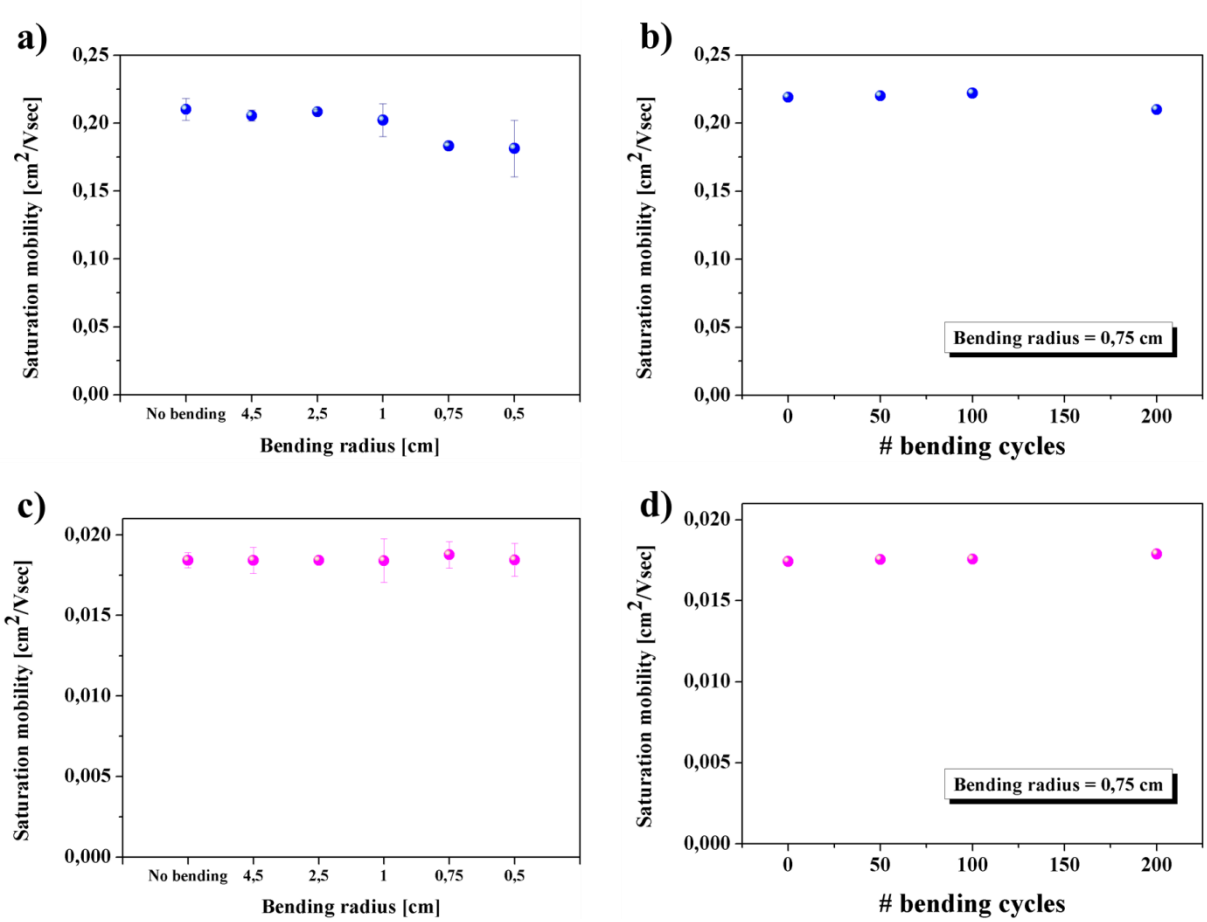


Figure 3. (a,c) Average saturation mobility evolution for p-OFETs (a) and n-OFETs (c) before and during bending at different radius (R = 45, 25, 10, 7.5 and 5 mm). Error bars represent standard deviation. (b, d) Repeated bending tests at a bending radius R = 7.5 mm showing a no degradation of saturation mobility after 200 bend for both p- (b) and n-OFETs (d). Mobility was extracted from transfer characteristic curves in saturation regime (V_{DS} = - 5 V for p-OFETs, and V_{DS} = 5 V for n-OFETs).

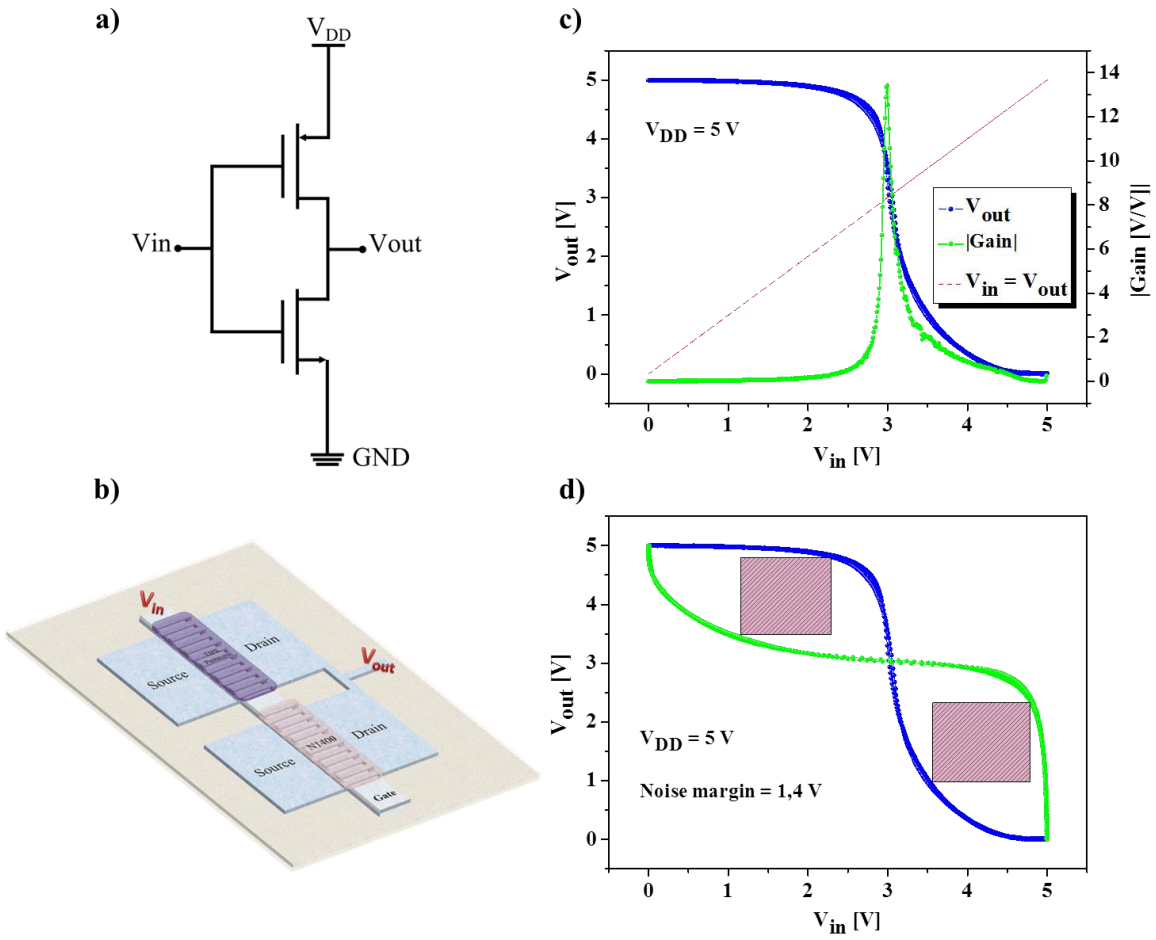
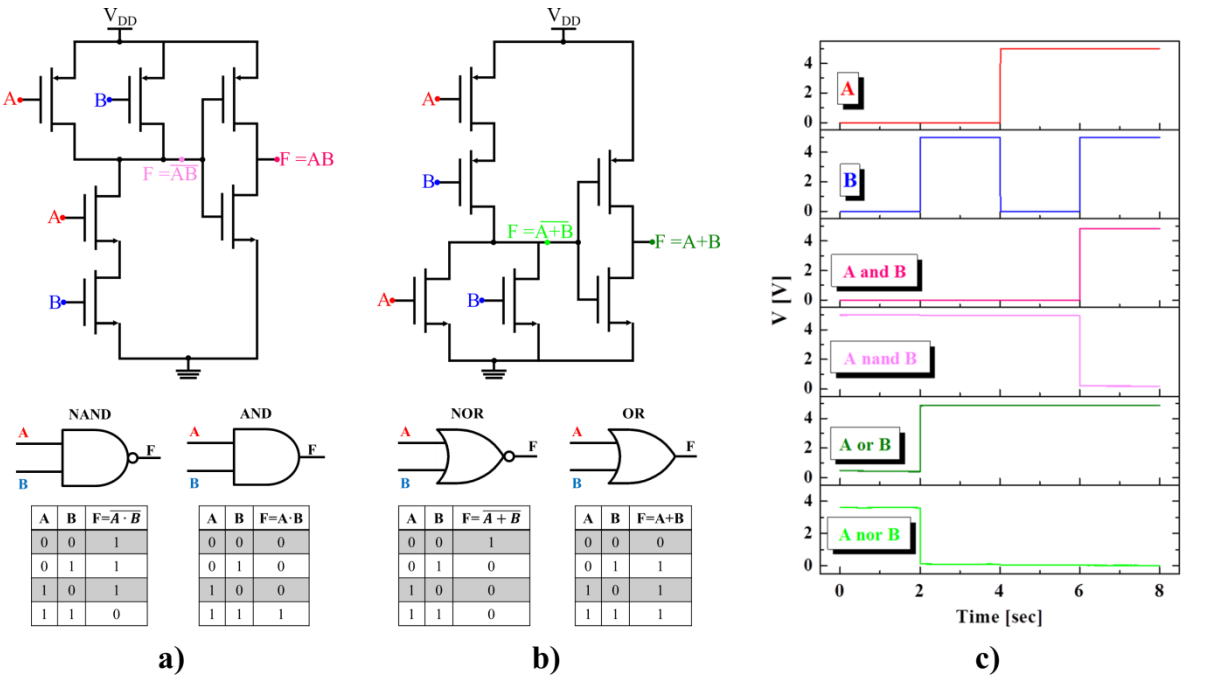


Figure 4. a) Schematic of an inverter with complementary p- and n-type transistors. b) 3D cartoon of the inverter structure. c) Inverter voltage transfer curve with definition of logic threshold voltage and gain. d) Determination of the noise margin of the inverter as the size of the larger square fitting between inverter transfer curve and the mirrored curve.



A	B	F=$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

A	B	F=A·B
0	0	0
0	1	0
1	0	0
1	1	1

A	B	F=$\overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

A	B	F=A+B
0	0	0
0	1	1
1	0	1
1	1	1

Figure 5. (a, b) Circuit schematic, symbols and truth tables for NAND, AND (a), NOR and OR gates (b). c) Outputs versus two inputs (A and B) voltage characteristics of AND, NAND, OR and NOR logic gates. The operating voltage applied is V_{DD} = 5 V. The two input voltages, A and B, are 5 V for logical 1 and 0 V for logical 0. The characteristics have been obtained in a static form, i.e. by imposing the different logic states (A and B combined values) in separated measurements. Transition between states is not representative of the actual dynamic response of circuits, which was not evaluated.

Table 1. Average and 1-σ confidence band for basic electrical parameters of p- and n-OFETs.

Parameter	p-OFETs	n-OFETs
Threshold voltage V_{TH} [V]	-0.4±0.2	0.5±0.3
Charge carrier mobility μ [$cm^2/(Vs)$]	0.2±0.1	$(1.0\pm0.5)\cdot10^{-2}$
Subthreshold slope [V/decace]	0.5±0.2	0.6±0.4
I_{ON}/I_{OFF}	$(6\pm4)\cdot10^3$	$(4\pm3)\cdot10^2$

A low voltage, all organic transistor fabricated on paper substrate is presented. Large-area, cost-effective and low-temperature techniques, as inkjet printing are employed. Process reliability, reproducibility of electrical performances and mechanical stability are demonstrated for both n- and p-channels transistor. Complementary electronic circuits are developed as proof of concept of future low cost, flexible, portable, and easy recyclable electronic products.

ToC Keyword: Organic transistors on paper

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Printed, Low Voltage, All-Organic Transistors and Complementary Circuits on Paper Substrate