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Enhancing Thermal and Radiation Hardness of All-Organic Printed Transistors by a Flexible and Transparent Encapsulation Layer for Low Earth Orbit Applications

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Organic electronics is a valuable technology for the development of cost-effective, large-area, flexible devices, which have been exploited in several application fields. Although these features are potentially interesting for new space economy applications, such as CubeSat deployment, the actual suitability of organic materials in representative environmental conditions is substantially unexplored. In this article, thermal and radiation hardness of organic field-effect transistors are discussed as a preliminary reliability assessment for their exploitation in low Earth orbit operating devices. The role of eventual encapsulation layers in the variation of electrical parameters is investigated. The effect of temperature step stress in a wide range (20–120 °C) is analyzed, as well as the influence of monochromatic and broad-band radiation in the ultraviolet range. Results demonstrate that an appropriate encapsulation reduces the effect and variability of space-representative environmental conditions, thus making organic electronics worth further investigation toward their actual employment in aerospace applications.

1. Introduction

Flexible organic electronics is under the lens of the scientific community as a suitable technology for the development of cost-effective devices and circuits by means of low-temperature processes over large areas and flexible substrates,[1,2] which can thus be adapted to any surface, even not flat. To date, several examples of organic electron devices and circuits fabricated onto flexible substrates have been reported in the literature, covering a wide range of application scenarios from electronics, sensors, and optoelectronics.[3–5] A novel frontier for flexible organic electronics could be represented by space applications, in particular those related to the so-called new space economy (NSE), i.e., the rising commercialization in space exploration. NSE deals with different application scenarios, covering a wide range of technologies and costs: for instance, a significant example among recent developments is represented by CubeSats, small satellites that emerged in the space sector in the early 2000s.[6] Their design philosophy differs from the traditional one, dominated by highly reliable components and conservative designs built for durability under extreme environmental conditions of space, featuring redundancies, extensive qualification and performance testing at part, sub-system, and integrated system levels.[7] In CubeSats, low budget and deployment and a subsequent fast delivery are fundamental to ensure their success in the NSE: to this aim, the employment of state-of-the-art commercial off-the-shelf components has been particularly targeted,[8,9] also because the high prices associated with hard-rad (hardening by design and by process) electronics are not affordable. In addition to the low-cost constraint, CubeSat standardized design requests weight- and space-saving requirements. This aspect implies that single devices and systems are designed with the lowest possible way, and that an effective volume and surface occupation is realized. For these reasons, CubeSat technology is a paradigmatic example of how NSE could take advantage of the peculiar properties of organic materials, such as low fabrication costs, relevant flexibility, and overall lightweights. Moreover, flexible organic electronics enhance redundancy, generally very limited in CubeSats applications: the lighter and less expensive they development of electronic circuits, the more of them can be integrated into a single CubeSat, thus further reducing costs related to the improvement of the reliability of a single element.

Despite the possible advantages related to the employment of organic electronics in space applications, this field has been poorly explored. Even if some studies have been reported in literature,[10–15] a general assessment of organic electronics as a technology suitable for space applications is still missing, in particular for what concerns the reliability of organic electronic devices. Reliability represents a vital characteristic of a space system and must be adequately evaluated to ensure the mission objectives. In space applications, electronics must withstand a

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssa.202500381.

DOI: 10.1002/pssa.202500381

severe environment that includes several degradation stresses such as cycling temperature, high-energy radiation, vibrations, vacuum, atomic oxygen, and debris impact,[16] depending on where the devices operate. Taking CubeSat application as an example, devices must be able to face the low Earth orbit (LEO) environment, which usually involves exposure to cycling temperatures in the range of -40 e $+ 85$ °C if mounted inside the satellite or even –120 °C to + 120 °C outside of it. A review of the approaches to thermal robustness for the most important organic semiconducting materials is reported in the work of Lee et al.[17] Only a few studies show the influence of temperatures above 300 K on the pentacene semiconductor.[18] Several studies refer to the thermal stability of the physical and electrical properties of poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS).[19–22] Similarly, radiation hardness is a key parameter to be evaluated for electronics operating in a space environment. A wide spectrum of radiations can affect the performance of electronics in space: in literature, some works reported results on specific tests through gamma-ray irradiation and high-energy protons.[13,23,24] On the other hand, ultraviolet (UV) rays are effective starting from the upper part of the atmosphere and can determine surface erosion and degradation of thermal, electrical, and optical properties. In the presence of contamination, UV radiation can darken materials, induce photodegradation, and damage polymers by either cross-linking (hardening) or chain scission (weakening).[25,26] For organic thin-film-transistors, the near ultraviolet radiation (in the 180 to 400 nm wavelength region) might be a serious concern.[10,27]

In this article, a quantitative evaluation of the influence of environmental conditions representative of LEO space missions on flexible organic field-effect transistors (OFETs) is reported for the first time in the literature. Several all-organic, inkjet-printed devices have been fabricated and subjected to different stress, including prolonged exposure to different temperature values ranging from -20 °C and $+120$ °C, and to broad- and wide-band UV radiation at fixed energy. In both tests, single stresses (temperature or radiation) were chosen not to induce multiple failure mechanisms, which can generally interact and compete in real applications, but are more challenging to interpret. The aim was to recognize the failure mechanism that really dominates the degradation process induced by each stress. Different assemblies are considered: in particular, the influence of an encapsulation layer on electrical performance stability during stress is explored. Even if requirements vary in dependence on the mission (profile and duration, exact orbit, and satellite shielding), a feasibility study can provide a preliminary insight into specific durability and performance of the device in space applications.

2. Results and Discussions

2.1. Structure and Materials

The basic transistor structure is a bottom-gate bottom-contact OFET, fabricated on a 125-μm-thick polyethylene naphthalate (PEN) substrate (**Figure 1**). Specifically, two different OFET configurations, from now on nonencapsulated and encapsulated OFETs, are proposed: the last configuration differs from the previous one for the lamination onto the channel area of a PDMS layer, sealed with a further deposition of Parylene C. The fabrication process is mainly based on large-area techniques: inkjet printing of a commercially available PEDOT:PSS-based ink for gate, source, and drain, chemical vapor deposition (CVD) of Parylene C films for gate insulator, and final device encapsulation. An interdigitated configuration with 10 channels (single length L = 150 μm, single width W = 1 mm) is chosen for source and drain electrodes. A 6,13-Bis(triisopropylsilylethynyl) pentacene (TIPS pentacene) solution was drop-casted on the OFETs channels. All the fabrication process was carried out at low temperatures, with a maximum of 60 °C for inkjet printing. More details on the fabrication process and characterization are reported in the Experimental Section.

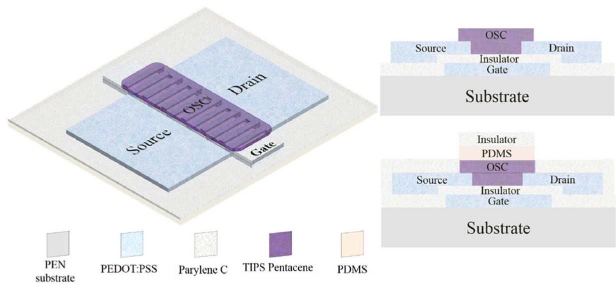

Figure 1. Cartoon and schematic cross sections of the OFET structure with the indication of all materials.

2.2. Electrical Characterization

At first, a complete electrical characterization was carried out on all fabricated devices. **Figure 2** shows typical output and transfer characteristics of nonencapsulated and encapsulated OFETs. As already demonstrated in previous works for very similar OFETs,[28,29] such kind of devices can be operated at low voltages (not exceeding 5 V) with a quasizero threshold voltage. Fundamental parameters as threshold voltage and charge carrier mobility, were extracted from transfer characteristic curves, using the basic approach of linearization of the square root of I_D.[30] Average and 1-σ values of these parameters have been evaluated in a set of 15 pristine encapsulated and 15 pristine nonencapsulated devices. Threshold voltage is (0.98 ± 0.08) V for nonencapsulated devices, and (1.9 ± 0.1) V for encapsulated devices: this shift is related to the addition of the encapsulation layer but does not significantly compromise device performance. Charge carrier mobility (capacitance per unit area of 9.5 nF cm^{-2}) has been evaluated in (0.13 ± 0.01) and (0.19 ± 0.02) $cm^2 V^{-1} s^{-1}$ for nonencapsulated and encapsulated devices, respectively.

Variation of these parameters in time was monitored through aging tests performed in ambient conditions. Specifically, electrical measurements were recorded at regular intervals for a period of 500 days on 15 encapsulated and 15 nonencapsulated OFETs. Interestingly, the obtained results show that the choice of a flexible encapsulation layer plays an important role in reducing variability in device performances over time and ensures the stability of several electrical parameters, such as threshold voltage, OFF current, and subthreshold slope, while being less effective in minimizing the degradation of charge carrier mobility. Nonetheless, since devices will operate in reduced oxygen and humidity conditions, keeping a certain degree of flexibility and reduced weight can be considered preferential to the employment of more efficient, but rigid and heavy encapsulation. Details on the obtained results

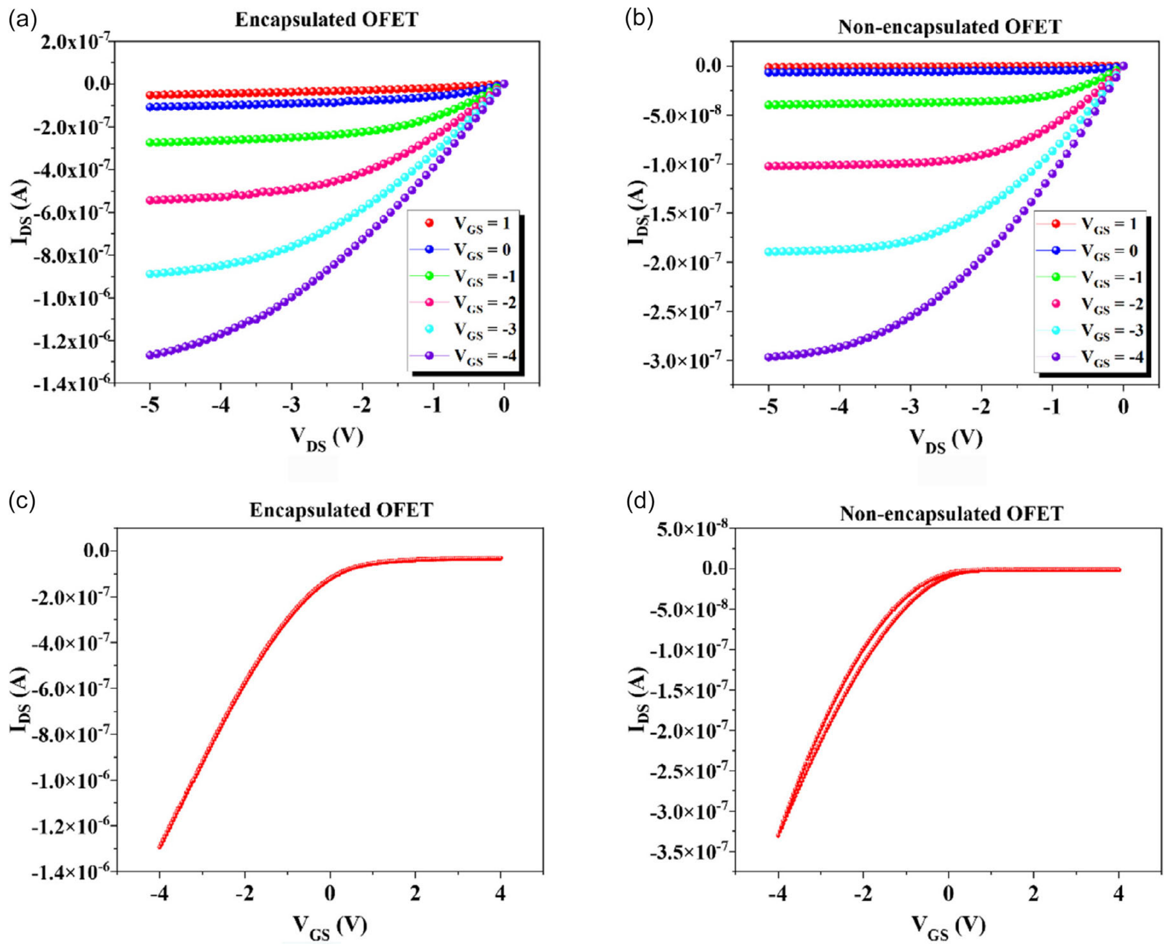

Figure 2. Typical output a,b) and transfer characteristic curves c,d) of encapsulated a,c) and nonencapsulated b,d) OFETs. Transfer characteristics were measured with $V_{DS} = -5$ V.

are reported in Supporting Information (Figure S1, Supporting Information).

2.3. Temperature Stress Test

In order to verify functionality and withstand of the device over a temperature range representative for the operation scenario, a step stress test in a range of temperatures between +125 °C and −20 °C has been performed. Specifically, four different devices for both kinds of OFETs have been tested with the following test protocol, applied for each selected temperature value: 1) transfer characteristic acquisition, 2) temperature exposition for a period of 90 min, 3) waiting a settling time of 60 min, 4) transfer characteristic acquisition immediately after the settling time and 5) after 24 h, in order to verify irreversible degradation of device performances.

Threshold voltage and mobility have been evaluated for each device before stress test, after a settling time of 1 and 24 h (before the application of the next temperature) from the stress test. The exposure time (90 min) was chosen because a satellite takes approximately that time to circle the low Earth orbit. Results are reported in **Figure 3**. In particular, Figure 3a shows the average absolute variation $\Delta V_{TH} = V_{TH,i} - V_{TH,0}$, where $V_{TH,i}$ is the threshold voltage after 1 or 24 h from the stress application, and $V_{TH,0}$ is the one extrapolated before the temperature exposition. In the case of nonencapsulated samples, a decrease of the threshold voltage (negative ΔV_{TH}) has been recorded at lower temperatures (<25 °C), while an increase of this value (positive ΔV_{TH}) has been obtained for temperatures in the range 25°–100 °C. As shown in the graph of Figure 3a, such variations persist also after 24 h. As regards encapsulated devices, it is possible to observe a general increase in the threshold voltage until a breaking temperature of about 100 °C. For larger temperatures, encapsulated devices underwent a dramatic variation of the threshold voltage, related to a probable degassing of the PDMS layer that partially dissolved the semiconductor film, or the release of residual solvent in the PDMS. These physical mechanisms must be further investigated, also considering that degassing of materials is a serious issue in space applications, since it can cause instrumentation contamination. A limitation on the maximum operative temperature of this class of devices is thus derived. However, in this case, the variation results are generally smaller than the one observed in nonencapsulated ones (in a range of 400 mV), and it is substantially recovered within 24 h for temperature values below 50 °C. Similarly, Figure 3b shows the relative mobility variation $\Delta\mu/\mu = (\mu_i - \mu_0)/\mu_0$, where μ_i is the mobility after

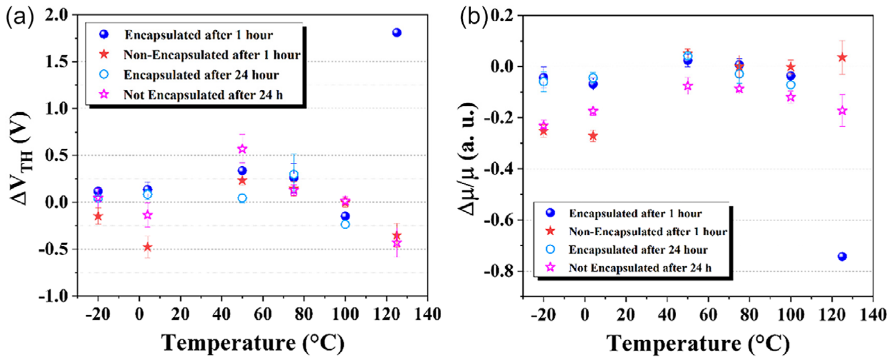

Figure 3. Threshold voltage absolute variation a) and mobility relative variation b) with temperature for transistors encapsulated and nonencapsulated.

1 or 24 h of settling time, and μ_0 is the mobility before the stress test. In particular, nonencapsulated OFETs are characterized by a significant decrease in the mobility for low temperatures, while for temperatures exceeding 0 °C, a clear dependence on applied temperature is missing. After 24 h, the mobility reduction observed for temperatures lower than 0 °C is kept, while a general mobility decrease is observed for the other temperatures considered. Encapsulated OFETs' mobility shows a lower variability with variations within a tolerance range of a maximum 7% until the breaking temperature of 125 °C, which causes a reduction of about 80%, i.e., the device failure.

To complete this analysis, a set of encapsulated and nonencapsulated devices was subjected to repeated abrupt temperature variations between +100 °C and −20 °C, in which the extreme temperature values were kept for 30 min, i.e., for a time characteristic of satellite exposure toward or against the Sun. Results, described in Supplementary Information (Figure S2, Supporting Information and related text), substantially resemble those obtained in step stress experiments, but provide a deeper insight into the robustness of encapsulated devices to temperature variations during satellite orbit.

2.4. UV Radiation Stress Test

In order to verify OFETs' stability during exposure to UV radiation, stress tests have been performed on different sets of devices with and without an encapsulation layer in two different scenarios. At first, radiation at fixed wavelengths in the deep UV range (250, 310, and 360 nm) was employed to evaluate possible effects of specific wavelengths on device performances. An exposure period of 30 min was chosen to be representative of a significant portion of the CubeSat orbital period; the power density was fixed to 0.1 mWcm^{-2}, following indications for UV testing in a space environment.[31,32] Specifically, for each kind of transistors and for each radiation at a different wavelength, the following test protocol has been applied: 1) transfer characteristic acquisition, 2) exposure to radiation for 30 min, 3) settling time of 24 h, and 4) acquisition of a post-stress transfer characteristic.

Results are reported in **Figure 4**: average and 1-σ error bars are calculated over four devices. Interestingly, a radiation of 250 nm, which falls in the UV-C band (thus being characterized by the higher ionization capability), is capable of inducing a substantial failure of nonencapsulated devices, with a large threshold voltage variation and variability (6.7 ± 1.0 V) and a reduction of charge carrier mobility larger than 90%. It is noteworthy that the same radiation is still capable of inducing a permanent variation of the threshold voltage of encapsulated devices, but to a lower extent (1.2 ± 0.5 V), and with less significant variation of the mobility (1%). This shows the potential of the encapsulation layer to prevent ionizing species from interacting with the organic semiconductor, thus avoiding failure mechanisms such as charge trapping mechanism (behind threshold voltage variations) and oxidation (which causes the mobility reduction). Moreover, absorption of UV radiation for low wavelengths in both PDMS and Parylene C could be taken into account. When the wavelength increases, radiation falls in the UV-B band, characterized by a lower

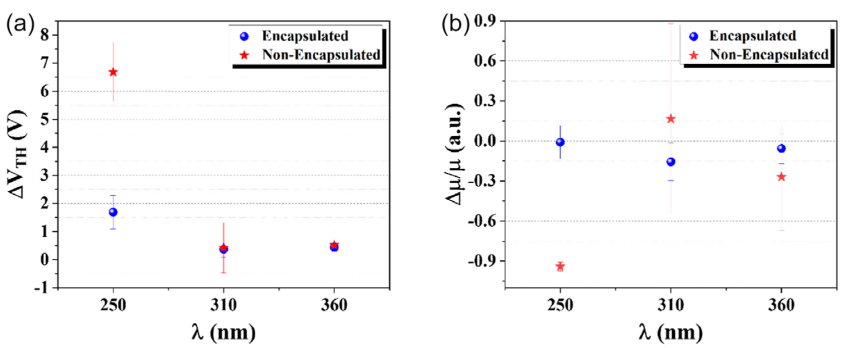

Figure 4. Threshold voltage absolute variation a) and mobility relative variation b) with radiation for encapsulated and nonencapsulated transistors. Each radiation stress test lasts 30 min. Parameters are extrapolated from measurements performed before and after 24 h from the exposition.

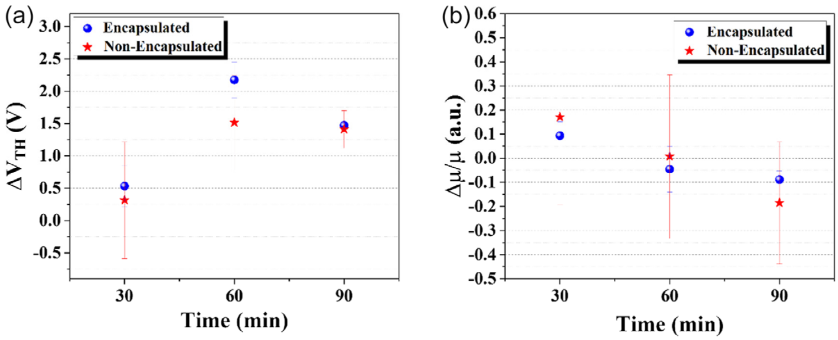

Figure 5. Threshold voltage absolute variation a) and mobility relative variation b) with broad spectrum radiation for encapsulated and nonencapsulated transistors for different exposure times. Parameters are extrapolated from measurements performed before and after 24 h from the exposition.

energetic content; therefore, the difference between encapsulated and nonencapsulated devices is less relevant for both threshold voltage and mobility variation, even if a significantly larger variability of these two parameters has been recorded for nonencapsulated devices. For less energetic radiation, transient effects have been observed by recording transfer characteristic curves immediately after the exposure to the radiation (Figure S3 in the Supporting Information), with a similar extent in both kinds of devices but with a lower variability for encapsulated ones. This information is also useful for a correct electronic design, since a robust approach to compensate temporary variation of device parameters should be employed.

Even if fixed wavelengths are useful for determining which energies are related to specific effects on transistor performances, radiation with a broader spectrum in the UV range is far more representative for real application scenarios. For this reason, a mercury lamp with a broad emission spectrum and a fixed power density of 0.1 $mWcm^{-2}$ was employed. Different exposure times (30, 60, and 90 min) within the orbital period of the CubeSat have been chosen. Results are reported in **Figure 5**: in these conditions, the difference between encapsulated and nonencapsulated devices is less significant than the one observed for the exposure to monochromatic radiation. Threshold voltage generally increases, thus demonstrating that electron trapping mechanisms are activated. A slight decrease in mobility is also observed, not exceeding the maximum recorded for high ionizing UV radiation. Nonetheless, the variability between different nonencapsulated devices is significantly larger than that one recorded for encapsulated ones. This has also been further confirmed by evaluating transient effects in a 30 min exposure (Figure S4 in Supporting Information) on pristine devices: the behavior of encapsulated devices immediately after the exposure was coherent with the one observed in previous tests, while nonencapsulated devices underwent a slight average increase of mobility but with a large tolerance interval. Therefore, the reliability enhancement of OFET performances related to the employment of an encapsulation layer has been demonstrated in both short and long-time operation.

3. Conclusion

This paper investigates the stability of OFETs exposed to extreme temperatures and UV radiation intervals representative of CubeSat operational conditions. The electrical properties of devices with and without encapsulation were investigated. The results obtained show that encapsulation plays an important role in reducing the variability of electrical performances and mitigating the device degradation with thermal and UV stress. Under temperature step stress, the encapsulation preserves the electrical performance of the devices until a breaking temperature of about 100 °C. After this point, it seems to contribute to the final degradation process, thus posing a limitation to its possible employment outside the satellite, while being compatible for application development inside the satellite. Nonetheless, the encapsulation layer resulted in effective protection of the devices from UV radiation, assuring better and more stable performances at higher ionization radiation. Therefore, a further optimization of the thermal stability of the encapsulation layer would represent a follow-up research for a complete exploitation of the proposed technology. In the same way, it is important to underline that the current study only partially covers the stress factors faced when orbiting LEO, and that other specific conditions (e.g., the effects occurring in thermal-vacuum environment or in the presence of atomic oxygen) still need to be investigated. Moreover, taking into account more energetic radiation sources, such as X-rays and high-energy particles, is fundamental for both LEO and, most of all, deep space applications. Consequently, the present results are not conclusive evidence, thus insufficient to thoroughly validate the degradation induced by space-related stress factors in harsh space conditions. However, the stability and degradation of the device and its materials retain their significance, and this work is paving the way toward a more detailed reliability evaluation of organic electronics operating in severe conditions, such as space applications.

4. Experimental Section

Device Fabrication: All bottom-gate bottom-contact OFETs were fabricated on a 125-μm-thick PEN substrate. A Dimatix Materials Printer DMP2830 (Fujifilm Dimatix) and a 16-nozzle cartridge with a single drop volume of 1 pL (DMC11601, Fujifilm Dimatix) were employed for the inkjet printing steps. Gate electrodes were inkjet-printed directly on the PEN substrate with a commercially available PEDOT:PSS-based ink (PJET HC, Heraeus, Germany). The ink was sonicated in an ultrasound bath for 30 min and subsequently filtered with a 0.45 μm PTFE filter prior to filling the cartridge. Specifically, printing was performed using a custom-designed waveform (Figure S5 in Supporting Information), three nozzles with a firing voltage of 30 V were selected, a drop spacing of 15 μm was set, and the temperature of the printer platen was maintained at 60 °C. A PDS 2010 Labcoater 2 (Specialty Coating System) was used for the CVD of the gate insulator, which is a 250-nm-thick Parylene C film. Interdigitated electrodes were inkjet-printed directly on the Parylene C surface without any surface treatment, employing a single nozzle of the same PEDOT:PSS-filled cartridge ink and the same printing parameter described for gate patterning. A curing step over a hot plate at 90 °C for 15 min was performed as post-processing of the source and drain. Subsequently, an ethylene glycol (Sigma–Aldrich) layer was deposited on the interdigitated structure by inkjet printing employing two nozzles of a cartridge with a single drop volume of 10 pL (DMC11601, Fujifilm Dimatix). Finally, a TIPS pentacene (Sigma–Aldrich) solution (1.5% in anisole anhydrous) was drop-casted on the OFETs channels at room temperature. The structure of a set of devices (encapsulated OFETs) was completed with an encapsulation layer, consisting of a 40 μm-thick polydimethylsiloxane (PDMS, Sylgard 186, Dow Inc.) film, and of a 2 μm-thick Parylene C capping layer subsequently deposited by CVD. Lamination was performed by hand-alignment of the PDMS layer cut out from a spin-coated film over the transistor's channel area. A picture showing an example of a 16-OFET matrix and a morphological characterization of the organic semiconductor area by atomic force microscopy (AFM) is reported in Figure S4 in the Supporting Information. AFM imaging reports typical morphology of TIPS pentacene, characterized by elongated crystalline domains with an average thickness of about 100 nm, thus demonstrating that material stacking is compatible with correct semiconductor crystallization.

Electrical Characterization: All electrical characterizations were carried out in ambient conditions at room temperature with a Keithley 2636 SourceMeter and a custom-made MATLAB software.

Morphological Characterization: AFM measurements were obtained by means of a SPM SOLVER PRO by NT-MDT in semi-contact mode using NT-MDT NSG01 tips.

Optical Characterization: The optical irradiation tests were performed by using a Laser-driven Xenon lamp (EQ-99X) with a final bandwidth of about 1 nm, the average optical power:1 mW nm^{-1} from 200 to 2000 nm. Band pass filters were utilized to define the excitation wavelength: Hg01-254-25 (Semrock Inc), 10BPF310 (Newport), and 10BPF360 (Newport) for emission at 254, 310, and 360 nm, respectively. Broadband UV irradiation has been performed with an ultrahigh vacuum Mercury lamp (Model 6285, 500 W), with an IR cut-off filter to avoid excitation in the IR region and thermal irradiation. The optical light intensity has been monitored with a 1918-C- Newport Optical Power Meters. All tests were conducted with irradiation coming from above the encapsulating layer.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work has been funded by "Fondazione di Sardegna" under the project "ARGOSAT – Microsatellite cluster for the observation of optical transients in Astronomy", CUP: F74I19001070007.

Open access publishing facilitated by Universita degli Studi di Cagliari, as part of the Wiley - CRUI-CARE agreement.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Giulia Casula: data curation (lead); formal analysis (equal); methodology (equal); validation (equal); visualization (equal); writing—original draft (lead). **Pier Carlo Ricci**: formal analysis (equal); methodology (equal); writing—original draft (equal). **Piero Cosseddu**: formal analysis (equal); methodology (equal); writing—original draft (equal). **Giovanna Mura**: conceptualization (equal); data curation (equal); formal analysis (equal); funding acquisition (lead); investigation (equal); methodology (equal); project administration (equal); supervision (equal); writing—original draft (equal). **Stefano Lai**: data curation (equal); formal analysis (equal); investigation (equal); methodology (equal); project administration (equal); supervision (equal); validation (equal); visualization (equal); writing—original draft (equal).

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

cubeSats, flexible printed electronics, organic field-effect transistors, thermal stability, UV radiation

Received: May 7, 2025
Revised: July 31, 2025
Published online: August 29, 2025

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