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Inductor Losses Estimation in DC-DC Converters by Means of Averaging Technique

Andrea Mocci, Andrea Lai, Alessandro Serpi, Ignazio Marongiu and Gianluca Gatto
Department of Electrical and Electronic Engineering, University of Cagliari, Cagliari 09123, Italy

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Abstract: A suitable inductor modeling for power electronic DC-DC converters is presented in this paper. It is developed with the aim of improving inductor losses estimation achievable by averaged models, which inherently neglect inductor current ripple. In order to account for its contribution to the overall inductor losses, an appropriate parallel resistance is thus enclosed into the inductor model, whose value should be chosen in accordance with the DC-DC converter operating conditions. This allows the development of improved averaged models of DC-DC converters, especially in terms of power losses estimation. The effectiveness of the proposed modeling approach has been validated through a simulation study, which refers to the case of a boost DC-DC converter and is performed by means of a suitable circuit simulator designed for rapid modelling of switching power systems (SIMetrix/SIMPLIS).

Key words: Averaging technique, current ripple, DC-DC power converters, modeling.

1. Introduction

At the present time, power electronic DC-DC converters are widely and successfully employed as the most suitable interface for supplying several electric and electronic devices in a number of applications, ranging from consumer electronics to electric vehicles. Due to such a widespread diffusion, both academic and industrial research are focused on further improving their performances by suggesting novel converter topologies and the employment of recently-developed semiconductor devices (MOSFETs, IGBTs, diodes, etc.), as well as of high-performance control and modulation strategies.

The efficiency of power electronic DC-DC converters surely represents one of their most important performance indexes. This should be maximized in order to both guarantee energy saving and limit temperature increase due to converter losses. This last aspect is particularly important during the design stage, i.e., an accurate losses estimation could enable an optimal design of heat-sinks, which, in turn, leads to a reduction of the overall cost, size and weight of the converter.

Accurate modeling of power electronic DC-DC converters thus represents a key aspect, especially in supporting the design stage. In fact, these models allow accurate estimations of converter performances and efficiency, on the basis of which the design of power electronic converters can be successfully optimized. For this purpose, a number of modeling approaches have been proposed in Refs. [1, 2], among which the averaging technique seems to be one of the most promising methods. It enables a ripple-free representation of power electronic converters, appropriately removing the non-linearity related to semiconductor devices. Thus, averaging technique is widely employed for estimating power electronic DC-DC converter performances, as well as for designing appropriate voltage and current control loops [3-6].

Several averaged models of power electronic DC-DC converters have been proposed Refs. [7-14], many of which, however, neglect parasitic elements of

Corresponding author: Gianluca Gatto, associate professor, research fields: power electronics, electrical machine and drives, electromagnetic compatibility. E-mail: gatto@diee.unica.it, alessandro.serpi@unica.it.

converter components, as well as the effects of switching phenomena. Such approximations significantly ease model implementation, but prevent accurate estimations of current and voltage evolutions, as well as the accomplishment of sound power losses and efficiency analysis. Particularly, inductor current ripple is almost always neglected, leading to mismatches in averaged inductor current and power losses estimations, especially when relatively low switching frequency is used [15-17].

In this context, this paper presents a suitable inductor model for power electronic DC-DC converters. It consists not only of an equivalent series resistance and an ideal inductance, but it also includes an additional parallel resistance with the aim of appropriately accounting for inductor losses due to current ripple. Based on this, an improved averaged model is achieved [18, 19], which enables a very good estimation of the overall inductor losses. This is proved by means of a simulation study, which is performed by means of suitable circuit simulator designed for rapid modelling of switching power systems (SIMetrix/SIMPLIS) and refers to the case of a boost DC-DC converter.

2. Boost Mathematical Models

The schematic representation of a boost DC-DC converter is depicted in Fig. 1. It can be seen that, it is made up mainly of an inductor L and a capacitor C, which are appropriately coupled by means of a switch S and a diode D. The boost DC-DC converter is assumed to be supplied by a generic DC source v_{in}, whereas i_0 denotes the load current.

2.1 Boost Operating Principle

In order to achieve the continuous-time model of the boost converter, reference is made to Fig. 2, which summarizes its different operating states. Assuming that, the boost converter is in the ON state at first, the input source charges L, while the load is supplied by C. Over this operating condition, S is modeled by means

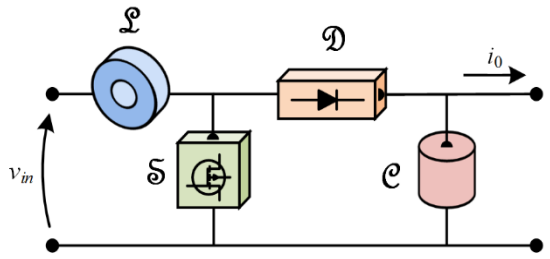

Fig. 1 Equivalent representation of a boost converter.

of an equivalent voltage source (w_s) and a parasitic series resistance (r_s), whereas D is reverse-biased.

As soon as the switch command signal (α) is set low, the Turn-OFF operating state occurs. Thus, the voltage across sand D gradually increases, until the latter is forward-biased. This phenomenon lasts t_{rv}, which is the voltage rise time. Subsequently, diode current (i_D) gradually increases, while switch current (i_S) decreases to zero, which is accomplished over the current fall time (t_{fi}).

Once Turn-OFF is accomplished, the OFF state occurs, in correspondence of which both the input source and the inductor supply the load and recharge the capacitor at the same time. Over this operating states, D is modelled by means of an equivalent voltage source (w_D) and a corresponding series resistance (r_D). It is worth noting that, if the inductor current becomes zero during the OFF state, the diode turns off, leading to DCM (discontinuous conduction mode). However, such an operating mode is not considered in this paper. It is assumed that, the boost converter always operates in CCM (continuous conduction mode), i.e., the inductor current is always greater than zero at the end of the OFF state.

When the switch command signal is set to high, Turn-ON occurs. Hence, i_D gradually decreases at first, while i_S increases. As soon as i_D becomes zero after the current rise time (t_{ri}), D is reverse-biased, thus the voltages across S and D both decrease until the ON state is restored. This is achieved after t_{fv}, which is the voltage fall time.

In conclusion, based on the previous considerations, it can be stated that, the boost operating principle

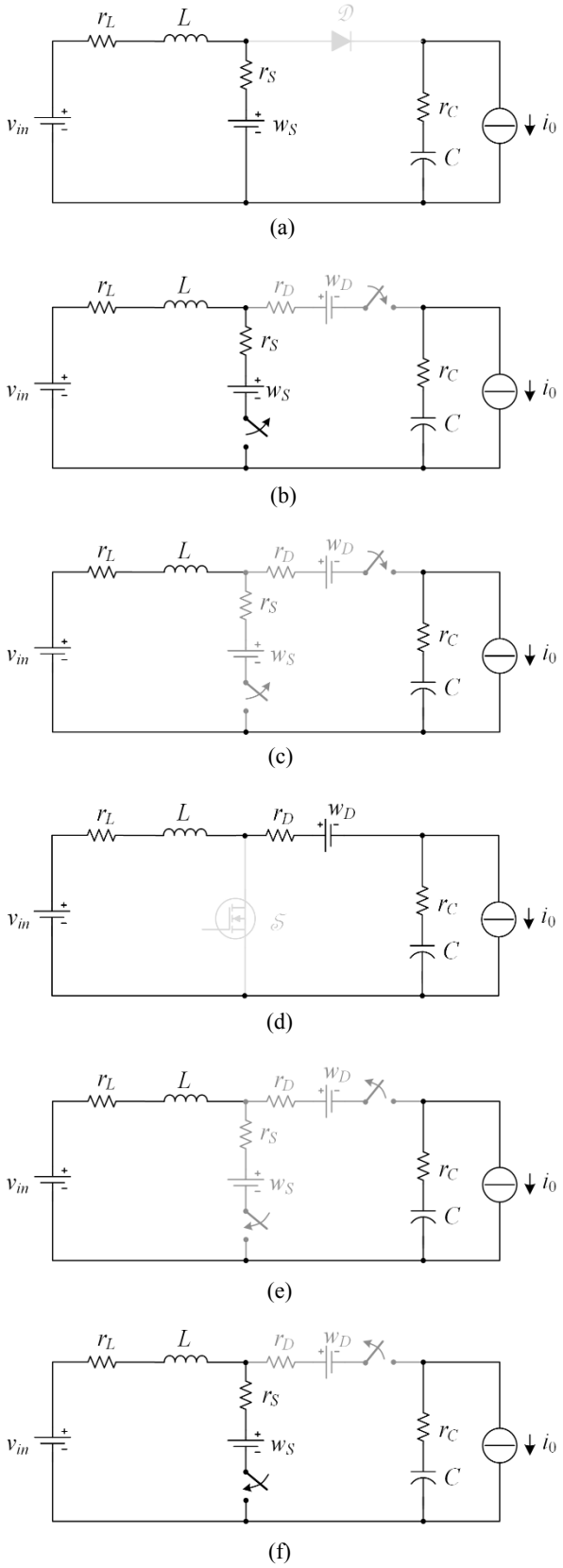

Fig. 2 Operating states of the boost DC-DC converters: (a) ON, (b), (c) Turn-OFF, (d) OFF and (e), (f) Turn-ON.

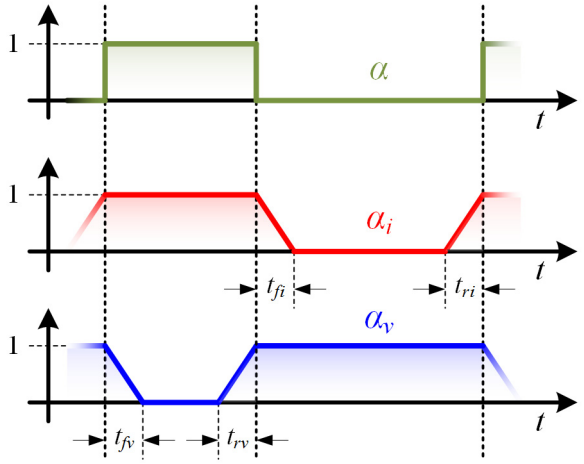

Fig. 3 The switching signals α (green), α_i (red) and α_v (blue).

consists of an appropriate sequence of ON and OFF states, which lasts in accordance with the imposed duty cycle. It is worth noting that, the transition between these states determines corresponding transitions of voltage and current across both *S* and *D*. This requires an accurate modelling in order to account for converter losses due to the switching phenomenon, as detailed in the following sub-section.

2.2 Continuous-Time Model

In order to account for voltage and current transitions over both Turn-OFF and Turn-ON, it is possible to introduce two signals, α_v and α_i, whose evolutions over a generic sampling time interval (T_s) can be defined as in Fig. 3. Particularly, α_v accounts for voltage fall and rise phenomena across the switch, whereas α_i accounts for the corresponding rising and falling current.

Hence, based on both α_i and α_v, it is possible to determine the continuous-time model of the boost converter as

$$\dot{x} = Ax + Bu + Cw \tag{1}$$

where, x denotes the state vector, whereas u and w are the input vectors. Particularly, x consists of the capacitor voltage (v_C) and inductor current (i_L), whereas u accounts for v_{in} and i_0. Regarding w, it takes into account the voltage drops occurring over *S* and *D*, which are denoted by w_S and w_D, respectively:

$$x=\begin{bmatrix} v_C \\ i_L \end{bmatrix},\quad u=\begin{bmatrix} v_{in} \\ i_0 \end{bmatrix},\quad w=\begin{bmatrix} w_S \\ w_D \end{bmatrix} \tag{2}$$

In conclusion, referring to Eq. (1), the matrices A, B and C all depend on both α_i and α_v as:

$$A=\begin{bmatrix} 0 & \dfrac{(1-\alpha_i)}{C} \\ -\dfrac{\alpha_v}{L} & -\left(\dfrac{r_L}{L}+(1-\alpha_v)\dfrac{r_S}{L}+(1-\alpha_i)\dfrac{r_D+r_C}{L}\right) \end{bmatrix}$$
$$B=\begin{bmatrix} 0 & -\dfrac{1}{C} \\ \dfrac{1}{L} & \alpha_v\dfrac{r_C}{L} \end{bmatrix},\quad C=\begin{bmatrix} 0 & 0 \\ -\dfrac{(1-\alpha_v)}{L} & -\dfrac{\alpha_v}{L} \end{bmatrix} \tag{3}$$

where, r_L represents the parasitic series resistance of the inductor, whereas r_C denotes that of the capacitor.

2.3 Averaged Model

Based on Eq. (1) and due to the linear time evolution of both α_v and α_i, the averaged model of the boost converter can be achieved as:

$$\dot{\bar{x}}=\bar{A}\,\bar{x}+\bar{B}\,u+\bar{C}\,w \tag{4}$$

where, $\bar{x}$ denotes the averaged state vector, whereas $\bar{A}$, $\bar{B}$ and $\bar{C}$ are the averaged system matrices. These can be determined directly from A, B and C by replacing both α_v and α_i with their corresponding averaged values, which can be computed as:

$$\bar{\alpha}_i=\bar{\alpha}+\frac{t_{ri}+t_{fi}}{2}f_S\quad,\quad \bar{\alpha}_v=1-\bar{\alpha}+\frac{t_{rv}+t_{fv}}{2}f_S \tag{5}$$

$\bar{\alpha}$ and f_S being the ideal duty cycle and the switching frequency, respectively.

Based on Eq. (4), it is thus possible to perform a power analysis of the boost converter by means of Eq. (6):

$$\bar{x}^T Q\,\dot{\bar{x}}=\bar{x}^T Q\left(\bar{A}\,\bar{x}+\bar{B}\,u+\bar{C}\,w\right) \tag{6}$$

in which

$$Q=\begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix} \tag{7}$$

In particular, the left-side term of Eq. (6) represents the power drawn or delivered by the inductor and the capacitor, whereas right-side terms account for all converter losses, as well as for input and output powers. Among these, Joule losses of the inductor is expressed as:

$$P_{J,L}=r_L\,\bar{i}_L^2 \tag{8}$$

Therefore, it can be stated that, Eq. (8) does not account for inductor losses due to current ripple occurring on i_L because this is inherently neglected by Eq. (4). Although this approximation does not impair the effectiveness of both Eq. (4) and Eq. (6) significantly, it may introduce detectable power balance mismatches, especially when relatively low switching frequency is employed. For this reason, an improved inductor modelling is suggested, which is presented in the following section.

3. Proposed Inductor Modeling

The inductor model presented in this paper aims to provide a more accurate estimation of inductor losses than that achievable by Eq. (8). Hence, reference can be made to the steady state evolution of the inductor current shown in Fig. 4. Particularly, it can be assumed that, i_L varies linearly over both the ON and the OFF states. In addition, Turn-OFF and Turn-ON can be also neglected, meaning that, both α_v and α_i equal α. Consequently, $P_{J,L}$ should be computed as:

$$P_{J,L}=r_L\,\bar{i}_L^2+\frac{1}{12}r_L\,\Delta i_L^2 \tag{9}$$

where, Δi_L denotes the inductor current ripple, which can be expressed as:

$$\Delta i_L\cong\bar{\alpha}\frac{v}{L f_s} \tag{10}$$

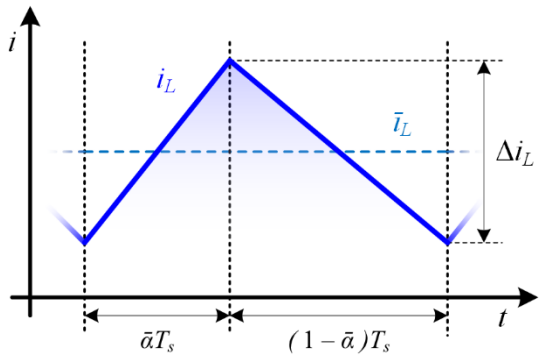

Fig. 4 Steady-state inductor current evolution.

Considering now the capacitor losses provided by Eq. (6) and still assuming that, both α_v and α_i equal α, they can be expressed as:

$$P_{J,C} = \bar{\alpha}\left(1-\bar{\alpha}\right) r_C \bar{i}_L^2 \tag{11}$$

Therefore, it can be stated that, Eq. (6) properly accounts for capacitor current ripple, even at steady state operation. This occurs because the capacitor current is not a state variable, thus it varies within T_s even if its averaged value is constant at zero. Consequently, since the same phenomenon occurs also on v_L, this seems to be a suitable candidate for accounting for inductor losses due to current ripple rather than i_L.

Based on the previous considerations, the inductor model shown in Fig. 5 has been proposed. In particular, an additional parallel resistance r_P is appropriately introduced in order to exploit v_L variations over T_s, even at steady state operation. As a result, the inductor voltage equation is:

$$v = r_L\, i + \frac{\mathrm{d}\, i_L}{\mathrm{d}\, t} \tag{12}$$

where, v and i denote the overall inductor voltage and current, respectively. Particularly, i can be further expressed as:

$$i = i_L + i_P, \quad i_P = \frac{L}{r_P}\frac{\mathrm{d}\, i_L}{\mathrm{d}\, t} \tag{13}$$

Consequently, based on both Eq. (12) and Eq. (13), inductor losses can be computed as:

$$P_{J,L} = r_L\, \bar{i}_L^2 + \frac{\left(L f_s\right)^2}{r_L + r_P}\frac{\Delta i_L^2}{\bar{\alpha}\left(1-\bar{\alpha}\right)} \tag{14}$$

Thus, by imposing that Eq. (14) matches with Eq. (9), r_P should be chosen as:

$$r_P = -r_L + \frac{12}{\bar{\alpha}\left(1-\bar{\alpha}\right) r_L}\left(L f_s\right)^2 \tag{15}$$

Therefore, based on Eq. (15), it can be stated that, a good estimation of inductor Joule losses requires that r_P varies with $\bar{\alpha}$, as highlighted in Fig. 6. However, it is worth noting that, Fig. 6 also reveals that, r_P is almost constant within a wide $\bar{\alpha}$ range, centred at 0.5. Since these operating conditions are quite common in the majority of applications, r_P can be assumed constant and equal to its minimum value, which is achieved when $\bar{\alpha}$ equals 0.5:

$$r_P \approx -r_L + \frac{48}{r_L}\left(L f_s\right)^2 \tag{16}$$

Referring to Eq. (16), it is also worthy of note that, r_P depends on the square values of both L and f_s. Particularly, as r_P increases with either L or f_s, i_P decreases in accordance with Eq. (13) and becomes negligible compared to i_L. This is justified by the fact that when large inductance and/or switching frequency is employed, inductor current ripple becomes negligible, as well as its contribution to inductor losses.

Hence, based on both Eq. (12) and Eq. (13), it is thus possible to determine a more accurate mathematical model of the boost converter, which can be still expressed by Eq. (1), but defining A, B and C as:

$$\begin{aligned}
A &= \begin{bmatrix} -\dfrac{\left(1-\alpha_i\right) r_P}{\rho_C C} & \dfrac{\left(1-\alpha_i\right) r_P}{\rho_C C} \\ -\dfrac{\alpha_v r_P}{\rho_L L} & -\dfrac{r_P\left(\rho_L - r_P\right)}{\rho_L L} \end{bmatrix} \\
B &= \begin{bmatrix} \dfrac{\left(1-\alpha_i\right)}{\rho_C C} & -\dfrac{\rho_C - \left(1-\alpha_i\right) r_C}{\rho_C C} \\ \dfrac{r_P}{\rho_L L} & \dfrac{\alpha_v r_C r_P}{\rho_L L} \end{bmatrix} \\
C &= \begin{bmatrix} 0 & -\dfrac{\left(1-\alpha_i\right)}{\rho_C C} \\ -\dfrac{\left(1-\alpha_v\right) r_P}{\rho_L L} & -\dfrac{\alpha_v r_P}{\rho_L L} \end{bmatrix}
\end{aligned} \tag{17}$$

where:

$$\begin{aligned}
\rho_C &= r_P + r_L + (1-\alpha_i)(r_D + r_C) \\
\rho_L &= r_P + r_L + (1-\alpha_i)(r_D + r_C) + (1-\alpha_v) r_S
\end{aligned} \tag{18}$$

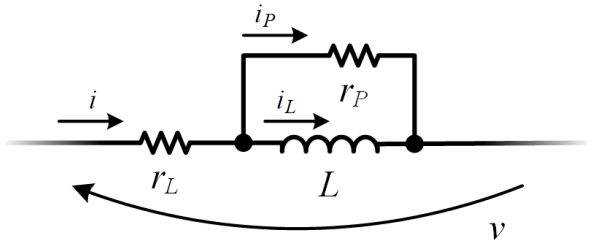

Fig. 5 The proposed inductor model.

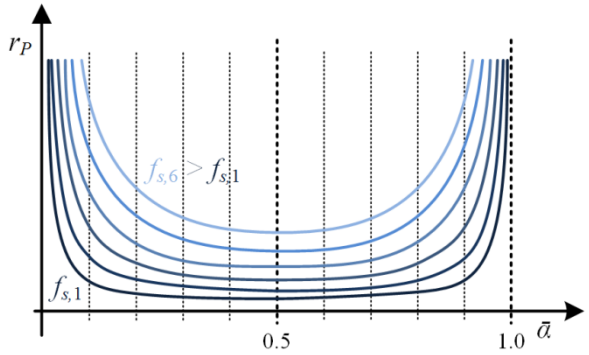

Fig. 6 The r_P evolution with $\bar{\alpha}$ for increasing switching frequency (from dark to light blue).

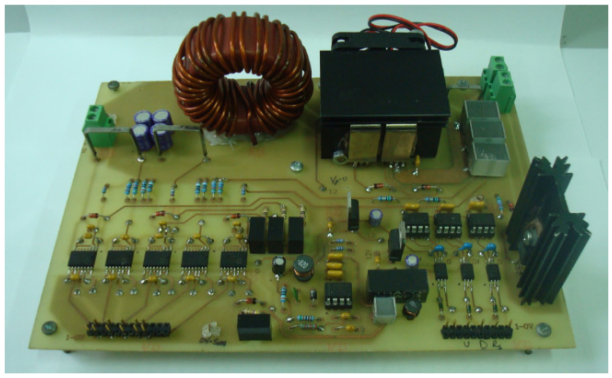

Fig. 7 Prototype of the boost DC-DC converter considered for simulations.

In conclusion, based on both Eq. (1) and Eq. (12), an improved averaged model of the boost converter can be defined. This can be still expressed by Eq. (4), but due to the non-linearity introduced by Eq. (12), $\bar{A}$, $\bar{B}$ and $\bar{C}$ have to be computed as:

$$\bar{M} = \frac{1}{T_s}\int_0^{T_s} M \, \mathrm{d}t, \quad M \in \{A, B, C\} \tag{19}$$

4. Simulation Analysis

In order to validate the proposed inductor modelling approach, a simulation study has been carried out by SIMetrix/SIMPLIS. Particularly, SIMPLIS is a circuit simulator designed for rapid modelling of switching power systems. It enables very fast simulation times by modelling devices using a series of straight-line segments rather than solving non-linear equations. As a result, SIMPLIS can characterize a complete system as a cyclical sequence of linear circuit topologies. This is particularly suitable for switching power systems, where the semiconductor devices operate as switches [20-23].

4.1 Simulation Setup

Simulations have been performed on a boost converter, whose components have been modeled based on the prototype shown in Fig. 7. This is a bidirectional boost converter equipped with two MOSFETs (IRFZ44E), whose main specifications are resumed in Table 1. Whereas, the inductor is made up of an appropriate toroidal core (T200-2B), whose main details are reported in Table 2. Particularly, the core material has been chosen in order to assure a constant inductance within the overall inductor current variation range, as well as negligible core losses. The core is wounded with a copper wire in order to achieve the desired inductance value, as still detailed in Table 2. Regarding the output stage, three film capacitors have been chosen (B32562J1106K), whose main details are briefly resumed in Table 3. Whereas the overall boost converter specifications are summarized in Table 4, together with rated input voltage and load current.

Table 1 MOSFET electric specifications*.

Electric parameters	Value	Unit
Drain-to-source breakdown voltage	60	V
Continuous drain current	48	A
Static drain-to-source on-resistance	23	mΩ
Diode forward voltage	0.6	V
Timing parameters	**Value**	**Unit**
Turn-On delay time	12	ns
Rise time	60	ns
Turn-OFF delay time	70	ns
Fall time	70	ns

* At specific operating conditions provided in the datasheet.

4.2 Simulation Results

Simulations are firstly carried out by setting the switching frequency and the duty cycle to 40 kHz and 0.4, respectively. Whereas the load has been varied from 40% to 100% the rated one. The corresponding inductor losses evolution is depicted in Fig. 8. These have been measured by means of specific probes of the SIMetrix/SIMPLISlibrary. It can be seen that,

Table 2 Inductor design specifications.

Geometric parameters	Value	Unit
Outer diameter	50.8	mm
Inner diameter	31.8	mm
Height	25.4	mm
Magnetic parameters	**Value**	**Unit**
Length	13	cm
Area	2.32	cm^2
Volume	30	cm^3
Inductance density	21.8	nH/N^2
Winding parameters	**Value**	**Unit**
Wire diameter	1.83	mm
Cross sectional area	2.63	mm^2
Turns	33	-

Table 3 Capacitor main specifications.

Electric parameters	Value	Unit
maximum DC voltage	100	V
maximum AC voltage*	63	V
capacitance	10	μF

* RMS (root mean square) value, $f \leq 60$ Hz.

Table 4 Overall boost parameters*.

	Value	Unit		Value	Unit
L	24.6	μH	r_L	17	mΩ
C	30	μF	r_C	2	mΩ
w_S	0	V	r_S	36.8	mΩ
w_D	0.6	V	r_D	10	mΩ
v_{in}	24	V	i_0	10	A

* Rated values.

inductor losses increase with the load, from about 1 W at 40% to almost 5 W at the rated load. Simulation results are then compared with those achieved by employing the simplified model defined by Eq. (3) (case *A*) and by the more accurate one defined by Eq. (17) (case *B*). The comparison results are shown in Fig. 9, which reveals significant mismatches between simulations and case *A*. These occur especially at lightload, in correspondence of which inductor losses estimation errors are about 15%. Much better results are achieved in case *B*, meaning that, the proposed inductor modelling enables a very good losses estimation, the corresponding errors being less than 1% at any load.

Subsequently, simulations have been performed by increasing the switching frequency up to 100 kHz with steps of 20 kHz, whereas the load has been varied within 40%-100%, as previously. Simulation results have been then compared with those achieved in both case *A* and case *B*, whose corresponding results are shown in Figs. 10 and 11, respectively. Focusing on Fig. 10 at first, it can be seen that, estimation errors occurring in case *A* decreases as the switching frequency increases. This is expected because the inductor current ripple decreases with the switching frequency, making r_P increasingly useless. Differently, in case *B*, inductor losses estimation slightly deteriorates as the switching frequency increases, this being highlighted in Fig. 11. However, it is worth noting that, inductor losses estimation errors achieved in case *B* are significantly less than those obtained in case *A*, whatever the load and the

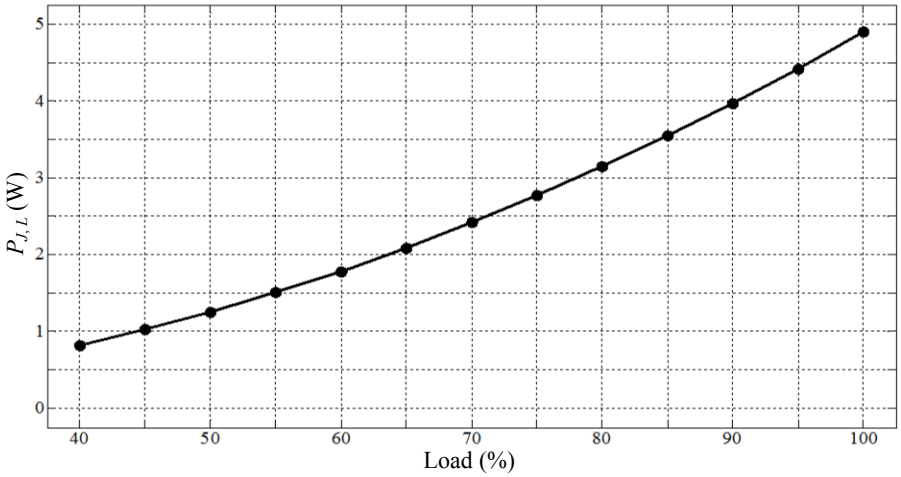

Fig. 8 Inductor losses evolutions achieved in simulations at 40 kHz.

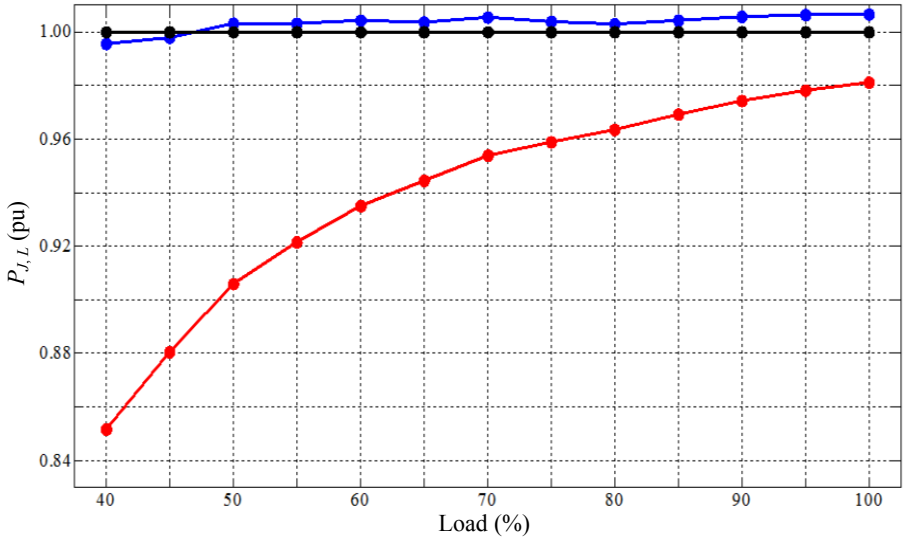

Fig. 9 Inductor losses comparison at 40 kHz: simulations (black), case *A* (red) and case *B* (blue).

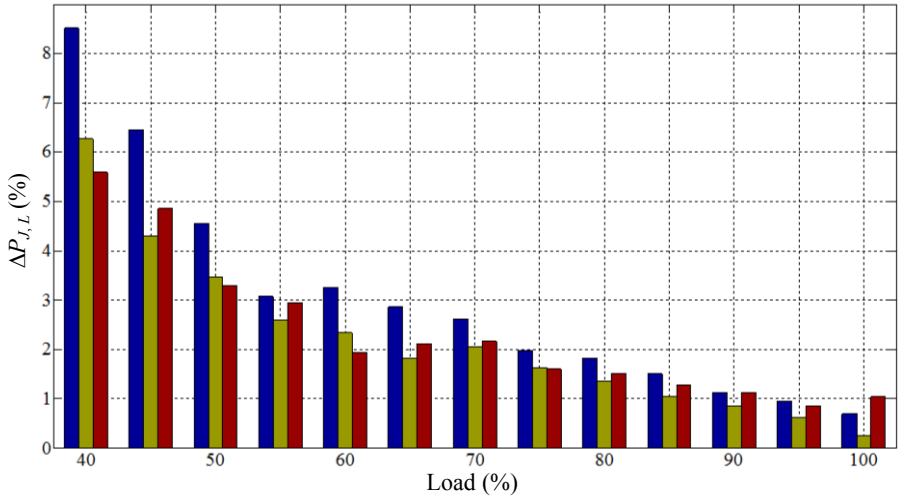

Fig. 10 Inductor losses estimation errors achieved in case *A* at different switching frequencies: 60 kHz (blue), 80 kHz (yellow) and 100 kHz (red).

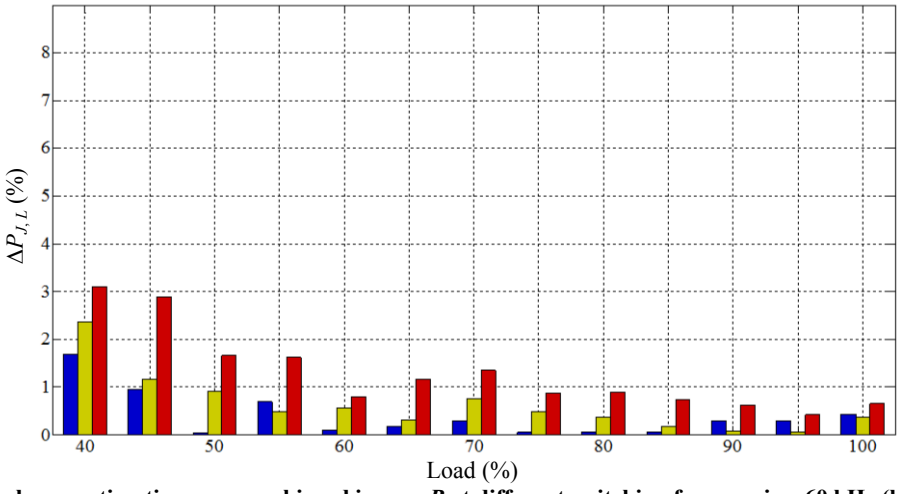

Fig. 11 Inductor losses estimation errors achieved in case *B* at different switching frequencies: 60 kHz (blue), 80 kHz (yellow) and 100 kHz (red).

switching frequency are. This corroborates the effectiveness of the proposed inductor modelling approach, which enables a very good estimation of inductor losses at any operating conditions of the boost converter.

6. Conclusions

An inductor modelling suitable for power electronic DC-DC converters has been presented in this paper. It enables the development of improved averaged models, which appropriately take into account inductor losses due to current ripple. The proposed modeling approach has been validated through a simulation study, whose results highlight a very good estimation of inductor losses by means of an improved averaged model. Consequently, this is revealed to be particularly suitable as a supporting tool for the design stage.

Acknowledgments

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