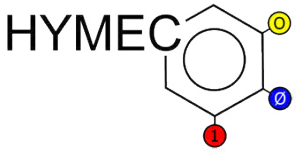


University of Cagliari

Non-volatile organic memory devices: from design to applications

Thesis for the Degree of Doctor of Philosophy

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Dedicated to my little angel, Jimmy.
You will be in my heart,
always and forever.

INTRODUCTION

Historically, progress in electronics has been driven by the so-called *Moore's Law*, first noted by Gordon Moore in 1965: the number of components in silicon microprocessors tends to double every 18–24 months, mainly through reductions in the sizes of the transistors. This trend is now so well established that it is used as the baseline assumption for the industry's strategic roadmaps, which guide the efforts of the entire industry. The Law has aroused in users and consumers an expectation of a continuous flow of faster, better, and cheaper high-technology products. Regular doubling of the components number on a chip means exponential growth in the complexity of integrated circuits year on year, driven by the search for profit. However, exponential growth cannot continue forever, since it also means that the fundamental physical limits of microelectronics are approaching rapidly. Indeed, as compononent geometries shrink towards atomic scales, the limits to Moore's law may be reached quickly. As soon as these physical limits are approached, other factors, such as design costs, manufacturing economics and device reliability, should be considered, and alternative ways forward must be sought.

In the 21^{st} century, advances in electronics are required from different viewpoints to achieve high compatibility with the global environment and human lives. Moreover, it is necessary to improve the performance and reduce the manufacturing cost of electronic devices as well as achieve reductions in the energy consumption and waste. Furthermore, industrial manufacturing processes should undergo a transformation with minimal impact on the environment. For these reasons, it is becoming more important to explore not only inorganic semiconductors, but also new electronic functional materials with

features alternative or complementary to those of silicon. In particular, great expectations are placed in organic molecular materials, which are mainly composed of carbon, and carbon nanomaterials. The use of organic materials provides many advantages including low fabrication costs, printability, high flexibility, easy processing, and large area fabrication. Supported by the intensive research and development in nanotechnology-related fields, organic electronics has markedly advanced in recent years. During the development of organic electronics, much of the focus has been on organic transistors, organic light emitting diodes, and organic photovoltaic cells. However, it stands to reason that organic electronics will need memory as much as regular electronics. The implementation of plastic electronic solutions to large area displays, disposable sensor arrays, radiofrequency identification tags (RFIDs), and various smart packaging devices require the development of high-performances non-volatile organic memories. Overcoming the main limitations of state-of-the-art organic memory elements may definitely contribute to the diffusion of organic electronic systems where several devices are connected to perform complex functions.

Organic electronic memories were first reported in 1970, and since then, a wide variety of organic materials have been reported to show memory behaviour. However, many of the earlier observed electrical memory effects showed performances which were not satisfactory for practical applications and received relatively little attention. A rapid growth in the interest in organic memories has occurred only in the last 15 years. Nevertheless, despite promising performances, organic memory devices are still in the exploratory stage of the research. Indeed, several important issues, such as the physical explanation of the memory behavior, are still not clear. Furthermore, stability and reliability in operational environment are still debatable.

The research activity described in this manuscript can be included in the wide field of organic memories. The aim of the proposed activity is to overcome the main limitations of the state-of-the-art memory devices based on organic materials. The final goal is to design and fabricate novel high-performances organic memory elements, which can be employed for the development of multi-bit memory systems suitable for integration with electrical sensors. In particular, the research activity has been mainly focused on the study, development, fabrication and characterization of new non-volatile organic memory elements based on resistive switching. This activity has been carried out within the European project “HYbrid organic/inorganic Memory Elements for integration of electronic and photonic Circuitry”(HYMEC, 263073), which aimed to resolve fundamental issues of materials science and to realize new hybrid

inorganic/organic devices with functionality far beyond the state of the art. A complementary activity on transistor-based organic memory devices has been also carried out and described in this thesis.
The manuscript is divided in six different parts. In the first part, the state of the art on organic memories is presented in order to define the background of the main solutions proposed in literature and the main limitations so far identified. The development of a novel non-volatile memory device based on the combination of an air-stable organic semiconductor and metal nanoparticles is described in the second part. This activity included design, fabrication and testing of a novel, high-performance memory structure: development of technology and procedures for easy and reliable production of devices, as well as the definition of measurement protocols, are reported. The third part describes the integration of memory elements with electrical sensor devices. In particular, the suitability of organic non-volatile memory devices for the detection and the storage of external parameters was demonstrated. As prototypical example, flexible arrays of mechanically switchable memory elements system were designed, fabricated and characterized. In the fourth part, the activity on trasistor memories is presented. In particular, this activity was related to the design, fabrication and characterization of transistor-based memories as well as to the development of reliable measurement procedures. Finally, part five and six report main conclusions and outlooks of the research activity and a detailed description of employed materials and methods, respectively.

INTRODUZIONE

Storicamente, il progresso scientifico dell'elettronica è stato guidato dalla cosiddetta *legge di Moore*, tratta da un'osservazione empirica di Gordon Moore nel 1965: la complessità dei microprocessori (misurata dal numero di componenti per chip o per area unitaria) raddoppia periodicamente, con un periodo originalmente previsto in 12 mesi, allungato a 2 anni verso la fine degli anni Settanta e dall'inizio degli anni Ottanta assestatosi sui 18-24 mesi. Questa tendenza è oggi così radicata da essere utilizzata come riferimento per la definizione dei piani d'azione delle maggiori industrie. Inoltre, la legge di Moore ha contribuito ad alimentare la richiesta da parte di consumatori e utilizzatori di un flusso continuo di prodotti tecnologici sempre migliori ed economici. Tuttavia, il regolare raddoppiarsi del numero dei componenti in un chip comporta la crescita esponenziale della complessità dei circuiti integrati, ovvero il rapido raggiungimento dei limiti fisici fondamentali della microelettronica. La progressiva riduzione delle dimensioni dei componenti elettronici dovrà fermarsi prima di raggiungere la scala atomica, segnando il limite ultimo della legge di Moore. Di conseguenza, fattori quali i costi di progetto/produzione e l'affidabilità dei dispositivi diventeranno sempre più dominanti nella ricerca di vie di sviluppo alternative per l'elettronica.

In quest'ottica, uno degli obiettivi principali del progresso tecnologico del XXI secolo è lo sviluppo di un'elettronica biocompatibile e biodegradabile. Risultano inoltre fondamentali il miglioramento delle prestazioni e la riduzione dei costi di fabbricazione dei dispositivi elettronici, lo sviluppo di processi industriali con il minimo impatto ambientale, così come la drastica riduzione del consumo e dello spreco energetico. Per queste ragioni, sta diventando sempre più

comune lo studio di materiali con proprietà alternative e/o complementari a quelle del silicio. In particolare, una grande attenzione è stata riposta recentemente sui materiali organici, ovvero i composti del carbonio. L'utilizzo di tali materiali presenta diversi vantaggi, tra cui la biocompatibilità, la compatibilità con materiali leggeri, flessibili e trasparenti utilizzabili come substrati, processi realizzativi a costi potenzialmente molto bassi. Negli ultimi anni, grazie anche al rapido progresso nel campo della nanotecnologia, l'elettronica organica ha raggiunto un progresso considerevole. Nello specifico, notevoli passi avanti sono stati compiuti soprattutto nel campo di transistor, diodi ad emissione di luce e celle fotovoltaiche. Tuttavia, l'implementazione dell'elettronica organica su dispositivi quali display flessibili, array di sensori portatili, tag di identificazione a radiofrequenza (RFID), smart packaging, richiede lo sviluppo di memorie organiche non volatili. Superare i principali limiti dello stato dell'arte dei dispositivi di memoria organici potrebbe contribuire alla definitiva diffusione di sistemi organici in grado di compiere funzioni complesse.
Le memorie organiche sono state introdotte per la prima volta nel 1970, e da allora una grande varietà di materiali organici si sono rivelati ideali per la fabbricazione di tali dispositivi. Tuttavia, nella maggior parte dei casi, le prestazioni non sono risultate soddisfacenti per l'utilizzo pratico. Un rapido incremento dell'interesse scientifico nei confronti dei dispositivi di memoria organici è avvenuto solo a partire dagli ultimi 15 anni. Nonostante i risultati promettenti, le memorie organiche sono ancora oggi nella fase esplorativa della ricerca. Infatti, diversi punti cardine di tale tecnologia, come la spiegazione fisica dell'effetto memoria, rimangono ancora irrisolti. Per di più, l'affidabilità e la stabilità dei dispositivi risultano ancora discutibili.
L'attività di ricerca descritta nel presente elaborato si inserisce proprio nell'ambito di ricerca sulle memorie organiche. L'attività presentata ha l'obiettivo di superare i principali limiti dello stato dell'arte della tecnologia organica per la realizzazione di elementi di memoria. Lo scopo finale prevede quindi sviluppo, fabbricazione e caratterizzazione di nuovi elementi di memoria non volatile, che possono essere utilizzati per la realizzazione di sistemi multi-bit per diverse applicazioni; nello specifico, è stata esplorata la loro integrazione con sensori elettrici. L'attività di ricerca è stata portata avanti principalmente nell'ambito del progetto europeo "HYbrid organic/inorganic Memory Elements for integration of electronic and photonic Circuitry" (HYMEC, 263073), i cui obiettivi erano proprio quelli di fabbricare nuovi dispositivi di memoria non volatile di tipo ibrido inorganico/organico con funzionalità che superino quelle attualmente allo stato dell'arte.

L'elaborato è stato diviso in 6 sezioni. Nella prima parte viene presentato uno stato dell'arte generale sulle memorie organiche, al fine di fornire una visione d'insieme delle soluzioni presenti in letteratura e dei loro eventuali limiti. Verrà poi presentato lo sviluppo di un nuovo dispositivo di memoria non volatile basato sulla combinazione di nanoparticelle metalliche e un semiconduttore organico stabile all'aria. Tale attività, descritta nella seconda parte dell'elaborato, comprende il progetto, la fabbricazione e la caratterizzazione di una nuova struttura, ovvero lo sviluppo di procedure per la fabbricazione affidabile e riproducibile dei dispositivi cosi come la definizione dei protocolli di misura. Nella terza parte verrà invece descritta l'integrazione degli elementi di memoria con sensori elettrici. In particolare, verrà dimostrata la possibilità di utilizzare tali dispositivi per la rilevazione e memorizzazione di parametri esterni. Come esempio, è stato progettato fabbricato e testato un sistema flessibile di elementi di memoria indirizzabili meccanicamente, e quindi in grado di memorizzare forme. La quarta sezione dell'elaborato descrive l'attività riguardante progetto, fabbricazione e caratterizzazione di memorie basate invece su una struttura di transistor organico a effetto di campo (OFET), oltre che la definizione accurata di procedure di misura affidabili. Infine, nella sezioni cinque e sei vengono riportati rispettivamente conclusioni e sviluppi futuri dell'attività di ricerca, e una descrizione dettagliata di materiali e metodi utilizzati.

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"Give thanks is the highest form of thought,
gratitude is happiness doubled by surprise."

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CONTENTS

Part I

Aim and Background

1 ELECTRONIC MEMORIES

Contents

1.1 Introduction: memory concept and classification

An **electronic memory** is a component, device or recording medium used to store data for retrieval on a temporary or permanent basis for use in a computer or other digital electronic devices. It is one of the fundamental components of all modern computers and electronic systems. There are two operations that a memory can perform: it can be read and written when connected to a central processing unit. The writing operation is performed to store data into the memory, whereas, the reading operation is performed to retrieve data from the memory. This feature distinguishes the electronic memory from the mechanical storage devices, such as CD, DVD, hard disk. These units require mechanical equipment to convert optical, magnetic or other signals to electrical signals for the central processing system to recognize.
Electronic memories can be divided into two primary categories: volatile and non-volatile memories,as shown in Figure 1.1. A **volatile memory** requires a costant power supply to retain the stored information: it loses written data as soon as the system is turned off. A

non-volatile memory can retain the stored information even when the electrical power supply has been turned off.

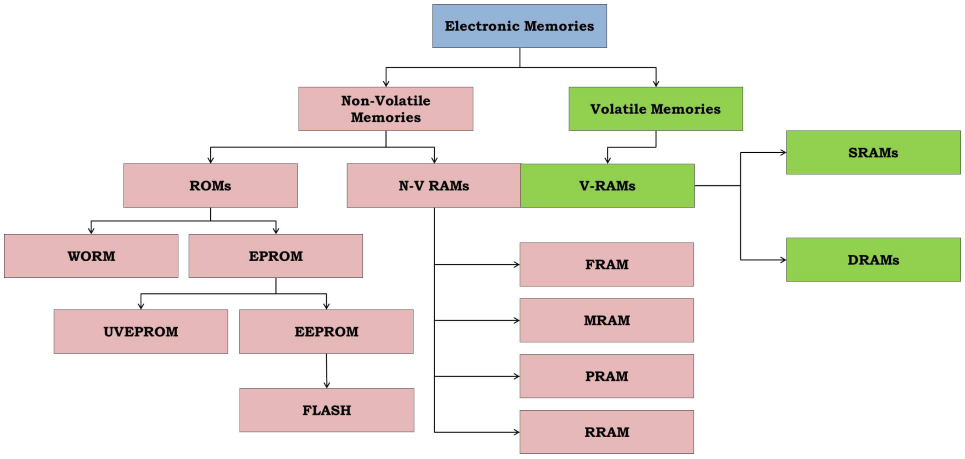


Figure 1.1: Classification of electronic memories.

Memories can be also classified according to how many times they can be rewritten into **random access memories**: i) (RAMs); ii)**read-only memories** (ROMs). In RAMs, as the name suggests, information can be written to or read from any cells without read/write cycle limitations, whereas in ROMs read/write cycles are limited. In RAMs, writing and reading times are almost the same, whereas in ROMs writing takes more time than reading.
RAMs can be further classified into *volatile RAMs* (V-RAMs) and *non-volatile RAMs* (NV-RAMs). *Dynamic RAMs* (DRAMs) and *static RAMs* (SRAMs) are examples of V-RAMs. **DRAMs** are one of the most commonly memory modules in personal computers and workstations. They store each bit of data into a separate capacitor in an integrated circuit. The capacitor can be discharged or charged and these two states represent the two values of a bit (0 and 1). Since real capacitors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory. The advantage of DRAM resides in its simplicity: only one capacitor and one transistor are required per bit (`Figure 1.2 a`). This allows DRAMs to reach very high densities. The capacitors and transistors used are extremely small: millions can fit on a single memory chip. A **SRAM** is designed to fill two needs: to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption. Unlike DRAM, it does not need to be refreshed. SRAM stores a bit of data on four transistors using

two cross-coupled inverters (`Figure 1.2 b`). The two stable states characterize 0 and 1. During read and write operations another two access transistors are used to manage the availability to a memory cell. The 0 or 1 state can be written and read instantly without waiting for a capacitor to fill up or drain. Moreover, SRAMs are faster and can operate at higher speeds than DRAM, but they are more expensive to manufacture because of its complex internal structure. SRAM's access time is a lot faster (about 10 nanoseconds) than DRAM's (about 60 nanoseconds). Additionally, SRAM's cycle time is a lot shorter than DRAM's because it does not need to refresh. However, the six transistors take more space than one transistor and one capacitor, thus making SRAM cells larger than DRAM ones. Due to its condensed size, SRAMs are not ideal for main memory, but they are best suited for secondary operations like the CPU's fast cache memory and storing registers. SRAM is most often found in hard drives as disc cache, in compact discs (CD's), printers, modem routers, digital versatile discs (DVD's) and digital cameras.

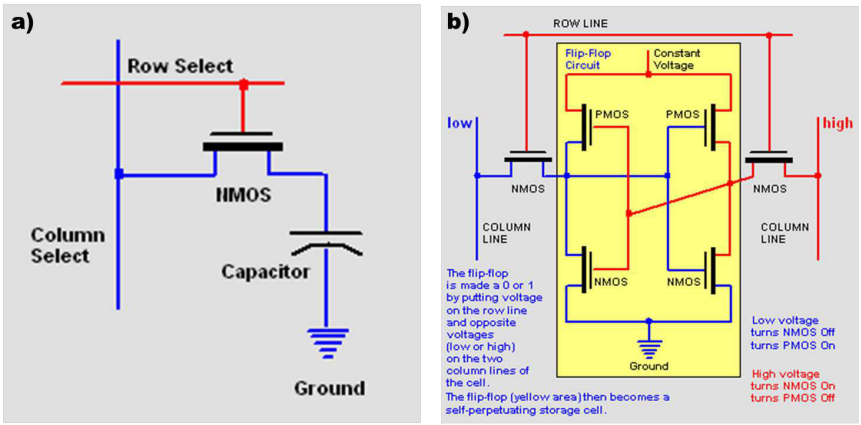


Figure 1.2: A static RAM cell (a) and a dynamic RAM cell (b).

NV-RAMs are memories that provide the random access facility and retain stored data even if the power is switched off. Different types of NV-RAMs are available. A battery-backed static RAM was the first NV-RAM: it was created by connecting it to a rechargeable battery for maintaining the power given to the static RAM when the power of the system is turned off. This technology is still available, but works effectively only for a limited time. The disadvantage is that the batteries occupy most of the useful space, and eventually get discharged. *Ferroelectric RAMs* (FRAMs), *magnetic RAMs* (MRAMs), *phase-change RAMs* (PRAMs) and *Resistive RAMs* (RRAMs) are other examples of NV-RAMs.

FRAMs use the electric field and ferroelectric effects to store data. They exploit a ferroelectric capacitor composed of a crystal made up of lead and oxygen atoms plus zirconium or titanium. When a sufficiently strong electric field is applied to a ferroelectric material, the consequent change in the ferroelectric polarization is hysteretic in nature. In an ideal case, a polarization versus electric field loop presents two distinguishable polarization states. This bi-stability in the polarization forms the basis of FRAMs. To enable this effect to be used in a memory cell an additional active element (tipically a field effect transistor, FET) is used. The cell has a word line and also a bit line to enable the individual cell to be accessed. FRAM cell structure resembles a DRAM cell with the exception of plate line (Figure 1.3 a), which carries variable voltages to realize the polarization switching of ferroelectric capacitor. FRAMs, introduced in the late 1980s, offer a number of advantages, notably, low-power consumption, fast write speed and good cyclability.

Unlike other RAM technologies, data in **MRAMs** is not stored as electric charge or current flows, but by magnetic storage elements. The basic MRAM cell is the so-called Magnetic Tunnel Junction (MTJ) which consists of two magnetic layers sandwiching a thin insulating layer (Figure 1.3 b). The magnetization of one of the layers, acting as a reference layer, is fixed and kept rigid in one given direction. The other layer, acting as the storage layer, can be switched under an applied magnetic field from parallel to antiparallel to the reference layer, therein inducing a change in the cell resistance. The corresponding logic state ("0" or "1") of the memory is hence defined by its resistance state (low or high), monitored by a small read current. MRAMs have similar performance to SRAMs, similar density to DRAMs but much lower power consumption than DRAMs, are much faster and suffer no degradation over time. This explains the huge amount of research being carried out into developing it.

PRAM exploits the unique property of phase-change materials (PCMs), which are typically higher chalcogenides. PCMs exhibit an ability for reversible phase transition between the amorphous and crystalline phases with the help of Joule heating. This phase transition brings about a change in the resistance as well as the reflectivity. In the amorphous state the material demonstrates a high level of resistance and also a low reflectivity. In the polycrystalline state the material has a low resistances as electrons are easily able to move through the crystalline structure, and it also exhibits a high reflectivity. The crystalline phase (logic 1) is configured by applying a low-power pulse. On the other hand, the amorphous phase (logic 0) is configured by applying a high-power electric pulse with a shorter duration than that of the crystalline phase. It is the switching time

and inherent scalability that makes PRAM most appealing, while temperature sensitivity is perhaps its most notable drawback.

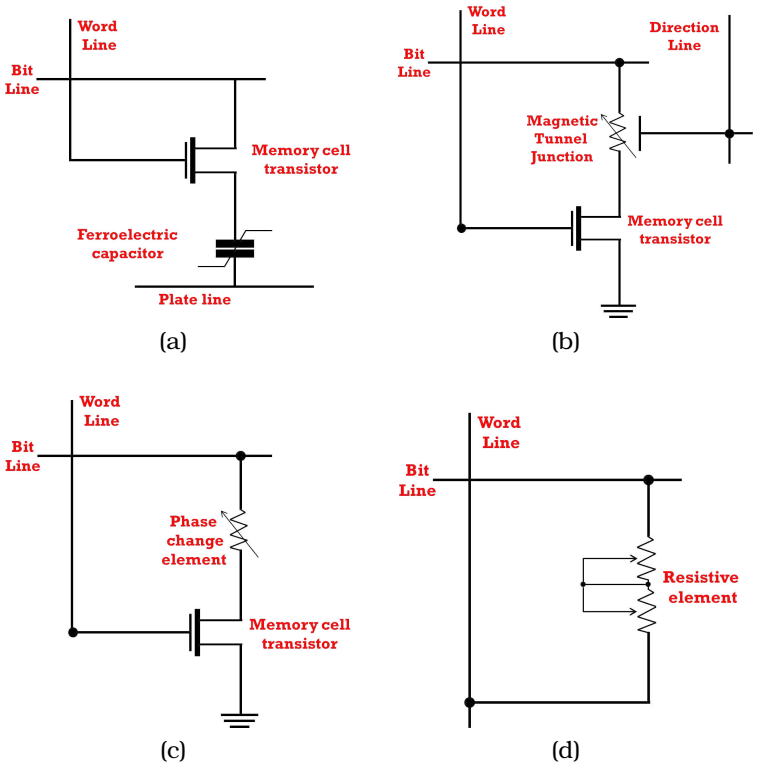


Figure 1.3: Electrical structure of (a) FRAM, (b) MRAM,(c) PRAM and (d) RRAM cell.

RRAMs nominally include all types of memories using two or more distinctive resistance states as the binary numbers '0' and '1'. Therefore, PRAMs and MRAMs in principle could be considered as resistance memories, but are relatively much more clearly understood. When RRAMs were introduced, the mechanism was not well understood. Pioneers named this memory type RRAM without specifying the mechanism. Each memory cell of a RRAM consists of a top electrode (TE) and a bottom electrode (BE) sandwiching a switching layer. This switching cell is characterized by two distinctive resistance states: a high resistance state (HRS) and a low resistance state (LRS). By applying either a voltage or a current to the cell, reversible switching between the HRS and LRS can be achieved. Once switched, the cell retains the particular resistance level for a long time. Compared to PRAM, RRAM operates at a faster timescale, while compared to MRAM, it has a simpler, smaller cell structure. Indeed,

RRAM cells can be fabricated without access transistors (Figure 1.3 d). This advantage enables RRAM to be integrated in crossbar arrays and stacked in multiple layers forming 3D memories.

Depending on reprogrammability, **ROMs** are classified as *write-once read-many times ROMs* (WORM) and *erasable programmable ROMs* (EPROMs). As a non-volatile memory, a **WORM** is capable of holding data permanenetly and being read repeatedly. It can be written only once phisically, as the name suggests, and it is not possible to modify or erase the stored data. WORM memories can be used to store archivial standards, databases and other massive data where information has to be reliably kept and made available over a long period of time. **EPROMs** can be erased either by exposing memory cells to ultraviolet radiation (*ultraviolet EPROMs, UVEPROMs*) or by electrical means (*electrically erasable PROMs, EEPROMs*). An **UVEPROM** cell consists of a transistor with the same basic structure as a standard MOS transistor, but with the addition of a second polysilicon floating gate isolated by layers of oxide (Figure 1.4).

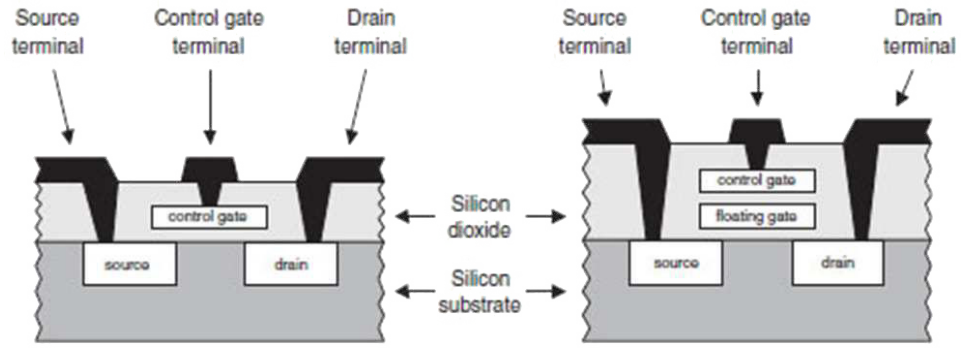


Figure 1.4: Comparison between: a) standard MOS transistor and b) UVEPROM transistor.

To program the bit, a high voltage is applied to the control gate. This causes electrons to tunnel through the insulating oxide layer into the floating gate, which impedes the subsequent operation of the control gate. The 0 or 1 is determined by whether the voltage on the control gate is blocked or not. Once programmed, an UVEPROM can be erased by exposing it to strong ultraviolet light source (such as from a mercury-vapor light). Importantly, all memory cells are simultaneously erased. UVEPROMs are easily recognizable by the transparent fused quartz window in the top of the package, through which the silicon chip is visible, and which permits exposure to UV

light during erasing. Although UVEPROMs can be reprogrammed, such memory is susceptible to light that may lead to an unintentional erase. Moreover, the quartz window package incurs a high production cost.

EEPROMs are introduced as the improvement to UVEPROMs. EEPROM bit cell is a CMOS-based transistor that hold a charge on a "floating gate." The EEPROM transistor is similar to that of an UVEPROM transistor, but the insulating oxide layers surrounding this gate are very much thinner (`Figure 1.5`). With no charge on the floating gate, the transistor acts normally, and a pulse on the control gate causes current to flow. When charged, it blocks the control gate action, and current does not flow. Charging is accomplished by grounding the source and drain terminals and placing sufficient voltage on the control gate tunnel through the oxide to the floating gate. A reverse voltage channeled from another transistor clears the charge by causing it to dissipate into the substrate. In contrast to UVEPROMs that requires ultraviolet light, EEPROMs can be electrically erased prior to reprogramming and what is more memory cells can be erased byte or block-wise. Other advantages of EEPROMs are reprogrammability while in a system, cheap packaging and insensitivity to light. Yet, the main disadvantage is the high production cost due to a complex cell circuit. Therefore, EEPROMs are suitable for, e.g., electronic systems that require non-volatility and in-system reprogrammability.

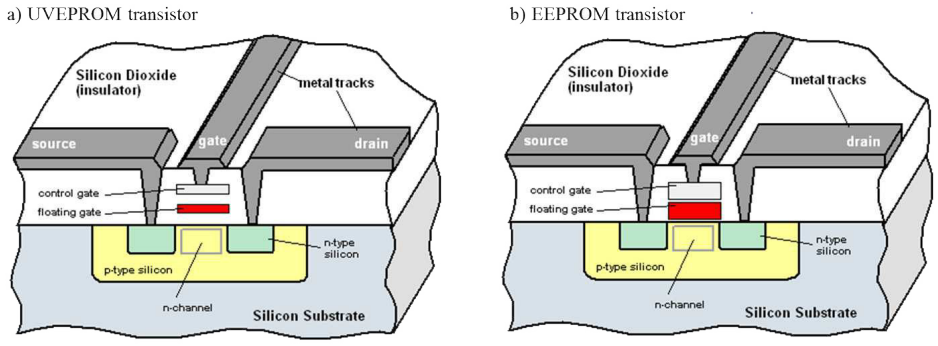


Figure 1.5: a) UVEPROM transistor; b) EEPROM transistor.

Finally, **FLASH memory** can be considered as a kind of EEPROMs, as they are also electrically written and erased. However, each memory cell in a EEPROM consists of two metal – oxide – semiconductor field - effect - transistor (MOSFET), while a FLASH cell is basically a single floating-gate MOS transistor (see `Figure 1.6 a`), i.e., a transistor with a gate completely surrounded by a insulating

layer, the floating gate, and electrically governed by a capacitively coupled control gate. Being electrically isolated, the floating gate acts as the storing electrode; charge injected in the floating gate is maintained there, allowing modulation of the "apparent" threshold voltage (i.e., seen from the control gate) of the cell transistor. Obviously the quality of the dielectrics guarantees the nonvolatility, while the thickness allows the possibility to program or erase the cell by electrical pulses. Usually the gate dielectric, i.e., the one between the transistor channel and the floating gate, is an oxide in the range of 9–10 nm and is called "tunnel oxide" since electron tunneling occurs through it. The application of voltage pulses to the control gate allows electrons from the channel to cross the tunnel oxide and charge the floating gate (modifying the threshold voltage V_t). Thus, the electrostatic potential of the floating gate screens the electrons of the channel, and the current between source and drain is substantially reduced (`Figure 1.6 c`). To remove the electrons from the floating gate, an opposite polarity voltage pulse is applied, which brings them back to the channel through the tunnel oxide. In this case, the source–drain current increases again (`Figure 1.6 d`).

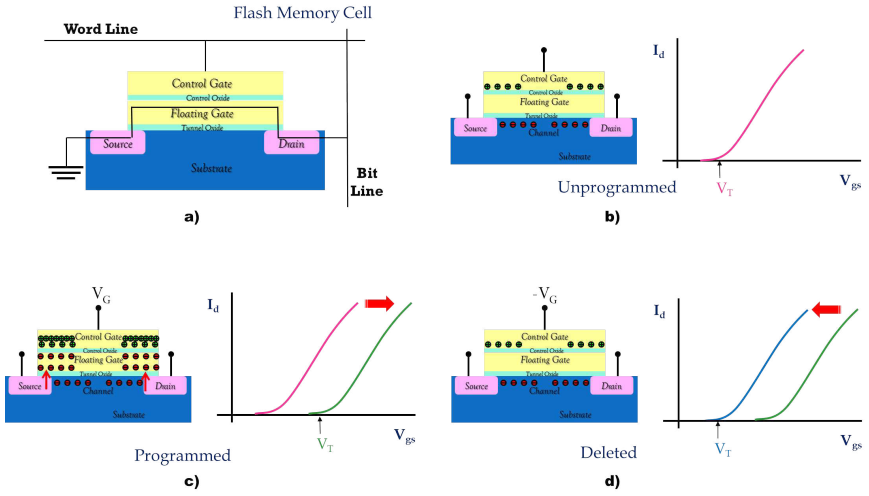


Figure 1.6: a) The structure of a FLASH cell; b) Unprogrammed FLASH cell; c) Writing process; d) Erasing process.

The reading operation is performed evaluating the threshold voltage of the floating gate through the measurement of the drain current at a gate voltage that does not disturb the writing and erasing states of the device. FLASH memories provide the best trade-off between cost and reprogammability. The "FLASH" name implies that the erasure process is faster as compared to EEPROMs. FLASH

memories erase and program data in blocks, whereas EEPROMs in bytes. Furthermore, FLASH memories are able to store more than one bit per cell. Because of these advantages, this memory is the most popular and widely used ROMs in computer and other electronic systems.

1.2 Conventional memory technologies

Nowadays, much of our daily life relies on information techonology, which can be seen anytime and everywhere in the form of mobile phones, personal computers, media players, e-books, digital cameras, navigation systems and many more. As the complexity of the mobile gadgets increases, miniaturization and data storage become important issues. Since the demand for mobile applications is the main driving force behind memory technologies and devices, there is an ever increasing demand for higher capacity and system performance, lower power consumption, smaller form factor and lower system cost. Therefore, it is not wonder that tremendous effort has been made to develop high-density, low-cost and non-volatile storage devices. Consenquently, memories can be also classified as conventional and emerging, according to the maturity level of such memories in product development and commercialization. The name *conventional* implies that the memories are mature in development and have been in sold as products for quite some time. On the other hand, *emerging* memories are in the early stage of development such that they either entered the market in recent years or they are in the prototyping phase.
Volatile RAMs (SRAM and DRAM) and all ROMs (WORM, UVEPROM, EEPROM, FLASH) can be considered as **conventional memories**. In particular, currently, DRAMs and FLASH memories constitute the biggest part of the semiconductor memory market. DRAMs were traditionally used as technology drivers for the semiconductor industry. However, FLASH memories have caught up with DRAMs and now are scaling ahead in terms of storage density as well as minimum feature size. In spite of the wide application in commercial products, the current memory technologies have some important disadvantages.
From a performance perspective, four attributes of memory technologies are of particular interest: cost per bit, programming speed, access speed, and whether the memory is non-volatile or volatile. The hard disk is the cheapest technology (10^{-3} \$/MB), but its access and program times are limited to several ms due to mechanical rotation of the disk. FLASH memories offer a considerable decrease in access times (in the order of 100 ns), but program times remain

long (write and erase times of 1 ms and 0.1 ms, respectively) and cost/bit is much higher (0.5 $/MB). DRAMs are even faster, with program and access times in the range of ns, and they are cheaper than FLASH memories (0.15 $/MB). However, these advantages in speed and cost are offset by DRAM's volatility. Finally, SRAM is the fastest technology (1 ns program/access times), but it is also volatile and the most expensive (2.7 $/MB)[1]. Although cost/bit, program times, and access times are key characteristics of memory technologies, a much longer list of characteristics are relevant in most applications. For instance, program voltages and durability are fundamental parameters. FLASH memories are rather limited in this characteristics. Indeed, durability is relatively low, as FLASH memories are tipically rated for 10^6 programming cycles (in comparison to $> 10^{16}$ write/read cycles for DRAMs). Moreover, FLASH memories require large programming voltages (> 10 V), due to the voltage needed to remove charges stored on the floating gate (by tunneling through the gate insulator). The reduction of this voltage is very hard, as this would require reducing the insulator thickness and, consequently, this would decrease the ability to store charges on the gate without leakage. This trade-off between operating voltages and gate insulator thickness could limit the opportunities for scaling of FLASH memories. Furthermore, the large programming voltages also lead to increase power consumption. Similarly, DRAMs, which are omnipresent in today's computers, have been meeting all the scalability requirements since their introduction in the beginning of 1970s, but a further improvement in the density is a problem. Moreover, system memory power (that is DRAM power) and disk power contribute as much as 40% to the overall power consumption, and the current trends suggest that this will continue to increase at a rapid rate. The energy efficiency therefore becomes a critical aspect. Replacing DRAMs with non-volatile memories may be the ultimate solution for energy efficiency. All these limitations of conventional memories have led to a considerable amount of research activity for new non-volatile memory technologies. In short, the focus of research is on obtaining non-volatile, fast, high-density, low-power consumption, high data transfer rate and reliable memories. If emerging memories will satisfy the positive points of RAMs and ROMs, then they can be universal future memories.

1.3 Emerging memory technologies

Numerous types of memories have been proposed in order to overcome the shortcomings of conventional memories. There are

more than tens memory types, based on different concepts, which have been considered as **emerging memories**. Some examples are ferroelectric RAMs (FRAMs)[2], resistive RAMs (RRAMs)[3], magnetic RAMs (MRAMs)[4], phase-change RAMs (PRAMs)[5], electrochemical metallization (ECM) memories or programmable metallization cell (PMC) memories[6], carbon nano-tube memories[7], molecular memories[8], nano-crystal floating-gate FLASH memories[9] and DNA memories[10]. However, among these memories, FRAMs, RRAMs, MRAMs and PRAMs have been considered as emerging memories to potentially overcome the limitations of DRAMs and FLASH memories.

FRAMs, introduced in the late 1980s a couple of years after FLASH memories, offer a number of advantages, notably, low-power consumption, fast write speed and good cyclability. FRAMs are still considered as emerging memories, although the expected density in the gigabit regime has not been achieved so far. Even if it started out with great promise, difficulty in scaling up the density due to the large cell size (compared with DRAMs and FLASH memories) has kept the density of FRAMs in the megabit regime and this is still a problem to get around.

MRAMs have been considered as possible candidates to replace several types of conventional memories, such as SRAMs, DRAMs and FLASH memories. Two main types of MRAMs have been developed: field-writing MRAMs and spin-transfer torque MRAMs (STTMRAMs). In a field-writing MRAM, each memory cell is written by a magnetic field around the current line. Field-writing MRAMs are currently in production as stand-alone 16 megabit MRAMs and embedded memories. The primary issue with field-write MRAMs is their high write current, which makes scaling difficult. STTMRAMs, which exploit spin-polarized current, have relatively good potential as a next-generation memory type, combining advantages of SRAMs (high speed), DRAMs (scalability) and FLASH memories (non-volatility). However, the OFF/ON ratio is of some concern since it must increase as the bit line voltage becomes lower. Moreover, an important issue is also the energy dissipation during operation.

An idea to use **phase-change materials** in memory devices dates back over four decades[11]. However, material quality and power consumption issues have prevented the commercialization of this technology. The progress in semiconductor manufacturing technology and the development of high-quality phase-change materials during the last few decades are the main reasons for the recent revival of PRAMs. Currently, PRAMs are promising as emerging memories and they are expected to replace FLASH memories in the memory market. Recent progress in PRAM technology has provided a clear demonstration of the excellent scaling potential[5]. The large

power consumption during the reversible phase transition between the amorphous and crystalline phases would be the most serious obstacle to their commercialization.

RRAMs have been demonstrated to exhibit excellent miniaturization potential down to 10 nm [12], sub-ns operation speed [13], very low energy consumption ($< 0.1pJ$) [14] and high-endurance ($> 10^{12}$ switching cycles)[15]. Therefore, RRAMs are also a potential alternative to the current main memory. As already mentioned, in general, a RRAM cell is composed of a conductor/switching layer (insulator or semiconductor)/conductor sandwich structure, as shown in `Figure 1.7`. The intrinsic physical phenomenon behind RRAMs is resistive switching, which means that the device can be freely programmed into a high resistance state (HRS, or OFF state) or a low resistance state (LRS, or ON state) under external electrical stimuli.

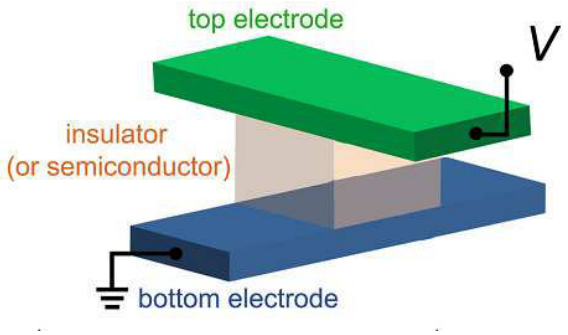


Figure 1.7: Schematic of conductor - insulator (or semiconductor) - conductor sandwich structure.

It has been almost a half century since the initial experimental observations of resistive switching. In 1962, Hickmott[16] observed large negative differential resistance in five thin anodic oxide films including silicon oxide (SiO_x), aluminum oxide (Al_2O_3), tantalum pentoxide (Ta_2O_5), zirconium dioxide (ZrO_2) and titanium dioxide (TiO_2). Subsequently, more materials were demonstrated to show resistive switching, and the switching mechanisms started to be explored as well[17, 18, 19]. However, strong research interest in resistive switching lasted approximately a decade due to the fact that the observed switching at that moment was not sufficiently robust for memory application, and also due to the prosperity of Si-based integrated circuit technology. Since the late 1990s, interest in RRAM starts to revive because of the need for an alternative to Si-based memories. In 1994, Blom et al. [20] observed resistive switching in ferroelectric materials. However, their system had the limitation

that the signal level was weak, which was an obstacle to the application of this system in memory devices since sense amplifiers and discriminators cannot read the signal reliably. Current research on resistive switching started in the early millennium. In 2000, Liu et al. found an electric-field-induced resistance-change effect in a perovskite-type oxide [21]. In 2000, resistive switching was also found in another perovskite-type oxide [22], and the application of this material in non-volatile memories was demonstrated. These findings triggered enormous interest in resistive switching in oxides for application in RRAMs, which had been out of the minds of researchers for more than three decades. This attention inspired much research on resistive switching in various materials, e.g. dielectric, paraelectric, ferroelectric, ferromagnetic and semiconducting materials. The first practical application of RRAMs was reported by Zhuang et al. [23]. These researchers fabricated a 64-bit RRAM array using a 0.5-mm complementary metaloxide-semiconductor (CMOS) process. The device showed good performance with low operation voltage (< 5 V), fast speed ($\sim$ 10 ns) and a large high/low resistance ratio (> 10^3). In 2004, Baek et al. [24] successfully demonstrated the world's premier binary transition-metal-oxide-based RRAMs with operation below 3 V and 2 mA, 10^6 set/reset operations and 10^{12} reading cycles, triggering a surge of studies in this research topic.
Recently, RRAMs have been suggested for new application fields including unconventional computing [25] and logic devices [26]. Moreover, combinations of RRAMs and ferromagnetic, optical, and even superconducting properties have recently been reported as well [27, 28, 29]. Consequently, RRAMs have been attracting extensive attention from academia and from application-oriented societies, demonstrated by the increasing number of publications per year, as shown in Figure 1.8.

1.4 Potential and challenges of organic memory devices

Among the emerging candidates for non-volatile memories, organic materials are promising candidates for future molecular-scale device applications. The primary benefits of organic memory are simple fabrication, low cost and rapid access, as well as compatibility with roll-to-roll printability for mass industrial production. Indeed, the main drive to develop organic nonvolatile memory is currently for applications of thin-film, flexible or even printed electronics. By thin-film technologies, electronic functionality can be foreseen in very large quantity and at very low cost on substrates such as plas-

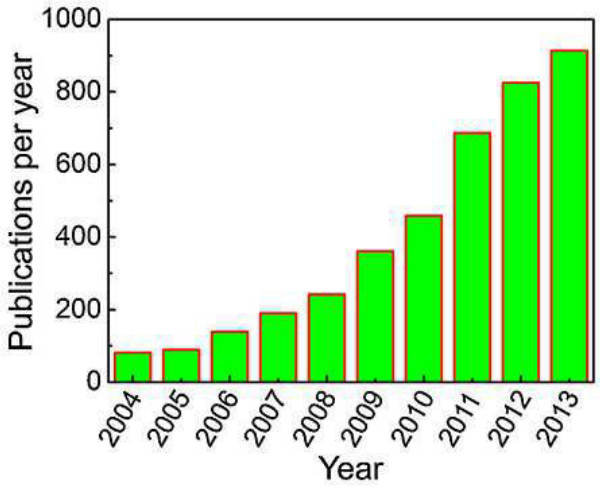


Figure 1.8: Publications per year on organic resistive memories from 2004 to 2013 [3].

tic and paper. Items where today integration of a silicon chip is not economical, such as toys, cards, labels, badges, value paper, and medical disposables, could be imagined to be equipped with electronics and memory. The promise of ubiquitous computing has inspired researchers to integrate electronic circuits into everyday objects and biological tissues. The vision is for distributed sensors and processing devices to monitor and respond to the environment autonomously, enhancing the way humans interact with objects around them. For example, sensors incorporated into clothing or attached to skin can allow continuous monitoring of vital signs and alert people, both locally and remotely, if dangerous thresholds are exceeded. To enable widespread penetration of these systems, the electronic hardware must be inexpensive and minimally intrusive. Organic electronic components provide mechanical flexibility and stretchability as well as low-cost manufacturability, complementing the computing power of silicon electronics. Moreover, the low-temperature fabrication process of organic memory also offers benefits for integrating memory devices into stretchable electronic systems on an elastic polymeric substrate.

Polymer electronic memories were first reported in 1970 by Sliva et al. [30], from devices based on a thermoplastic resin. Reproducible bistable switching was also observed by Carchano et al. [31] in gold/polymer/gold junctions. Following these pioneering works, a wide variety of polymers have been reported to show memory switch-

ing effects [32, 33, 34, 35]. However, many of the earlier observed electrical memory effects showed performances which were not satisfactory for practical applications and they received relatively little attention. A rapid growth in the interest in organic memories has occurred in the last 15 years, as indicated by the number of publication and citations each year worldwide (Figure 1.9).

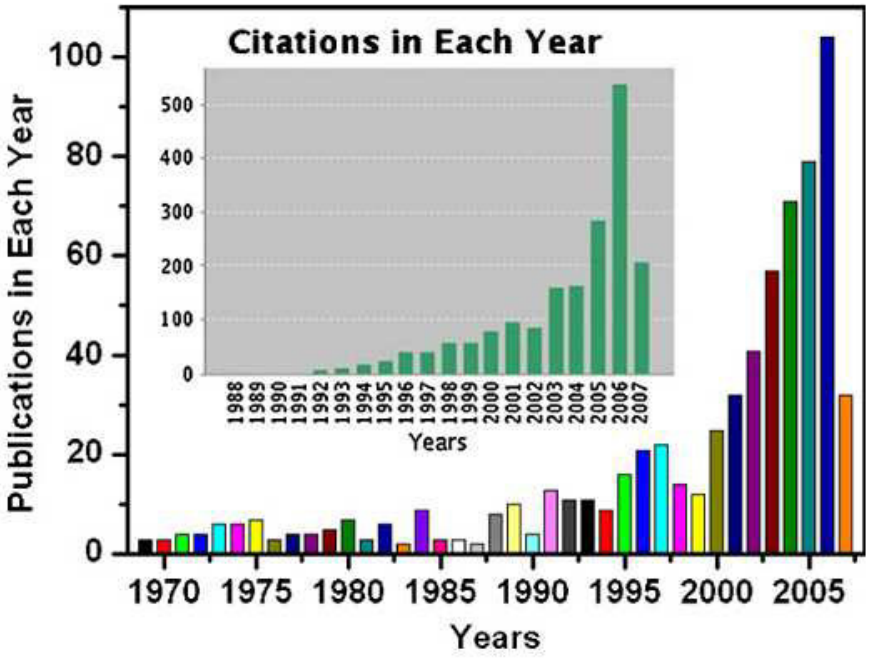


Figure 1.9: Statistics of publications and citations on organic memories during 1970-2007. [36].

The International Technology Roadmap for Semiconductors (ITRS) has identified organic memory as an emerging memory technology since year 2005 [37]. Moreover, the ISI Web of Sciences has also identified organic/polymer memory as a research front recently.

2

ORGANIC ELECTRONIC MEMORIES

Contents

2.1 Introduction

In an attempt to create a novel organic memory, several types of memory devices based on organic and polymeric materials have been evaluated. It is possible to characterize the organic memory devices that have so far appeared in the literature into one of three broad categories: capacitor-type memories, transistor-based memories and resistor-based memories. The purpose of this chapter is to

outline materials and device structures, operating principle and performances for each organic memory category.

2.2 Capacitor-type memories

2.2.1 Materials and device structures

In its simplest form, a capacitor stores charges, of opposite sign, on two parallel plate electrodes, indicating the bit level (either "0" or "1"). When the medium between the electrodes is merely a dielectric, there is nothing to stabilize the charged state, and hence the capacitor tends to discharge through whatever leakage path it can find. The storage capacitor needs to be periodically refreshed. Longer retention times are achieved if the medium includes molecular species that can be electrochemically reduced or oxidized. Among the compounds that have been explored for this form of “molecular memory” are metallo-porphyrins [38, 39, 40], and ferrocene derivatives [40, 41].These species are chemically attached to one electrode of the capacitor, and the rest of the medium acts as a solid electrolyte. Alternatively, a ferroelectric medium can be placed between the capacitor electrodes, as for istance poly(vinylidene difluoride) (PVDF) and its copolymer with trifluoroethylene (TrFE) [41]. The ferroelectric polarization is inherently bistable, directed towards either electrode, and may be reversed by application of a sufficiently high voltage of the appropriate polarity. Thus, a memory based on ferroelectric capacitor (FeRAM) is a non-volatile memory [42]: it does not need periodic refreshing and it still retains its data in the case of power failure.
According to the definition of a ferroelectric material, i.e. it has a polar unit cell and a high electric field can change the orientation of its dipole moment [43], only a few categories of polymer are ferroelectric [44]. Among them, the P(VDF–TrFE) copolymers, have been widely used as polymer capacitors in FeRAMs for the following advantages. The vinylidene fluoride (VDF) copolymers exhibit a large spontaneous polarization [45], excellent polarization stability, low leakage for high resistivity, and switching times as short as 0.1 μs [46]. Furthermore, they do not require high-temperature processing, have outstanding chemical stability and low fabrication costs, and are non-toxic. In addition to VDF copolymers, there are also nylon-based and other ferroelectric polymers. However, they generally have poor performance. The switching time of ferroelectric nylons, for example, is known to be longer by four orders of magnitude than that of P(VDF–TrFE) at the same applied field [44]. In the following, only the FeRAM will be considered, as their performances are, so far,

the best reported for capacitor-type memories.

2.2.2 Operating mechanism

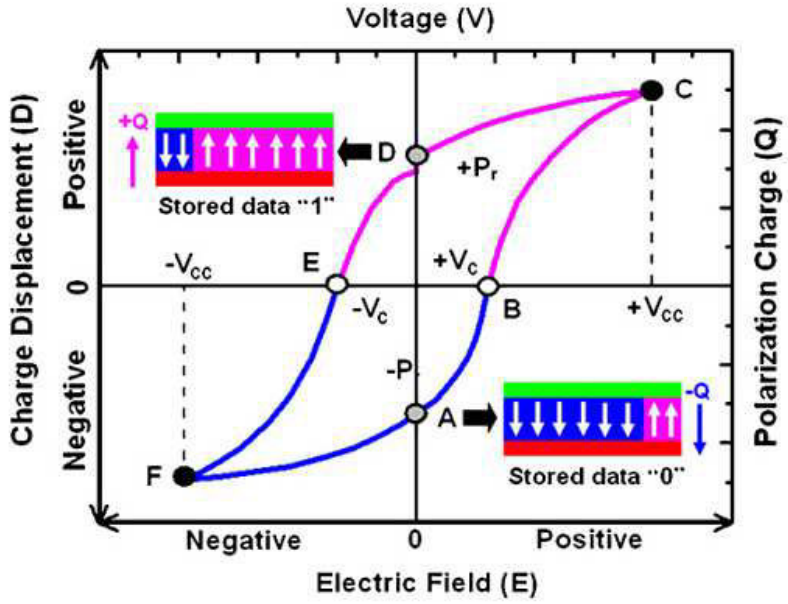


Figure 2.1: Charge displacement electric field (D–E) hysteresis loop and ferroelectric capacitor polarization conditions[36].

A ferroelectric material exhibits a polarization–electric-field hysteresis loop, analogous to the magnetization–magnetic-field hysteresis loop exhibited by a ferromagnetic material. In addition, like the magnetic material, ferroelectric material can form domains, each with a unique polarization axis. As shown in `Figure 2.1`, when voltages are applied from 0 V to $+V_{cc}$ and from 0 V to -V_{cc}, the polarization state changes progressively around the loop from point A to B to C, and point D to E to F, respectively. When voltages are applied from $+V_{cc}$ to 0 V and from $-V_{cc}$ to 0 V, the polarization state changes, moving from point C to D and from point F to A, respectively. Under this situation, the amount of polarization charges decreases slightly, without reversing its direction. Thus, the hysteresis loop is characterized by the magnitude of the zero-voltage remnant polarization (P_r, points A and D) after saturation with a large voltage ($+V_{cc}$) and by the magnitude of the coercive voltage (V_c), the minimum value of the voltage necessary to reverse, or switch, the polarization state. To apply these ferroelectric characteristics to a memory, the two net

stable states, "upward polarization" and "downward polarization", are defined as "1" and "0" signals [36]. Writing "1" or "0" data to a cell requires the application of the voltage $+V_{cc}$ or $-V_{cc}$ to both electrodes of the ferroelectric capacitor.

2.2.3 Developmental status

Two major technical limitations of polymer FeRAM are degradation and scaling problems. The degradation problem is associated with the read-out operation for a ferroelectric capacitor. It consists of applying a field and measuring the displacement response that is either high or low, depending on the initial polarization direction. If the response is high, then the previously stored orientation needs to be restored with a second programming operation. This kind of a read-out operation can affect the stored information (destructive read-out). A major disadvantage of this mode of operation is that the number of programming cycles of the device is enormous (10^{12} cycles [47]). Unfortunately, ferroelectric capacitors degrade when they are programmed repeatedly. The amount of ferroelectric polarization decreases with the number of programming cycles. This decrease makes it harder (and eventually impossible) to sense the displacement charge response during the read operation.

The second major disadvantage of using ferroelectric capacitors is their scaling behavior. Reduction of the capacitor area is highly desirable to increase the memory density. The average current during a ferroelectric switching event scales with capacitor area and ferroelectric switching time: a reduction in area will therefore reduce the signal.

2.3 Transistor-type memories

Inorganic transistors are widely used in conventional semiconductor memories. As already said in Chapter 1, for example, a SRAM cell is typically made of six field-effect transistors and a FLASH memory cell is made of a floating gate transistor. Organic transistors have also shown potential applications in memories. Organic thin-film transistors (OTFTs) are particularly interesting as their fabrication process is usually simpler than the one employed in the conventional silicon technologies. Compared to capacitor-type, one of the main advantages of transistor-based memories is that they have no cross-talk problems between adjacent memory cells, it provides for non-destructive read-out, for stable data sensing, and excellent compatibility with integrated circuits. In the following, Organic Field-Effect Transistor will be considered.

2.3.1 OFETs: materials and device structures

The organic transistor is generally fabricated using the thin film transistor (TFT) configuration already employed for inorganic transistors based on low mobility semiconductors. It is composed of three main components, as illustrated in Figure 2.2: 1) source (S), drain (D) and gate (G) electrodes; 2) a dielectric layer; 3) an active semiconductor layer [48]. The separation between the source and drain electrodes defines the channel length (L), ranging typically from 10 to 100 μm; the width of the electrodes defines the channel width (W) and is usually between 100 μm and 1 mm. Within the basic TFT design, there are two types of device configuration: top contact and bottom contact (Figure 2.2 (a) and (b)). In the former, the source and drain electrodes are fabricated onto a predeposited semiconductor layer, whereas the latter is constructed by depositing the active layer over the contacts.

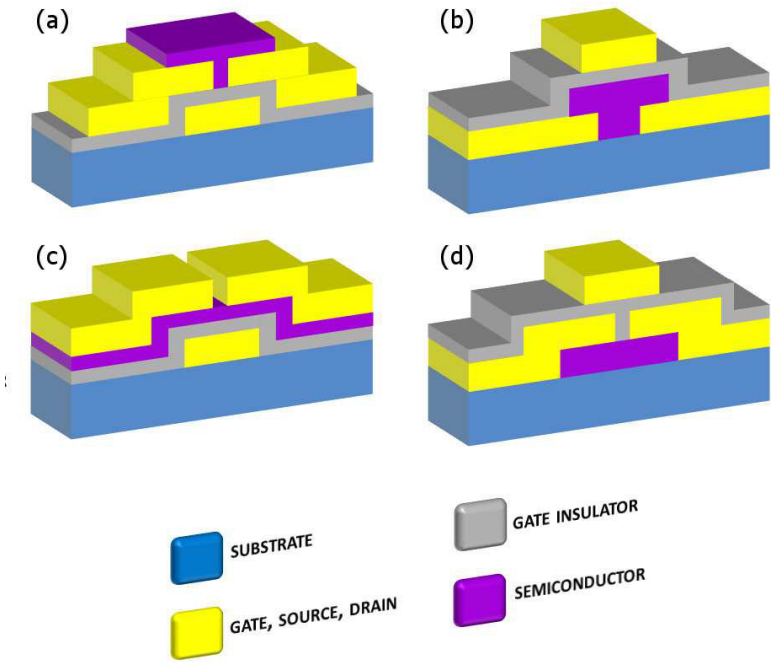


Figure 2.2: OFET configurations: a) bottom gate/bottom contact; b) bottom gate/top contact; c) top gate/bottom contact; d) top gate/top contact. [36].

The device is usually supported by a glass, wafer, or plastic substrate. The electrodes can be n-or p- Si, Indium Thin Oxide

(ITO), Poly(3,4-ethylenedioxythiophene) Polystyrene sulfonate (PEDOT:PSS), gold (Au), alluminum (Al) and other conductors. Among them, Au electrodes are often used for polymer-based FETs because its work function of around 5 eV creates an ohmic contact with conjugated polymers, such as polythiophene, since they typically have an ionization potential of around 5 eV. The dielectric material can be an inorganic or a polymeric insulator, whereas, the active layer has to be made out of an organic semiconductor.
The semiconductor is a critical functional component of an OFET. A large variety of organic materials have been used over the years. Depending on the nature of the charge carriers, the semiconductor can work either as a p-type or n-type semiconductor. In p-type semiconductors, the majority carriers are holes, while in n-type semiconductors, the majority carriers are electrons. Accordingly, the transistors are p-type transistors or n-type transistors.
OFETs are close relatives of the classic Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). If compared to inorganic ones, organic semiconductors are characterized by a low conductivity. Therefore, Thin Film Transistor (TFT) architecture is typically preferred in this case. One of the main differences between an OFET and the classic MOSFET is that, while the latter typically works in inversion mode, OFETs usually work in accumulation mode. When a negative (positive) voltage V_{GS} is applied between the gate and the source electrodes, an electric field is induced in the semiconductor that attracts positive (negative) charge carriers at the semiconductor/insulator interface between source and drain electrode and overlapping with the gate. Applying a negative (positive) voltage between source and drain electrodes V_{DS}, it is possible to drive the positive (negative) charge carriers across the channel area. Charge transport in OFETs is substantially two-dimensional. Charge carrier accumulation is highly localized at the interface between the organic semiconductor and the gate dielectric, and the bulk of the material is hardly or not affected by gate induced field. The threshold voltage V_{th} can be hence defined as the minimum gate-source voltage V_{GS} necessary to create the channel. With an increase in V_{GS}, a layer of mobile charges, injected by the source, can accumulate at the interface between the semiconductor and the insulator. When a sufficient density of carriers is collected, and a percolation path is established, the channel of the device is created. Consequently, the OFET current I_{DS} increases due to the increased charge carriers in the semiconductor and thus the transistor is in the ON state. Generally, two main working regimes are considered for OFETs, according to the applied V_{DS}. Indeed, if for a given value of the gate voltage, $V_{DS} < V_{GS} - V_{th}$, the device is in its *linear regime*, and its current

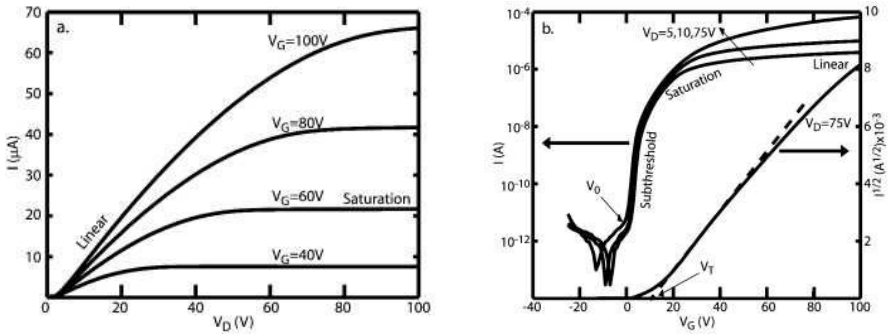
could be written as

$$I_{DS,lin} = \frac{W}{L}\mu C_i V_{DS}\left(V_{GS} - V_{th}\right) \tag{2.1}$$

If $V_{DS} > V_{GS} - V_{th}$, the current value becames independent of the applied V_{DS}, and the device reaches its *saturation regime*,

$$I_{DS} = \frac{W}{L}\mu C_i \left(V_{GS} - V_{th}\right)^2 \tag{2.2}$$

FETs are typically characterized in one of two ways, either by holding V_{GS} constant and sweeping V_{DS}($I_{DS} - V_{DS}$ or output curves `Figure 2.3 (a)`) or by holding V_{DS} constant and sweeping V_{GS} ($I_{DS} - V_{GS}$ or transfer curves `Figure 2.3 (b)`) [49] .



(a) (b)

Figure 2.3: (a) Typical $I_D - V_D$ curves for an OFET for various values of V_G. (b) Typical ID−VG curves for the same device for various values of V_D [49].

For describing materials and device performance, charge mobility is one of the most significant parameters. It describes how easily charge carriers can move within the active layer under the influence of an electric field and it is, therefore, directly related to the switching speed of the device. Another important parameter is the ON/OFF current ratio, defined as the ratio of the current in the ON and OFF states. It is indicative of the switching performance of a FET. A low intrinsic conductivity (OFF current) is desired to eliminate leakage while in the inactive state. To achieve a high ON state current I_{DS}, OFETs are usually operated at very large voltages, typically greater than 30–50 V. Such large biases will incur excessive power consumption. A viable approach to substantially increase I_{DS}, while operating at a low bias, is to increase the capacitance of the dielectric [49].
The crucial parameters for a dielectric insulator are the maximum possible electric displacement $D_{max}(= \varepsilon\kappa E_B)$ the gate insulator can

sustain, and the capacitance per area $C_i(= \varepsilon/d)$, wherein ε is the permittivity of vacuum, κ is the dielectric constant, E_B is the field for dielectric breakdown and d is the insulator thickness. Thus, to minimize operation voltages and improve ON/OFF ratios, high-κ dielectric materials are desirable. Another advantage of high-k materials is that the thickness of the insulating layer does not need to be dramatically reduced, thus preventing greater leakage currents. However, high-κ materials can negatively affect the carrier mobility because they usually have randomly oriented dipole moments near the interface, which can increase the energetic disorder inside the semiconductor. For these reasons, when the mobility it's high enough it's possible to use low-κ dielectrics. A benefit of the low-κ dielectric is a reduced hysteresis between forward and reverse sweeps of the gate and in some cases improved V_{th}. The lifetime and stability of a homogeneous low-k dielectric is also likely to be better [50].

2.3.2 OFET-based memories

Control over source–drain current in OFETs via a third terminal has resulted in their widespread application in switches, shift registers and logic elements. Nevertheless, in such application fields, OFETs are volatile, which means that when V_{GS} is removed, the accumulated charges are depleted and the transistor switches off. In order to employ a transistor as a non-volatile memory device, it is necessary to create a bistable behavior, by inducing, for instance, charge storage in different areas of the device, such as the bulk of the dielectric layer, or at the interfaces between the gate contact and the semiconductor channel. An additional voltage, via charge storage or polarization, is thus introduced between the gate and the semiconductor channel to alter the charge distribution in the transistor. This phenomenon results in a shift of the threshold voltage or hysteresis in the transfer curve. On the basis of charge storage and polarization methods in the dielectric layer or interfaces, OFET memories can be divided into three categories (`Figure 2.4`):

- **floating gate OFET memory**: charges carriers are stored on a conducting or semiconducting layer (floating gate) completely sorrounded by a dielectric; this dielectric layer is used to block the transfer of charge carriers between the gate and the floating gate during programming/erasing operation `2.4 (c)`;

- **charge trapping OFET memory**: charge carriers are trapped in the gate dielectric which has a quasi-permanent electric charge or dipolar polarization `2.4 (e)`;

- **ferroelectric OFET memory**: the gate dielectric is a ferroelectric material, which can adopt either of two stable polarization states, because of its remanent polarization 2.4 (f).

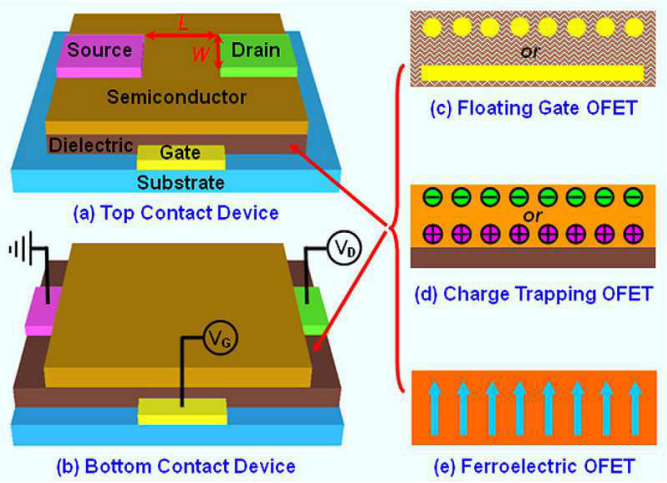


Figure 2.4: (a) top contact and (b) bottom contact OFETs, with different dielectric layers, for exhibiting memory effects: (c) floating gate OFET, (d) charge trapping OFET and (e) ferroelectric OFET. [36].

2.3.3 Floating gate transistor memories

The idea of using a floating gate transistor to obtain a non-volatile memory was suggested for the first time in 1967 by Kahng and Sze [51] for MOSFETs. In a floating gate FET, the charges are stored on a conducting or semiconducting layer (floating gate) that is completely surrounded by a dielectric (Figure 2.4 (c)). The dielectric layer between the floating gate and the semiconductor must be very thin in order to obtain a sufficiently high electric field to allow the injection of charges toward the floating gate, yet be able to prevent back tunneling and current leakage. Charging the floating gate changes the V_{th} of the transistor because the charge on the floating gate partially screens the electric field between the control gate and the semiconductor. This V_{th} shift can be detected by measuring the drain current at a certain gate-source voltage. Because the floating gate is completely isolated by the dielectric, charge stored on the floating gate remains there without the need for any applied voltage (non-volatile memory). Thus, the dielectric layer between the floating gate and the gate electrode must be thick enough to prevent discharge when V_G is removed. To discharge the floating gate, a reversed voltage

is applied at the gate, removing the charges from the floating gate. Floating gate FET is commonly used for conventional semiconductor memories such as FLASH and EEPROM memory. An alternative, also pioneered in silicon, is the **nano floating gate memory**. In this kind of memory with discrete-trap storage node, the floating gate consists of multiple nanocrystal dots or charge trapping defects in an insulator. The multiple floating dots are separated and independent, and charges are injected to the dots via different paths. The retention time can be improved in the discrete-trap memory. Because the nano floating gate device mitigates charge loss to local tunneling oxide defects, it permits scaling of the tunneling oxide from about 10 nm for the conventional floating gate memory technology to about 5 nm. This, in turn, scales the operating power supply voltages from about 9 V to about 6 V [37]. While most studies have been performed with silicon nanocrystals, other nanocrystal materials can be chosen to optimize device performance.
In 2003, Kolliopoulou et al. [52, 53] demonstrated a hybrid silicon–organic memory device using gold nanoparticles as charge storage elements deposited by a chemical self-assembly technique. The nanoparticles are separated from the silicon channel by a 5 nm thermal SiO_2 layer and from the gate electrode by an organic insulator `Figure 2.5 a)`) deposited by the Langmuir–Blodgett technique at room temperature. Charge injection/rejection into the nanoparticles takes place by applying different low-voltage pulses (less than $\pm 6V$) to the gate electrode, resulting in significant V_{th} shift (`Figure 2.5 b)`). Charge retention measurements reveal that the device has nonvolatile behavior (`Figure 2.5 c)`).

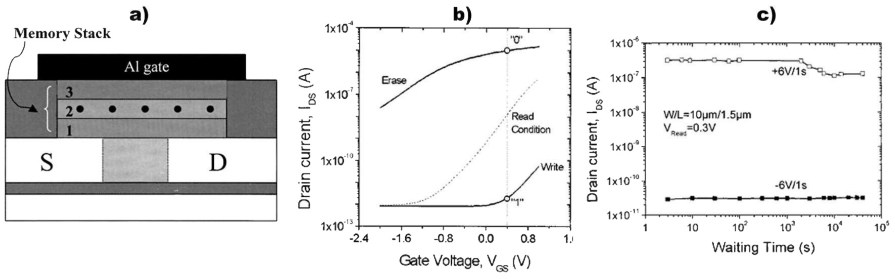


Figure 2.5: a) Schematic of the device: S and D are the source and drain of the device, with the channel area inbetween them. The memory stack is made of a 5 nm SiO_2 (bottom, numbered by 1), gold nanoparticle layer in the middle (2) and organic insulator on top (3). b) Write/erase process obtained by applying - 6 and 6 V voltage pulses, respectively. The pulse period was 1 s. c) Retention characteristics of sample after application of $\pm 6V$ on the gate for 1 s [52].

The device can be batch fabricated, and it does not show any change in its characteristics with time under normal ambient conditions. For efficient fabrication of the device, two very different processing technologies, silicon technology and organic thin film deposition, have to be adequately integrated. This technology also has the potential for fabricating low-cost silicon–organic hybrid memories, as well as all-organic memories at room temperature.
Benefiting from these pioneering works, Liu et al. [54] have integrated the self-assembled film of gold nanoparticles into the gate dielectric of an OFET to produce memory effects. The transistor is fabricated on a heavily doped n-type silicon (n^+ – Si) substrate with a thermally grown oxide layer of 100 nm in thickness. The n^+ – Si substrate serves as the gate electrode while the oxide layer functions as the gate dielectric. The gold nanoparticles behave as the floating gate for charge storage, and were deposited on the gate oxide by electrostatic layer-by-layer self-assembly method. A self-assembled multi-layer of polyelectrolytes, together with a thin spin-coated poly(4-vinyl phenol) (PVP) layer, covers the gold nanoparticles and separates them from the poly(3-hexyl thiophene) (P3HT) semiconductor channel. The device fabrication process is shown schematically in Figure 2.6.

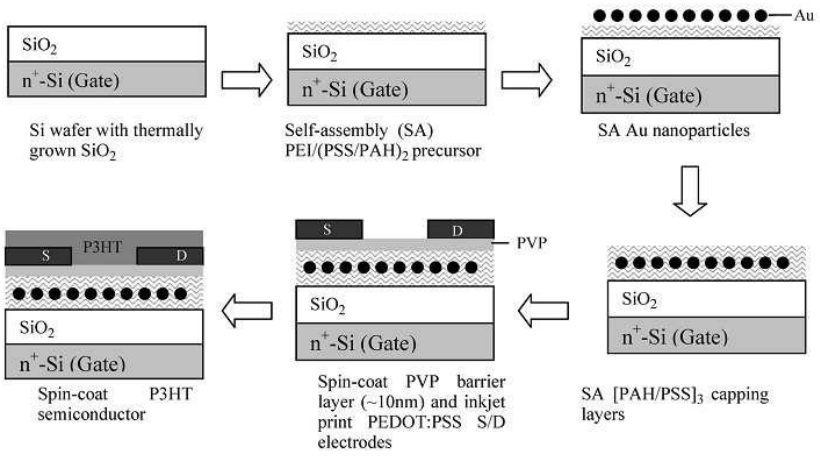


Figure 2.6: Schematic illustration of the fabrication process of a nano floating gate OFET for non-volatile memory application[54].

Gold nanoparticles (Au NPs) are charged or discharged with different gate bias so that the channel conductance is modulated. The transistor exhibits significant hysteresis in its $I_D - V_G$ characteristics (Figure 2.7 a)). Charge storage in the Au NPs is confirmed by comparing the electrical characteristics with those of the Au NP-free

devices, although the effects of interfacial traps are also significant (Figure 2.7 b)). The memory transistor has an ON/OFF current ratio over 1500 and data retention time of about 200 s (Figure 2.7 c)). The short retention time can probably be attributed to the poor insulating property of the PVP barrier layer and the fast release of charges from interfacial traps.

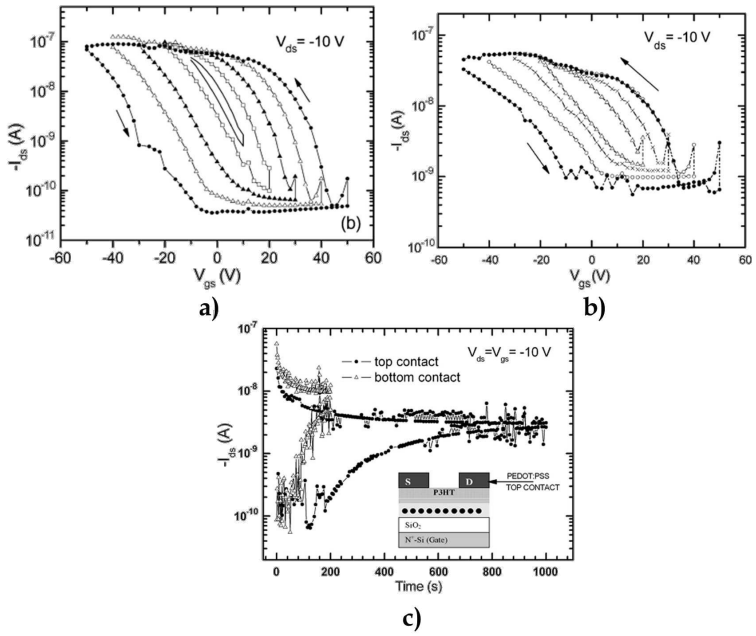


Figure 2.7: a) Transfer characteristics of the organic transistor memory device. b) Transfer characteristics of OFET without gold nanoparticles in gate dielectric. c) Data retention of the organic transistor memory device [54].

Zhen et al. [55] reported an all-organic memory device with copper phthalocyanine (CuPc) as an active channel and e-beam-deposited Au NPs inside a polyimide gate dielectric layer (Figure 2.8). Holes are injected from CuPc into the Au NPs by application of a negative gate bias by tunneling. The stored charges could be expelled from the Au NPs into the CuPc under the positive gate bias to erase the memory. Current–voltage (I–V) measurements at room temperature show the memory behaviour of the devices: an anticlockwise hysteresis loop is observed when a bi-direction scan voltage is applied to the gate electrode. To confirm the charge storage effect of gold nanocrystals embedded in the dielectric, a control sample without gold nanocrystals is tested: negligible hysteresis is seen in the transfer characteristic of the control sample. Since the control sample has

the same processing flow as the sample containing gold nanocrystals, the absence of hysteresis for the control sample can lead to the conclusion that the charging effect is attributed to the existence of gold nanocrystals.

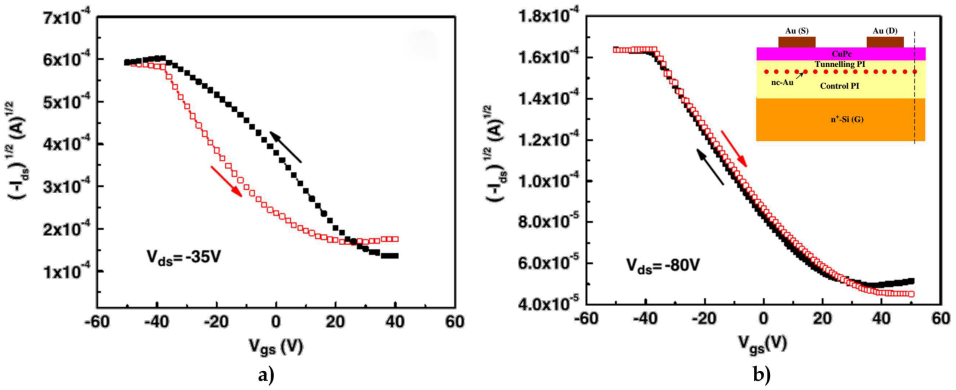


Figure 2.8: a) Transfer characteristics with bi-direction scan gate voltage ranges of the device with nc-Au embedded in polyimide gate dielectrics. b) Transfer characteristics with bi-direction scan gate voltage ranges of the control sample without nanocrystal Au embedded. In the inset: schematic cross section of the organic nanocrystal memory with three sequential layers of PI/nc-Au/PI (with a thickness of 250, 2, 50 nm) as a whole insulator layer [55].

Recently, Sekitani et al. [56] have developed flexible floating gate transistors with small program and erase voltages (–6 V to +3 V); it is one of the best results reported to date for floating gate OFET memory. The control and floating gates are layers of evaporated aluminum with a thickness of 20 nm, the top and bottom dielectrics are both a combination of an aluminum oxide (AlO_x) layer (4 nm thick) grown through an oxygen plasma treatment, at room temperature and an alkyl-phosphonic acid self-assembled monolayer (SAM) (2 nm thick) prepared from solution at room temperature. The small thickness of the dielectrics allows very small program and erase voltages ($\leq$6 volts) to produce a large, nonvolatile, reversible threshold-voltage shift. As shown in `Figure 2.9 c)`, when the applied voltages are – 6 V and + 3 V, the floating gate is charged and discharged, causing a threshold-voltage shift and hysteresis in the current-voltage characteristics. The transistors endure more than 1000 program and erase cycles, which is within two orders of magnitude of silicon-based floating gate transistors widely employed in FLASH memory.

In 2010, Baeg et al. [57] developed flexible nano-floating gate memories by embedding in the gate dielectric different sizes of ther-

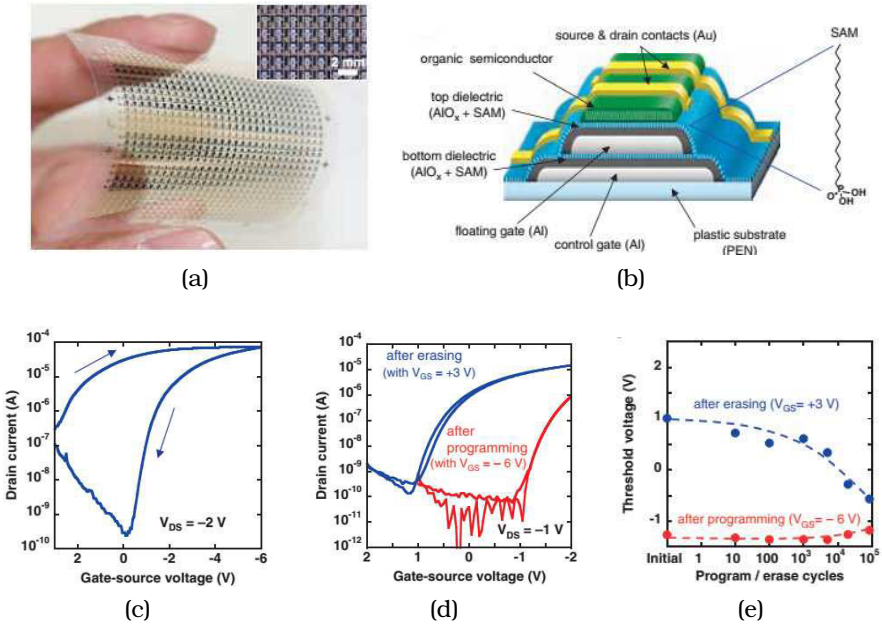
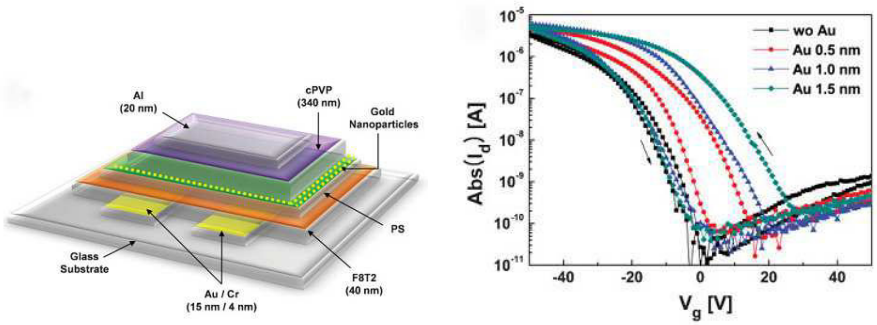


Figure 2.9: a) Photograph of an organic floating-gate transistor sheet comprising 26 by 26 memory cells (effective area: 50×50 mm^2. The inset shows a magnified image of the array. b) Schematic cross section of the floating-gate transistors. c) Drain current as a function of the voltage applied between control gate and source contact. d) Read-out operation performed on a floating gate transistor after programming and after erasing for 1 s. e) Endurance of the memory transistors [56].

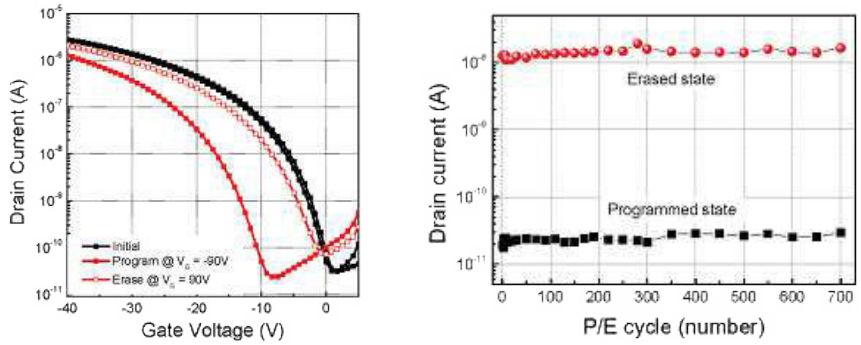
mal deposited gold (Au) nanoclusters as electrons trapping elements at the interface between the layer of polystyrene (PS) (tunnelling dielectric layer) and cross-linked poly(4-vinylphenol) (PVP) (blocking dielectric layer) (Figure 2.10 a)). The top-gate bottom-contact FLASH memory was fabricated on a polyethylene naphthalene (PEN) substrate with the solution-processed poly [9,9 - dioctylfluorenyl - 2,7 -diyl]- co - (bithiophene) (F8T2) as semiconductor layer. The flexible memory device showed large memory window ($\sim 40V$) and high ON/OFF ratio ($> 10^3$) (Figure 2.10 b)).
As an alternative, electrostatically self-assembled metal NPs monolayer has also been applied for flexible floating gate FLASH memory. For example, Kim et al. developed flexible FLASH memory on plastic substrates with the device structure polyether sulfone (PES)/Ti/ Au gate/PVP/3-aminopropyltriethoxysilane(APTES)/Au NPs/PVP/pentacene/Au source-drain electrodes. Large memory window (∼ 10 V) was achieved under –90 V/ +90 V programming/erasing operation (Figure 2.11 a)). The endurance (> 700 cycles), data retention (around 50 % loss more than one year) and bending cyclic

(> 1000 cycles) measurements confirmed that the flexible FLASH memory exhibited good electrical reliability as well as mechanical stability.



(a) (b)

Figure 2.10: a) Schematic of a top - gate bottom - contact polymer field - effect transistor. b) Transfer characteristics of F8T2 FET devices after thermal evaporation of different thicknesses of Au, from 0.5 to 1.5 nm [57].



(a) (b)

Figure 2.11: a) Transfer curve of the memory device at initial state, programmed state and erased state. The program/erase operation is application of –90V/ +90 V for 1 s. b) Endurance characteristics of flexible organic memory devices with respect to the number of program/erase operations. [58].

A relatively short retention time and high operating voltages are two main challenges for the development of recent FLASH memories. The short retention time could be improved by more adequate selection of robust tunnelling dielectrics with densely packed molecules

that should lead to a reduction of the leakage current. The operation voltage is related to the capacitance and thickness of dielectric layer so that it can be reduced by using thinner pinhole-free blocking dielectric layer with high dielectric constant and large dielectric breakdown strength. Anodization of aluminium, for instance, represents a good candidate for the realization of dense barrier oxide film with excellent dielectric properties that could be grown on flexible substrates. Kaltenbrunner et al. [59] showed that potentiostatically anodized aluminium could be versatile blocking and tunnelling dielectric layers for room temperature processed flexible non-volatile FLASH memories operating below 5 V. Memory devices were fabricated on different flexible substrates including PEN and polyimide (PI). A large charge retention time exceeding 10^5 s with minor degradation of the memory window was observed (Figure 2.12).

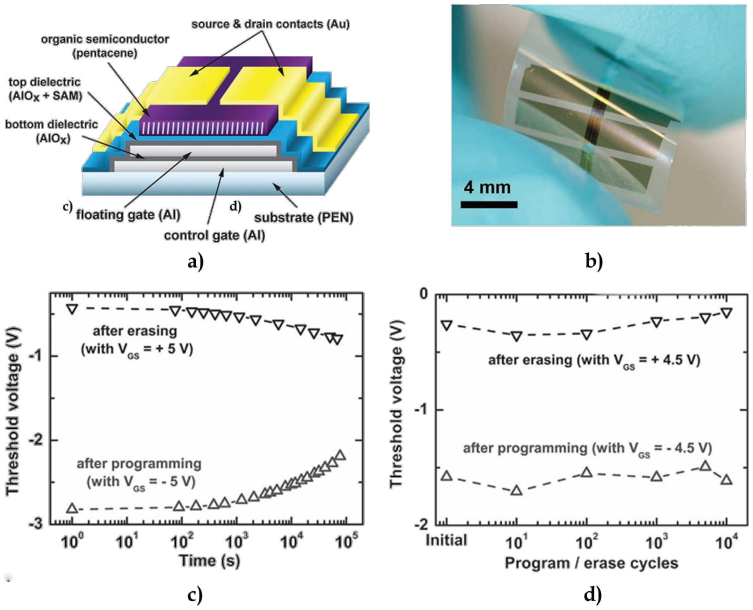
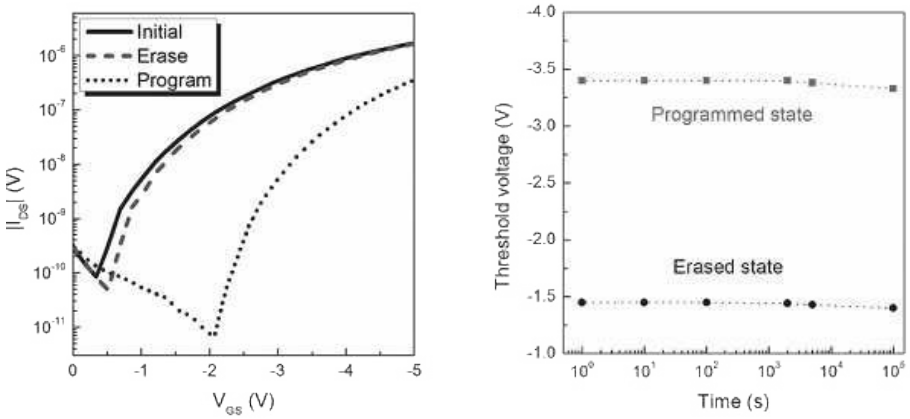


Figure 2.12: a) Schematic diagram of the non-volatile organic memory element on flexible substrates with a potentiostatically anodized aluminum oxide control gate (8.5 nm) and a floating gate (8.5 nm) dielectric. b) Photograph showing the bending flexibility of the memory transistors. c) Time evolution of the threshold voltage after programming (black upward pointing triangles) and after erasing (grey downward pointing triangles), showing a small degradation of the memory window after 10^5 s. d) Memory window versus program and erase cycles; no observable degradation after 10^4cycles [59].

Utilizing double floating gate architecture is another efficient

protocol to improve the retention capability for FLASH memories. Recently, a new architecture for low voltage FLASH memories based on solution processed layer-by-layer assembled reduced graphene oxide (rGO) sheets-Au NPs hybrid double floating gate on the flexible PET substrate has been reported [60]. In comparison with single Au NP floating-gate memory devices, the FET characteristics, including mobility ($\mu = 0.1cm^2V^{-1}s^{-1}$) and ON/OFF ratio ($3 \times 10^4$), are significantly improved in rGO sheets/Au NP double-trapping-layer memory devices. Most importantly, the memory characteristics, including the memory window (1.95 V) and the retention capability ($> 10^5 s$), are improved (`Figure 2.13`). The proposed memory device demonstrates a strong improvement in both FET and memory characteristics.



(a) (b)

Figure 2.13: a) Transfer characteristics of double floating gate memory device at the intial state, the programmed state, and the erased state. b) Data-retention capability as function of the retention time of double floating gate memory device [60].

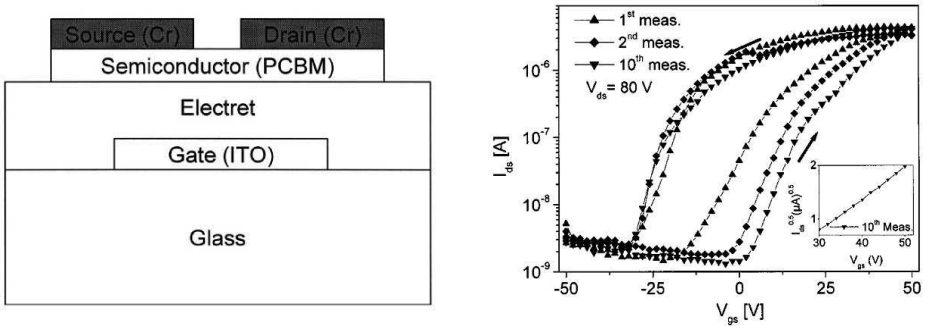
2.3.4 Charge trapping transistor memories

In charge trapping transistor memory, the charge carrier is stored in an appropriate dielectric layer with electret properties. An electret is defined as a dielectric material that has a quasi - permanent electric charge or dipolar polarization, including ferro -, piezo -, and pyro - electric polymers [61]. The only difference between the floating gate and charge trapping transistor memory is the charge storage layer in which conductive floating gate is replaced by the insulating dielectric layer.

In 2002, Katz et al. [62] firstly demonstrated a memory transistor

based on an OFET configuration with a polarizable gate insulator (and subsequently others [63, 64]). In these devices, hexadecafluorocopper phthalocyanine (F15-NTCDI, n-type), and a series of mixed phenylene(P)–thiophene (T) oligomers (such as PTPTP, p-type) with terminal n-hexyl groups (to improve solubility, such as dH-PTTP and dH-PPTPP), or terminal perfluoroalkyl groups (such as DFO-PTTP,n-type), are used as the semiconductor. Four dielectric materials, including two inorganics (SiO_2 and glass resin) and two hydrophobic polymers (poly(α-methylstyrene), or $P\alpha MS$, and TOPAS (cyclic olefin copolymer), are used. The OFETs exhibit a reversible, tunable, and stable memory effect with a quasi-stable V_{th} shift. In particular, programming voltages V_{prog} were applied via the gate relative to a common source and drain voltage for a continuous period of time varying between 1 and 25 minutes. It turned out that a negative (positive) V_{prog} always induces a shift of the transistor threshold voltage V_{th} towards less negative (more positive) values. The authors proposed a possible mechanism for this memory effect in which static charges induced by the programming voltage are injected between the semiconductor and gate electrode, either in the bulk of the dielectric and/or at one or both dielectric interfaces. This phenomenon results in a shift in the electrical potential between the gate and the semiconductor and alters the charge distribution in the transistor. The best performance is observed for fluorooctyl-substituted oligomer (DFO-PTTP), which exhibits a mobility of $\backsim 0.1 cm^2 V^{-1} s^{-1}$ and an ON/OFF current ratio of $\backsim 10^7$. This oligomer also exhibits the largest transistor memory effect for this class of semiconductors [64]. However, the stability of stored charges and the overall device reliability of OFET are inadequate for long-term applications.
In 2004, Singh et al. [65] reported the first OFET memory elements containing an electret as gate insulator. Polyvinyl alcohol (PVA) was used as gate insulator and PCBM (methanofullerene [6,6]-phenyl C_{61}-butyric acid methyl ester) as n-channel semiconductor (`Figure 2.14 a)`). A large hysteresis was observed in the transfer characteristics cycling the gate voltage (`Figure 2.14 b)`). The magnitude of the source–drain current I_{DS} increases up to 10^4 at $V_G \approx 50V$ with respect to the initial OFF state with $V_{GS} = 0V$. However, I_{DS} remain at high values even when V_{GS} reduces back to 0 V. In order to completely erase the memory, a reverse voltage $V_{GS} \approx -30$ V should be applied. A large shift in V_{th} by 14 V is observed when measured for the second time with respect to the initial cycle. Each measurement is performed with a long integration time of 1 s and a step voltage of 2 V, indicating that there is minimal gate bias stress in these devices. This observation is proposed to be due to locally trapped charges that induce shifts in V_{th}. The ON state can be retained for

more than 15 h, which implies that once the electret is fully charged, the relaxation of charges is a slow process, as expected for charged electrets. The switching effect cannot be explained by a dipole polarization mechanism of the electret either, since capacitance voltage measurements show negligible hysteresis. Therefore, trapping of the injected charges has been proposed.



(a) (b)

Figure 2.14: a) Schematic of the non-volatile memory OFET. b) Transfer characteristics of the OFET with $V_D = 80V$ demonstrating the non-volatile organic memory device. Each measurement was carried out with an integration time of 1 s. Inset:$(I_D)^{0.5}$ vs V_g plot for the tenth measurement [65].

Recently, the hydrophobic polymer electret, PαMS, has also been used by Baeg et al. [66] in another OFET memory with pentacene as the semiconductor and SiO_2 as the gate insulator (`Figure 2.15 a)`). This OFET memory device displayed reversible shifts in the threshold voltage (V_{th}) when an appropriate gate voltage (V_G) was applied above a certain threshold via a relatively short switching time. `Figure 2.15 c)` shows shifts in the transfer curve for this OFET memory after applying an appropriate V_G within a relatively short time (1 µs). The entire transfer curve was substantially shifted in the positive direction when a large gate bias V_G = 200 V was applied for 1 µs, and it was then steadily sustained at the shifted position during subsequent sweeps. As a result, V_{th} was changed by more than 90 V. On the other hand, the shifted transfer curve returned to its initial position when a reverse gate bias V_G = –100 V was applied for 1 µs. In addition to the positive direction shift, the transfer curve could also be substantially shifted in the negative direction by a reverse gate bias, as depicted in `Figure 2.15 d)`.

This OFET device shows a large memory window (about 90 V), a high ON/OFF current ratio (10^5), a short switching time (less than $1\mu s$), and a long retention time (more than 100 h). These memory

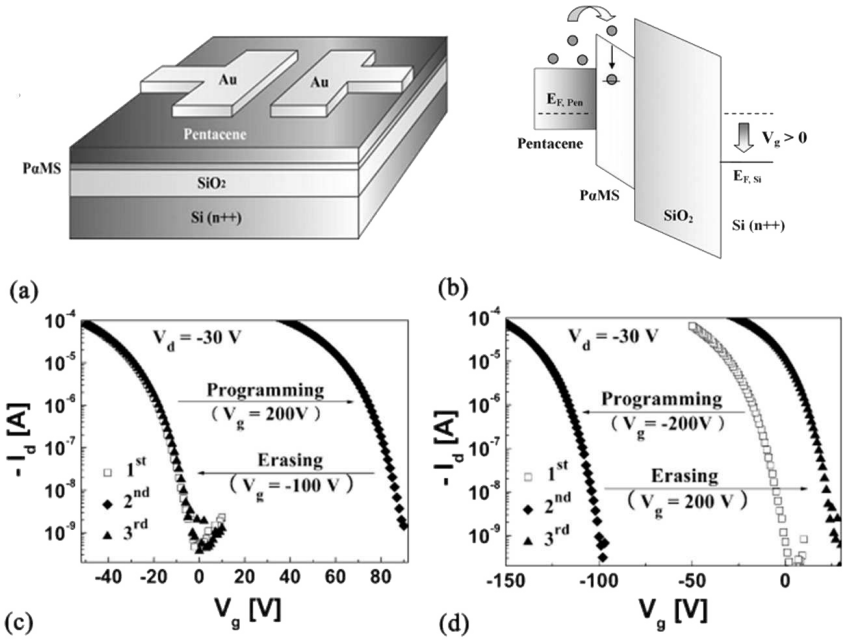
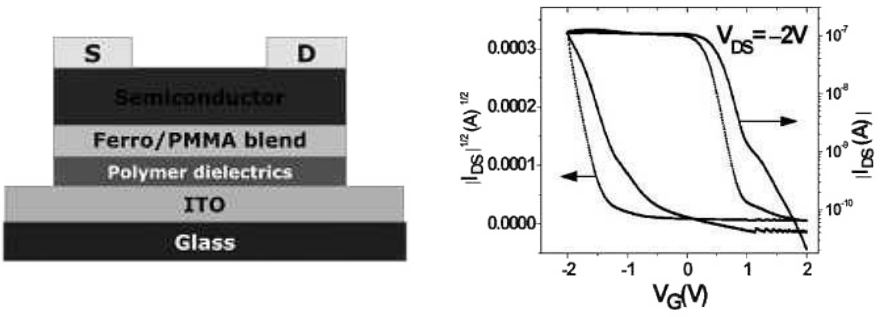


Figure 2.15: a) Schematic of the OFET memory device. b) Proposed model for charge transfer and trapping between pentacene and PαMS, where $E_{F,Pen}$ and $E_{F,Si}$ are the Fermi energies of pentacene and silicon, respectively. c)-d) Shifts in transfer curves at V_D = – 30 V in the c) positive and d) negative directions for an OFET memory device with a 300 nm thick SiO_2 layer [66].

characteristics can be obtained only when an appropriate polymeric gate electret layer (e.g. PαMS) is inserted between the SiO_2 gate insulator and the pentacene channel in the typical OFET structure. Indeed, when a pentacene OFET device was fabricated without a PαMS layer, no significant shifts in V_{th} were observed under the same gate bias conditions that were used in the previous experiments. Therefore, the shifts in V_{th} and memory behavior in the OFET memory device originate from the additional electret layer. Since PαMS has a weak polarity due to its nearly symmetrical chemical structure, the mechanism might not be dipolar polarization. In addition, the device only exhibits weak hysteresis behavior between the upward and downward scans for the transfer curve. Thus, the trapped charges at the interface between pentacene and PαMS have little effect on the memory characteristics in this OFET memory device. The shifts in V_{th} after the programming process are therefore thought to be due to the effect of trapped charges in the PαMS layer via charge transfer between the pentacene and the PαMS layer. This result indicates

that the additional PαMS gate dielectric layer behaves as a polymeric gate electret, similar to a floating gate in a FLASH memory. Although the exact mechanism for charge transfer and trapping in PαMS in this OFET memory device was not precisely understood at that time, the authors proposed a potential mechanism, which is schematically shown in 2.15 b). When mobile hot carriers are field-generated in pentacene near the interface, they are transferred into the polymer by the transverse electric field. In this model, the applied transverse electric field simultaneously facilitates charge transfer by reducing the effective thickness of the potential barrier at the interface. Therefore, once charges are transferred into the polymer, most of these electrons are trapped deeply in a very short period of time.
In 2008, Wu et al. [67] reported high performance OFET memory elements with steep hysteresis loops using donor-polymer-blend buffer layers containing a donor-polymer blend on a SiO_2 gate insulator. For comparison, the compounds tetrathiafulvalene (TTF), ferrocene (Fc) and 5, 10, 15, 20-tetra-phenyl-21H, 23H-porphine nickel (II) (NiTPP) were chosen as donors, while poly (ethylene oxide) (PEO), PS, polycarbonate (PC), and PMMA were used as the blend matrix (Figure 2.16 a)).



(a) (b)

Figure 2.16: a)Schematic drawing of the organic transistor memory elements using a cross-linked polymer as the dielectric. b) Typical transfer characteristics of memory devices with a crosslinked polymer as the dielectric [67].

These devices exhibited steep hysteresis loops with an on/off memory ratio of up to 2×10^4, and a retention time greater than 24 h. A low operational voltage is essential for practical applications. To achieve a low operating voltage, OFET devices were fabricated containing polymer dielectrics (cross-linked PMMA, with 1,6-bis(trichlorosilyl)hexane as a cross-linking agent) and a donor /

polymer blend buffer layer, which showed memory characteristics with a reduced operating voltage of less than 2 V (Figure 2.16 b)). This is one of the lowest operating voltages obtained for OFET memory to date.

A number of studies have been devoted to understanding charge trapping phenomenon in OFETs. In 2009, Debucquoy et al. [68] found that the mechanism of charge trapping is tunneling from the semiconductor channel into the gate dielectric. They studied the injection of electrons and holes in bilayer gate dielectric memory transistors, and demonstrated a reprogrammable ambipolar memory transistor in which trapping of electrons and holes from the transistor channel into the gate dielectric allows to program and erase the memory device at relatively low voltages. The transistors in this study had a bottom gate structure with top source and drain contacts as depicted in Figure 2.17 a). All devices were fabricated on a highly n-doped Si wafer, which serves as the gate electrode, with 20 nm of thermally grown SiO_2 on top. On this substrate, a thin (3-5 nm) layer of PαMS was deposited before a 40-nm thick layer of pentacene. Finally, source and drain contacts were made of gold. The typical measurement protocol was as follows. First, the initial characteristics were measured. The initial turn-on V_{ON} voltage of the device is defined as the gate-source voltage at which the drain current reaches 100 pA. Then, the device is subjected to a series of programming pulses, with intermediate gate voltage sweeps. The drain-source voltage during programming $V_{DS,prog}$ is always kept at 0 V. The exact measurement procedure is illustrated in Figure 2.17 d). First of all, two subsequent pulses with the same duration (t_{prog}) and equal but opposite gate voltage ($V_{GS,prog}$) were applied. The pulse with negative (positive) $V_{GS,prog}$ shifts the transfer characteristics towards negative (positive) V_{GS}. This is done twice to have a stable result. After each of the last two pulses, a small part of the transfer characteristics is measured to determine V_{ON}. V_{ON-} denotes the turn-on voltage after the negative pulse, and V_{ON+} denotes the value after the positive pulse. ΔV_{ON} is defined as the difference between V_{ON+} and V_{ON-} . This last value is the memory window between the two different memory states. Figure 2.17 b) shows the transfer characteristics obtained with with a series of programming pulses of $\pm$17 V and $\pm$20 V. In this case, t_{prog} was kept constant at 1.5 ms. A shift of the turn-on voltage with the same polarity as the gate voltage was observed. This is attributed to the trapping of electronic charges in the vicinity of the semiconductor/insulator interface. When pentacene is deposited directly on SiO_2, the change in turn-on voltage was less than 1 V. This indicates that the presence of the PαMS is key to achieve the desired charge trapping and that these charge

carriers are probably trapped in the polymer dielectric and/or at the interface between the polymer dielectric and SiO_2.

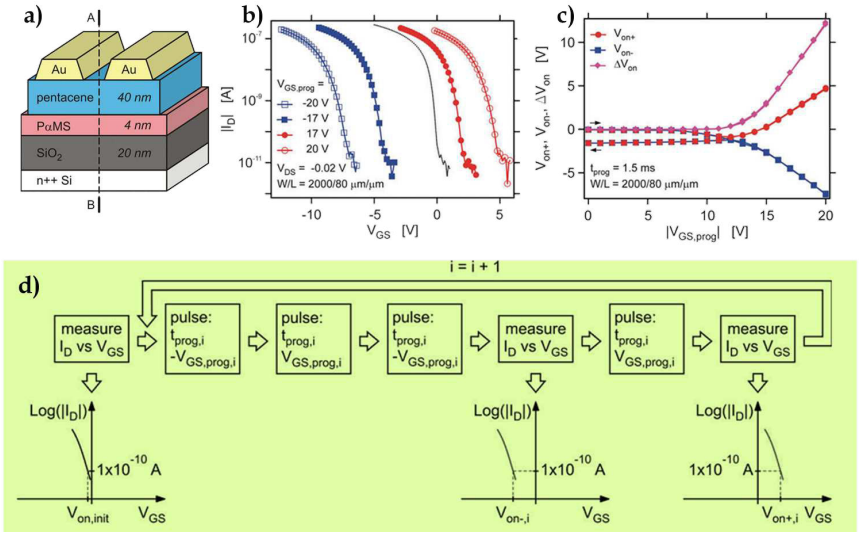


Figure 2.17: a) Schematic view of a pentacene memory transistor. b) Transfer characteristics of pentacene transistors: a shift of the turn-on voltage with the same polarity as the gate voltage is observed. c) V_{ON+}, V_{ON-} and ΔV_{ON} showed in function of $\mid V_{GS,prog} \mid$. d) Typical measurement protocol [68].

In `Figure 2.17 c)`, V_{ON+}, V_{ON-} and ΔV_{ON} are shown in function of $\mid V_{GS,prog} \mid$. For small values of $\mid V_{GS,prog} \mid$, the transfer characteristics are hardly changed. When $\mid V_{GS,prog} \mid$ increases, the effect becomes significant above a critical value of $\sim$ 10 V. ΔV_{ON} reaches a maximum value of 12 V for $\mid V_{GS,prog} \mid$ = 20 V. A number of important attributes, which makes this effect promising to utilize as memory cells, were observed. Firstly, the negligible threshold voltage shifts at low programming voltages allow non-destructive read-out. Moreover, the large value of ΔV_{ON} allows easy read-out as this is translated into a large difference in source-drain current for the different programmed states. Interestingly, V_{ON} can be shifted towards both positive and negative voltages by a sufficiently large respectively positive and negative pulse to the gate. This indicates that both electrons and holes are trapped in the gate dielectric. These results indicate that optimal memory performance requires charge carriers of both polarities, because the most efficient method to lower the programming field is by overwriting a trapped charge by an injected charge of opposite polarity. The programming voltage is dictated by the minimum gate field required to induce charge carrier tunnel-

ing into the polymer electret. Initial work reported relatively high programming voltages, as a result of the use of a thick SiO_2 layer. Recently, a device with a low operating voltage was demonstrated using very thin dual gate dielectrics (a 20nm thick SiO_2 layer and a 4 nm thick PαMS layer. This memory device could be written and erased at voltages as low as 15 V [69].
More recently, studies on flexible charge-trapping OFET memories have been reported. Indeed, the polymer electret is a promising candidate for flexible charge-trapping FLASH memories due to its solution-processability and low temperature fabrication process.
In 2012, Baeg et al. [70] reported a high-performance top-gated OFET memory using a polymer semiconductor with alkyl-substituted thienylenevinylene (TV) and dodecylthiophene (PC12TV12T) and bi-layered polymer dielectrics, i.e., P(VDF-TrFE) (poly(vinylidene fluoride - trifluoroethylene)) and electrets [poly(2-vinylnaphthalene) (PVN) and polystyrene (PS)]. The PC12TV12T OFETs with PVN /P(VDF-TrFE) showed excellent non-volatile memory characteristics: an opened memory window of more than 90 V, a high ON\OFF current ratio ($\backsim 10^5$), a relatively low operation voltage of less than 20 V, and a long retention time of $\backsim 10^7 s$, as well as a stable writing-reading-erasing cycling endurance and multi-level (two bits per one cell) memory capability. The excellent memory properties originated from efficient and reversible charge trapping and release in the PVN electret layer. However, the memory characteristics effectively disappeared after replacing PVN with PS. The PS /P(VDFTrFE) devices showed a small open memory window under low-bias conditions and a narrow memory window of $\backsim$34 V even at an applied bias of more than $\pm$90V (`Figure 2.18`). These distinctive memory characteristics between the PS /P(VDF-TrFE) and PVN /P(VDF-TrFE) devices were attributed to a different alignment of the energy levels for the charge transfer from the semiconductor to the electret.

2.3.5 Ferroelectric transistor memories

In a capacitor-type polymer FRAM (see `paragrah 2.2`), the stored datum is read out destructively, leading to degradation problem. The other problem is related to the scaling of FeRAM. Reduction in capacitor area is accompanied by reduction in current signal.
Another type of ferroelectric memory based on transistor was proposed in the 1950s [71]. The simplest layout of a FeFET comprises a metal-ferroelectric-semiconductor layer stack (`Figure 2.19 a)`), in which the ferroelectric layer serves as the gate dielectric. Sometimes another dielectric layer is inserted between the semiconductor and the ferroelectric material. The ferroelectric layer, because of its

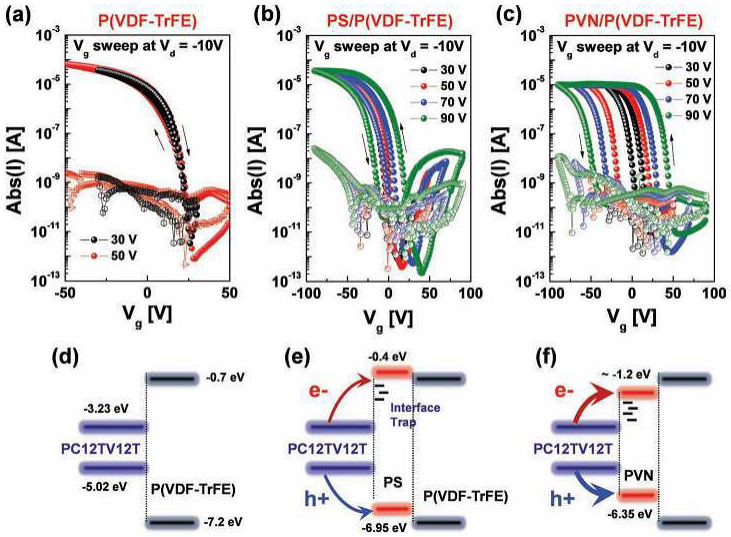
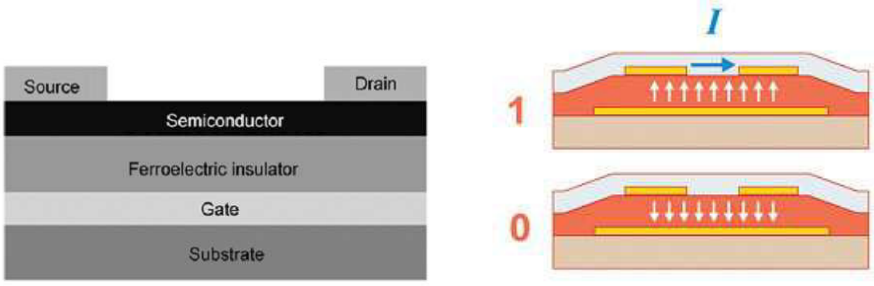


Figure 2.18: Transfer characteristics of the OFETs with a) P(VDF-TrFE), b) PS /P(VDF-TrFE), and c) PVN /P(VDF-TrFE) dielectrics. Schematic diagram for different modes of charge transfer and storage in each gate electret layer: d) P(VDF-TrFE), e) PS /P(VDF-TrFE), and f) PVN /P(VDF-TrFE) dielectrics [70].

remanent polarization, can adopt either of two stable polarization states. These states persist when no biases are applied. Switching from one polarization state to the other can occur by applying a sufficiently large gate bias.Depending on the direction of the polarization, positive or negative counter charges are induced in the semiconductor at the semiconductor-ferroelectric interface, effectively causing a positive or negative onset voltage shift of the transistor. Hence, a gate bias window, defined by the shifted onset voltages, exists wherein the drain current may have either of two levels depending on the actual polarization state of the ferroelectric gate dielectric. The corresponding drain current levels can be used to define “0” and “1” states of a non-volatile memory with nondestructive read-out. This is illustrated schematically in `Figure 2.19 b)`. Non-destructive read-out provides the advantage that the memory is not subjected to the destructive read/rewrite cycle commonly employed in ferroelectric capacitor memories, so the lifetime of the device is limited only by the number of times the memory is written.
Inorganic ferroelectric FET memories have been studied for decades. The major problems turn out to be injection and subsequent trapping of charges in the ferroelectric material and depolarization in response to a depolarization field. For FeFETs made from organic

materials, charge injection should not be a problem and the depolarization should not obstruct memory performance. Because of these features, most OFET memory devices are fabricated using organic ferroelectric (or ferroelectric-like) gate dielectric materials.



(a) (b)

Figure 2.19: Ferroelectric FET memory: a) Schematic diagram and b) basic cell [72].

In 1986 the first FeFET based on a polymeric ferroelectric was demonstrated [73]. It was shown that ferroelectric polarization within a film of P(VDF/TrFE) could induce an inversion layer in a bulk silicon semiconductor substrate. In 2001, Velu et al. [74] reported an OFET memory device comprised of an active layer of sexithiophene and a ferroelectric gate insulator of Pb (Zr, Ti) O_3 or PZT. Although the performance of this device was not good, since then, ferroelectric OFET memories have attracted extensive attention. In 2004, all-organic FeFET devices incorporating a ferroelectric-like polymer as the gate insulator and pentacene as the organic semiconductor were first reported by Schroeder et al. [75]. The ferroelectric-like polymer is a nylon, poly(m-xylylene adipamide), "MXD6". A clear hysteresis in transfer characteristic was observed with an ON/OFF ratio of 200 at V_g = - 2.5 V, and 30 at V_g = 0 V (`Figure 2.20 a)`). Importantly, the memory writing process is just like turning on a regular transistor, but subsequently the OFET can be read without an applied gate voltage. This is in contrast to other non-volatile electret transistor, which require charging with a high voltage of opposity polarity compared to normal operation and also necessitate a gate voltage to read the state. Retention time was around 3 h: `Figure 2.20 b)` shows that the memory loss over 3 hours is around 20%, after the initial drop. Unni et al. [76] fabricated a pentacene FeFET memory with P(VDF-TrFE) (70:30) as the gate insulator. They reported similar values for the ON/OFF ratio and retention time. In a follow-up paper [77], the MXD6 deposition was improved leading to much better memory characteristics. ON/OFF increased to 10^4,

data retention increased from hours to days (Figure 2.20 c)-d).

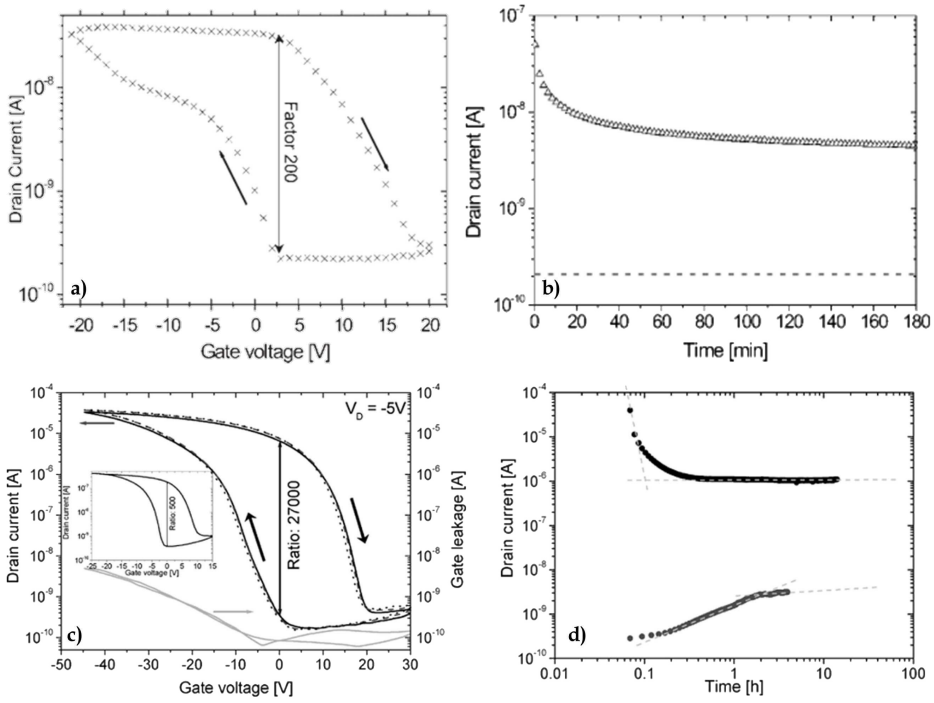


Figure 2.20: a) Transfer characteristic of an MXD6-Pentacene ferroelectric OFET [75]. b) Memory retention of the ON and OFF state for an MXD6-Pentacene ferroelectric OFET [75]. c) Transfer characteristic of an improved MXD6-Pentacene ferroelectric OFET [77]. d) Memory retention of the ON and OFF state for an improved MXD6-Pentacene ferroelectric OFET [77].

A major breakthrough was made in 2005 by Naber et al. [78] when they demonstrated high-performance solution-processed polymer FeFET memories consisting of P(VDF–TrFE)(65:35) as the gate insulator and MEH-PPV (poly [2-methoxy-5-(2'-ethyl-hexyloxy)-p-phenylene-vinylene]) as a semiconductor. The operation voltages of FeFETs are $\pm$ 60 V and $\pm$ 35 V, corresponding to ferroelectric layer thicknesses of 1.7 and 0.85 μm, respectively. The polymer FeFETs also have a long data retention time (> 1 week), a high programming cycle endurance (> 1000 cycles) and a short programming time (OFF to ON: 0.3 ms, ON to OFF: 0.5 ms). In particular, Figure 2.21 a) shows that the ON state is stable for a week, whereas the OFF current has an initial increase that stops after 1 day. This increase is largely due to an increased gate current and not due to the channel conductance. The ON/OFF ratio after a week is 10^4 and

it is completely stable. Figure 2.21 b) shows that even after 1000 programming cycles the devices still have considerable drain-current hysteresis. The high performance can be attributedto the lack of defects at the ferroelectric–semiconductor interface.

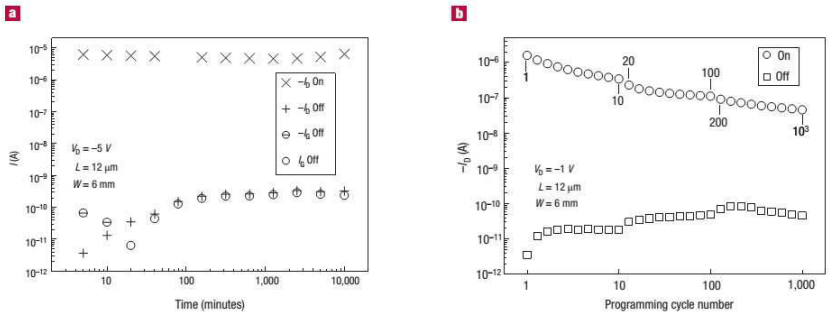


Figure 2.21: a) Data retention measurement obtained by programming the ON or OFF state once and monitoring the drain current at zero gate bias for a week. b) The ON and OFF state drain current at zero gate bias as a function of the number of applied gate voltage sweeps [78].

In spite of the encouraging developments, the operation voltages for polymer FeFETs are still quite high. To reduce the programming voltage and the gate insulator, thickness should be scaled down. However, when using thin films, a great deal of attention needs to be paid to the interfaces, electrodes and sample quality for devices to work reliably. In capacitors, using PEDOT:PSS as electrode material results in superior characteristics, particularly at low P(VDF-TrFE) layer thickness. Therefore, Gelinck et al. [79] fabricated all-polymer FeFETs using thin P(VDF-TrFE) films sandwiched between electrodes (gate and source/drain) made of conducting PEDOT:PSS. The electrodes were patterned by photoexposure of the deposited films. Alkoxy-substituted polyphenylene vinylene derivative, OC_1C_{10}, was used as p-type semiconductor and PCBM, a C_{60} derivate, was used as n-type semiconductor. All layers were solution processed by spincoating. The technology was scaled up to a wafer size of 150 mm. For both unipolar p- or n- type semiconductor channels, the transistors have a retention time of hours, can be switched in 0.1-1 ms at operating voltages less than 10 V (Figure 2.22).

Since then, several groups reported flexible organic ferroelectric FET based on pentacene and P(VDF-TrFE). Different approaches have been proposed that improve the ferroelectric/semiconductor interface (reduced surface roughness leads to higher mobility) and/or leakage current. For istance, Kang et al. [80] proposed a bottom gate FeFET containing PVDF/PMMA (80:20) blend films of 200 nm

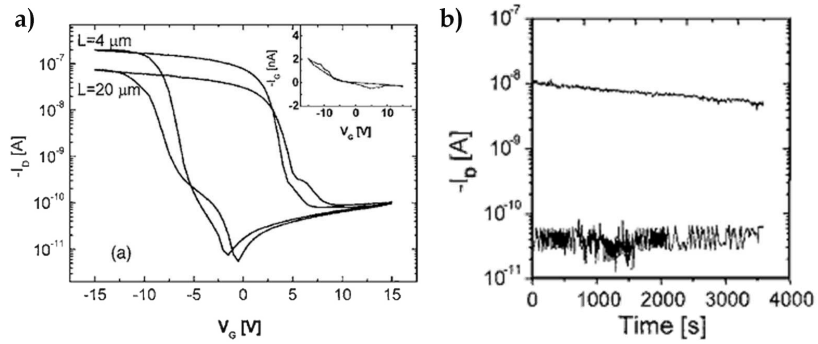
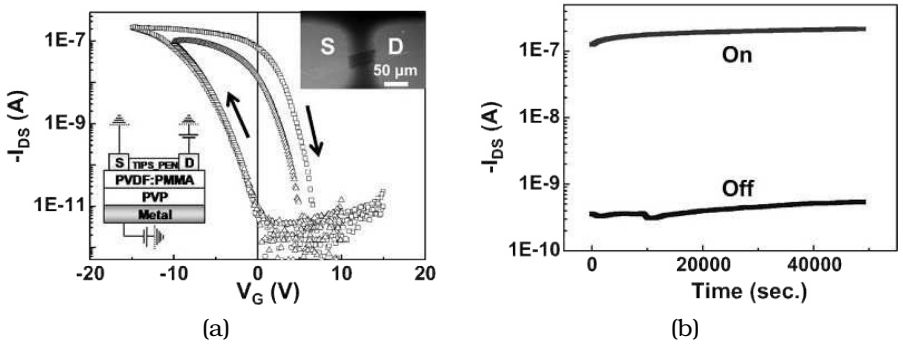


Figure 2.22: a) I_D–V_G curve of transistors with channel length 4 and 20 μm, recorded with V_D = − 2 V. Inset: I_G–V_G curve of the 20 μm transistor. b) Retention times of OC1OC10–PPV ferroelectric transistors with a 150 nm thick P(VDF/TrFE) gate dielectric layer [79].

thickness with low surface roughness. These devices exhibit an ON/OFF bistability ratio of 10^4 with data retention capability over 15 h at an operation voltage of 15 V (Figure 2.23). In that work, polycrystalline and single crystalline 6,13-bis(triisopropyl-silylethynyl) pentacene (TIPS-PEN) was used as the active semiconductor. Because the low surface roughness was equal or lower than the width of the accumulation layer, charge transport in the accumulation layer was not inhibited significantly.



(a) (b)

Figure 2.23: a)Transfer curve of a single-crystal TIPS-PEN FeFET with a thin PVDF/PMMA (80:20) gate insulator melt-quenched and subsequently annealed on a PVP layer at 150°C. The inset on the left depicts the schematic of the FeFET. The inset on the right shows an image of top view of the FeFET, visualizing the single crystal TIPS-PEN bridged between Au source and drain electrode. b) Data retention characteristics of a single-crystal TIPS-PEN FeFET [80].

In 2010, Yoon et al. [81] proposed a fully transparent non-volatile memory thin-film transistor with a hybrid-type gate stack composed of organic ferroelectric P(VDF-TrFE) and oxide semiconducting Al-Zn-Sn-O (AZTO) layers and ITO electrodes. A 6nm thick Al_2O_3 layer was in between the AZTO and P(VDF-TrFE) to protect the AZTO during the coating and etching processes of P(VDF-TrFE) (`Figure 2.24 a)`). The field-effect mobility, on/off ratio, and gate leakage currents were obtained to be 32.2 $cm^2V^{-1}s^{-1}$, 10^8 , and 10^{-13} A, respectively. All these characteristics correspond to the best performances among all types of nonvolatile memory transistors reported so far, although the programming speed(>500 ms) and retention time ($\backsim$1 h) should be more improved.

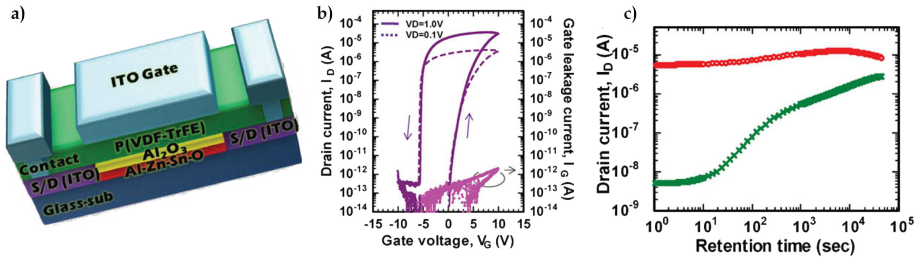


Figure 2.24: a) Schematic cross-sectional diagram of the transparent non-volatile memory transistor. b) Transfer curves and gate leakage currents of the fabricated OFET with the gate width of 20 mm and length of 10 mm. Indicated arrows describe the direction of transfer curves in a double sweep of V_G from - 10 to 10 V. c) Variations in current programmed into both states with the lapse of memory retention time [81].

2.3.6 Developmental status

Tremendous progress has been made in the field of OFET memories since it was first described. Currently, OFET memories exhibiting good performances in terms of operating voltages, program/erase cycles, and retention times. In addition, OFET memories integrated with other electronic elements have been reported. OFET memories have great potential for application in low cost, large areas, plastic systems, but many challenges still remain. These include: program/read/erase voltages are still large; data retention times are too short to satisfy the requirements of practical applications; operating mechanisms of OFET memories are not clearly understood. All of these issues need to be addressed in the future to allow the design of high performance devices.

2.4 Resistor-type memories

Devices incorporating switchable resistive materials are generally classified as resistor-type memory, or resistive random access memory (RRAM). Unlike capacitor and transistor memories, a resistor-type memory does not require a specific cell structure (e.g., OFET) or to be integrated with the CMOS (complementary metal-oxide-semiconductor) technology. Moreover RRAMs offer simplicity in fabrication and allow possibility for high data storage density via two dimensional, or even three-dimensional (stacking) cross-bar arrays. This kind of devices can store data by defining the two states of electrical bistability (high and low conductivity) as "1" and "0" in response to an applied electric field. For this type of memory, organic small-molecule compounds, polymers, inorganic materials, and inorganic/organic hybrid materials have been successfully applied.
Due to the advantages of good scalability, flexibility, low cost, ease of processing, 3D-stacking capability, and large capacity for data storage, organic resistive memories have been a promising alternative or supplementary devices to conventional inorganic semiconductor-based memory technology. Extensive studies toward new polymer materials and device structures have been carried out to show good memory performances, such as a large ON/OFF current ratio, low operation voltage, relatively long retention time, and high endurance.

2.4.1 Materials and device structures

An organic resistive memory device consists of a cross-point array of top and bottom electrodes, separated by a resistive material as shown in Figure 2.25. Each place where the top and bottom electrodes cross is one memory cell. The supporting substrate can be made of plastics, wafer, glass or metal foil. The configuration of electrodes can be symmetric or asymmetric, with Al, Au, Cu,p- or n- doped Si, and indium tin oxide (ITO) as the most widely used electrode materials. The resistive layer can be made of small organic semiconducting molecules (anthracene, pentacene, tris-(8-hydroxyquinoline)aluminum (Alq_3)), homogeneous polymers (polystyrene, poly(9-vinylcarbazole) (PVK), thiophene derivatives), donor–acceptor complexes (copper (Cu) coupled with 7,7,8,8-Tetracyanoquinodimethane (TCNQ) or Zinc phthalocyanine (ZnPc)), systems containing mobile ions and redox species (conjugated polymers and oligomers dopped with electron-donors or acceptors), composites containing nanoparticles (NPs) [82].

In general, the following four device structures, which are classified by the configuration methods used to place the resistive material

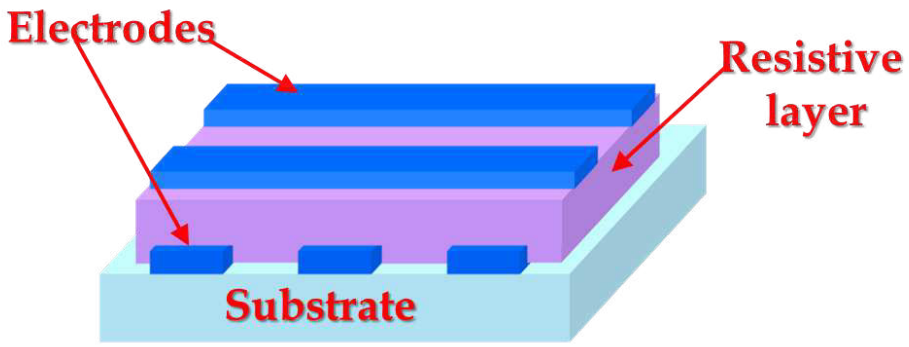


Figure 2.25: Structure of a resistive switch memory device.

between electrodes, have been suggested for the fabrication of two-terminal organic resistive memory devices:

- a single-layer structure containing only one type of material and no NPs 2.26 (a);
- a bilayer structure containing two types of materials and no NPs 2.26 (b);
- a trilayer structure in which NPs are placed in the middle of an organic layer 2.26 (c);
- blends in which NPs are randomly distributed throughout the entire region of the host matrix 2.26 (d).

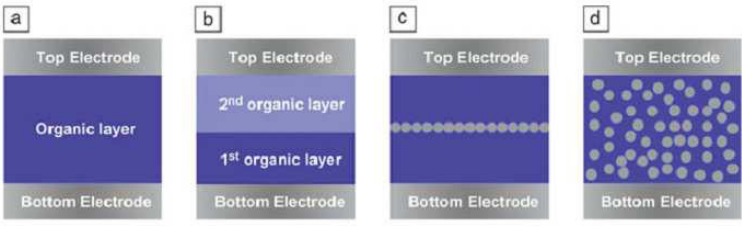


Figure 2.26: Typical structures of organic resistive memory cells: (a) a single-layer structure without NPs, (b) a bilayer structure containing two kinds of polymers, (c) a structure with NPs buried in the middle of an organic layer, and (d) a composite with NPs randomly distributed throughout the entire host polymer [83].

2.4.2 Working principle and basic electrical characteristics

The key function of RRAM devices is the **resistive switching**, i.e. the reversible modulation of electronic conductivity in thin films under electrical stress. By applying an appropriate voltage, the resistance of the memory can be reversibly switched between a high-resistance state (HRS, or OFF state) and a low-resistance state (LRS, or ON state). These two states can represent the logic values 0 and 1, respectively. In general, the operation which changes the resistance of the device from HRS to LRS is called a 'SET' process, while the opposite process is defined as 'RESET'. In literature, the RESET is sometimes called 'erase' operation. During the SET process the current level increases from HRS to LRS as the voltage increases from 0 V to the critical point which is called as set voltage V_{set}, while the current level abruptly decreases from LRS to HRS at the reset voltage V_{reset} under RESET process. The resistances of HRS and LRS can be read at a small voltage, which does not affect the resistance state.
The electrical switching characteristics of organic memory devices are categorized in two classes, volatile (Figure 2.27 a)) and non-volatile switching, depending on the ability to retain information. Non-volatile switching is often classified into four types based on current-voltage (I– V) curves: write-once-read-many-times (WORM), unipolar, bipolar and non-polar switching memory. WORM-type memory devices show electrically irreversible switching characteristics, and the original state is never recovered (Figure 2.27 b)). These devices can be used as storage components for radio-frequency identification (RFID) tags. Both unipolar and bipolar memory systems exhibit electrically reversible switching. In unipolar device, the SET and RESET operations are performed at the same polarity (Figure 2.27 c)). In bipolar memory devices, SET and RESET operations require opposite voltage polarities (Figure 2.27 d)). Finally, for non-polar switching devices, switching the RESET and the SET operations can be done with either positive or negative voltage (Figure 2.27 e)). Both unipolar and non-polar memory devices exhibit N-shaped I-V characteristic showing a negative differential resistance (NDR): there is a local maximum in the current followed by a region of negative differential resistance and a local current minimum. In general, regardless of the type of switching, the current during the SET operation should be limited not exceeding the current compliance to avoid over programming.

As in the case of other types of organic memory devices, some basic parameters of importance to the performance of organic RRAM

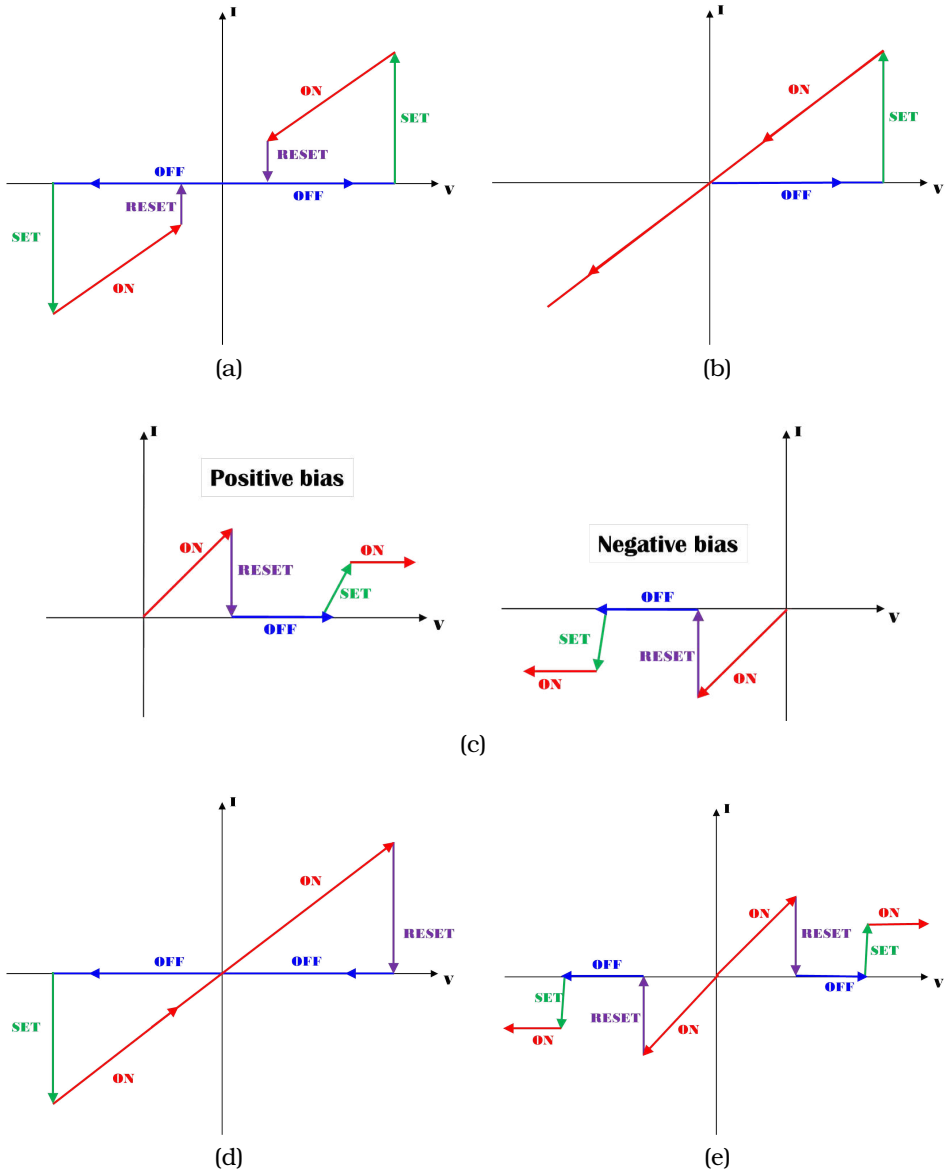


Figure 2.27: Typical switching characteristics of organic resistive memory devices: a)I– V curve of volatile switching behavior; b)I–V curve of WORM switching behavior; c)I– V curve of unipolar switching behavior; d)I –V curve of bipolar switching behavior; e)I –V curve of non-polar switching behavior.

device include: operating voltage, ON/OFF current ratio, switching (write and erase) time, read time, retention ability for non-volatile RRAM, programme cycles, stability under voltage stress (endurance), long-term stability. It is well known that a high operating voltage is

a fatal flaw in practical application. This is because a high operating voltage means high power consumption, and thus reduced portability of the devices. In addition, reliability can be a problem with a high operating voltage. To gain advantage over FLASH memory, which does suffer from high operating voltages, both the programming and erasing voltages for RRAM devices should be only a few volts. *ON/OFF current ratio*, i.e. the ratio of the current at HRS to the current at LRS, plays an important role in RRAM applications because it directly influences the accuracies of programming and erasing: a higher value is essential for the device to distinguish the two resistance states and to function with minimal misreading error. An RRAM device can be switched between HRS and LRS frequently, but each operation can introduce permanent damage, normally indicated as degradation. To gain an advantage over FLASH memory, which shows a maximum number of set/reset cycles between 10^3 and 10^7, depending on the type, RRAM should provide at least the same, preferably a better one. *Retention time*, the amount of time a memory cell will stay in one state after programming or erasing, indicates the intrinsic ability of a memory cell to retain its content. Most commercially available products are guaranteed to retain information for at least 10 years, either with the power on or off.

2.4.3 Conduction mechanisms

RRAM is based on conductivity change of materials in response to the applied electric field (non-ohmic conductivity). Since conductivity is essentially a product of carrier concentration (N) and charge mobility (μ), non-ohmic conductivity can be induced by a change in carrier concentration, a change in charge mobility and a change in both (N and μ). The electrical conduction mechanism in organic materials is much more complex than in ordered inorganic materials. It cannot be explained adequately on the basis of band theory, as most polymers are amorphous in nature. Therefore, their energy bands are poorly defined with discrete levels, producing localized states for the trapping of charge carriers. The localized states can also originate from chain folding, chain ends, bulk and surface dipole states, crystalline–amorphous interfaces, and impurities present in the material. Conduction in polymers may also depend on sample preparation and history. As a consequence, different conduction mechanisms may have often been reported for the same material. The conduction in organic materials is normally explained by intrinsic charge carrier generation and charge carrier injection from contacts at high fields. Charge injection from the electrodes to organic materials is more common in RRAM devices which can thoroughly described using the

following well-established conduction mechanisms: Schottky emission, tunnelling current, thermionic emission, space charge-limited current, hopping conduction, ionic conduction and impurity conduction. These mechanisms have been invoked to explain the generation, trapping and transport of charge carriers in organic RRAMs. A substantial amount of research has been dedicated to understanding the switching phenomena associated with these devices. Although the subject is still controversial, researchers have proposed several switching mechanisms based on theoretical simulations, experimental results and advanced analytical techniques. In the following, the most widely used switching mechanisms in organic resistive memory devices, such as filamentary conduction, space charge and traps, charge transfer, conformational change, are summarized.

Filamentary conduction

In general, when the ON state current is highly localized to a small fraction of the device area, the phenomenon is termed *filamentary* conduction [84, 85]. It has been suggested that filament conduction is confined and generally arises from device physical damages in RRAMs. If filaments are formed in a device, the ON state current will exhibit metallic I–V characteristics and will increase as the temperature is decreased, and the LRS current will be insensitive to the device area or show a random dependence, because the dimension of the filaments is much smaller when compared to the device area [86].
Filament formation have been observed in various systems, but the nature of the conductive pathways appeared to be very different in each system. Although it is difficult to elucidate the nature of the localized conductive paths, two kinds of filamentary conduction have been conceptually suggested. One kind is associated with **carbon-rich filaments** formed by the local degradation of organic films [34, 87], and the other kind is associated with **metallic filaments** resulting from local fusing or migration of electrodes through the films [84]. The latter has been considered to be more common than the former. Their occurrence depends on three parameters: electrode thickness, film thickness, and the nature of the “forming” atmosphere.
For a polymer at sufficiently high-applied electric field strengths, Joule heating may exceed heat dissipation. Thermal runaway will then occur at the *weakest* points of the sample, and the current and temperature will increase up to a limit set either by the impedance of the potential source or by the occurrence of certain thermally activated structural change within the sample. The corresponding

effects of atmosphere, electrode thickness and film thickness are as follows. In vacuum or an oxygen-free atmosphere, the localized high temperatures (at the thermal runaway points) lead to pyrolysis of the polymer and the subsequent formation of conductive carbon-rich material surrounding the breakdown region Figure 2.28 a). Alternatively, the polymer is oxidized in an oxygen atmosphere, leaving behind little or no residue. Electrostatic attraction between the electrodes then results in the formation of a metallic contact Figure 2.28 b). Both of the above processes involve liberation of gas which could break the unsupported upper electrode and possibly also the lower electrode when the latter is thin. The carbon-rich filament is not established if the electrodes are more than about 200 nm thick, since the higher heat dissipation capability of such electrodes limits the degree of pyrolysis of the polymer film.

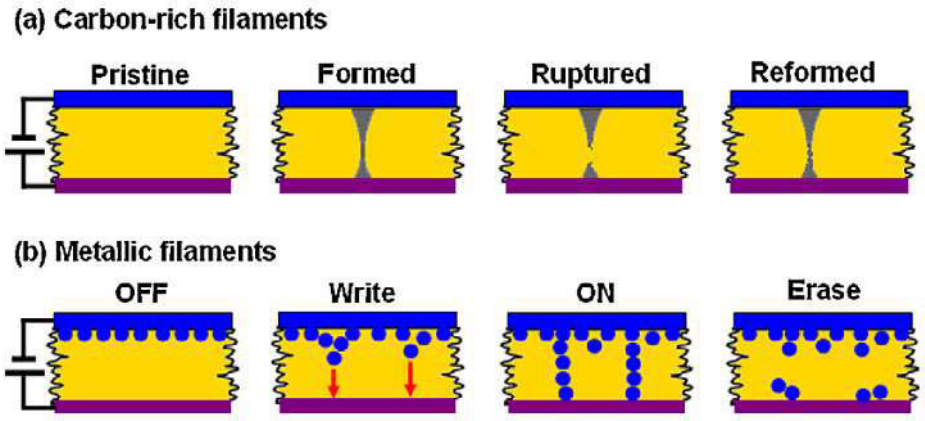


Figure 2.28: Schematic illustration of the formation of (a) carbon-rich filaments and (b) metallic filaments, and relevant switching effects [36].

The rupture of the filament should return the device to the OFF state. In order to break a formed filament, it would be necessary to supply enough heat to rupture at least a portion of the filament and cool it quickly enough so that the ruptured section does not reform. Thus, the current pulse must have sufficient magnitude and duration to rupture the filament, but also be short enough so that the heat produced does not become too dispersed.
Electrical switching in polymer devices is then a consequence of the formation, rupture and reformation of these filaments. Recently, a wide range of polymer and electrode materials have been used to study the formation of filaments. Several analysis methods have been widely employed to confirm the filamentary switching effect.

For example, temperature-variable current voltage measurements have been found to represent the metallic property of the low resistance state, i.e., linearly increasing resistance with increasing temperature in the case of conduction through metal elements [88]. Elemental depth profiles using X-ray photoelectron spectroscopy or secondary ion mass spectroscopy have verified the presence of top metal elements diffusing into the organic matrix [89]. However, the formation and rupture, distribution, shape, and composition of filament in organic RRAM are still unclear and ambiguous.

Space charge and traps

Space charges in materials may arise from several sources, as for example: the injection of electrons or holes from the electrode, the presence of ionized dopants in interfacial depletion regions, and the accumulation of mobile ions at the electrodes interfaces. Traps may be present in the bulk material or at interfaces where they will act to reduce carrier mobility. When the traps are located at interfaces, they may also affect the injection of charges into a material. The role of space charges and traps in organic electronic devices is reviewed recently by Taylor [90].
If the contact between the electrodes and the organic material is ohmic, it is possible to observe the effect of space-charge-limited conduction. In a organic trap-free material and neglecting diffusion effects, it is readily shown that when the concentration of carriers injected from the ohmic contact exceeds the thermally generated carrier concentration, the accumulation of carriers near the electrode builds up a space charge. Mutual repulsion between individual charges restricts the total charge injected into a sample, and the resulting current is called *space charge limited current* (SCLC) [91, 92]. When the organic material is characterized by a set of shallow traps with spatially uniform distribution, at sufficiently high injection rates, it may become possible to fill all the traps so that the free carrier concentration greatly exceeds the trapped concentration and transport is dominated again by space-charge-limited conduction. At low injection rates, transport is dominated by trapping/detrapping. In general, trapping and detrapping are closely related to the trap distribution in terms of spatial and energy [93]. It is possible that traps may have several discrete energy depths or even continuous energy distribution. Spatially, trap distribution may vary for a sample as the material may experience different processes including physical, thermal, and chemical treatments. This is especially true for the region near to the surface. Depending on the type of defects, traps may capture electrons or holes that have been injected into (or

generated within) the material under the application of electric field. It has been suggested that some defects can trap both electron and hole although the trap may have different energy levels for each type of charge carrier. Charge carriers can be generated via charge injection from the electrodes and ionization within the material. There are several processes that can lead to the current injection such as Schottky injection and tunneling. Generally speaking, the current increases exponentially with the applied field and decays exponentially with the time. The time effect can be explained in terms of the space charge field. The field near to the electrode will decrease due to the formation of trapped space charge. The reduction in local electric field results in a reduced current injection. When the applied field is removed the amount of trapped charges decreases with time, known as charge decay. Trapped charge carriers can release from the traps by several mechanisms such as photon assisted detrapping, phonon assisted (thermal) detrapping, impact ionization, and tunneling. Impact ionization and tunneling occurs mainly at high electric fields, while thermal detrapping occurs when the trapped charge carrier receives its energy from the thermal lattice vibrations. Several models have been proposed to simulate the formation and decay of space charge with certain degree of success. However, due to many parameters introduced in these models the exact physical processes of trapping and detrapping are not detailed.
The *electrical switching behaviors* of some organic materials has been reported to be associated with space charges and traps [36]. In particular, some resistive switching phenomena can be explained by the trap-filled SCLC. Supposing that initially the device is at its OFF state (Figure 2.29 a)). Under a low bias voltage, a Schottky barrier is formed near the anode (Figure 2.29 b)). When the field exceeds the Schottky barrier, carrier generation near the anode occurs, leading to an accumulation of space charges and a redistribution of the electric field (Figure 2.29 c)-d)). At near the turn-on voltage, the generated carriers fill some of the charge traps and the cathode also becomes an electron-injecting contact, leading to double injections and thus enhanced carrier concentration and mobility (Figure 2.29 e)-e)). The current increases rapidly to switch the device to the ON state. A reversed voltage pulse causes detrapping of the filled traps. Resistive switching phenomena have also been observed in many organic films embedded with granular metal or semiconducting islands to serve as the trapping sites (*nano-trap memories*)[94, 95]. Charge transport through these devices can occur either through the semiconducting medium itself or by tunneling among the NPs. In both cases, the charge transport falls into the category of "hopping", and the electronic states are highly localized. In the case of

hopping between molecular sites in an amorphous semiconductor, it is well documented that phonon assistance overcomes the energetic disorder, leading to exponentially activated temperature dependence. In the case of hopping between the metallic NPs themselves, the mechanism is direct tunneling and is known to be temperature independent.

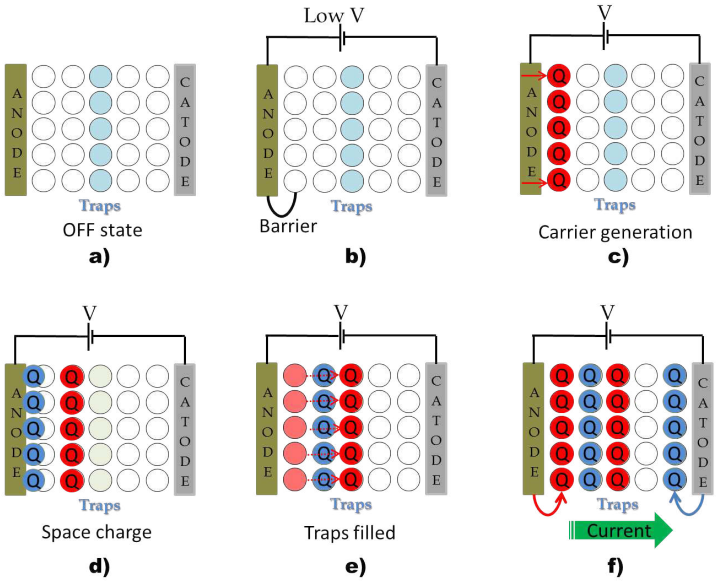


Figure 2.29: Operational mechanism of the charge-trapping memory: a) device in the OFF state; b) Schottky barrier for low voltages; c) carrier generation near the anode, d) accumalation of space charge and redistribution of the electric field for fields exceeding the Schottky barrier; e) carriers fills some of the charge traps; f) double injection and switch to the ON state.

The conduction mechanism in nano-trap RRAM can be explained by the trap-filled SCLC mode [96]. The mechanism is depicted schematically in Figure 2.30. At low voltages, the current is due to the thermally generated free carriers (Figure 2.30 a)), and shows a linear voltage dependence. At a higher applied electric field, the carriers injected into the film are from a thermionic process across the barrier (Figure 2.30 b)). As a consequence, the free carrier concentration is much lower than the concentration of trapped charge. The I–V characteristic shows a quadratic voltage dependence. With further increase in applied voltage, in addition to thermionic emission, tunneling can also occur (Figure 2.30 c)). The number of injected carriers, increase rapidly and the traps are nearly filled. The current thus has an exponential dependence on voltage. At the last

stage with the highest applied voltage, the traps are completely filled and the I–V characteristics follow the trap-filled model (Figure 2.30 d)).

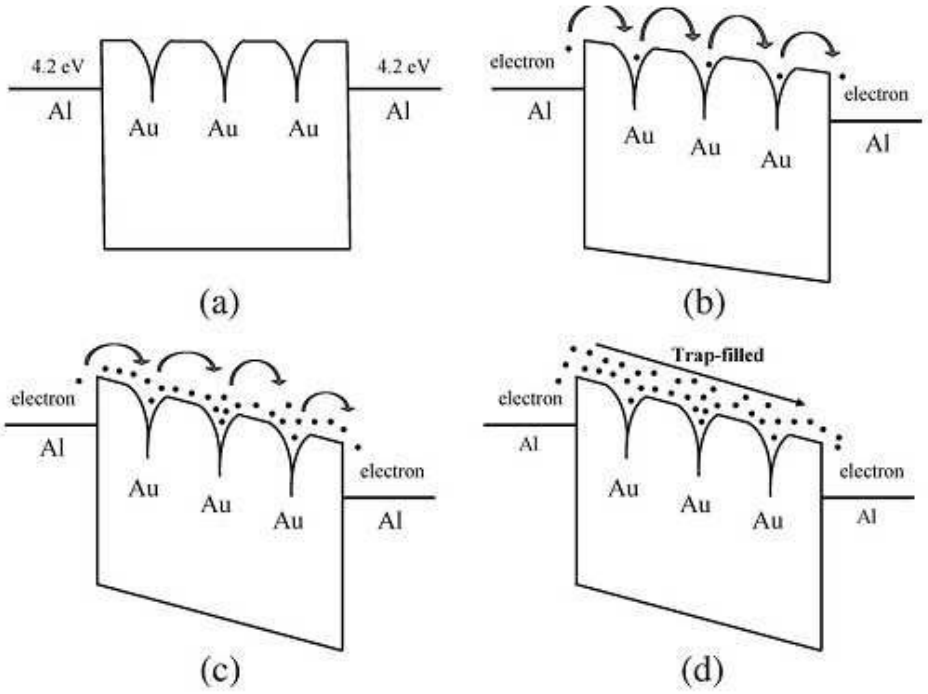


Figure 2.30: Schematic band diagrams for the transport mechanism of trappedfilled space-charge limitation conduction. (a) Region I: thermally generated carrier conduction. (b) Region II: with traps. (c) Region III: nearly filled. (d) Region IV: traps filled. [96]

Charge transfer

Charge transfer (CT) is defined as a process of an electron donor-acceptor system in which there is a partial transfer of electronic charge from the donor to the acceptor moiety by applying an appropriate voltage, which can result in a sharp increase in conductivity. The formation of an organic conductor from a donor, acceptor, and mixed donor–acceptor molecules is depicted schematically in Figure 2.31. Ion-radical species, formed by oxidation of a donor or reduction of an acceptor, might undergo further transformations, such as dimerization, fragmentation, and reactions with solvent, moisture, or oxygen from air. For a stable CT species, a relationship between ionic binding and conductivity exists. For instance, donors which

are characterized by small size and low ionization potential form strongly ionic salts. Under this circumstance, there is complete transfer of charge from the donor to the acceptor and, hence, these ionic salts are insulators. At the other extreme, donors which are too large and/or have too high ionization potential will form neutral molecular solids. In between, donors with intermediate size and ionization potential tend to form weakly ionic salts. These partially ionic, mixed-valence salts tend to have incomplete charge transfer and are likely to exhibit high conductivity.

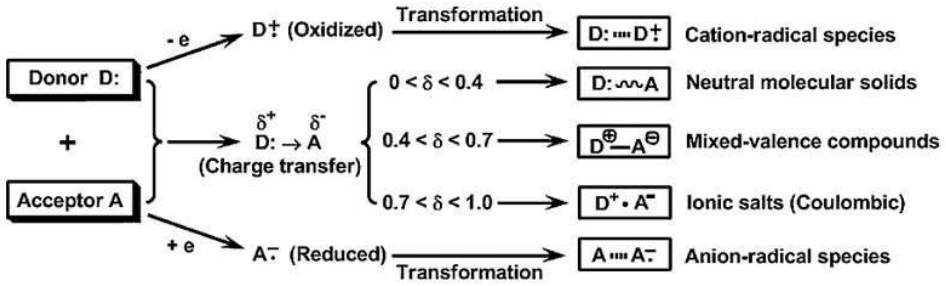


Figure 2.31: Schematic representation of the formation of ion - radical species and charge transfer complexes [36].

Charge transfer is expected to occur most frequently in the polymer with donor – acceptor structure. The memory characteristics based on the D–A polymer can be adjusted over a wide range through the modifications on polymer structures. By tuning the electron-donating or -accepting ability of D-A polymers, different memory effects can be obtained. The formation of strong dipole moment in polymer helps to sustain the conductive CT state, usually leading to a non-volatile behavior. Otherwise, the conductive CT state is not stable and can dissociate after removal of the electric field when the dipole moment is not strong enough, and consequently volatile memory device will be obtained.

Conformational change

A conformational change is a change in the shape of a macromolecule, often induced by environmental factors. A macromolecule is usually flexible and dynamic. It can change its shape in response to changes in its environment or other factors; each possible shape is called a conformation, and a transition between them is called a conformational change. Factors that may induce such changes include temperature, pH, voltage, ion concentration.

Resistive switching often arises from electrically induced conformational changes in molecules or molecular bundles. Some nonconjugated polymers containing carbazole groups in the side chain, such as poly(N-vinylcarbazole) (PVK) derivatives (poly(2 - (N - carbazolyl)ethyl methacrylate) or PMCz, poly(9 - (2 - ((4 - vinylbenzyl)oxy)ethyl) - 9Hcarbazole) or PVBCz [97]), can exhibit electrically induced conformational changes between a regiorandom and a regioregular structure (a polymer in which each repeat unit is derived from the same isomer of the monomer), resulting in the variation in conductivity state. The carbazole group is an electron-donor and hole-transporter and has a tendency to form a partial or full face-to-face conformation with the neighboring carbazole groups to result in extended electron delocalization. Such regions of electron delocalization provide pathways for charge-carrier hopping via the carbazole groups in the direction of the electric field. The switching effect in these devices probably arises from a field-induced change in conformation of the polymers via rotations of the randomly oriented carbazole groups to result in a more regioregular arrangement. At low applied voltages, the carbazole pendant groups attached to the main chain via flexible C-O linkages are initially in random orientations, as shown, for instance, by the simulated 3D models from molecular mechanics in Figure 2.32 b). This geometry corresponds to the minimum energy conformation of the polymer in the OFF state, and charge-carrier hopping along the carbazole groups is difficult. Under a higher bias, charge injection from the electrode oxidizes the carbazole groups near the interface, forming positively charged species. As an effective electron donor, the nearby neutral carbazole groups undergo charge transfer or donor - acceptor interactions with the positively charged carbazole groups to form partial or full face-to-face conformation with the neighboring carbazole groups. The positive charge is then delocalized to the neighboring, ordered carbazole groups. The process can then propagate through the bulk polymer film. When the applied voltage exceeds the threshold value, a significant fraction of the carbazole groups has undergone such a conformational change, resulting in enhanced charge transport through neighboring, aligned carbazole groups either on the same or neighboring polymer chains (intrachain or interchain hopping), producing the ON state, which has a more regioregular arrangement, similar to that depitcted in Figure 2.32 a). The field-induced conformational ordering in polymers can be elucidated unambiguously from fluorescence, high resolution TEM, the dependence of the ON/OFF state current ratio and the ON state conduction mechanism on the degree of regioregularity of the carbazole groups. The extents of regioregularity, conformation ordering,

and conformational relaxation, in turn, are dictated by the chemical structure and steric effect of the spacer units between the carbazole moiety and the main chain. Through the rational modification of polymer structures and tuning of conformational changes, excellent resistive memory performances can be realized.

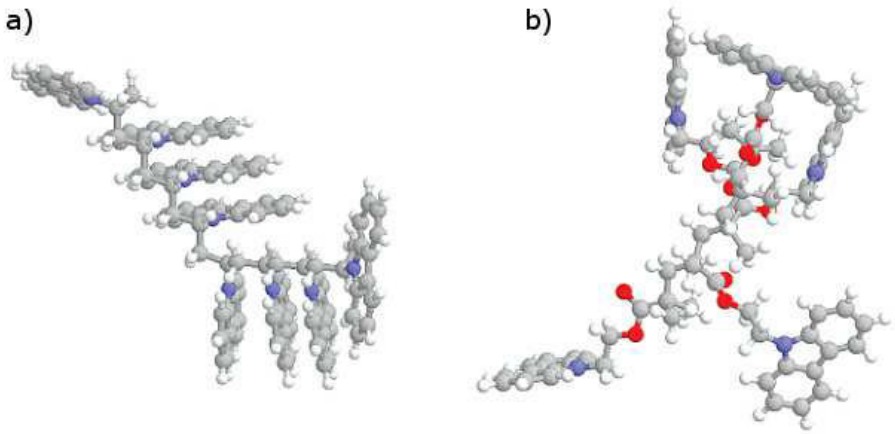


Figure 2.32: Simulated 3D models by molecular mechanics showing the geometry corresponding to a) the ON and b) OFF states [97].

Ionic Conduction

Ionic conduction occurs in polymers which contain ionic groups or to which ionic materials have been added. In these materials, adsorption of water plays a dominant role because water may act as a source of ions, as a dielectric impurity, or as a local structure modifier. In amorphous polymers, ionic conduction can also occur due to drift of defects on application of an electric field. Ionic conduction is characterized by its high activation energy, in comparison to the activation energy for electronic conduction, and the noticeable polarization effect under the action of a DC field. In addition, a large transit time for ions is also observed. Activation energies are also found to increase with temperature.
Electrically rewritable memory effects can be obtained by migration of dopant ions in and out of a polymer depletion layer at a Schottky contact. Migration of dopant ions facilitate ossidation and reduction of the polymer, resulting in the formation of a p–n junction. This mechanism is supported by the temperature dependence of the I–V characteristics. At low temperatures, where mobility of ions is in-

hibited, the hysteresis is significantly reduced. Conversely, at high temperatures, the mobility of ions is higher and relaxation to the thermodynamically favored state is faster. Hence, the hysteresis is suppressed as well.
The memory effect can also arise from the presence of an interfacial depletion layer at the polymer/electrode interface. At the interface, a Schottky barrier is readily formed in which the depletion region is composed of a layer of unscreened dopant ions. Since the dopants are not chemically bound to the polymer, they may undergo a slow drift under the action of an applied electric field, hence changing the capacitance of the depletion layer. Such a change will manifest itself as a change in the displacement current measured during a voltage sweep. The memory effect is a consequence of increased or decreased charge injection into the device resulting from a voltage-induced change in the concentration of dopant ions in the vicinity of the electrode.
Memory devices can be obtained inducing a conductivity change in an electroactive polymer by changing its dopant concentration. The process for doping is an electrochemical process controlled by the applied voltage. Thus, when a voltage larger than the threshold value is applied, the conductivity of the polymer can be switched ON or OFF. Accordingly, when a voltage lower than the threshold value (or no voltage at all) is applied, the ions are stable in the polymer, and the device conductance remains at a constant value. The amount of the injected/expelled iodine dopants in the polymer layer is related to the amplitude, as well as the duration, of the applied voltage.

2.4.4 Progress in resistive memory devices

The number of organic device structures that have been reported to show resistive switching is truly remarkable. The simplest structure, and among the earliest reported, is that of a *metal – insulator – metal* (MIM) sandwich proposed by Gregor in 1968 [98]. In this work, both electrodes were made out of lead (Pb) and the organic insulator was 10 to 25 nm of glow-discharge-deposited poly(divinylbenzene). These devices exhibited resistance changes of several orders of magnitude at a voltage of 1–2 V, with a retention time in air of 30 minutes, and could be cycled 250000 times. *Small organic molecules* were also incorporated into early MIM structures. In a 600 nm tetracene film, between gold and aluminum electrodes, the resistance decreased abruptly by 5 decades at irreproducible voltages between 4 and 8 V [99]. The same group soon claimed reproducible switching in perylene and tetracene [100]. In 1971, Carchano et al. [31] observed reproducible bistable switching in Au-Polymer-Au junctions, which

can be switched more than 2000 times and with a resistance ratio $> 10^7$. Samples submitted to switching were examined with a scanning electron microscope: circular dots, ranging between 5 and 10 μm diameter, are observed on the surface. The authors supposed that these dots were probably due to current-carrying filaments. In a different work, Pender et al. [34] observed two distinct forms of memory switching in thin films of glow discharge polymerized styrene, acetylene, benzene, and aniline. These two forms, called the high-voltage switching regime (HVSR) and the low-voltage switching regime (LVSR) are characterized by high (> 20 V) and low (1-5 V) threshold voltages, respectively. The low-resistance (ON) state of both modes is associated with highly conductive filaments. It is suggested that in the HVSR the filaments are metallic and result from localized fusing of the two electrodes. In the LVSR the filaments are thought to be of carbon, formed from localized pyrolysis of the polymer film.

Nominally homogeneous polymers have been also used in MIM devices, including true insulators such as polystyrene and acrylates [33, 87]. Combinations of functional components have been explored as potential storage media, most commonly electron donors and acceptors, motivated by the conductive properties of organic charge-transfer complexes. In 1979, Potember et al. [101] observed stable and reproducible current-controlled bistable electrical switching in polycrystalline films of copper-tetracyanoquinodimethane (Cu-TCNQ). The transition from a high- to low-impedance state occurs with delay and switching times of approximately 15 and 10 ns, respectively. Switching with high power dissipation yields a low-impedance memory state which can be erased by application of a short current pulse. They proposed that the bistable switching and memory effect associated with Cu-TCNQ thin films is a bulk phenomena of the organic semiconducting material.

These very early results already reveal the experimental difficulties associated with the irreproducible behaviors. For this reason, investigation has continued over the succeeding three decades but with relatively little attention, accelerating only in recent years. In 2000, Ma et al. [102] presented a new organic switching device consisted of a polymer derivative of anthracene called poly(methylmethacrylate-co-anthracenylmethacrylate) (MDCPAC), in a sandwich structure between gold and aluminium electrodes. The device had a switching time shorter than 0.5 ms and could switch several thousand times. It was proposed that the mechanism for the change in conductivity was trap sites in the polymer film being filled upon the application of an electric field, but no conclusive evidence was presented, and the performance of the devices as memory elements was not dis-

cussed. It was also noted that the gold bottom electrode was crucial for switching to take place, with no switching occurring when aluminium bottom electrodes were used.
The next progression in devices came from structures first proposed by the Yang group [103] at the University of California. The structure of their devices is fairly simple and consists of an organic/metal/organic, triple-layer structure interposed between an anode and a cathode (Figure 2.33 a)). 2 - Amino - 4,5 - imidazoledicarbonitrile (AIDCN), an organic semiconducting polymer, was used for the organic layers, and aluminum as the embedded metal layer and also as electrode layers. All materials depositions were carried out in an evaporator, and all the steps were conducted without breaking the vacuum.

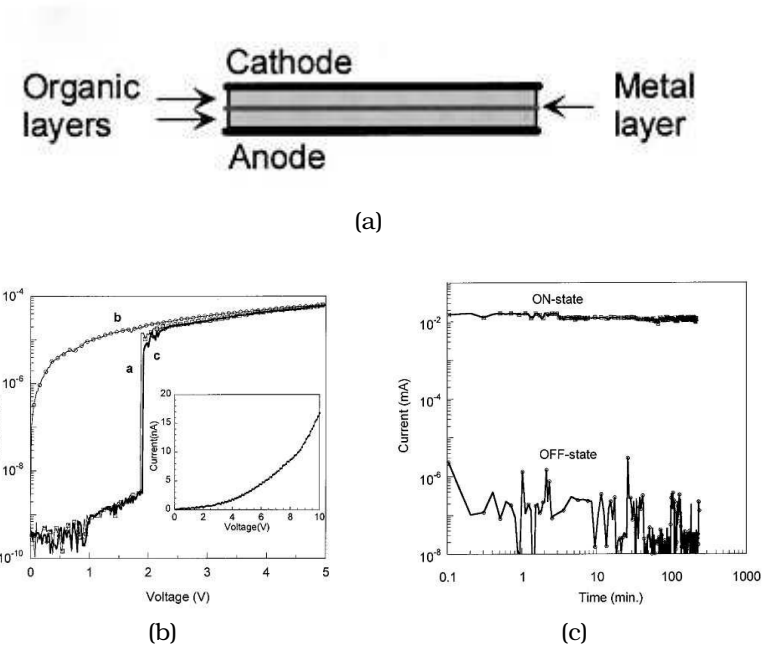


Figure 2.33: a) The structure of an electrical bistable device; b) I–V characteristics of a device with the structure Al / AIDCN(50 nm) / Al(20 nm) / AIDCN(50 nm) / Al; c) The stability test in either the ON or OFF state under a constant bias of 1 V [103].

All electrical tests were conducted in ambient condition without any device encapsulation. Figure 2.33 b) shows typical I–V curves for an AIDCN-based memory. The first voltage scan depicted by curve (a) shows a sharp increase in the injection current at about 2 V indicating the transition of the device from the low conductivity state (OFF state) to a high conductivity state (ON state). The ratio of

the conductivities achieved between the two states is about 10^4. After this transition, the device remained in this state even after turning off the power (curve (b)). The OFF state can be recovered by the simple application of a reverse voltage pulse. The bistable behavior and the creation of non-volatile memory effects can be observed only in the presence of the embedded thin metal layer. The inset of Figure 2.33 b) shows the I–V curves of a device without the metal interlayer, where switching can no longer be observed. More than one million write-erase cycles were conducted on AIDCN-based memories with good rewritable characteristics. The memory retention ability was tested by leaving several devices in the ON state at ambient conditions. It was found that the devices remained in the ON-state for several days to weeks. The stability of the memories under stress was evaluated in the continuous bias condition. A constant voltage (1 V) was applied to the devices in the OFF state and the ON state and the current recorded at different times. As can be seen from Figure 2.33 c), there is no significant degradation of devices in both the OFF and ON states after 4 hours of continuous stress test, indicative of the stability of both the material and the metal/organic interfaces. As regard the mechanism behind the resistive switchiing, the authors suspected that trapped charges in the middle metal layer and dynamic doping process of organic films is responsible for the observed electrical bistability.

One year later, it was realized that the performance of AIDCN-based memories is sensitive to the nanostructure of the middle metal layer [104]. UV–visible absorption spectrum, surface morphology, and electrical conductance studies suggest that the middle metal layer for the bistable device consists mainly of partially oxidized, small metal nanoclusters, instead of pure metal, as previously described. Typical device structure, the proposed energy diagram and the AFM image of the middle metal cluster are given in Figure 2.34. The device operating mechanism can be illustrated by the schematic energy band diagram. The middle Al layer consists of multilayer nanoclusters (consisting of a metallic core and an Al-oxide coating), resulting from the slow evaporation process, with a very thin oxidized layer between the nanoclusters so that the charge can easily tunnel through. The energy diagram of the unbiased Al nanoclusters layer shows a distribution of many energy wells next to each other, which are sandwiched between the two organic layers with relatively high lowest unoccupied/highest occupied molecular orbital energy levels. When the applied bias to the device is high enough, free electrons in the metallic cores of the nanoclusters tunnel through the barrier against the applied electric field direction, resulting in the Al-nanocluster layer being polarized. Subsequently, the charge

is stored at both sides of the middle Al nanocluster layer. The stored charge at both sides of the middle metal layer enables the adjacent organic layers to undergo a conductance change, by doping the organics. Hence, the device undergoes a dramatic conductance change upon forward bias. When the electrical bias is removed, because of the oxide barrier layers between the metallic cores, the polarized charges cannot recombine, and they remain at the two ends of the middle metal layer: only a reverse bias could re-install the device to the OFF-state.

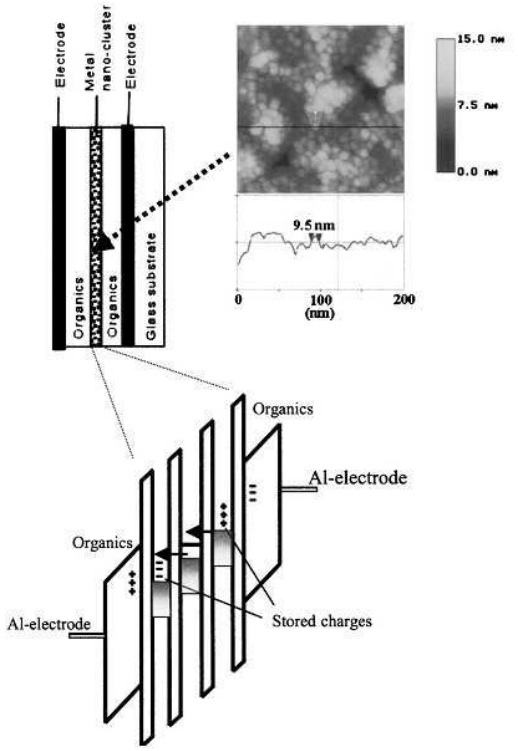
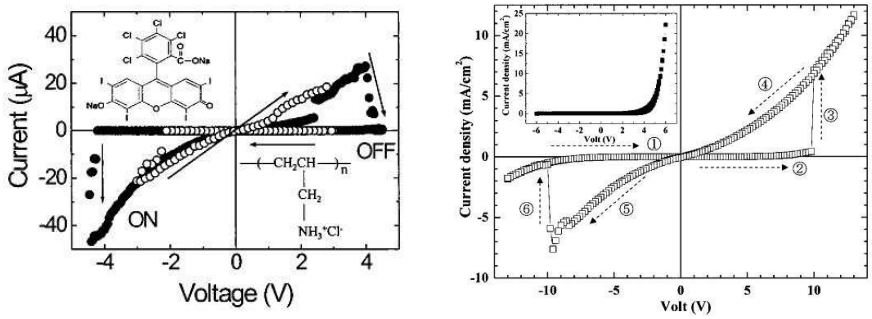


Figure 2.34: Typical device structure, the proposed energy diagram at bias condition, and the AFM image of the middle metal layer of the device [104].

At the same time, Bandyopadhyay et al. [105] observed a large electrical conductance switching in devices based on spin-cast and layer by layer electrostatic self-assembled films of Rose Bengal. In these devices, the current ratio between the ON and OFF states has been as high as 10^5: the key parameter for such a high ON–OFF ratio in Rose Bengal-based devices is their low OFF-state leakage current. Oyamada et al. [106] observed reproducible electrical switching

in devices with an ITO/Al/Cu:TCNQ/Al configuration with a large ON/OFF ratio of 10^4. This characteristic switching phenomenon was observed more than 1000 times. However, no switching effect was observed in the ITO/Cu:TCNQ/Al device, suggesting that the Al_2O_3 layer plays an important role in switching. Moreover, the lack of switching characteristics in the TCNQ neat layer suggests that charge transfer between Cu and TCNQ could be also responsible for switching.



(a) (b)

Figure 2.35: a) I–V characteristics of devices based on spin-cast films of Rose Bengal for two sweep directions. Arrows show the sweep direction of applied voltage. Molecular structures of Rose Bengal and PAH are shown in the second and fourth quadrants, respectively [105]; b) J–V characteristics of an ITO / Al / Al_2O_3 Cu:TCNQ / Al device.(Inset) J–V characteristics of an ITO / Cu:TCNQ / Al device [106].

In 2004, Ma et al. [107] demonstrated an organic non-volatile memory device by controlling the Cu-ion concentration within an AIDCN layer. Devices with the structure of Cu/Buffer-layer/AIDCN/ Cu have been fabricated by vacuum thermal deposition method. A small voltage pulse around 0.5 V can switch the device to high conductance state, and a voltage pulse above 2 V can restore it to low conductance state. They proposed that when the Cu-ion concentration is high enough, the device exhibits a high conductive state due to the metallization effect. When the Cu-ion concentration is low, the device displays a low conductance state. These two states differ in their electrical conductivity by more than seven orders of magnitude and can be precisely switched by controlling the Cu-ion concentration through the application of external biases. The retention time of both states can be more than several months.
The mechanisms for bistability in these devices were thoroughly investigated by Bozano et al. [94]. In particular, they proposed that the resistive switching phenomenon observed in organic layers

containing granular metal particles conforms to a charge storage mechanism. Specifically, aluminum tris(8-hydroxyquinoline) (Alq_3) has been used as the organic medium and granular aluminum for the charge-trapping sites. Aluminum was also used for the electrodes. The authors emphasized, however, that the mechanism is very general and that many other material combinations show similar behavior. They concluded that: the mechanism responsible for the bistable resistance behavior of these devices is charge trapping and space-charge field inhibition of injection; a discontinuous, granular layer is critical to the bistability of the device; the trapping properties can be tailored by the choice of metal, the size of the particles and their position in the device structure. However, at the same time Tondelier et al. [108] report a bistable organic memory made of a single organic layer embedded between two electrodes, and compared to the organic/metal nanoparticle/organic tri-layers device. They found that one-layer and three-layer organic bistable devices exhibit similar current–voltage characteristics (`Figure 2.36 b)`) and similar current–temperature dependencies. They also observed on-state current over off-state current ratios as large as 10^9. This behavior was attributed to the inclusion of metal nanoparticles into the organic material during the top electrode evaporation for both types of devices, with metallic filaments of nanoparticles forming in the polymer under high electric fields, giving rise to a high conductivity ON state.

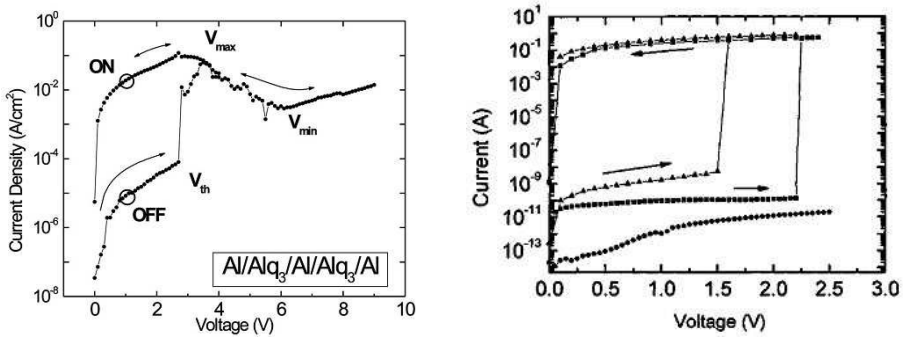
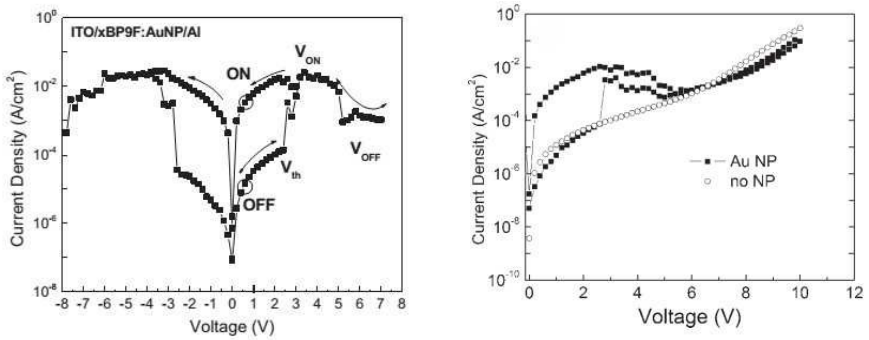


Figure 2.36: a) Current–voltage characteristic of an Al (50 nm) - Alq_3 (50 nm) - Al (5 nm) - Alq_3(50 nm) - Al (50 nm) device [94]; b) Typical current–voltages curves for the three layer device (■) with the structure pentacene (170 nm) - aluminum (20 nm) - pentacene (170 nm); for the one layer (▲) with a pentacene film of 400 nm.(●) I–V curve for a one layer device (400 nm of pentacene) without the top Al electrode and mechanically contacted with a thin gold wire [108].

A novel organic memory device fabricated by solution processing was presented by Ouyang et al. [109]. The device has a simple structure with an organic film sandwiched between two aluminium electrodes. The organic film was formed by spin-coating a 1,2-dichlorobenzene solution of 1-dodecanethiol-protected gold nanoparticles (Au-DT NPs), 8-hydroxyquinoline (8HQ) and polystyrene (PS). They demonstrated that these devices would behave in a manner similar to the metal nanocluster devices previously studied by Ma et al. . Whether tested under a nitrogen atmosphere or in air, the device showed similar electrical behaviour. The presence of oxygen and moisture in the environment did not affect the threshold voltages for the electrical transitions and the current in the high-conductivity state, but it caused the current in the low-conductivity state to be one order of magnitude higher than that in vacuum. The change in conductivity in these devices is attributed to the transfer of electrons from the 8HQ molecules to the Au-DT. A tunnelling mechanism between 8HQ molecules was proposed as being responsible for the high conductivity ON state. Ouyanget al. [110] later studied MIM structures including nanoparticles capped with 2-naphthalenethiol (Au-2NT) embedded in a polystyrene matrix. Here, a transfer of electrons from the capping ligands of the nanoparticles and the nanoparticle core itself is proposed as the charging mechanism, with tunnelling between the nanoparticles responsible for conduction in the ON state. These devices were found to only exhibit WORM characteristics, with no transition back to the OFF state, implying that the electron transfer is irreversible.
Other studies, investigating the effect of different metallic nanoparticles, as well as the position of the nanoparticles in the structure and electrode material, has been carried out by Bozano et al. in 2005 [95]. They asserted that bistability should be surprisingly independent of the materials chosen and the structures investigated. Three architectures were considered for the fabrication of bistable devices: spun-cast polymer-NP blends where the nanotraps are randomly distributed throughout the entire thickness of the host matrix; spun-cast blends layered with pure polymer; and evaporated structures where the nanotraps are located in the middle of organic layer. In addition, they examined single-layer devices without NPs. Figure 2.37 a) shows typical semilogarithmic curve of current density versus applied voltage (I-V) for a switchable element at room temperature. The device current switches between states of low and high conduction at the threshold, reaches the maximum, and then goes through a negative-resistance region to a minimum, after which it increases again almost exponentially. Comparison of devices with and without NPs shows that the NPs increase the conduction of the

device. The NPs appear to have the dual role of traps and conduction sites for the injected charges. For example, Figure 2.37 b) shows the I-V characteristics of a device without NPs (open symbols) compared to those of a device in which the polymer is blended with NPs (closed symbols). The results of this work suggest that the specific materials used play at most a secondary role in the determination of device properties. The specific energy-level structure provided by the electrode and metal NP Fermi energies and the HOMO-LUMO of the host is relatively unimportant. One explanation for this may lie in the uncontrolled nature of the particle size distribution. Moreover, transport seems to occur predominantly by tunneling between NPs.



(a) (b)

Figure 2.37: a) DC I-V characteristics at room temperature for an ITO / polymer / NPs / Al device; b) I-V characteristics comparing the device with (closed symbols) and without (open symbols) NPs. In both cases the film thickness is 50 nm. [95].

The next progression in terms of perfomance were obtained by Lai et al. [111], who demonstrated bistable resistance switching characteristics of an Aluminum/poly(N-vinylcarbazole) (PVK)/Aluminum structure. In particular, reproducible resistance switching with a large ON/OFF ratio of 10^4 have been achieved for spin-coated PVK films (Figure 2.38 a)). The devices also exhibited a good retention time of about $10^5 s$ in ambient conditions. The mechanism is explained on the basis of the filament theory.
In 2007, Song et al. [112] presented an bistable device based on PVK mixed with gold nanoparticles (GNPs), which serve as the active layer between two metal electrodes. Electrical bistability and memory effect in the Al/PVK:GNPs/TaN devices are due to the incorporation of GNPs in the PVK. By mixing the GNPs into the PVK polymer, the PVK serves both as the matrix for GNPs and electron donor since it has a strong capability to provide electrons, while the GNPs act

as electron acceptors. Since PVK is dominant in the active layer of these devices, it serves as the path for charge carrier transport. An ON/OFF current ratio as high as 10^5 at room temperature has been achieved.

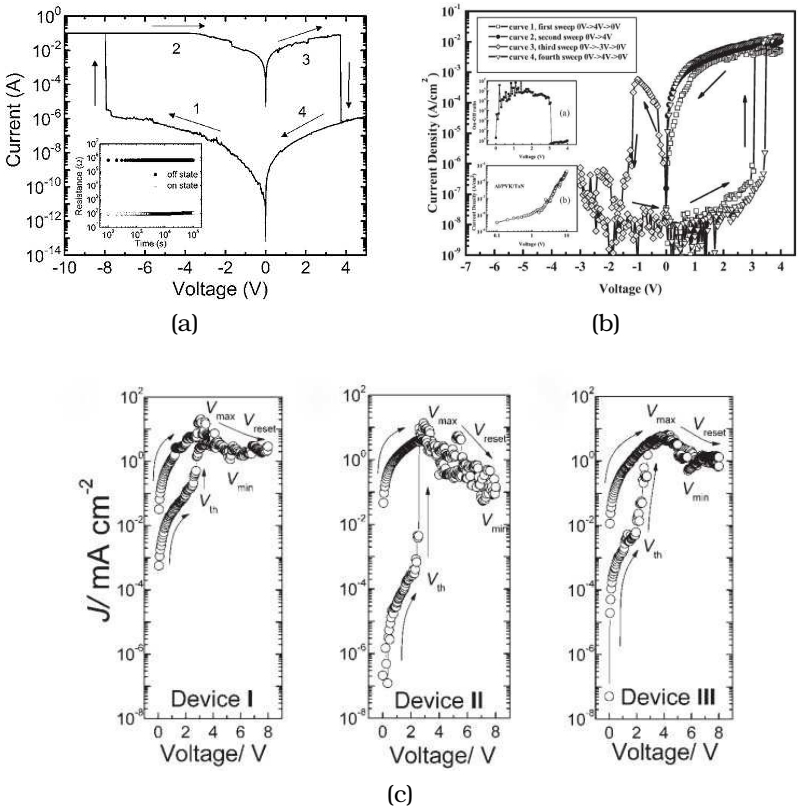
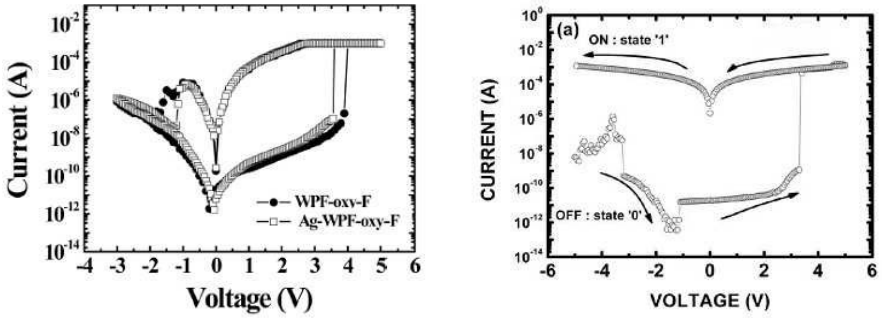


Figure 2.38: a) Typical current-voltage curves for the PVK films. The inset shows the plot of on- and off-state resistances after reading at 1 V per 100 s [111]; b) Typical J–V characteristics of the Al / PVK:GNPs / TaN device. Inset: (a) The ON-OFF current ratio as a function of applied voltage and (b) J–V characteristics of the Al / PVK / TaN device [112]; c) Typical current density–voltage (J–V) characteristics for device I with the structure ITO - PVK (150 nm) - Al, device II with the structure ITO / Ag-NDs / PVK (150 nm) / Al, and device III with the structure ITO / PVK Ag-NPs (150 nm)/ Al [113].

PVK was also used embedded between an Al electrode and ITO modified with Ag nanodots (Ag-NDs) [113]. These devices exhibit ON/OFF switching ratios of 10^4 and have retained a programmed state for at least 3 days in nitrogen atmosphere. This level of performance could be achieved by modifying the ITO electrodes with some Ag-NDs that act as trapping sites, reducing the current in the

OFF state (Figure 2.38 c)). Temperature dependence of the electrical characteristics suggests that the current of the low-resistance state can be attributed to Schottky charge tunnelling through low-resistance pathways of Al particles in the polymer layer and that the high-resistance state can be controlled by charge trapping by the Al particles and Ag-NDs.
Later, Kim et al. [114] investigated the effects of Ag nanoparticles on the switching behavior of polyfluorene-based organic non-volatile memory devices fabricated on heavily-doped p-type silicon substrates. Polyfluorene-derivatives (WPF-oxy-F) with and without Ag nanoparticles were synthesized. The Ag-nanoparticles did not significantly affect the basic switching performances, such as the current-voltage characteristics, the distribution of ON/OFF resistance, and the retention time (Figure 2.39 a)). The ON/OFF ratios of mean resistance values for both WPF-oxy-F and Ag-WPF-oxy-F were more than three orders of magnitude. A retention characteristic test of WPF-oxy-F was performed under ambient conditions at room temperature: both the HRS and the LRS of the Ag-WPF-oxy-F memory device were maintained for 10^5 s without showing any degradation. The pulse switching time of Ag-WPF-oxy-F was faster than that of WPF-oxy-F, indicating the effect of Ag-nanoparticles on switching behavior of polyfluorene-based organic non-volatile memory devices. Ag-WPF-oxy-F memory devices showed an area dependence in the high resistance state, implying that formation of a Ag metallic channel for current conduction. It seems that the Ag nanoparticles, which were well dispersed in WPF-oxy-F, acted as current paths, allowing the current to flow through the whole area in the HRS. In case of the LRS, the resistance values did not change significantly with the cell area due to the formation of localized current paths through Ag nanoparticles in Ag-WPF-oxy-F. Hence, formation of a Ag metallic channel in Ag-WPF-oxy-F is responsible for this filamentary conduction.
In the same year, Son et al. [115] investigated the electrical properties of flexible non-volatile organic bistable devices fabricated with graphene sandwiched between two insulating poly(methyl methacrylate) (PMMA) polymer layers. Current-voltage (I-V) measurements on the Al/PMMA/graphene/PMMA/indium - tin - oxide (ITO)/ poly (ethylene terephthalate)(PET) devices (Figure 2.39 b)) showed a current bistability due to the presence of graphene, indicative of charge storage in it. The maximum ON/OFF ratio of the current bistability for the fabricated device was as large as 10^7, and the endurance number of ON/OFF switchings was 1.5×10^5 cycles; an ON/OFF ratio of 4.4×10^6 was maintained for retention times larger than 10^5 s in an ambient environment.



(a) (b)

Figure 2.39: a) I-V curves of WPF-oxyF and Ag-WPF-oxy-F [114]; b) I-V curves for the Al/PMMA/graphene/PMMA/ITO/PET device [115].

The bistable behavior for the Al/PMMA/graphene/PMMA/ITO/PET devices might be attributed to conducting filaments formed in the PMMA layer at the state transition. The graphene layer and the intrinsic trap states of PMMA act as trapping sites, which capture electrons injected from the electrode. The electrons captured in the graphene and in the traps generate a local internal field in the PMMA layer, and a conducting filament can be formed in the PMMA layer under a high internal field. However, the electrons captured in the traps are easily emitted to the lowest unoccupied molecular orbital (LUMO) level because the traps in the PMMA layer are exponentially distributed over energy. Because the trap density near the LUMO level is highest, many captured electrons can be emitted by a small amount of a thermal energy. The traps in the PMMA are partly occupied by the electrons. Therefore, only the electrons captured in the traps cannot generate sufficient internal field to form conducting filaments, resulting in the disappearance of the memory effect in the device without the graphene layer. In the devices with the graphene layer, the electrons captured in the graphene layer are sufficient to generate an internal field, higher enough to form the conducting filament in the PMMA layer. No metal component, except the Al electrode, is used in the device. Therefore, the conducting filament might be caused by diffusion from the Al electrode during the metal deposition.
In 2011, Liu et al. [116] proposed organic non-volatile memories based on Au/Alq_3/metal nanoparticles/Alq_3/Al. Two kinds of metal nanoparticles (i.e., Au and Al) were used in the sandwiched structure. In particular, they concluded that the electrical characteristics of devices with gold NPs display much better performances with respect to those with aluminum NPs (Figure 2.40).

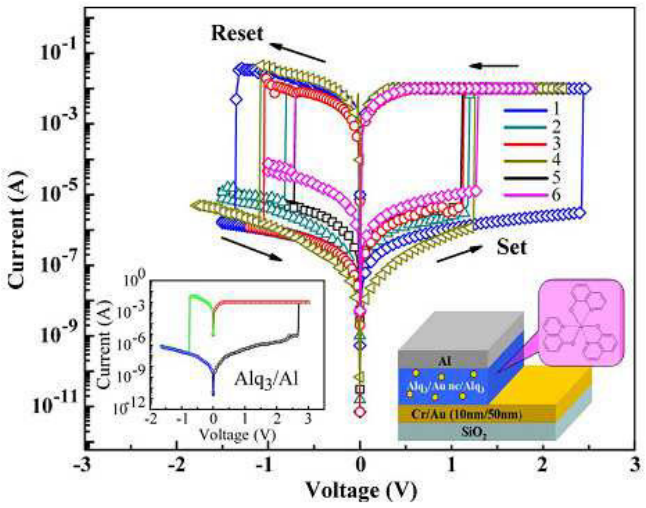


Figure 2.40: Typical six-cycle measured I–V curves of the Au/Alq_3/Au-NPs/Alq_3/Al device. Right inset shows schematic diagram of the device structure. Left inset shows the typical I–V curve of Al-doped device [116].

These devices showed reproducible resistive switching, a high ON/OFF current ratio of about 10^4, a retention time of 4 h ($\backsim 1.5 \times 10^4 s$) and a reasonable stability under bias stress test in ambient conditions. The conduction mechanism of the devices was demonstrated to be charge trapping. At low voltages, the device stays in the OFF state, and the conduction is dominated by intrinsic carriers of the organic material. In this region, the deep traps are mostly empty, the injection of excess carriers is negligible. As the bias increases, the deep traps in this trap-filling region are gradually filled. Once the charge traps are filled with holes, the device turn into ON state, and a sharp increase of current density is observed.

More recently, B- and N-doped carbon nanotubes (CNTs) with controlled workfunctions were successfully employed by Hwang et al. [117] as charge trap materials for solution processable, mechanically flexible, multilevel switching resistive memory. The controlled work function and high dispersibility of substitutionally doped CNTs significantly improved the resistive memory performance of CNT nanocomposite devices (`Figure 2.41`). An ON/OFF ratio larger than 10^2, endurance cycles of more than 10^2, and a retention time longer than 10^5 s were achieved with good mechanical flexibility and long-term air stability. At the same time, Gao et al. [118] observed bipolar resistive switching effect in Cu/poly(3-hexylthiophene):[6,6]-phenyl C61-butyric acid methyl ester (P3HT:PCBM)/ITO structures,

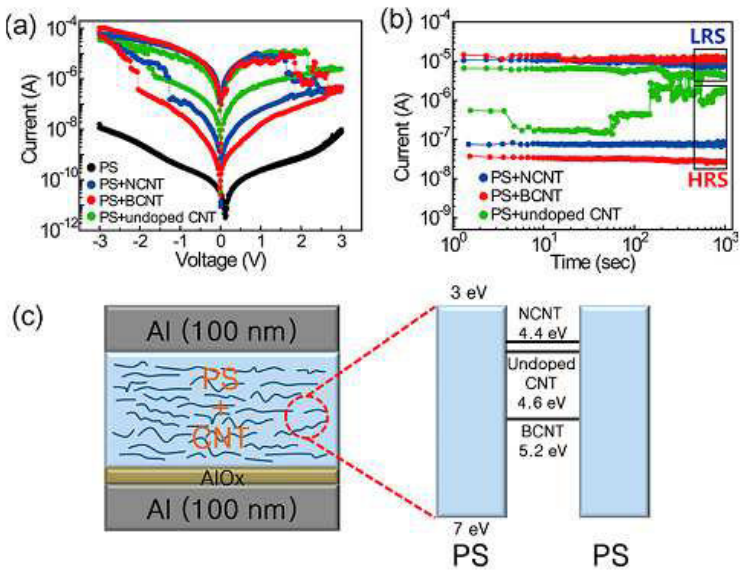


Figure 2.41: a) I–V and b) retention characteristics of resistive memory devices. c) Energy band diagram of the device [117].

with good retention property (longer than 10^6 s) in air. By combining the symmetry of current–voltage curves with corresponding energy band diagrams in different resistance states, it is demonstrated that the Cu filament grows from Cu/organics interface, ends at organics/ITO interface, and ruptures near organics/ITO interface (`Figure 2.42 a)-d)`).

2.4.5 Strategies for memory applications

The viability of a memory technology is usually decided by parameters such as switching speed, cycling endurance, retention time, and cell density. These parameters should enable organic memory devices to meet the minimum specifications necessary for next generation memory applications. Uniform statistical data for these parameters, obtained from a large number of samples, are another essential requirement. This section presents essential strategies for practically implementing organic resistive memory devices.

Memory performance enhancement

The switching characteristics of organic resistive memory devices are strongly influenced by the properties of interfaces and active materials. Accordingly, various approaches to control and optimize

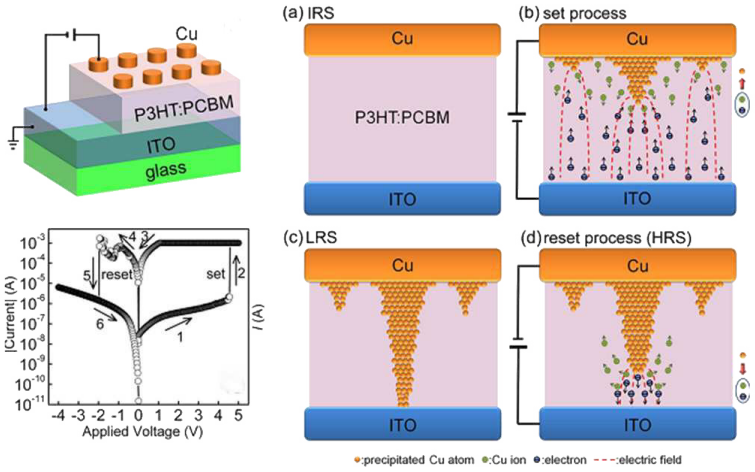


Figure 2.42: Schematic of the sample layout and typical I–V curve of bipolar resistive switching behavior on tE left. Schematics of dynamic resistive switching processes on the right: a) Virgin device structure with two clear interfaces. b) Growing of Cu filament due to oxidation and reduction of Cu atoms under positive voltage. c) Cufilament finally reaches BE, leading to the appearance of LRS. d) The weakest part of Cu filament near organics/ITO interface ruptures under negative voltage, switching the device back to HRS [118].

these switching properties have been applied. In particular, the interface state between an electrode and an organic material influences the charge injection barrier, and new interfaces can be designed to adjust the electrical characteristics of organic devices. The simplest method for modulating this interface is to change the type of electrodes used in organic resistive memory devices. The effects of different electrode combinations on conductance switching devices have been studied by Mukherjee et al [119]. Moreover, the resistive switching voltage in polymer-metal nanoparticle films can be tuned by changing the work function of the electrode [120]. Introducing additional layers at the metal–polymer interfaces is an effective strategy for controlling the mobility or number of charge carriers that pass through organic devices, as demonstrated for example by Kondo et al. [113].

The importance of morphology in organic electronics has been emphasized because charge conduction through a device is often strongly governed by the surface morphology of an organic film. For this reason, the morphology of the organic layer has been carefully controlled to produce excellent non-volatile memory effects. For example, the deposition of a pentacene layer at a low deposition rate was found

to play a definitive role in the occurrence of the resistive switching, while the deposition of a pentacene layer at a high deposition rate stabilized device performance [121]. Metal atoms can move inside an organic layer during the evaporation of the top electrode, and this inter-diffusion phenomenon strongly depends on the grain size of an organic film [122]. The deposition rate is one of the growth parameters that can be adjusted to change electrical characteristics in the organic memory.
Generally, the electrical switching characteristics of memory devices fabricated with composite materials can be modulated by controlling the nanomaterial concentration, as demonstrated by Song et al. [112].

Architectural concepts for advanced memory devices

The cross-talk phenomenon in memory cells often occurs due to parasitic leakage paths (called sneak paths) through neighboring cells with low resistances in cross-bar array structures or the presence of excess currents that can cause electrical damage. These phenomena disturb the reading process in selected cells, which must be eliminated in practical memory applications. To solve the cross-talk problem, a switching element (diode or transistor) can be added to each memory cell. The International Technology Roadmap for Semiconductors has also stressed the incorporation of switching elements in cross-bar array memory structures. Indeed, one diode-one resistor (1D-1R) or one transistor-one resistor (1T-1R) architectures improve reading accessibility without disturbing the reading process. Compared to the integration of the 1T-1R structure, the 1D-1R architecture is preferred because it occupies less area. Furthermore, the design and fabrication are simpler for 1D-1R circuits than for 1T-1R devices. For these reasons, 1D-1R systems have recently been developed [123, 124]. Electrically rewritable switching in the 1D-1R structure can be achieved only with the use of unipolar-type switching memory.
Unnecessary leakage paths in cross-bar array structures can form through the neighbors of a selected cell if the polymers lack rectification properties. These paths affect the reading process and cause misreading errors (i.e., they produce crosstalk phenomena). This reading disturbance problem can be prevented by adding diode components. If rectifying diode components are integrated into the resistive memory cells, the unintentional leakage path through the cell can be prevented, and misreading can be avoided. This improved reading capability can enable the production of high-density organic memory devices integrated with an array architecture.

Flexible Memory Applications

Flexibility is required for future electronic applications, such as foldable and stretchable electronics. A variety of technologies have been conceived and applied to achieve flexibility in organic and inorganic electronics, and new concepts are being developed. In particular, the evolution of flexible electronic applications that require information storage components has advanced research on flexible memory devices. The use of flexible memories based on organic materials is important because of their simplicity, low manufacturing costs, and the flexibility itself. Several studies on organic memory devices fabricated on flexible substrates have been conducted in the last years, as for example in work of Son et al. [115].
Printable organic materials are one of the most important emerging technologies for the mass production of large flexible electronics. These technologies should be used in organic resistive memory devices. Indeed, printability is necessary for item-level RFID tags, large-area sensors, flexible displays, and many other emerging electronic applications.

2.4.6 Developmental status

Over the past four decades, a wide variety of organic materials have been explored for memory applications. Advanced technologies in film deposition, device fabrication, device testing, memory structure and memory architecture have been developed. Many phenomenological explanations, theoretical models and calculation methods have been proposed and developed to better understand the mechanisms. Despite these efforts, many of the RRAM phenomena remain to be ascertained and have become a major obstacle in the research and development of organic RRAM memory technology. Another serious problem is the reproducibility of research results, as many apparently contradictory results can be found in the literature. It is recognized that the details of sample preparation and morphology, electrode materials, interfacial properties, device structures, testing methods and environment, all have a profound effect on the device performance.

3 RESEARCH ACTIVITY MOTIVATIONS

Contents

3.1 Progress beyond the state of the art

Research on organic electronic memories is currently at a rapid growth stage, since it is recognized that they may be an alternative or supplementary to the conventional memory technologies. Despite considerable progress in the advancement of novel memory technologies in recent years, some challenging tasks still need to be resolved. In particular, as already thoroughly described in the previous chapter, tremendous progress has been made in the field of **OFET memories** since they were first described. OFET memories have great potential for application in low cost, large areas, plastic systems, but many challenges are still open. These include:

- program/read/erase voltages are still large;
- data retention times are too short to satisfy the requirements of practical applications;
- operating mechanisms of OFET memories are not clearly understood.

All of these issues need to be addressed in the future to aid the design of high performance devices.
Similarly, thanks to the efforts of scientists and engineers all around

the world working on organic **RRAMs** over the past decades, the progress of research in this field is extremely noteworthy and significant. However, despite significant advances made in the last years, organic resistive memory devices are still at an early stage, if compared to organic optoelectronic devices; it must be admitted that some serious challenges are still open. Several future directions in this field should be followed in order to develop high performance polymer resistive memory materials and devices, and exploit their further practical applications.

The first challenge is a thorough understanding of the switching mechanisms, which is a long-term desire of scientists and can serve as a guide for engineers who work on optimizing the structure and performance of RRAMs. So far, inconstant switching mechanisms have been suggested by different research groups even in the same sandwich structure. This phenomenon was most likely caused by the differences in the fabrication process of the same device, which has seriously confused the researchers committed to revealing the underlying switching mechanisms. Therefore, more systematic works are needed to obtain a exhaustive knowledge of the resistive switching mechanisms.

Another important mission is to develop fabrication techniques that improve device reproducibility and consequently reduce deviations in electrical characteristics. Identifying and systematizing critical fabrication parameters for the control and optimization of switching characteristics is central to this effort. Furthermore, correlations between the memory parameters (ON/OFF ratio, retention time, cycling endurance, switching speed, and so on) should be investigated to optimize memory performance. Close attention should be paid to the performance enhancement of organic RRAMs which will certainly play an important role in future flexible electronics. Indeed, for practical applications, a larger attention must be oriented on memory devices fabricated on flexible substrates.

The real employment of organic resistive memories in operational environment represents a fundamental issue. Indeed, many reported works show excellent performances but the devices have been only characterized and stored in inert atmosphere. As illustrated in the previous chapter, only few reports show a reproducible bi-stable behavior under ambient atmosphere. The demonstration of significant improvements in organic RRAMs in terms of reproducibility and stability under ambient atmosphere should represent one of the main aims and motivations for further research in this area.

The Ph.D. research activity of this thesis is related to these still - opened challenges in the organic memories technologies. In particular, it has been mainly focused on the study, development, fabrication

and characterization of new non-volatile organic memory elements based on resistive switching. The activity has been carried out in the frame of the European project "HYbrid organic/inorganic Memory Elements for integration of electronic and photonic Circuitry" (HYMEC), which has involved the University of Cagliari during the last three years; more details will be discussed in next paragraph.
A complementary activity on transistor-based organic memory devices has been also carried out. Specifically, highly flexible organic field effect transistors (OFETs) have been employed for memory applications.
In the next three parts, the activity will be presented:

- in the Part Two, the development of a novel non-volatile memory device based on the combination of an air-stable organic semiconductor and metal nanoparticles will be presented; the research activity included design, fabrication and testing of a novel, high-performances memory structure; this topic required the development of technology and procedures for easy and reliable production of devices as well as the definition of measurement protocols;

- in the Part Three, the integration of memory elements with electrical sensor devices will be presented; in particular, this last activity required first of all the selection of electrical sensors to be integrated with organic memory elements and definition of their fabrication procedures; fabrication and characterization of integrated sensor/single memory element system has been carried out; to conclude, the activity was concentrated on the development of integrated sensors/array of memory devices system;

- finally, in the Part Four, the activity on the trasistor-based memories will be presented; this part includes the testing of an high performances OFET structure as flexible memory element; in particular, this activity was related to the development of reliable measurement procedures.

3.2 The HYMEC project

3.2.1 Goals

The objectives of the HYMEC project were to resolve fundamental issues of materials science and to realize new hybrid inorganic/organic devices with functionality far beyond the state of the art. Specifically, research was supposed to be performed towards

understanding and controlling all relevant properties of systems comprising inorganic metal nanoparticles (NPs) embedded in matrices of conjugated organic materials. Moreover, cost-efficient production routes, such as printing, were proposed to be implemented. Electronic, optical, dielectric, structural, and morphological properties of systems were supposed to be determined using state of the art experimental techniques and modelling to establish a reliable specific knowledge base for device fabrication and integration.
Consequently, the following key objectives were defined:

- reveal the fundamental mechanisms for information storage and addressing in non-volatile memory elements based on metal nanoparticles in conjugated organic matrices;
- expand the functionality of hybrid memory elements by including optical addressing;
- develop cost-efficient fabrication routes of hybrid memory elements ranging from micro- to nanoscales;
- demonstrate fully functional electrically and optically addressable hybrid memory element arrays, including integration with other functions.

As already said, the experimental data available for devices based on hybrid nanoparticle/organic matrix systems are insufficient to consistently explain the current/voltage characteristics, which inhibits further progress and implementation of such elements in applications. HYMEC wanted to relieve this highly unsatisfactory situation by a concerted experimental and device modelling/simulation effort towards establishing clear-cut structure-property-function relationships for devices based on metal NPs embedded in organic matrices. Going beyond establishing a reliable knowledge-base (first objective from above), it proposed to expand the functionality of non-volatile memory elements (NVMEs) towards optical addressing capability (second objective), to implement cost-efficient fabrication methods (printing and nanostructure formation) and integrate NVMEs with other functional elements to reveal the full potential of this technology (last two objectives).

3.2.2 UNICA tasks

The main tasks of the University of Cagliari (UNICA) can be summarized as following.

- *Fabrication of defined model memory element structures.* Single memory element structures with ultimate control of device structure and morphology were supposed to be fabricated by means of vacuum sublimation based methods and solution-based processing. Systems comprising metal NPs embedded in matrices of conjugated organic materials with different initial device structures (see `Figure 3.1` were supposed to be investigated in order to unambiguously identify the operation principle. As shown in `Figure 3.1`, the investigated structures are defined by varying organic matrix materials and sequence, as well as layer thickness of A and/or B components, position of metal NPs in the matrix, their size, distribution and spatial location. In particular, all the devices were supposed to be realized in a controlled way, and key parameters were supposed to be varied systematically through appropriate fabrication: organic matrix materials and/or sequence (A or B in `Figure 3.2 a)`), their respective layer thickness (d_1, d_2), metal NP mean size and average distance (d_{NP}), electrode materials (E_1, E_2).

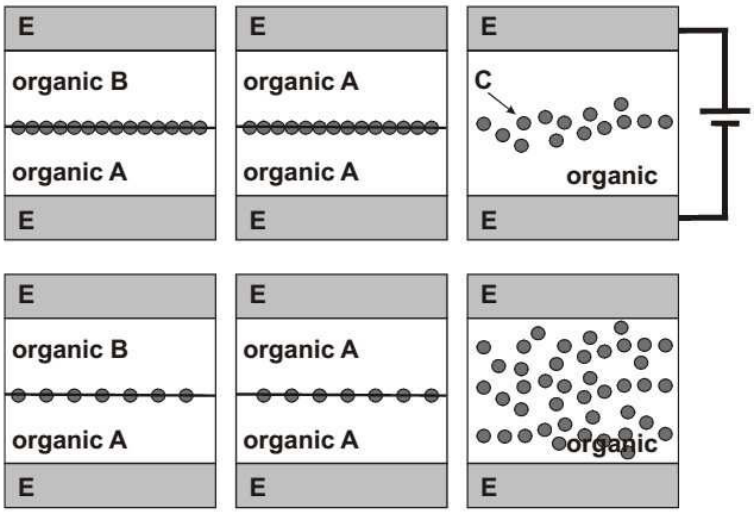
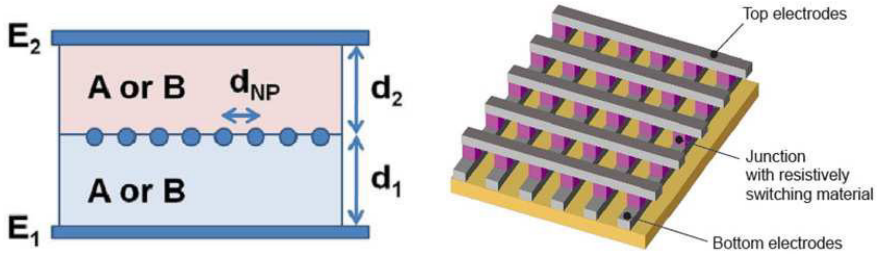


Figure 3.1: Schematic of different initial device structures of NV-MEs to be investigated in HYMEC.

- *Fabrication and characterization of basic crossbar memory element arrays.* Besides the classical sandwich structure, planar device structures were supposed to be used in a matrix of memory elements (`Figure 3.2 b)`).
- *Integration of memory elements with electrical sensor devices.* Single memory elements were suppopsed to be integrated with



(a) (b)

Figure 3.2: a) Key paramenters of the structure of NV-MEs to be investigated in HYMEC. b) Schematic of crossbar memory element arrays.

an electrical sensor device (resistive or capacitive) to form a system storing a specific state, readable by the memory element. The interaction between the sensitive element, initially connected in series with the memory element, and an external stimulus should induce a change in the electrical behaviour of the device (change of the conductivity/dielectric constant of the resistive/capacitive sensor). The induced change should be used for writing/erasing a HYMEC system. One critical issue of the NV-ME-sensor system is that only the sensor resistor/capacitor should be sensitive to the target parameter (temperature, analyte, mechanical stimulus), while the characteristics of the NV-ME should remain constant.

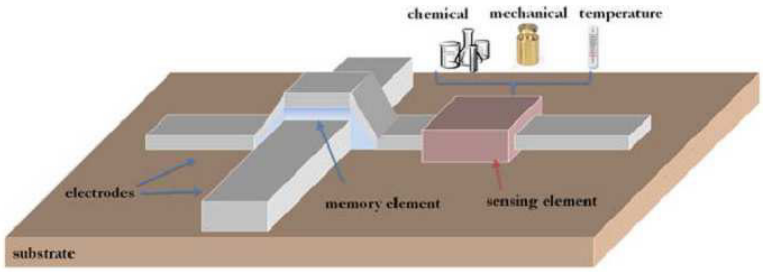


Figure 3.3: Scheme of integration of electrical sensor device with NV-ME devices.

Part II

Non-Volatile Organic Resistive Memories

4 AN AIR-STABLE ORGANIC RRAM

Contents

4.1 Introduction

As already explained in Chapter 2, so far, several materials have been studied for RRAM applications, and many groups have demonstrated the resistive switching in several types of organic and polymeric materials with different device structures. However, despite these promising performances, organic bi-stable memory devices

are still in the exploratory stage of the research. Several important issues, such as the physical explanation of the resistive switching behavior, are still not clear. Although a remarkable amount of research has been made and many plausible mechanisms have been proposed by different groups, the understanding of the resistive switching phenomena is still controversial. Furthermore, their stability and reliability are still debatable. Indeed, organic memories should benchmark against inorganic FLASH memories in terms of data retention time, number of operation cycles, power consumption and stability in ambient conditions, in order to allow them to be employed in commercial products. One of the main issues concerning the real employment of such devices in operational environment deals with their long time stability. Indeed, many reported works show excellent behaviors but the devices have been only characterized and stored in inert atmosphere. Only few reports show a reproducible bi-stable behavior under ambient atmosphere [114, 115, 117]. Among them, the best results were obtained for devices with a (measured) retention time in ambient atmosphere in the order of 10^5 s, which is still far to be a satisfactory performance for real applications. For these reasons, significant improvements in organic RRAMs in terms of retention time under ambient atmosphere should represent one of the main aim and motivation for future research in this area.
In this Chapter a novel non-volatile memory device based on the combination of an air-stable organic semiconductor and metal NPs is presented. The device is particularly conceived for allowing long-term data storage in ambient conditions with high ON/OFF ratios. A complete electrical characterization of the memory element will be provided, together with an in-depth morphological investigation of the structure in order to precisely define its working principle.

4.2 Structure and materials

The memory devices fabricated in this study are two terminal elements, consisting of an hybrid layer between a cross-point array of top and bottom electrodes. The hybrid layer is a nanocomposite material obtained by sandwiching a metal nanoparticles interlayer between two organic semiconductor layers. The schematic view of the device structure is shown in Figure 4.1.

Memories were fabricated on different Indium Thin Oxide (ITO) coated substrates, including glass (KINTEC, $2.5 \times 2.5\ cm^2$) and PET (Delta Technologies). Both are transparent substrates, and the second one is a plastic material, which is suitable for the fabrication of flexible structures.

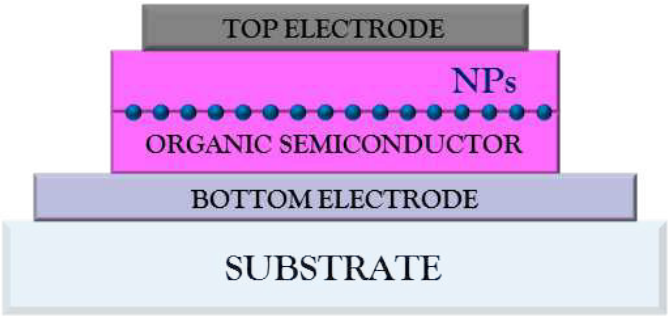


Figure 4.1: Schematic view of the layered memory element.

Bottom electrodes were made of ITO, in order to have a trasparent conductor which can be directly patterned on the substrate. Top electrodes were made of gold (Au) or silver (Ag).
A commercially available perylene derivative, namely *ActivInk*^{TM} *N1400* (Polyera), was employed as organic semiconductor. It is an n-type semiconductor, which can be deposited by thermal evaporation but also from liquid phase since it is soluble in chlorinated solvents. Moreover, it shows stable performances in ambient conditions. Two different types of metal nanoparticles, namely aluminum (Al NPs) and gold (Au NPs), were employed for the intermediate nanoparticles layer. More details on materials che be found in the Appendix A.

4.3 Layout definition

Different layouts have been designed and tested during the Ph.D. research activity in order to define the best trade-off between fabrication process of each component, project requirements and performances of the devices. In particular, an overlap area of $150 \times 150\ \mu m^2$ was defined as HYMEC design rule. Moreover, a significant number of memory devices should be fabricated on each substrate in the foresight of making matrixes for multi-bit data storage.
`Figure 4.2 a)` shows the first implemented layout. The project specification about memory area was fulfilled by reducing the size of the sole top electrode, which was patterned as a small pad. On the contrary, an unique ITO film was employed as common bottom electrode for all the devices. Two main drawbacks were found in this layout:

- the connection to measurement systems through the top electrode resulted difficult, as probes can easily scratch the pads and determine short circuits between the stacked, thin layers;

- a significant cross-talk between the memory devices can be determined by the common bottom electrode.

In order to overcome such limitations, a strong effort was devoted to the definition of technological processes for the patterning of ITO bottom electrodes. The development of an ITO photolitographic process led to the layout shown in Figure 4.2 b).
In order to prevent any possible cross-talk or parasitic effect between memories, a more refined layout was conceived. As shown in Figure 4.2 c) and d), clear-cut top electrodes have been gradually obtained and the N1400 area was reduced to the minimum according to constraints of the fabrication process.
Finally, Figure 4.2 e) shows the layout employed for flexible memory devices. In particular, the design was conceived to allow the integration of memory elements with electrical sensors, as it will be shown in the following chapters.

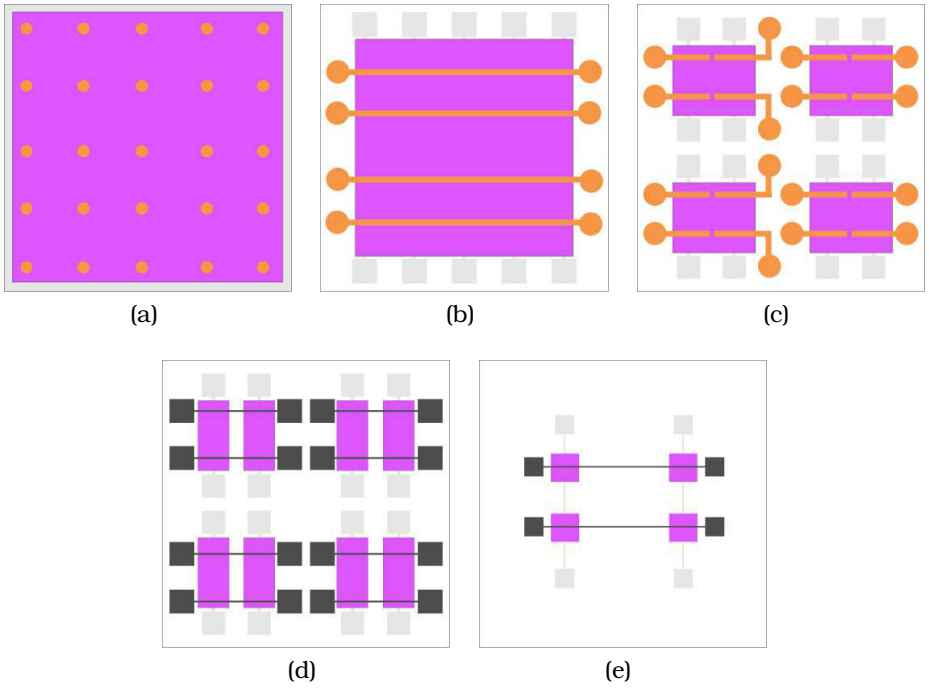


Figure 4.2: Implemented layouts.

4.4 Fabrication process

The fabrication process for a single memory element is schematically depicted in Figure 4.3. It starts from an ITO coated susbtrate,

on which bottom electrode is directly patterned. The first N1400 film, metal NPs and the second N1400 layer are consecutively deposited. Finally, the top electrode deposition makes an end of the process. In the following, the details of each fabrication step will be provided in reference to the scheme of Figure 4.3. The reader can find more details on the employed materials and methods in the Appendix A.

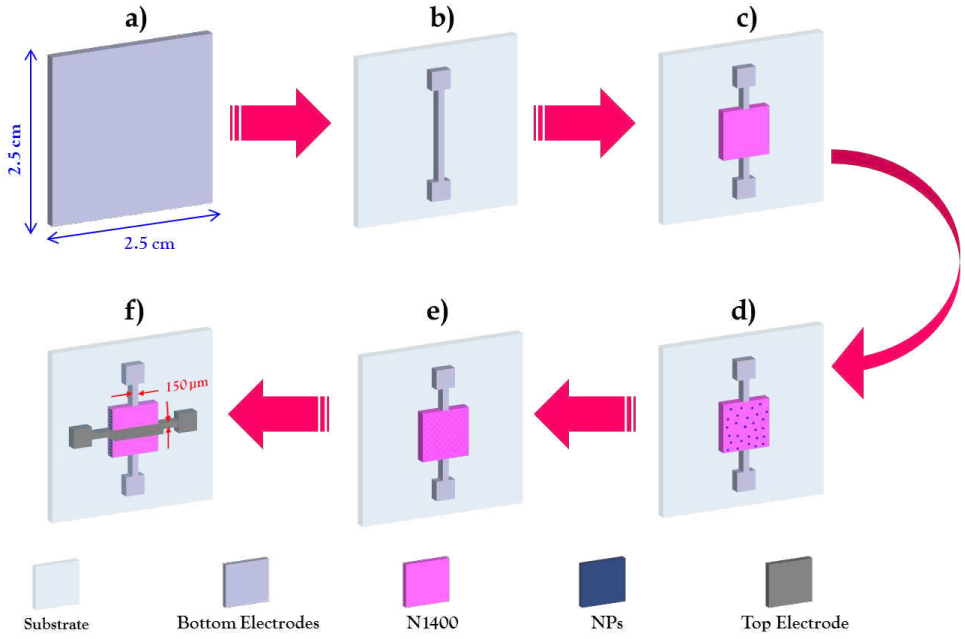


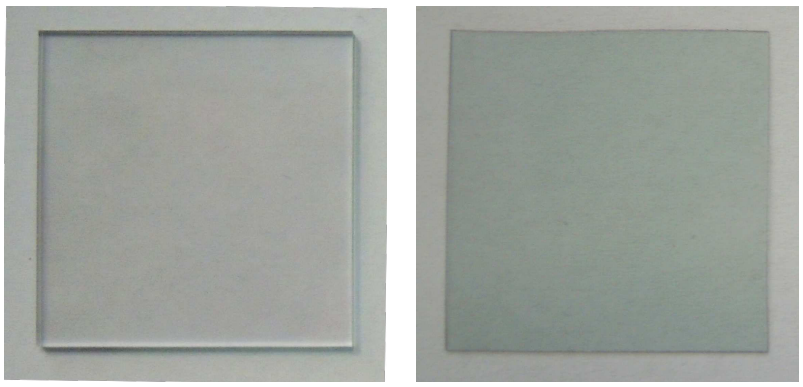
Figure 4.3: Scheme of the fabrication process: a) ITO coated substrate; b) ITO bottom electrode patterning; c) first N1400 layer, d) NPs, e) second N1400 and f) top electrode deposition.

4.4.1 Substrate preparation

No particular preparation of the substrates (both glass and PET) was necessary before the actual fabrication steps, apart from a basic cleaning procedure performed by a subsequently rinsing with acetone, isopropyl alcohol and deionized water. Finally, samples were dried under a nitrogen flux. Figure 4.4 depicts the employed substrates.

4.4.2 ITO bottom electrodes patterning

The ITO bottom electrodes were defined using a photolithographic process. In particular, a strong effort was devoted to the definition



(a) (b)

Figure 4.4: Employed substrates: a) ITO coated glass; b) ITO coated PET.

of a reliable and reproducible ITO patterning process. Patterning of thin films of ITO is usually done by lithography, which includes an etching step. Both wet and dry etching are suitable for ITO patterning according to different application [125, 126]. Wet etching is widely used in industry for pattern transfer due to its low cost, excellent selectivity and large yield. For these reasons, wet etching process was preferred for ITO patterning in this study. In the following, the details of the developed technique will be provided for glass as well for PET substrates.

ITO coated glass patterning

A ITO coated glass was used as the starting substrate. As ITO is hydrophobic, a 30-minute surface activation with an UV-Ozone treatment is necessary before starting the photolithograhic process (Figure 4.5 a)). A positive photoresist (Microposit AZ1518®) was employed. An uniform photoresist film was deposited on the whole substrate by means of spin-coating (Figure 4.5 b)-c)), and then dried into an oven at 40 °C for half an hour. In this way, the solvent was removed and the cross-linking of the photoresist molecules was obtained (Figure 4.5 d)).

The patterning of the electrodes was made by exposing the photoresist to UV-B radiation through a mask reporting the exact shape to be transfered (Figure 4.5 e)). In a first step, the photosensitive material was developed by means of a 175 mM solution of sodium hydroxide in water (pure developer), which removed the photoresist not shadowed by the mask. However, only 40% of electrodes resulted successfully patterned. Therefore, some tests were carried out in order to determine the best solution of sodium hydroxide in water

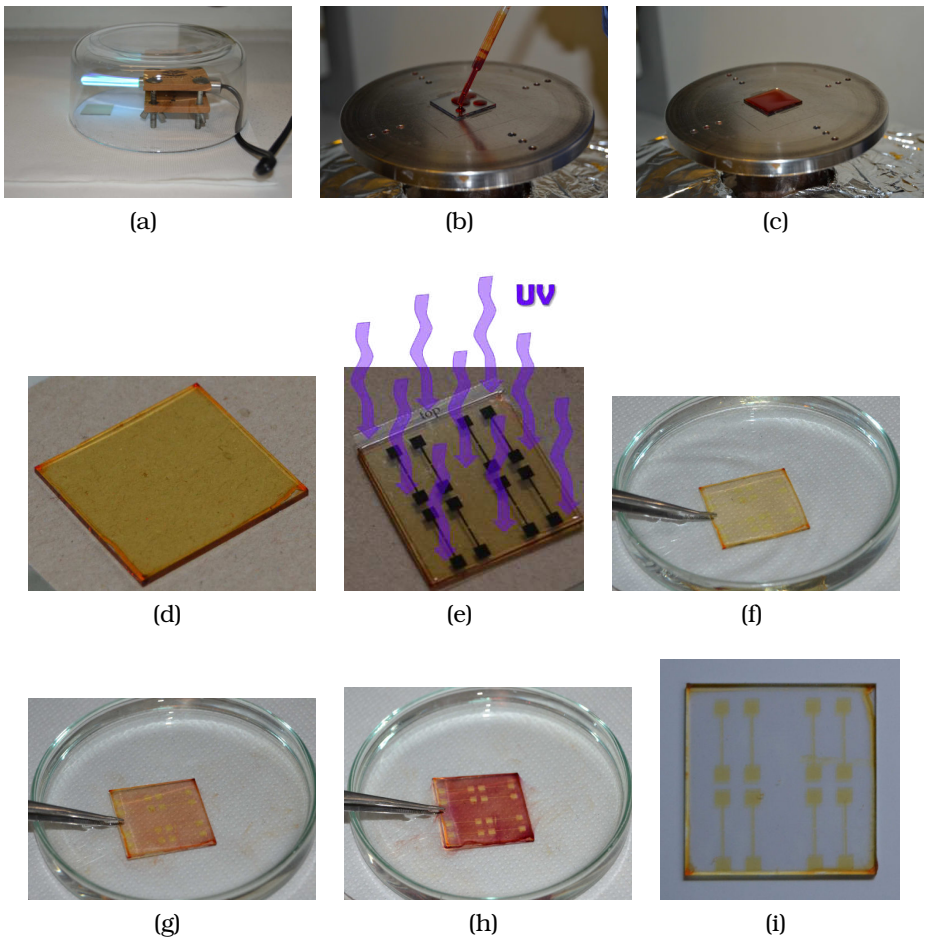


Figure 4.5: ITO photolithography on glass substrate: a) surface activation; b) and c) photoresist deposition; d) dried photoresist; e) photoresist exposition to UV-B radiation through a mask; f)-h)photoresist development; i) developed electrodes.

for a realiable photoresist development. It was found that a solution of 2/3 of pure developer and 1/3 of deionized (DI) water in volume allows to develop the 100% of electrodes (`Figure 4.6`). The excess of ITO resulted finally exposed, thus being etchable (`Figure 4.5 i)`).

According to literature [127], hydrofluoric acid (HF) can be used as ITO etchant. Different HF solutions were tested:

- *HF : DI water = 1:50*: ITO was not removed;
- *HF : DI water = 1:10*: ITO was not removed;
- *pure HF*: ITO was removed in 10 sec but HF started to etch also the glass substrate.

	Without surface activation	With surface activation
Pure developer	*0%*	*40%*
Dilute developer	-	*100%*

Figure 4.6: Statistic data related to ITO surface activation and photoresist develepment process.

This technique cannot be used for a reliable and controllabe ITO electrodes patterning. Hydrochloric acid (HCl) and HCl with additional nitric acid (HNO_3) are often used as wet etchants for ITO films [128]. Hence, in the next step a HCl-based solution was used for the ITO etching. In particular, the best results were obtained with the formula $HCl : H_2O : HNO_3 = 4 : 2 : 1$ by volume. The concentration of HCl is 37% and that of HNO_3 is 70%. In this case, the yield of the etching process was of about 55%, which is still not satisfactory.
Subsequently, HCl was used in combination with zinc powder. The zinc/acid reaction produces hydrogen which reduces the oxides, and the residue are attacked directly by the acid. The developed technique is depicted in `Figure 4.7`. In particular, the procedure can be summarized as following:

- sprinkle zinc powder uniformly over the dry substrate (`Figure 4.7 b)`);
- drop 37% HCl on the zinc powder (`Figure 4.7 c)`);
- after few seconds flush the sample with water to remove the acid (`Figure 4.7 d)`);

Finally, the residual photoresist covering the ITO was removed by rinsing the sample with acetone. The result of the photolithography is shown in `Figure 4.7 e)`. `Figure 4.8` demonstrates the perfect transfer of the pattern from the mask to the substrate and illustrates optical microscopy image which clearly shpwing the high resolution of the patterned electrodes. In particular, electrodes width as small as 150 μm were obtained. Moreover, the process yield resulted to be 100%, thus making this chemical etching the best technique for ITO patterning.

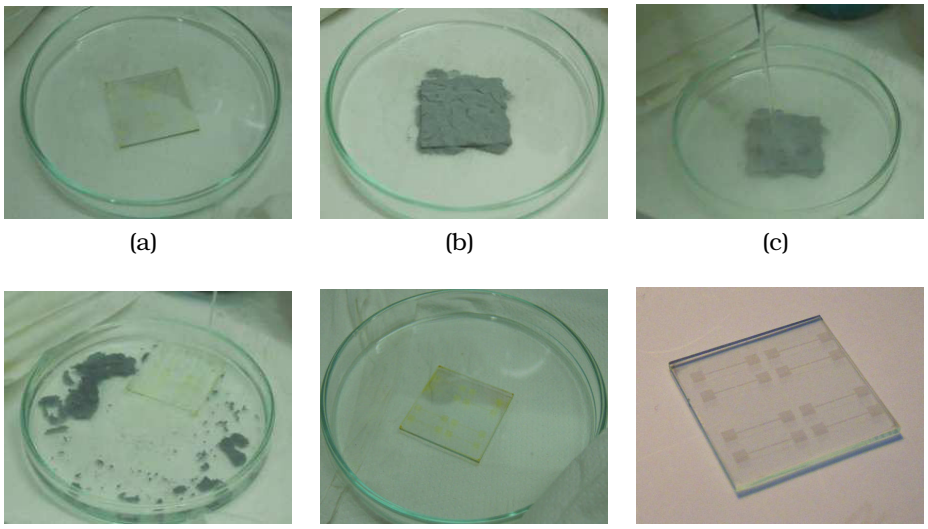


Figure 4.7: ITO etching on glass substrate: a) dry substrate; b) zinc powder sprinkled uniformly over the dry substrate; c) HCl dropped on the zinc powder; d) removal of the acid with water; e) residual photoresist covering the ITO; f) result of the photolithography.

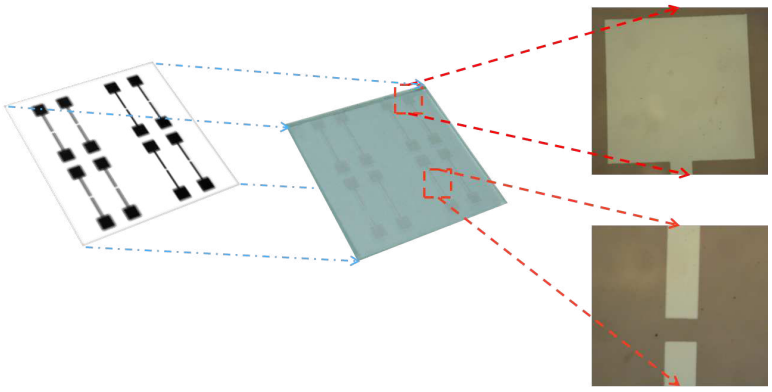


Figure 4.8: Perfect transfer of the pattern from the mask to the glass substrate and optical microscopy images of the high resolution electrodes.

ITO coated PET patterning

ITO patterning on PET substrate required some adjustments in the etching step. Indeed, the process is identical to one of glass substrate up to the photoresist development, but in order to avoid the PET corrosion, a solution of 1/3 of 37% HCl and 2/3 of DI water was employed for the etching. Moreover, it turned out that zinc

powder needs to be sparkled after the HCl solution drop. Hence, the etching process steps were modified as following:

- cover all the sample's surface with the diluted HCl solution (`Figure 4.9 a)`);
- sprinkle zinc powder on the HCl covered substrate (`Figure 4.9 b)`);
- after few seconds flush the sample with water to remove the residual of HCl/zinc (`Figure 4.9 c) and d)`).

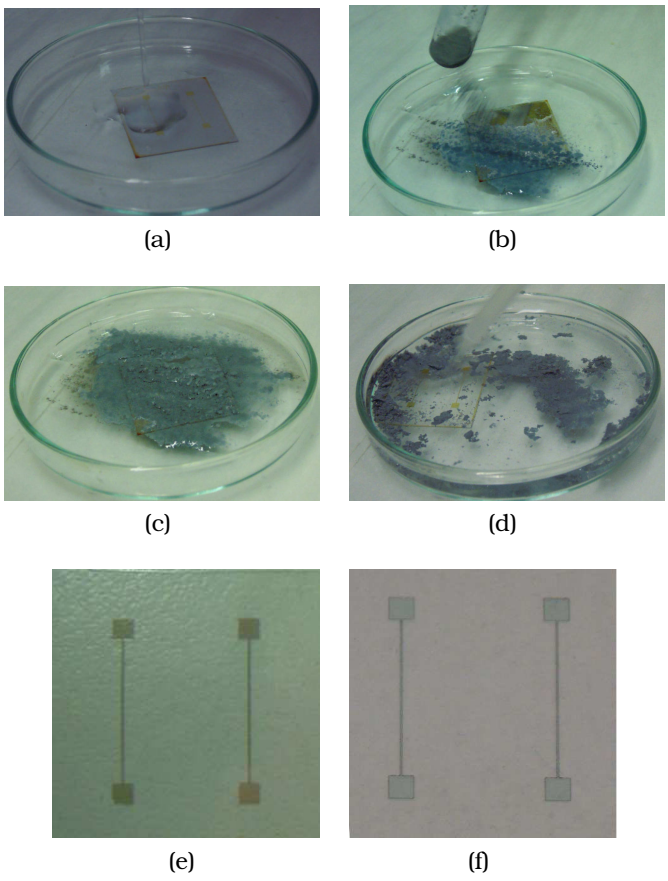


Figure 4.9: ITO etching on PET substrate: a) HCl dropped on the dry substrate; b) zinc powder sprinkled uniformly over HCl; c) HCl/zinc powder reaction; d) removal of the acid with water; e) residual photoresist covering the ITO; f) result of the photolithography.

The residual photoresist covering the ITO was removed as usual by rinsing the sample with acetone. The etching process is shown in

Figure 4.9. Also in this case, electrodes width as low as 150 μm was obtained.

4.4.3 Hybrid layer deposition

The hybrid layer is obtained by sandwiching a metal nanoparticles interlayer between two organic semiconductor films. In particular, N1400 layers were thermally evaporated with a shadow mask (Figure 4.10) under a pressure of about 10^{-5} Torr with a deposition rate of about 1 Å/s. The film thickness was thoroughly monitored during the thermal evaporation with a quartz crystal microbalance.

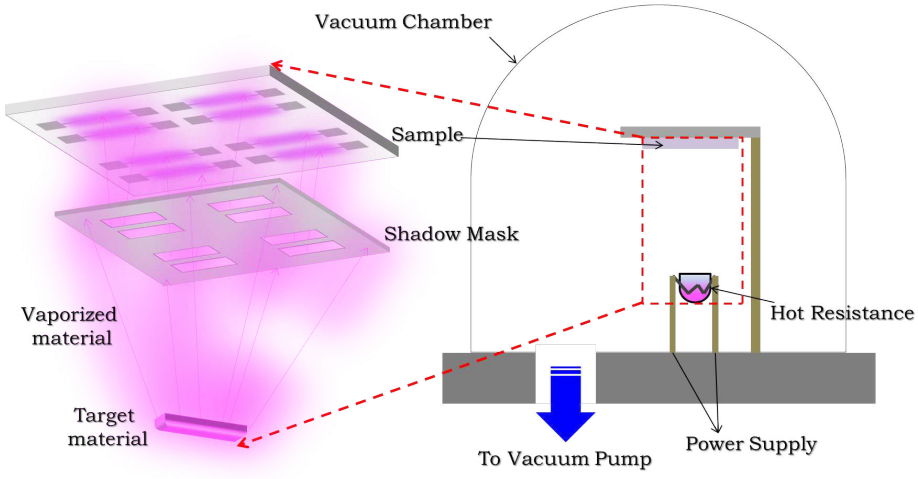
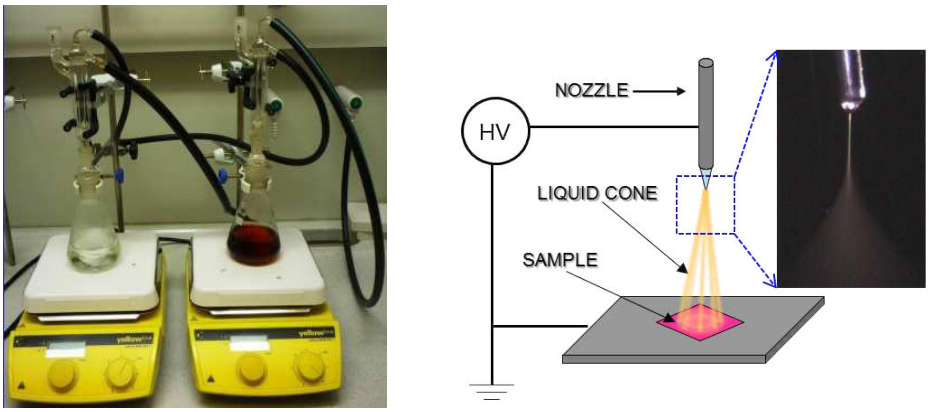


Figure 4.10: Thermal evaporation through a shadow mask.

As already reported, two different metal nanoparticles, Al NPs and Au NPs, were tested as intermediate layer. Specifically, two different deposition techniques were employed. Al NPs were deposited by thermal evaporation with a shadow mask under a pressure of 10^{-5} Torr. Also in this case, the nominal thickness of such interlayer was thoroughly monitored during the deposition with a quartz crystal microbalance.
Gold nanoparticles were synthesized and deposited at the University of Łódź (Poland). In particular, NPs were synthesized according to chemical reduction method described in [129]. Briefly, a mixture of sodium citrate tribasic dihydrate (0.9 g, 1 wt%) and tannic acid (0.8 g, 1 wt%) was added to the boiling aqueous chloroauric acid solution (98 g, 0.009 wt%) under reflux. The color of the solution

immediately changed from yellow to dark red, as a result of Au NPs formation (Figure 4.11 a)). Afterwards, the mixture was stirred for additional 15 minutes and then cooled down to room temperature. The NPs final concentration was 50 ppm with an average size of 9 $\pm$ 2 nm.
Au NPs were deposited on samples by means of electrospraying. In particular, 6 ml of purified colloid were obtained by several cycles of centrifugations and adding deionized water. The solution actually employed in the electrospraying equipment was obtained by mixing 2 ml of purified colloid, 1 ml of deionized water and 1 ml of pure ethyl alcohol (96%). A single jet deposition mode was employed (Figure 4.11 b)), with applied voltage ranging from 6 to 7 kV and with a distance between the nozzle and the substrate of 2 cm.



(a) (b)

Figure 4.11: a) Au NPs synthesis (the color of the solution changes from yellow to dark red, as a result of Au NPs formation); b) Au NPs electrospraying.

4.4.4 Top electrodes deposition

The fabrication process ends with the deposition of top electrodes. In particular, silver and gold were employed. Both metals were thermally evaporated under a pressure of 10^{-5} Torr. The pattern of the electrodes was defined by means of high resolution shadow mask reporting the same shape of the ITO bottom electrodes (with a width as low as 150 μm). Figure 4.12 a) and b) shows the design and and a picture of the employed mask, respectively. Figure 4.12 c) and d) depicts pictures of fabricated devices on glass and on PET substrates.

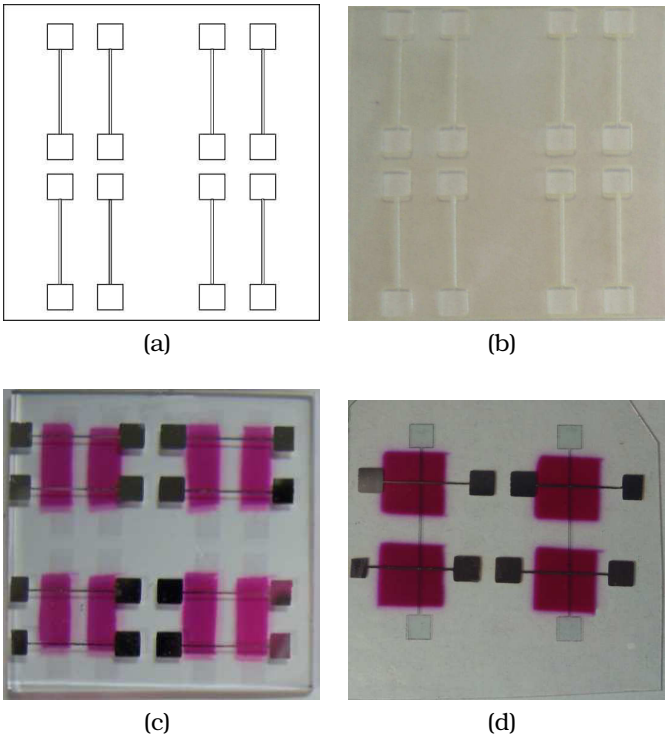


Figure 4.12: a) Design and b) picture of the top electrodes mask; picture of the fabricated devices on glass c) and d) PET.

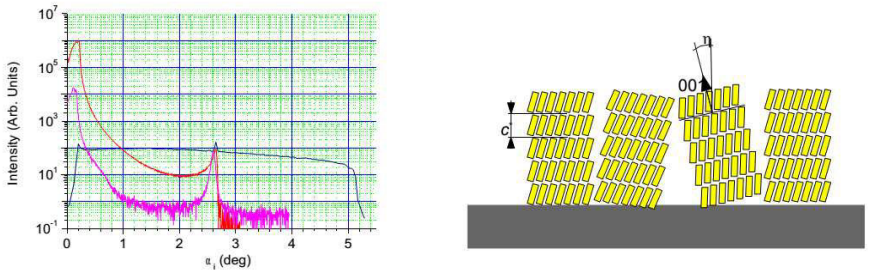
4.5 Morphological characterizations

Knowledge of the structural and morphological properties of a memory element is necessary in order to obtain a reproducible switching effect, maximize the ON/OFF current ratio, the retention time and the overall lifetime of the devices. Indeed, for each hybrid device structure incorporating metal NPs, performace will strongly depend on the size and spatial distribution of metal NPs within the host matrix. A thorough understanding of their growth and structure is essential, since the morphology of organic semiconductors has a strong impact on their charge carrier mobility and other physical properties. Thus, there is a need to investigate the different structural aspects of the hybrid structures, e.g. the growth and morphological properties of the host organic films, the controlled ordering and density distribution of NPs with a desired area coverage within the organic layers and their potential impact on the properties of the organic host.
During this Ph.D. research activity, a morphological characterization of every element of the resistive hybrid layer was carried out

thanks to the collaborations with the University of Namur and Tubingen, partners of UniCA within the scope of HYMEC project. In particular, the structure of the organic film, the metal clusters layer, and the thin films morphology were studied by X-ray specular reflectivity (XSR), Grazing Incidence Small Angle Scattering (GISAXS), and Atomic Force Microscopic (AFM). Moreover, the metal NPs interlayer was characterized by High Resolution X-ray Photoemission Spectroscopy (HR-XPS), which allow determining the metal content, studying the metal-organic interface and characterizing the metal NPs oxidation shell.

4.5.1 N1400 layer characterization

First, the organic layer was fully characterized by means of XSR. `Figure 4.13 a)` shows XSR, off-set scan, and rocking scan through the 001 Bragg reflection of an N1400 layer with a nominal thickness of 100 nm: red, magenta, and blue curve, respectively. Data are plotted as function of the incidence angle of the X-ray beam. It turned out that the organic film grows with long molecular axis of N1400 almost parallel to the substrate normal and 001 net planes parallel to the substrate surface (`Figure` 4.13 b)). As follows from the broad rocking scan through the Bragg reflection the layer is composed of mosaic blocks with the c-axis misorientation larger than 2.5 °. The spacing of 001 N1400 net planes, as follows from the position of the Bragg peak, is $c^* = (1.68 \pm 0.01)nm$.

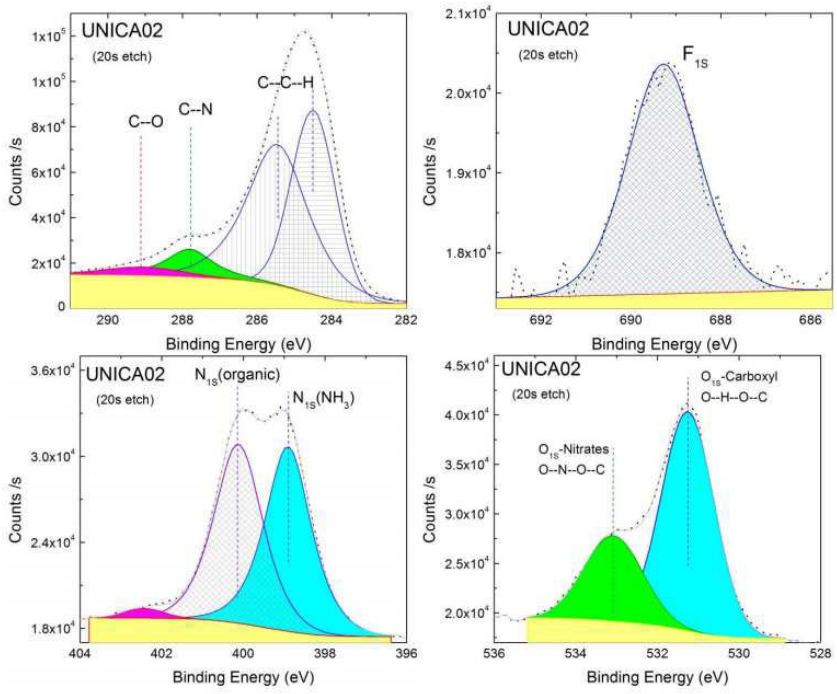


(a) (b)

Figure 4.13: a) Specular X-ray reflectivity, off-set scan, and rocking scan through the 001 Bragg reflection of N1400: red, magenta, and blue curve, respectively; b) Scheme of N1400 film composed of mosaic blocks with 001 net planes dominantly oriented parallel to the sample surface.

Subsequently, the organic layer was characterized in terms of quantification of the elemental species (evaluation of the atomic percent) and characterization of their chemical environment (HR-XPS). The organic layer resulted to be composed by carbon (C), nitrogen

(N) and oxygen (O) atomic species. All the samples studied had an oxygen and carbon surface contamination layer of few nanometers thickness which has been characterized and then removed,*in-situ*, by low energy argon ions etching. Argon (Ar) ions acceleration energy was set at 500 eV. Few seconds exposure time (less then 20 s) were needed in order to remove the contamination layers. The Ar energy was weak enough to ensure that the organic layer is not modified by the etching process. As shown in `Figure 4.14`, the presence of fluorine surface contamination ($\backsim$ 1 at%) was revealed and the chemical environment for all atomic species present in the molecule was identified. In particular, fluorine contamination ranging from 0.2 at% to 0.5 at% was present in all the samples. Atomic element quantification is shown in the `Figure 4.14`, the oxygen contamination layer is evidenced by the O at% drop. From top left to bottom right, C_{1S}, F_{1S}, N_{1S}, O_{1S} peaks. Peak fitting main components are shown in the figures.



Ar Etch time	C At%	O At%	N At%	F At%
0s	81	11	7	1
20s	87	6	7	0

Figure 4.14: HR-XPS spectra of N1400 layer.

4.5.2 NPs/N1400 interface characterization

Hybrid films comprising N1400 layers with different thicknesses and a 15-nm-thick Al layer deposited at various growth rates were characterized by X-ray specular and off scan reflectivity, GISAXS, AFM, and HR-XPS, in order to identify influence of the Al growth rate on the clusters and organic thin film structural properties. The thin films of N1400 were grown using thermal evaporation on $Si - SiO_x$ substrates. Al clusters were thermally evaporated on top of the N1400 layer at various growth rates between 0.17 and 25 Å/s. Additionally, reference samples of bare N1400 were characterized. X-ray specular reflectivities of all studied samples are shown in Figure 4.15 a). Three distinct regions A, B, and C are indicated in the graph. Each of them corresponds to different regimes of the reflectivity curves and provide information on different structural properties. In region A, the position of the peak (above which the intesity starts to decrease) is related to the mass density of the present layers. For all samples with Al clusters it is possible to rule out the presence of a continuous layer of Al (confirming formation of clusters), since no shift of the peaks are observed towards higher values, when compared to the sample with bare N1400.

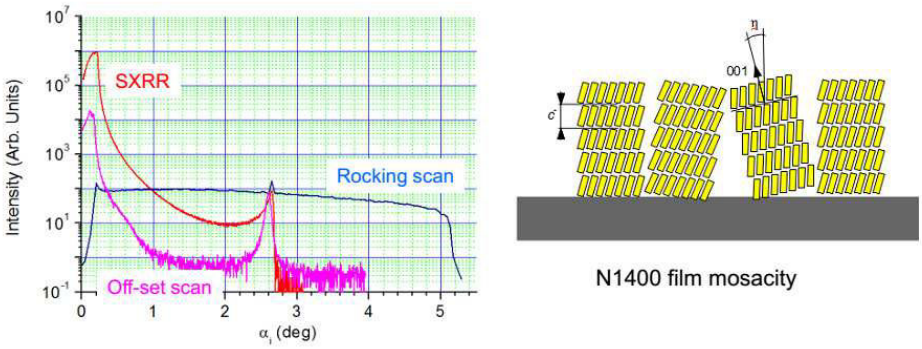


Figure 4.15: X-ray specular reflectivities on the left and relative vertical crystal coherent size and N1400 layer thickness plotted as a function of the Al deposition rate, on the right.

From regions B and C, it is possible to determine the thicknesses of N1400 layer and the vertical coherent size of N1400 cristallites or grains. Figure 4.15 b) shows relative vertical crystal coherent size, i.e ratio between the vertical coherent size of N1400 grains and N1400 film thickness, as a function of the Al deposition rate. Additionally, N1400 film thickness of these samples is plotted in the same graph. The relative vertical crystal coherent size amounts to

approximately 80 % of the total layer thickness with a variation of only 5 %: this means that it is independent both on Al growth rate and film thickness within the parameter determination error.
X-ray reflectivity off-set scans are shown in Figure 4.16. The well pronounced peak in the region between 0.6 and 1.1 nm^{-1} in the scan measured on the sample with Al growth rate of 5 Å/s evidences for a small polydispersity of Al clusters' heights for this sample, i.e. for better defined clusters compared to other samples. From the positions of the minima of the peaks, the height of the clusters can be estimated to be 14±2 nm.

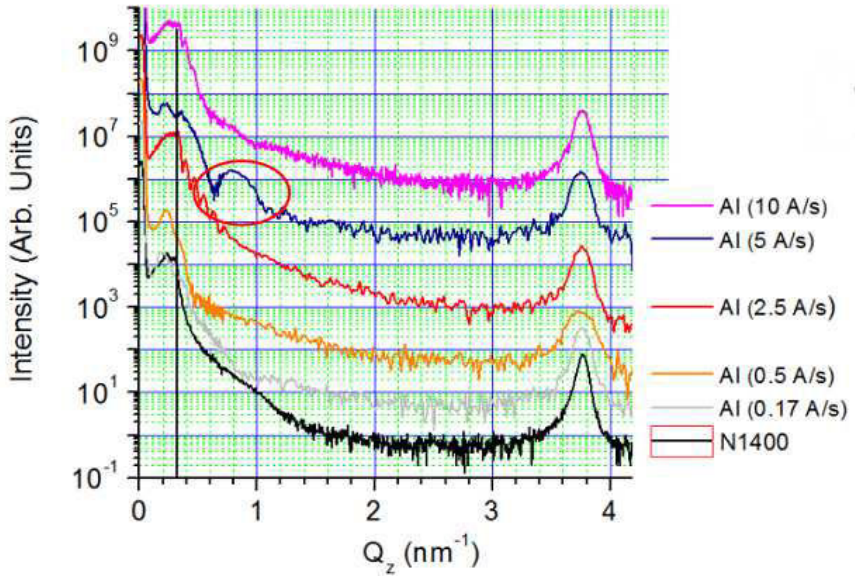


Figure 4.16: Off-set X-ray reflectivity scans. The Al growth rate is indicated in the legend for samples with Al clusters.

GISAXS analysis were also performed on bare N1400 thin film and on samples with Al clusters atop N1400. For all samples with Al evaporated atop N1400, GISAXS provided a clear indication of Al cluster formation. The presence of the Al clusters is indicated by a broad diffuse scattering shoulder along Q axis, which is missing for samples without Al, as shown in Figure 4.17. All GISAXS images for samples with an Al layer show two side rods of enhanced intensity parallel to the Q axis (i.e. the direction perpendicular to the sample surface). The position of the rods is inversely proportional to the average distance between the Al clusters. Horizontal section through the GISAXS images for all measured samples are shown in Figure 4.18. The position of the rods (i.e. peaks in Figure

4.18) is constant for Al clusters grown using deposition rates 0.17 – 10 Å/s and corresponds to cluster distance of 78±3 nm. For Al clusters grown at rate 25 Å/s, the average cluster distance increases to 109±5 nm.

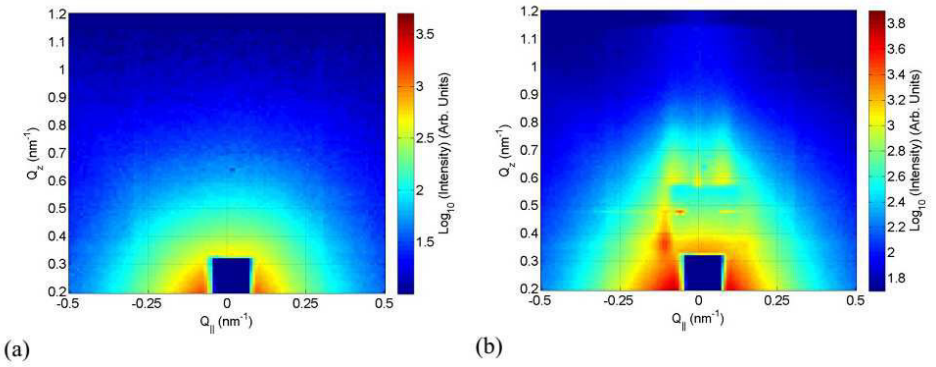


Figure 4.17: GISAXS images taken on: a) bare N1400 and (b) Al clusters atop N1400.

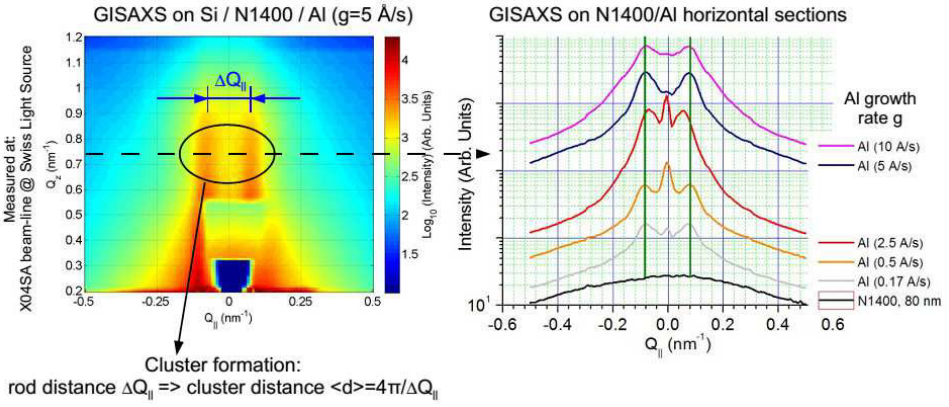


Figure 4.18: On the left, GISAXS image taken on a sample with Al clusters atop N1400 with evidence of cluster distance. On the right, horizontal sections through the GISAXS images. The green vertical lines through the correlation peaks serve as a guide for an eye.

The presence of the Al clusters is also visible in complementary AFM measurements. Representative AFM images of 4 different samples are shown in Figure 4.19.

The surface root mean square roughnesses averaged over images taken at several different positions on the samples are indicated in Table 4.1.

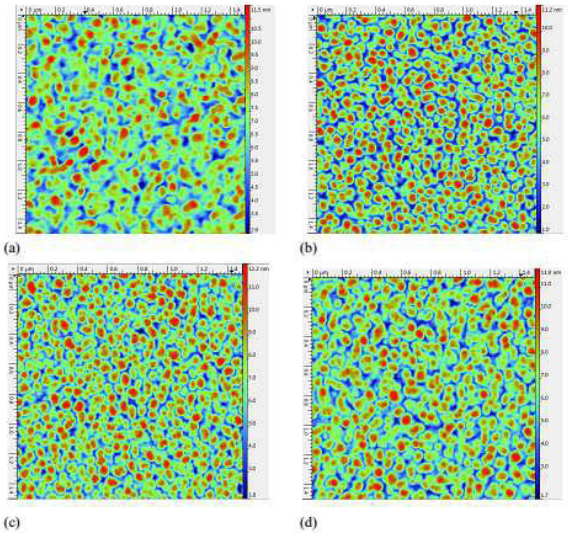


Figure 4.19: AFM images of: a) bare N1400, and samples with Al clusters atop N1400 (different Al growth rate of b) 0.17 , c) 5 , and d) 2.5 Å/s).

Sample	**Al growth rate** [Å/s]	**Al thickness** [nm]	**N1400 thickness** [nm]	**Surface roughness** [nm]
1	-	-	40	1.4
2	-	-	80	3.9
3	0.17	15	40	1.9
4	0.5	15	40	1.2
5	2.5	15	40	1.7
6	5	15	40	1.9
7	10	15	40	2.8

Table 4.1: Nominal growth parameters of the studied samples and their structural parameters as obtained from specular X-ray scans and AFM images.

The surface roughnesses and layer thickness of N1400 (as obtained from X-ray analysis) for samples samples with the Al clusters, are plotted as a function of the growth rate of the Al layer in `Figure 4.20 a)`. From the graph, it is not possible to state any correlation between the surface roughness of these samples and the Al growth rate. On the other hand, the surface roughness is strongly correlated with the organic layer thickness. The fact is underlined in `Figure 4.20 b)` where the mutual dependence of the latter two quantities is plotted together with error bars. From AFM, it is possible to quantify average size and nearest neighbor distance of the clusters to be 50 nm and 90 nm, respectively. Moreover, average lateral size is independent on the Al deposition rate within the measurement

precisions. The lateral correlation length, determined from fitting of height-height correlations functions of AFM images, is 20±2 nm for all samples with Al clusters. It is larger for samples with bare N1400 layers. There is no dependence of the cluster size on the growth rates in range 0.17 to 10 Å/s. It seems that lateral size and distance of the Al clusters is mainly determined by the morphology of the underlaying N1400 layer. A possible scenario is represented by a morphology-driven NPs distribution: the roughness of N1400 determines the coalescence of the metal nanoparticles into its surface valleys, as shown in Figure 4.21.

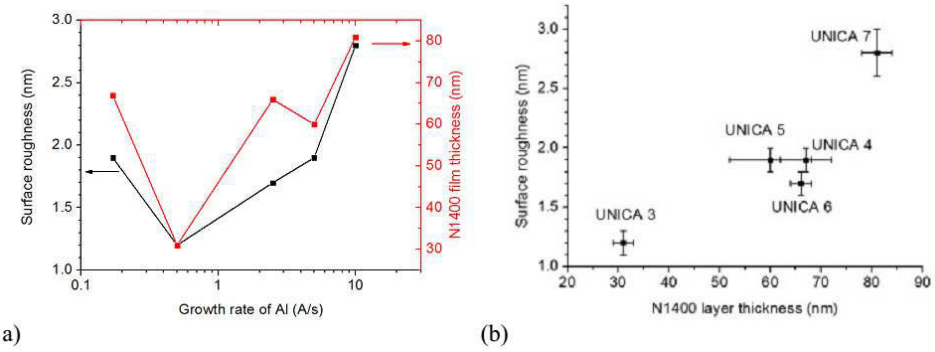


Figure 4.20: a) Surface roughness and N1400 layer thickness plotted as a function of the Al growth rate; b) Surface roughness plotted as a function of the N1400 layer thickness for the same set of the samples with error bars included.

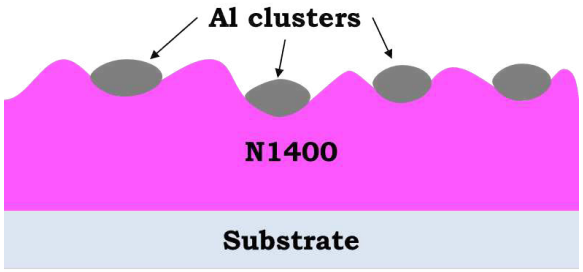


Figure 4.21: Possible scenario of Al clusters templated growth on N1400.

HR-XPS analysis had also provided useful informations on the Al/N1400 samples. In particular, the metal overlayer has been quantitatively characterized in terms of metal amount, oxidation state, and clusters effects.
By fitting the Al_{1S} peak, it was possible to resolve the chemical state

and the atomic percent relative to the Al cluster layer thermally evaporated at different rates. In most samples, the peak associated to the clusters was characterized by one single peak at $\sim$ 75 eV binding energy, consistent with Al_2O_3 oxidized state. This is not surprising since the samples have been exposed to atmosphere for several days before analysis with consequent carbon and oxygen contamination. The contamination layer was etched with 20s Ar etching. Figure 4.22 shows the Al peak for Al/N1400 samples with different Al growth rates (0.17, 5 and 10 Å/s).

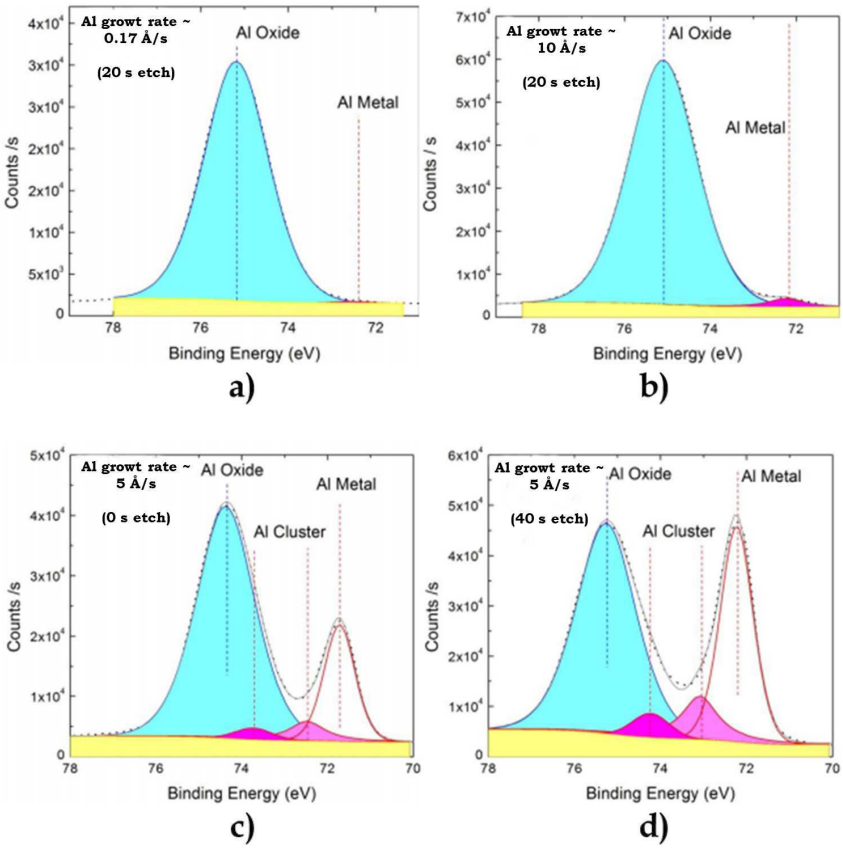


Figure 4.22: HR-XPS of the Al peak in samples with different evaporation rates and same Al nominal thickness (15 nm). Main components are identified in the panels.

Table 4.2 allows comparing the Al content respect to the organic layer and the ratio between the Al in the metal and in the oxide state.

It is clear that the sample with Al growth rate of 5 Å/s is the only one for which the Al is present in its metal state and in its oxide state.

Al growth rate [Å/s]	Etch level [s]	C [at%]	O [at%]	N [at%]	Al(metal) [at%]	Al (cluster) [at%]	Al (oxide) [at%]
0.17	20	36.5	40.5	1.5	< 0.2	/	20.5
0.5	20	77.5	12	6.5	0	/	4
5	0	20	46	0.2	6.5	1.7+0.7	24.5
5	40	2	44.5	< 0.2	16.5	5+2	30
10	0	20	51	< 1	1	/	28
10	20	5.5	55.5	0.2	1	/	37.5
25	20	25	48.5	1	< 0.2	/	25

Table 4.2: XPS at% results. Note that Oxygen at% is the sum of all contributions coming from the Al_2O_3 and the organic layer. Carbon contamination is evident in un-etched samples (0 s scan).

This means that the Al amount and the clusters size are higher than in the other samples. The Al and Al_2O_2 at% are consistent with the presence of metallic clusters embedded in an Al oxide shell. The higher evaporation rate (from 10 to 25 Å/s) seems to have led to relatively smaller and/or more isolated clusters, which have been almost fully oxidized. The lower sticking coefficient associated with the slower evaporation rate (0.17-2.5 Å/s) has led to a lower Al coverage, i.e. to smaller Al layer/clusters which are fully in the oxide state. Hence, it is possible to conclude that the sticking coefficient on N1400 organic layer is strongly dependent from the Al evaporation rate and should follow in first approximation the behavior shown in Figure 4.23, where the Al at% is plotted versus the Al evaporation rate. Since not only the maximum adhesion on N1400 layer, but also the least cluster polydispersity in the vertical direction were found to occur for an Al evaporation rate around 5 Å/s, this should be the best Al growth rate to be used for memory element fabrication.

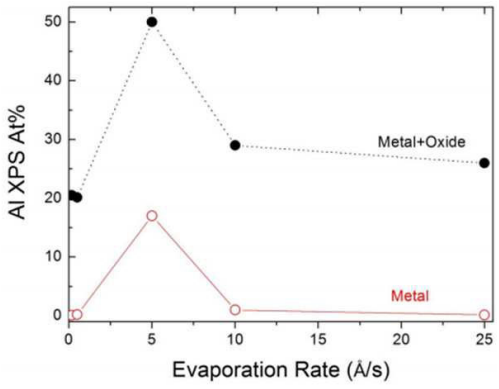


Figure 4.23: XPS at% of the Al peak in hybrid samples with different Al evaporation rates and same Al nominal thickness (15nm).

4.5.3 Au NPs characterization

Gold NPs colloid was characterized by different techniques such as: Dynamic Light Scattering (DLS), Atomic Force Microscopy (AFM), Transmission Electron Microscopy (TEM) and Small Angle X-ray Scatterinng (SAXS) in order to confirm the size and size distribution of nanoparticles. DLS and AFM analysis were perfomed at the University of Lodz. The statistic graph of Au NPs size resulted from DLS is depicted in Figure 4.24. The size distribution of obtained nanoparticles was calculated basing on scattered light intensity measurements. From the graph, it can be concluded that the size of gold nanoparticles is 15 $\pm$ 6 nm. In particular, the colloid is monodispersed, with a polydispersity index of 0.210.

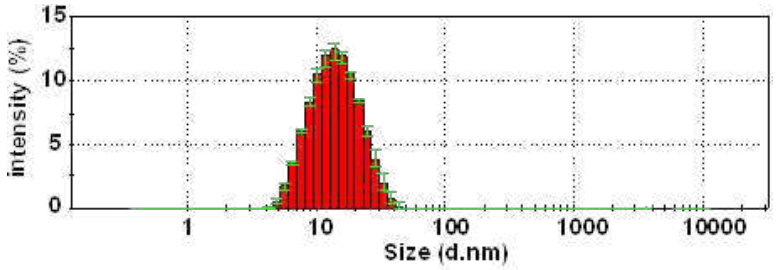


Figure 4.24: DLS size distribution histograms of Au NPs.

The AFM investigation show that the average value of nanoparticles diameter calculated for more than 100 particles is 9.5 $\pm$ 1.1 nm. (Figure 4.25). The AFM technique require deposition of gold nanoparticles on a substrate. Negatively charged Au NPs were electrostatically bonded to a chemically modified Si wafer. For the modification 3-aminopropyldimethylethoxysilane (APDMS) was used.

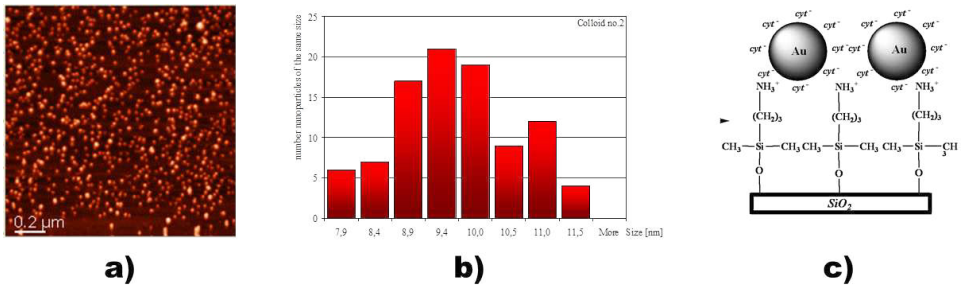


Figure 4.25: a) AFM image of Au NPs; b) histogram of the size distribution; c) scheme of Au NPs deposition on the substrate.

The size and shape of Au NPs were investigated using TEM technique at the University of Strasbourg. Au NPs resulted to be spherical with a mean particle size of 8.8 ± 1.7 nm. Figure 4.26 reports TEM image and the NPs size distribution histogram.

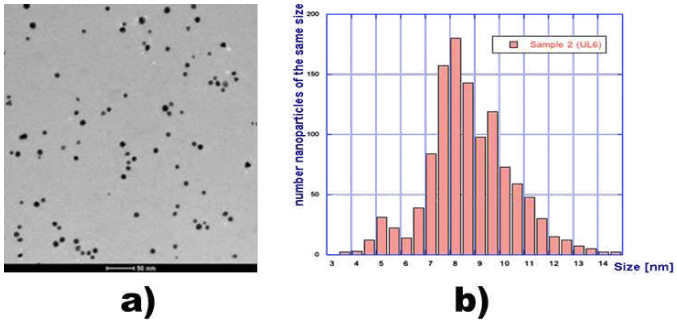


Figure 4.26: a) TEM image of Au NPs; b) histogram of the size distribution.

Finally, Au NPs were also characterized by SAXS technique performed at University of Tubingen. The average size and the standard deviation of Au NP are shown in Figure 4.27. The average size of Au NPs is about (8 ± 0.5) nm with a standard deviation diameter of (1.6 ± 0.2) nm.

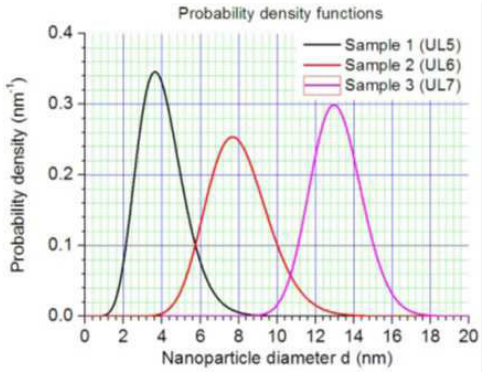


Figure 4.27: SAXS image of AuNPs Colloids.

All results obtained for Au NPs colloid are summarized in Table 4.3. The average value of Au NPs resulted to be (8.8 ± 0.8) nm. It was calculated using results obtained from AFM, TEM and SAXS techniques. Results obtained from DLS differ from the other, because in this technique hydrodynamic diameter of nanoparticles is measured in the colloidal solution.

DLS [nm]	AFM [nm]	TEM [nm]	SAXS [nm]	Average value [nm]
15±3	9.5±1.1	8.8±1.7	8.0±0.5	8.8±0.8

Table 4.3: Average sizes of AuNPs calculated with different techniques.

To conclude the morphological investigation, AFM was also perfomed on Au NPs atop N1400 layer. The results were compared with bare N1400 and Al NPs atop N1400 AFM results. Figure 4.28 shows (a) bare N1400, (b) Al NPs and (c) Au NPs on N1400 surfaces. For the bare N1400 surface, a root mean square surface roughness (RMSR) of about 1.4 ± 0.2 nm was found, while RMSR = 1.9 ± 0.2 nm and RMSR = 2.3 ± 0.2 nm for Au NPs and Al NPs, respectively. It is clearly evident that the surface roughness of the N1400 is not substantially varied after the deposition of both kinds of metal NPs. This leads to the conclusion that the morphology of the nanocomposite hybrid film is dominated by the one of the underlying organic semiconductor. Moreover, it is possible to observe that Au NPs and Al NPs on N1400 surface seem to be very similar in size, even if they were deposited with different techniques and the Au NPs had a very small average size before deposition by electrospraying. This confirms that the final morphology of the nanoparticles film is likely driven by the characteristics of the N1400 film.

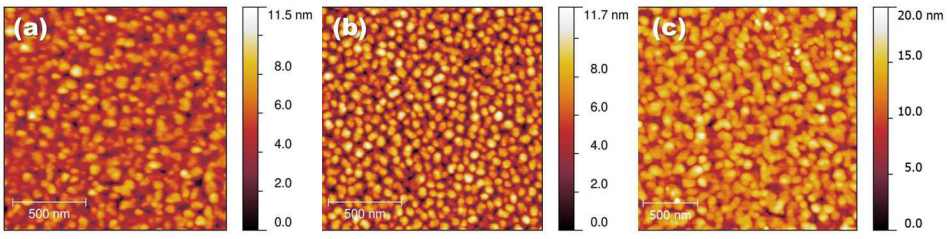


Figure 4.28: AFM images: (a) N1400 surface; (b) evaporated Al NPs on N1400 surface and (c) electrosprayed Au NPs on N1400 surface.

4.6 Electrical characterization

Different structures of memory elements have been fabricated and electrically characterized. In particular, some attempts with different nominal gold nanoparticles coverages were explored by varying the electrospraying deposition time. In the case of Al NPs interlayer,

as a consequence of the morphological characterizations, memory elements with a fixed deposition rate (5 Å/s) and nominal thickness (15 nm) were fabricated and characterized. Different thicknesses of the organic layer were also explored. Two metal, gold and silver, were tested as top electrodes. Finally, structures without the metal nanoparticle interlayer were fabricated along with hybrid RRAMs. This choice can be justified by the needing of a valuable reference for finally demonstrating the metal NPs role in device performances and reliability. In the following, a complete electrical characterization will be provided.

4.6.1 Typical measurement procedure

Electrical measurements were performed in nitrogen atmosphere or in ambient conditions (temperature of about 22 °, humidity in the order of 50%) with an HP – Agilent 4155A Semiconductor Parameter Analyzer, a Keithley 2636 or a Agilent B1500A Semiconductor Parameter Analyzer. Each memory element was contacted with tungsten tips.
Generally, the memory devices did not require electrical preconditioning in order to achieve bi-stability. A typical measurement procedure is described in the following.

- **I-V characteristic**: I-V curves are obtained by sweeping from a negative to a positive voltage, and back. This allows determining the writing and erasing voltages, i.e. the threshold voltages that cause the device switching from its high resistance state (HRS, OFF state) to its low resistance state (LRS, ON state) and from the LRS to the HRS, respectively. The initial state of the memory device can be a LRS state or a HRS. When the initial state is a LRS and the applied bias exceeds a threshold value V_{OFF}, the resistance of the device increases abruptly by several orders of magnitude. During the reverse voltage sweep, an abrupt current increase occurs at a critical voltage V_{ON} and the device switches from the HRS back to the LRS.

- **Writing**: when the device is in the OFF state, it yields a low current; a voltage pulse $V_{SET} < V_{ON}$ can be applied to induce the switching from the HRS to the LRS, i.e. to set the ON state. This OFF-to-ON transition represents the *writing process*. Once the device is in its ON state, it remains there, even after the power is turned off (*non-volatile memory* behavior).

- **Erasing**: the device can be switched OFF from the LRS back to the HRS by applying a voltage pulse $V_{RESET} > V_{OFF}$. This

ON-to-OFF transition represents the *erasing process*.

- **Reading**: the voltage range between V_{ON} and V_{OFF} is the region of bi-stability: the state of the device can be read by applying a voltage V_{READ} within this range, but significantly far from its limits.

- **ON/OFF current ratio**: I_{ON}/I_{OFF} is the ratio between the current through the device in the ON state and the current in its OFF state at the same reading voltage V_{READ}. A large separation between the two resistance states is essential in order to achieve a large noise margins, so that the ON and OFF states could be clearly distinguishable for readout electronics.

- **Retention time test**: data retention time is the period of time the memory can retain data. After switching the devices to the LRS or HRS, they were kept in ambient conditions and their state was periodically probed. In particular, reading tests during the lifetime of the devices were performed and the state of the memories was recorded from time to time.

- **Endurance/stress tests**: voltage stress tests were performed by applying to the device a continuous readout voltage for a relatively long time (much longer than the one generally required for reading the memory in normal applications) in both ON and OFF states. From these tests, it is possible to check the capability of the memory device to retain its ON/OFF state during a continuous constant bias.

- **Endurance/cycling tests**: writing/erasing cycling tests were performed in order to test the devices operational lifetime and their capability to continuously perform programming/erasing cycling.

4.6.2 Structures without NPs

Several tests were carried out on devices without metal NPs interlayer, in order to understand its role in the resistive switching of the memory elements. As previously mentioned, different thicknesses of the organic layer were considered, while gold and silver were tested as top electrodes materials. Moreover, fabricated devices were tested both in ambient and in nitrogen atmosphere. A list of the fabricated and characterized structures is reported in Table 4.4.

Firstly, structures with Au top electrodes were tested, since gold is a recommended contact type for N1400. For each structure three sets of devices were fabricated: the devices of the first group

Structure	N1400 thickness [nm]
GLASS/ITO/N1400/Au	160
GLASS/ITO/N1400/Au	240
GLASS/ITO/N1400/Ag	100
GLASS/ITO/N1400/Ag	240

Table 4.4: Fabricated and tested structures without NPs.

were measured in a nitrogen atmosphere, the devices of the second set were measured in ambient conditions, while the elements of the third were measured both in a nitrogen atmosphere and in air. In all the cases, no switching behaviour was observed. As an example, representative I-V characteristics of devices measured both in air and in inhert atmosphere are reported in Figure 4.29. In particular, Figure 4.29 a) e b) shows the I-V characteristics of a 160 nm-thick N1400 device measured in air and in nitrogen atmosphere, respectively; any difference can be noticed in the curves. Similarly, Figure 4.29 c) and d) depicts I-V curves for a 240 nm-thick N1400 device measured in air and in nitrogen atmosphere, respectively. Independently of the measurement environment, and the N1400 thickness, diode-like curves have been obtained.

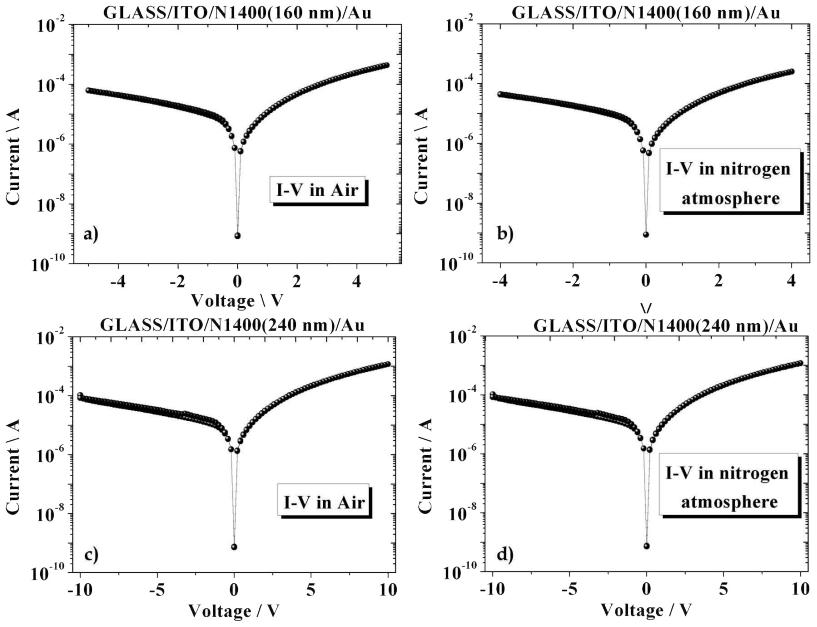


Figure 4.29: Rapresentative I-V characteristics for the structure GLASS /ITO/N1400/AU with different N1400 thicknesses (160 and 240 nm) measured in air or in nitroger atmosphere.

Thereafter, structures with Ag top electrodes were fabricated and characterized. Just as previously reported for the devices with gold top electrodes, two different N1400 thickesses were employed, and characterization was performed i) only in ambient or ii) inhert atmosphere, or iii) in both the conditions. The results turned out to be indipendent of the measurement environment and the N1400 thickness. Indeed, in all the cases 50% of the devices have never shown switching behavior (as for example reported in Figure 4.30 a) and c)), even if repeatedly stressed (many hours of continuous cycling). In the remaining 50% (Figure 4.30 b) and d)), switching events occurred occasionally, but in a non-reproducible way. In particular, the threshold voltages are not always the same: sometimes the devices switch ON (or OFF) at a positive voltage, sometimes at a negative voltage. In addition, once switched, devices could never be restored in their original state. Moreover, it resulted that thicker N1400 layers seem to need a higher switching voltage, as it can be also observed from 4.30 b) and d).

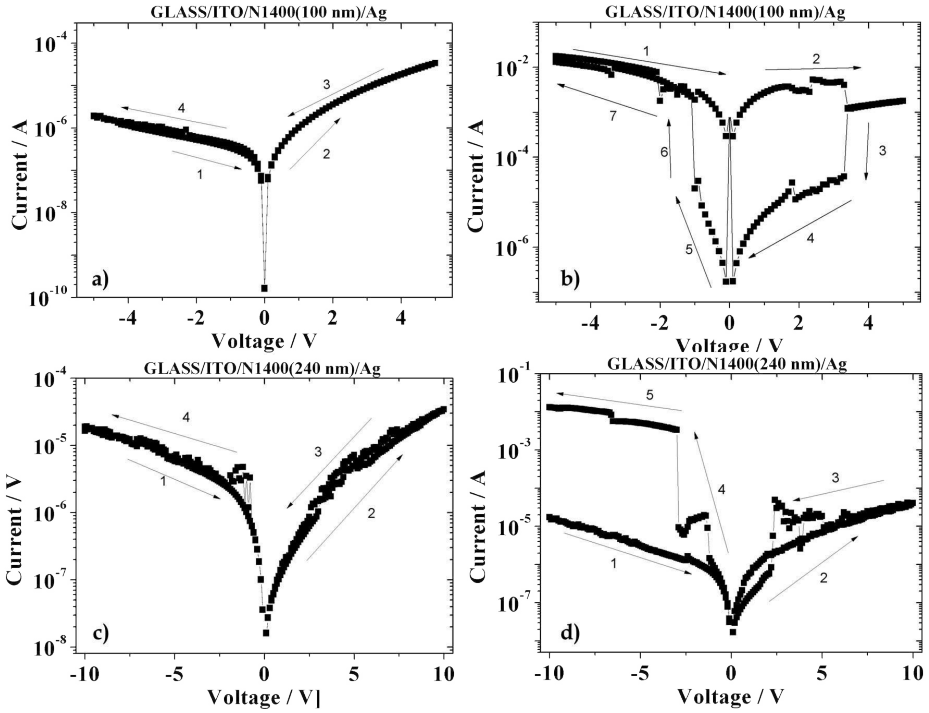


Figure 4.30: Representative I-V characteristics for the structure GLASS /ITO/N1400/Ag with different N1400 thicknesses (100 or 240 nm) measured in air or in nitroger atmosphere: a) and c) I-V characteristic of devices which have never showed switching behavior; b) and d) I-V characteristic of devices with unreliable switching behavior.

To summarize, switching events were observed with the structures GLASS/ITO/N1400/Ag, both in nitrogen atmosphere and in ambient conditions, and for different N1400 thicknesses. This evidence suggests that silver is a better candidate than gold for the final fabrication of memory devices. However, the very low predictability and reproducibility of of switching events do not promote the use of bare N1400 as resistive layer for the fabrication of reliable memory elements.

4.6.3 Structures with Al NPs

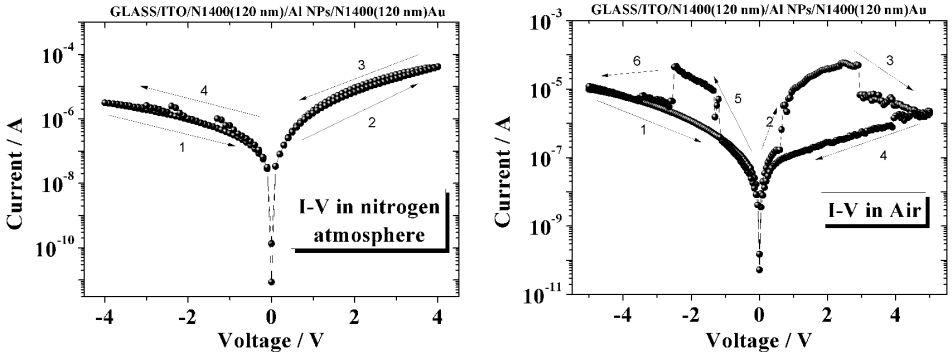
In this section, the electrical characterization of devices hosting an Al NPs interlayer is provided. In particular, as well explained in the morphological analysis, the nominal thickness of the Al interlayer is 15 nm, deposited at a rate of 5 Å/s. As for devices without NPs, gold and silver were tested as top electrodes materials and measurements were performed both in air and in nitrogen atmosphere. Moreover, two different thicknesses of the N1400 matrix were investigated. Table 4.5 reports a list of the fabricated and characterized devices.

Structure	Total N1400 thickness [nm]
GLASS/ITO/N1400(80 nm)/Al NPs/N1400(80 nm)/Au	160
GLASS/ITO/N1400(120 nm)/Al NPs/N1400(120 nm)/Au	240
GLASS/ITO/N1400(50 nm)/Al NPs/N1400(50 nm)/Ag	100
GLASS/ITO/N1400(120 nm)/Al NPs/N1400(120 nm)/Ag	240

Table 4.5: Fabricated and tested structures with Al NPs.

At first, devices with Au top electrodes were studied. For all these elements no switching behaviour was observed when measurements were perfomed in nitrogen atmosphere (Figure 4.31 a)). On the contrary, switching behavior was observed when the devices were measured in ambient conditions, as shown, for example, in Figure 4.31 b) for a device with a 240-nm-thick N1400 matrix.

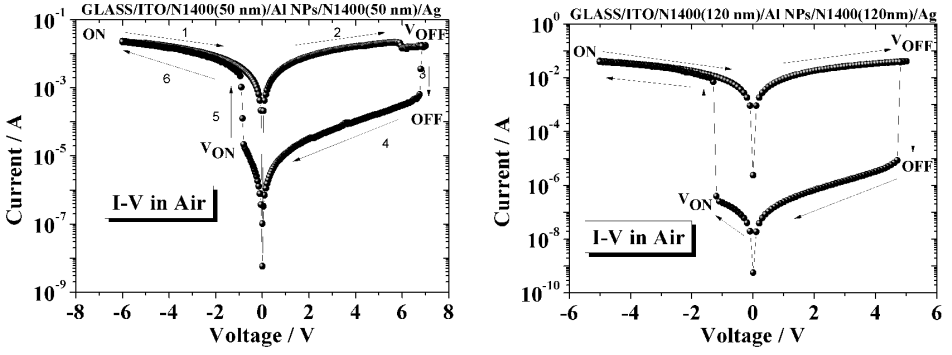
From these results, it turned out that the presence of metal NPs seems to play a role in conditioning the switching behaviour of the devices, indipendently of the N1400 layer thickness. Nevertheless, it is noteworthy that the change in conductivity resulted very small and not reproducible. Moreover, the switching behaviour was completely lost after a few cycles. Consequently, since better results were obtained with the Ag top electrode for devices without NPs, in the next step GLASS/ITO/N1400/Al NPs/N1400/Ag structures were thoroughly investigated. In particular, two different thicknesses of



(a) (b)

Figure 4.31: Representative I-V curves for a device with the structure GLASS/ITO/N1400/Al NPs/N1400/Au measured in nitrogen atmosphere (a) or in air (b).

the organic layer were studied: 100 nm and 240 nm. In both cases no switching behaviour was observed when devices were measured in nitrogen atmosphere. Therefore, in the following only characterization in ambient condition will be considered. An I–V characteristic of a device with a 100-nm-thick N1400 matrix is shown in `Figure 4.32 a)`. In this example, initially, the memory is in its LRS. At the threshold voltage V_{OFF} = 6.5 V the current drops abruptly by two orders of magnitude, and the memory switchs OFF to its HRS.



(a) (b)

Figure 4.32: Representative I-V curves for device with the structure GLASS/ITO/N1400/Al NPs/N1400/Ag measured in air: a) 100-nm thick N1400 matrix, b) 240-nm thick N1400 matrix.

During the reverse voltage sweep, the device switches back to the LRS at a threshold voltage V_{ON} = – 1 V. Only 25% of the tested devices showed a resistive switching. Moreover, the I_{ON}/I_{OFF} current

ratio is not sufficiently high to make the ON and OFF states clearly distinguishable, because of a quite high OFF current. Better results were obtained with the 240-nm-thick N1400 matrix. In this case, 80% of tested device showed a reproducible switching behaviour. Figure 4.32 b) shows a typical I–V characteristic for this group of elements. The behavior is always the same: the initial state of the exemplifying memory element is the LRS; it turns OFF at V_{OFF} =4.7 V; finally, at V_{ON} = – 1.3 V, the memory switchs from the HRS back to the LRS. Average values of V_{ON} and V_{OFF} are (-1.4±0.4) V and (5.0 ±1.0) V, respectively. The ratio between the currents recorded in the two states (I_{ON}/I_{OFF}), at the same reading voltage V_{READ} = 0.2 V, is typically 10^4, which allows to have well-separate ON and OFF states. Statistic data for writing voltage, erasing voltage and I_{ON}/I_{OFF} are reported in Figure 4.33.

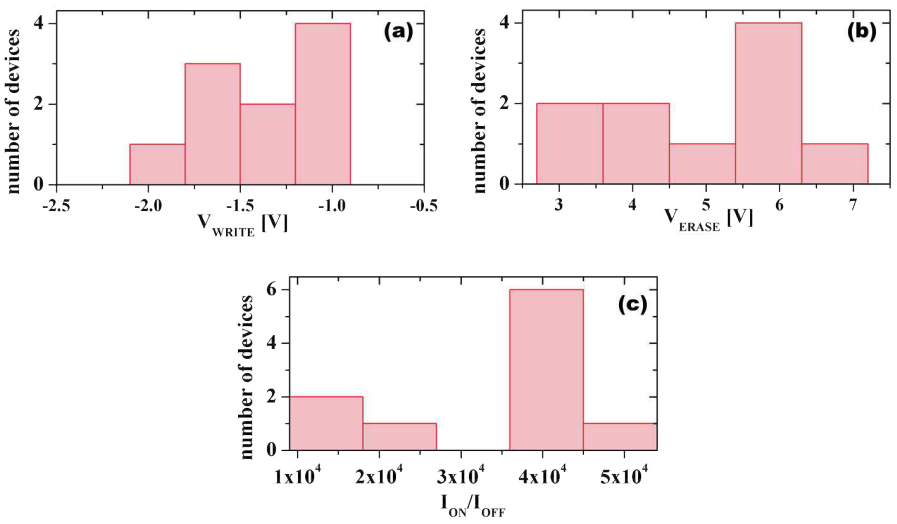


Figure 4.33: Histograms showing: Al NPs-based memories statistics for (a) writing voltage, (b) erasing voltage, (c) current ratio.

In order to complete the investigation of the memory performance, endurance and retention time tests were carried out. Figure 4.34 a) shows representative data from the endurance tests. Voltage stress tests were performed by applying to the devices a continuous readout voltage of 0.2 V for about 10^3 s in both ON and OFF states. It is noteworthy that a steady current level is perfectly maintained in both states, thus proving that the device is stable and not affected by bias stress even for a continuous reading time well beyond the one employed in routine applications. The retention time for both ON and OFF states was investigated periodically at a reading voltage of 0.2 V.

The measured retention time for this kind of memories is 4×10^5 s, as it is clearly shown in Figure 4.34 b). Indeed, from this time, the memory starts to deviate from its ON state and the ON/OFF current ratio start to decrease. Moreover, as shown in Figure 4.34 c), the original ON and OFF states were not recovered in tests carried out after several months. It is clearly noticeable that writing and erasing processes performed after six months could not retrieve the original ON and OFF states of the memory, proving that this kind of device lose their full functionality after several months.

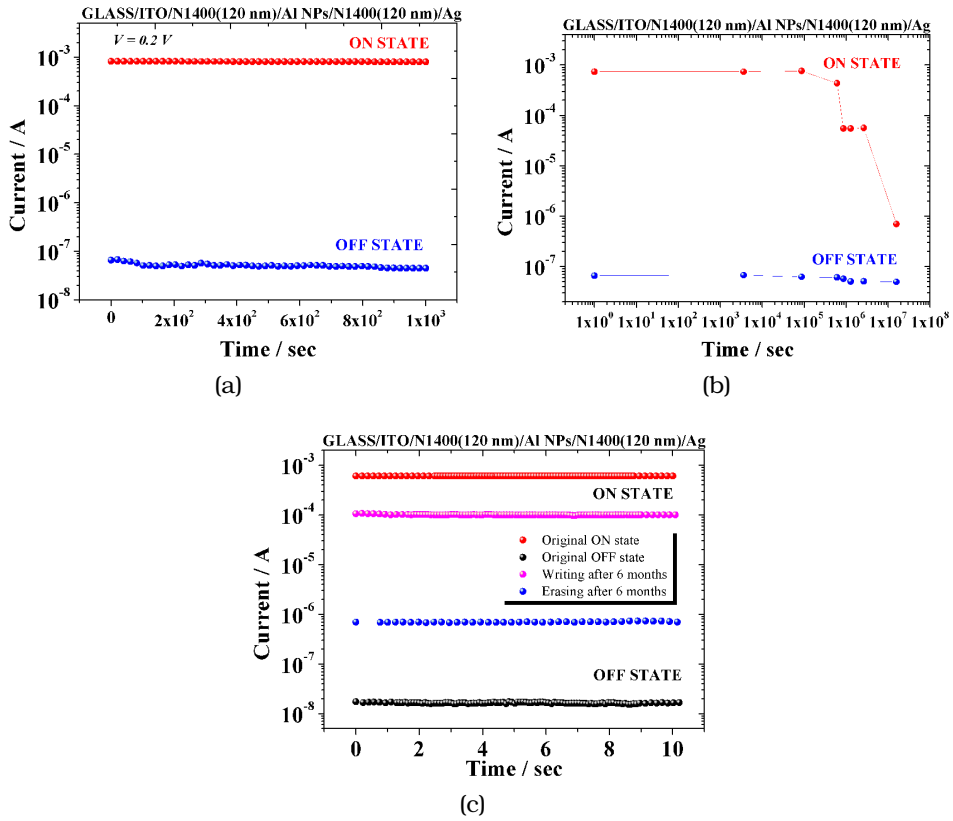


Figure 4.34: Representative a) endurance and b) retention time tests performed in air for Al NPs based memories; c) Writing and erasing tests performed on Al NPs based memories within 6 months.

4.6.4 Structures with Au NPs

The electrical characterization of memory devices hosting gold NPs will be provided in the following. In particular, two structures with different nominal NPs coverage were tested. Indeed, the coverage of the organic layer with NPs can be tuned by playing on different

parameters of the electrospraying system: flow rate, deposition time, acceleration voltage. Moreover, the final composition and morphology of the hybrid film may also depend on the distance between the sprayer nozzle and the substrate, the concentration of nanoparticles in the colloidal solution or the solvent used. In this study, the deposition time was varied to tune the NPs density of the interlayer. In particular, 2-hour and 4-hour depositions were explored. Both structures were measured first in nitrogen atmosphere and then in ambient conditions. As for the structures analysed in the previous sections, both gold and silver top electrode were employed. The N1400 matrix thickness was kept costant at 240 nm-thick, since better results were previously obtained with such thickness.
First tests were carried out using gold top electrode. For all these elements, indipendently of NPs coverage, no switching behaviour was observed when measurements were perfomed in nitrogen atmosphere (Figure 4.35 a)), as obtained for Al-NPs-based devices. Resistive switching was observed only when the devices were measured in ambient conditions, as shown, for example, in Figure 4.35 b) for a device with a 4 hours Au NPs coverage. No significant differences were observed between devices with 2 or 4 hours Au NPs coverage. However, only 10% of tested devices showed a switching behaviour, which also resulted not reproducible.

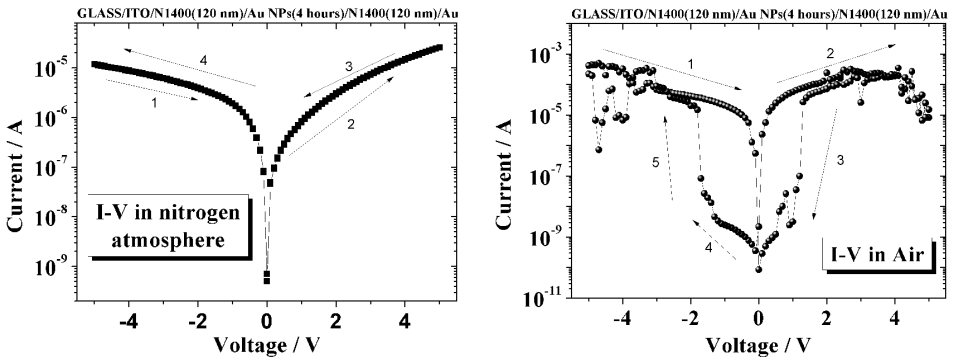


Figure 4.35: Representative I-V curves for a device with the structure GLASS/ITO/N1400/Au NPs/N1400/Au measured in nitrogen atmosphere (a) or in air (b).

Therefore, as previously, structures with Ag top electrodes were thoroughly investigated. Also in this case, no switching behaviour was observed for both Au NPs covereges when devices were measured in nitrogen atmosphere. Therefore, in the following only characterization in air will be considered. Figure 4.36 a) and b)

shows representative I-V characteristics for a GLASS/ITO/N1400/Au NPs/N1400/Ag structure with 2 and 4 hours deposition of Au NPs, respectively.

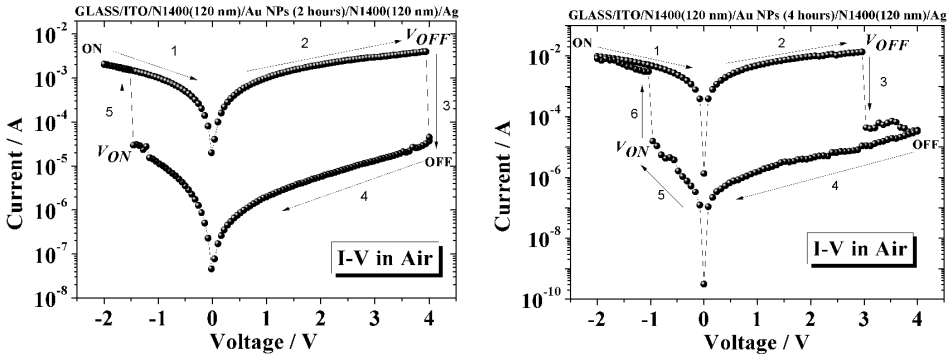


Figure 4.36: Representative I-V curves for a device with the structure GLASS/ITO/N1400/Au NPs/N1400/Au measured in air: a) 2 and b) 4 hours deposition of Au NPs.

Interestingly, no significant differences can be noticed between the two kind of structures. In both the examples, initially the memory is in its LRS (ON state). When the applied bias exceeds a threshold voltage V_{OFF}, the current of the device decreases abruptly by several orders of magnitude, and the memory switches OFF to its HRS. During the reverse voltage sweep, an abrupt current increase occurs at a threshold voltage V_{ON} and the device switches from the HRS back to the LRS. Average values of V_{ON} and V_{OFF} are (-1.6±0.4) V and (3.1±0.6) V, respectively. It is notewothy that all devices showed a resistive switching. The ON/OFF current ratio, at the same reading voltage V_{READ} = 0.2 V, is typically 10^3. Statistic data for writing voltage, erasing voltage and I_{ON}/I_{OFF} ratio are reported in `Figure 4.37`.

The investigation on the memory performances was completed with endurance and retention time test. In order to evaluate the stability of the memory elements in air, the devices have been measured and stored in ambient conditions during the whole period of investigation. `Figure 4.38 a)` shows representative data from the endurance tests, performed by applying to the device a continuous voltage V_{READ} = 0.2 V for a period of 10^3 s in both ON and OFF states. It is clearly evident that also for the devices with Au NPs a steady current level is perfectly maintained in both states. This proves that the memories are stable and not affected by bias stress even for a continuous reading time. The most interesting result achieved with

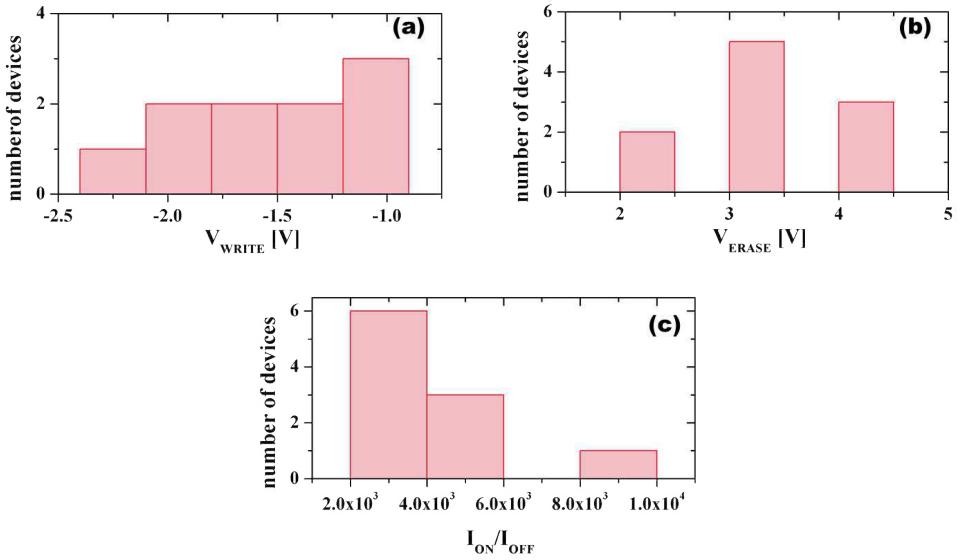


Figure 4.37: Histograms showing: Au NPs based memories statistics for (a) writing voltage, (b) erasing voltage, (c) current ratio.

this structure is surely related to retention time and lifetime. The retention time for both ON and OFF states was investigated periodically at V_{READ} = 0.2 V. As shown in Figure 4.38 b), the memory was able to retain the stored data for $\backsim 1.5 \times 10^7$ s ($\backsim$ 6 months), which is a record result for organic RRAMs measured and stored in air. In addition, at this time, the originally programmed devices were erased and re-written resulting in OFF and ON states that are exactly the same as the initial ones (Figure 4.38 c)). Furthermore, reading performed after another ten months (thus on devices belonging to a batch fabricated 16 months before the last retention test) allowed recording a new record value of retention time of $\backsim 2.6 \times 10^7$s; consequently, a lifetime of at least 16 months was also evaluated, which is, to our knowledge, the longer lifetime ever reported in literature. Figure 4.38 b) clearly demonstrates the stability of the ON/OFF ratio during this period of time. Finally, in order to test the operational lifetime, writing/erasing cycles were performed on Au NPs based devices after 16 months from the fabrication. Figure 4.38 d)) shows and demonstrates that such devices are able to reach, at this time, at least 500 cycles.

4.6.5 Summary of electrical performances

The electrical results reported in the previous paragraphs allow drawing important conclusions. First of all, the choice of the metal

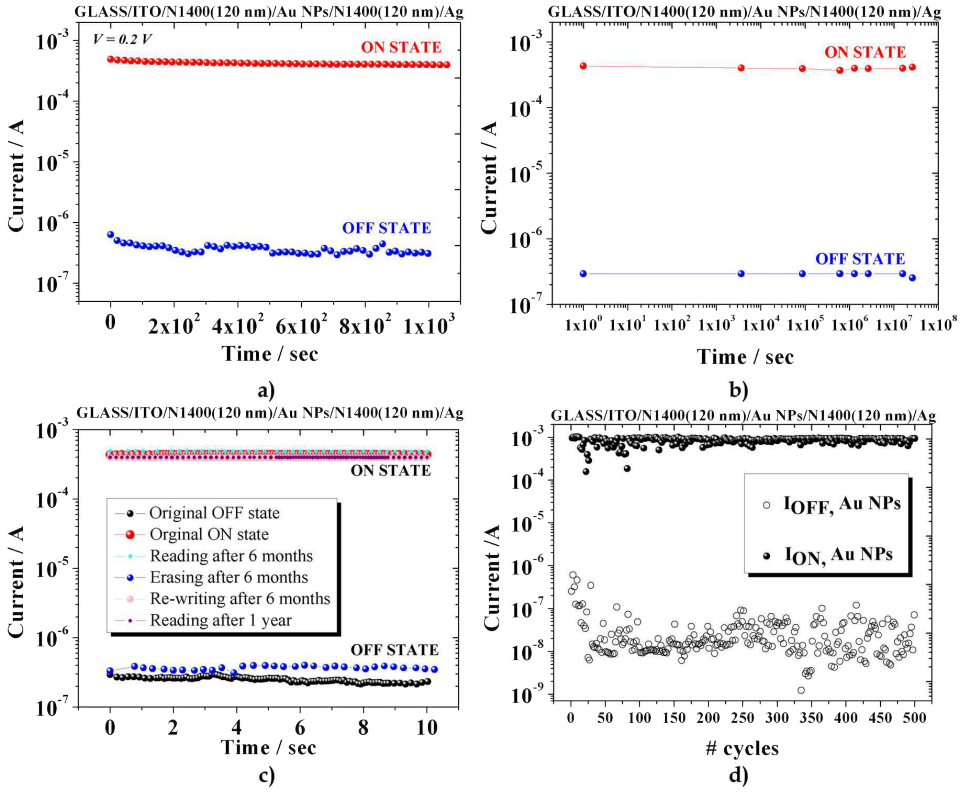
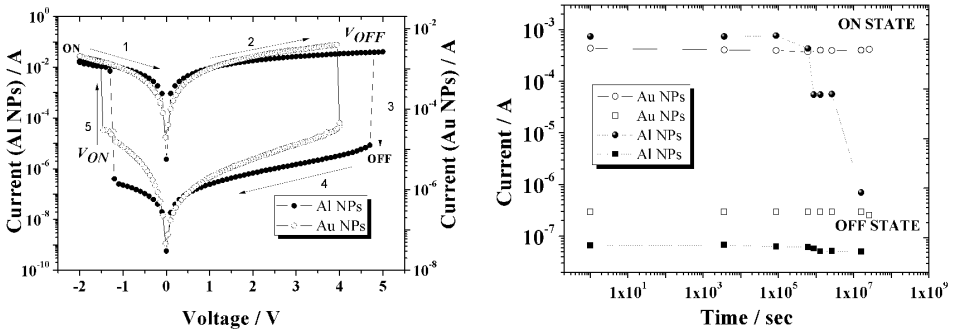


Figure 4.38: Representative a) endurance and b) retention time tests performed in air for Au NPs based memories; c) Writing and erasing tests performed on Au NPs based memories within 1 year; c) cycling test performed after 16 months on Au NPs based devices.

for the top electrode seems to significanty affect the final functionality of the memories. In particular, electrical results suggest that silver is better than gold for the final fabrication of memory devices. Moreover, the presence of a metal NPs interlayer turned out to be essential in order to have a reliable and reproducible resistive switching. Interestingly, devices with a metal NPs interlayer showed switching effect only when measeured in ambient condition: this is an indication that oxygen could play a role in promoting the switching mechanism. Finally, the performances of the memory device are strictly related to the choice of the metal for the nanoparticle interlayer. `Figure 4.39` shows a comparison between performances of the two kind of memories. In particular, `Figure 4.39 a)` reports typical I-V curves, where the left y-axis is referred to the Al NPs based memories and the right one is referred to the Au NPs based memories. The devices showed very similar operational characteristics and ON/OFF cur-

rent ratio with both types of NPs. However, for devices made with Al NPs, a lower retention time was observed, as shown in Figure 4.39 b). Moreover, as shown in Figure 4.34 c) , the original ON and OFF states were not recovered in tests carried out after several months. The actual reasons behind the degradation of the device performances with Al NPs are still under investigation. Nevertheless, it is possible to hypothesize that the oxidation of Al NPs, induced by the oxygen diffusion within the organic matrix, may play a role in devices performance degradation. In conclusion, the obtained results suggest that environmental stability of both organic and inorganic materials is needed for obtaining reproducible and stable memory effects.



(a) (b)

Figure 4.39: Comparison between memory elements employing Al and Au as metal interlayer: a) Typical I–V curves (the left y-axis is referred to the Al NPs based memories and the right one is referred to the Au NPs based memories); b) retention time test.

4.7 Conduction mechanism investigation

In order to shed light on the switching behavior of the proposed devices, thus understanding their peculiar characteristics such as the needing of a nanoparticles interlayer and silver top electrode for a reproducible switching behavior, a structural characterization was performed with High resolution X-ray Photoelectron Spectroscopy (HR-XPS) and Time of Flight Secondary Ion Mass Spectrometry (ToF-SIMS). Such techniques allow evaluating the material composition of multilayered devices. In this work, they were employed for investigating the possible formation of metallic filaments, which has been recently suggested being the driving mechanism for resistive switching in many organic bi-stable devices. In particular, XPS and ToF-SIMS depth profiles were carried out on pristine and conditioned

(written/erased/re-written several times) memories to quantitatively and spatially characterize the possible metal penetration inside the organic layer. Metal diffusion could occur during the top electrode evaporation and/or could be assisted by electrical field diffusion during the memory testing. The presence of point-like structures at the top electrode/organic interface was proposed to be fundamental for metallic filament growth in organic memories.
Figure 4.40 a) shows a typical XPS depth profile obtained on a pristine memory by alternating cycles of sputtering with argon ion beam and XPS analysis. The Ag_{3d} peak area (in log scale) is shown as a function of the sputtering depth. Interestingly, silver is present through the entire N1400 depth, as the mean atomic percentage over the analysis area of $200 \times 200 \mu m^2$ is still 0.1% close to the bottom electrode (P4). The HR spectra obtained at the corresponding depths are indicated and compared in the inset. The size-dependent binding energy shift of the Ag_{3d} peak (evidenced by the vertical bar in the inset) comes from electrostatic interaction between the leaving photoelectron and the positive charge left on the small supported cluster (typically < 5 nm) surface during the photoemission process [130]. The NPs signal was too weak to be quantified with XPS.

Dual beam ToF-SIMS imaging was performed to increase the sensitivity, and study the spatial distribution of elements with $1 \times 1 \mu m^2$ (in-plane)$\times 1nm$ in depth resolution. Figure 4.40 b) and c) shows respectively the ToF-SIMS depth profiles obtained on a pristine and on a cycled device finally set into the ON state. A higher silver diffusion is evident in the electrically stressed device. The spatial distribution of silver, indium and gold (in red, green and blue color scale respectively) was studied on $120 \times 120 \mu m^2$ maps, showing a clear inhomogeneous Ag diffusion in channel-like structures (filaments) which protracts through the entire N1400 layer till the ITO bottom electrode in electrically stressed devices (see Figure 4.40 e)). The sparse distribution of such filamentary paths suggests that the formation could be driven by defects in the organic layer. Pristine devices (Figure 4.40 d)) showed a weaker silver diffusion extending at most 50 nm under the Ag/N1400 interface, i.e. never determining a continuous electrical path between the electrodes. Field assisted diffusion of silver atoms during I–V scans appears necessary to establish a complete *filament* bridging the two metal electrodes. The presence of few diffusion areas and the fact that no differences were evidenced by the comparison of devices set into the LRS or into the HRS suggest that the same diffusion path could be locally activated and deactivated (ruptured) during the memory cycling, allowing a reproducible switching, as observed in the I–V testing. Weak signals from the metal interlayer were evidenced by

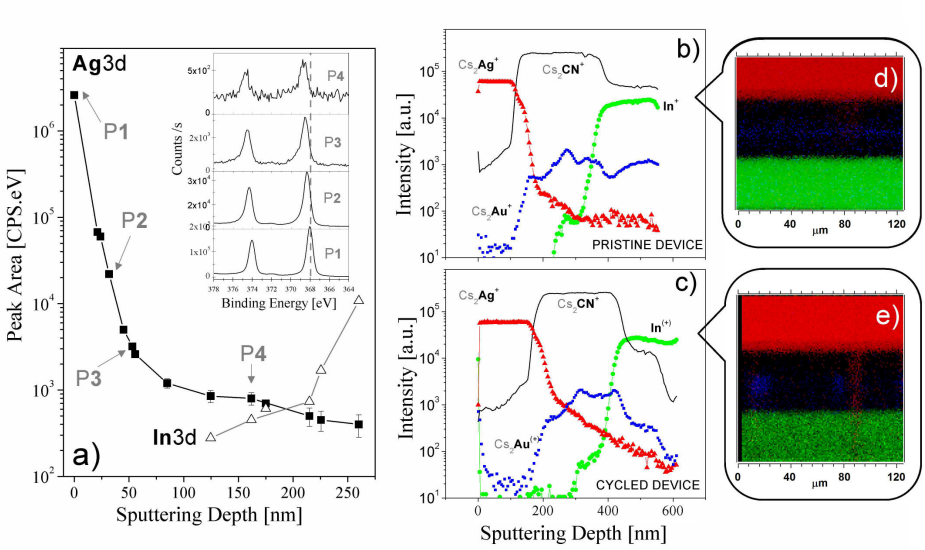


Figure 4.40: a) XPS depth profile of a pristine Ag/(N1400+AuNPs)/ITO memory element showing the Ag_{3d} and In_{3d} peak area as a function of the sputtering depth. The inset shows the vertically stacked HR Ag_{3d} spectra obtained at the corresponding points (depths) indicated in panel a): the spectra have been displayed with the appropriate y-scale to help the comparison. The dashed vertical line is to guide the visualization of the binding energy shifts. b) and c) ToF-SIMS depth profiles obtained on a pristine b) and operated c) device showing the intensity of the signal of silver (red triangles), indium (green dots), a N1400 fragment (grey line) and gold (blue dots) as a function of the sputtering depth. An enhanced Ag diffusion is evident in the operated device. d) and e) Two dimensional (XZ) cross sections extrapolated from the 3D ToF-SIMS images corresponding to b) and c) profiles (same color label) showing an Ag filament in the operated device.

ToF-SIMS analysis. As well-explained in previous sectios, resistive switching in devices without metal NPs resulted considerably less reproducible and reliable. Hence, it is now possible to assume that the NPs play an essential role in assisting the filament growth and in stabilizing its dynamics during conditioning. Indeed, considering the ToF-SIMS images in `Figure 4.41`, where pristine (a), b) and c)) and conditioned (e), f) and g)) devices are compared, a very different nanoparticles distribution can be noticed. In particular, NPs are almost uniformly distributed in pristine devices (`Figure 4.41 c)`). On the contrary, in conditioned devices, it is possible to observe a coalescence of Au NPs in correspondence of Ag filaments (`Figure 4.41 f)`). This behavior indicates that NPs could actually diffuse within the organic matrix, acting as seeds for filaments formation

and growth. This feature seems to play a crucial role in improving the stability and reproducibility of the switching behavior, just as already observed for inorganic resistive-switching devices [131, 132].

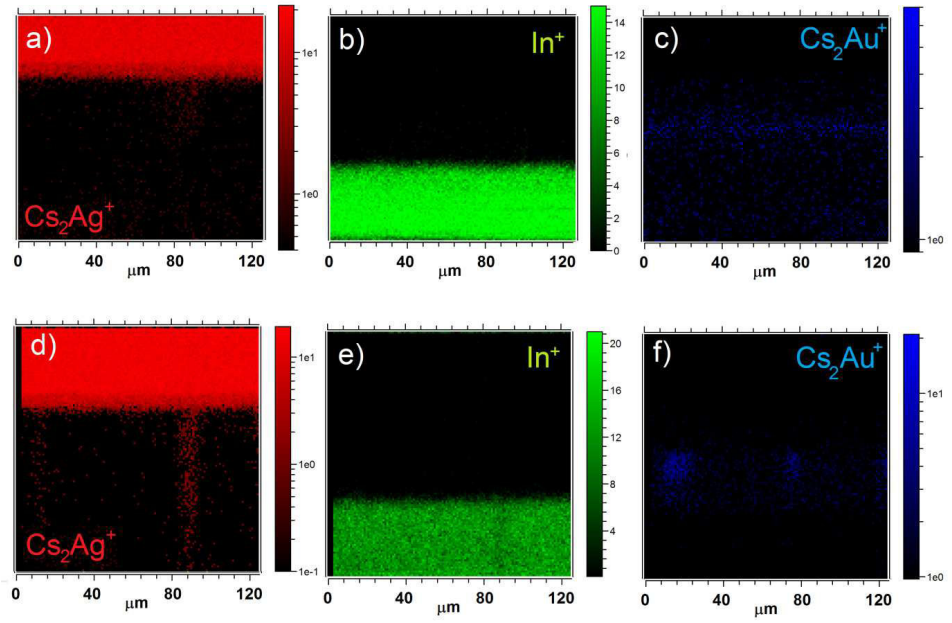


Figure 4.41: Two dimensional (XZ) cross sections extrapolated from the 3D ToF-SIMS images of a pristine (top panels a-b-c) and a cycled (bottom panels d-e-f) memory element. The spatial distribution and intensity of Ag ((a) and (d)) and Indium ((b) and (e)) and Au ((c) and (g)) are displayed to visualize the ions diffusion depth into the organic layer. Both the intensity and the diffusion depth of silver were found to be lower in pristine samples if compared to measured devices. In cycled devices, cross-sections have allowed identifying the presence of few micron size silver diffusion paths bridging the two electrodes and a higher Au signal in the filament area.

In conclusion, the results clearly evidence the top electrode material diffusion inside the organic layer. Resistive switching mechanisms in this material can thus be interpreted in terms of formation and rupture of metallic filaments inside the organic layer assisted by the metal NPs.

4.8 A step forward: flexible substrates

One fundamental advantage of organic electronics is the possibility of fabricating devices on thin and flexible substrate with relatively low production costs. Flexible electronics is one of the most debated

issues in the field of hi-tech research and it represents one of the most important challenges for future electronics. The possibility of fabricating flexible electronic circuits, which can be deformed and conformed to curved surfaces, would trigger a lot of applications in health and in many areas of technology such as robotics and energy. In particular, in the case of organic memories, currently the main applications can be identified where it is not essential a high volume of storage information, but where mechanical flexibility is fundamental (e.g. smart packaging). For these reasons, in a latter step the research activity has been focused on the development of flexible resistive memory devices.
Interestingly, the fabrication procedures developed for glass substrates were transferred on flexible substrates without substantial variation. As only difference with respect to devices fabricated on glass, a different photolithographic technique for the patterning of the ITO bottom electrodes was developed (see Section 4.4.2). So far, only devices using Al NPs has been fabricated and characterized. The deposition of Au NPs by electrosprying over plastic substrates is currently under optimization. This step resulted highly challenging, so the fabrication and characterization of flexible, reliable memory elements based on Au NPs is still ongoing. In the following, electrical characterization of Al NPs based memories will be reported. In particular, devices with a 15 nm thick Al NPs interlayer, a 240 nm thick N1400 matrix and Ag top electrodes were tested, as this configuration resulted the best for Al NPs-based devices fabricated on glass substrate.
As for devices fabricated on glass substrates, resistive switching was observed when measurements were perfomed in ambient conditions. Figure 4.42 a) shows a typical I-V characteristic of flexible devices with the structure PET/ITO/N1400/Al NPs/N1400/Ag. The memory polarity resulted substantially the same of devices fabricated on glass: the device is initially in its LRS or ON state, turning off at the threshold voltage V_{OFF}. During the reverse voltage sweep, an abrupt resistance decrease occurs at the threshold voltage V_{ON} and the device switches from the OFF state back to the ON state. The electrical performances are very similar to the previous on glass substrates: 87% of devices showed a reproducible switching behavior, with average writing and erasing voltages of (-2.0$\pm$0.4) V and (+2.3$\pm$0.5) V, respectively. The average I_{ON}/I_{OFF} ratio, at the reading voltage V_{READ} = 0.2 V, is $(2 \pm 1) \times 10^5$. Statistic data for writing voltage, erasing voltage and I_{ON}/I_{OFF} ratio are reported in Figure 4.43.

The device functionalities as memory elements have been evaluated by performing endurance tests as well as retention time tests; the results are reported in Figure 4.42 b) and c), respectively.

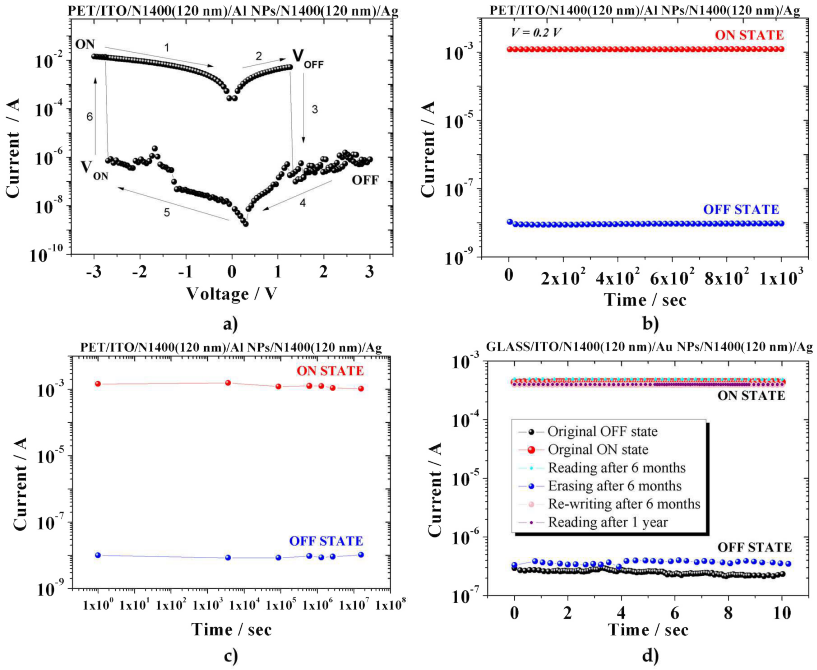


Figure 4.42: Representative a) I-V characteristic; b) endurance tests; c) retention time tests performed in air for flexible memories; c) Writing and erasing tests performed within 6 months from fabrication.

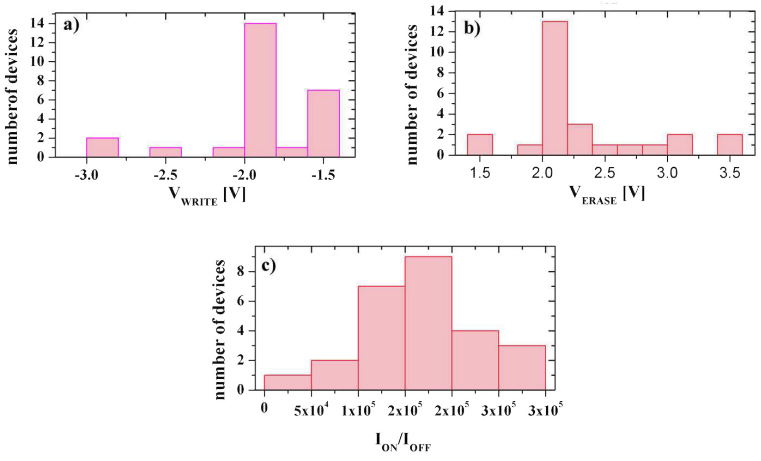


Figure 4.43: Histograms showing: flexible memories statistics for (a) writing voltage, (b) erasing voltage, (c) current ratio.

Endurance/stress tests demonstrated the stability of the memories for a continuous reading time in ambient conditions. As shown in

Figure 4.42 c), a maximum retention time of 1.5×10^7 s (6 months) was recorded. Moreover, at this time, the originally programmed devices were erased and re-written on purpose, resulting in OFF and ON states that are exactly the same as the initial ones (see Figure 4.42 d)). As the devices were measured and stored in ambient conditions for the whole period of investigation, the stability in air of the N1400-based memory was demonstrated also in this implementation.

4.9 Conclusions

In conclusion, a novel non-volatile hybrid organic–inorganic memory structure has been presented. *ActivInk*^{TM} *N1400*, a commercially available, environmentally stable, n-type organic semiconductor, was employed for the first time ever as organic matrix. This work clearly demonstrates the suitability of such a material in the fabrication of memory elements. Devices fabricated on glass substrates were firstly considered, employing different metal NPs as intermediate layer. In Au NPs based memories, a retention time of at least ten months was reproducibly demonstrated for devices stored in ambient conditions for sixteen months in total; in addition, after this time, the functionality of the devices in terms of writing, reading and erasing was perfectly maintained. These performances are the best reported so far in literature; it is also noteworthy that, to our knowledge, the statistic analysis is the larger ever reported for organic-based RRAMs. Devices employing Al NPs resulted less stable, showing not only a shorter retention time, but also the degradation of the ON and OFF states after less than 6 months from the fabrication. Nevertheless, the performances of the Al NPs-based devices are still absolutely competitive with the state of the art, and suitable for several applications such as smart packaging. The comparison of the performances of the two device structures suggests that environmental stability of both organic and inorganic materials is needed for obtaining reproducible and stable memory effects. Such a result is possibly general, thus defining a design rule for memory devices employing different materials and material combinations. The proposed structure was thoroughly characterized by surface sensitive (AFM) and depth profile (XPS and ToF-SIMS) techniques. The results clearly evidence the top electrode material diffusion inside the organic layer. Resistive switching mechanisms in this material can thus be interpreted in terms of formation and rupture of metallic filaments inside the organic layer assisted by the metal NPs. Finally, the developed memories technology has been successfully transferred

on flexible PET substrates. In particular, at the moment only devices incorporating Al NPs have been studied and results are very similar to the previous on glass substrates. Interestingly, higher retention times were recorded with flexible Al NPs based memory. Further investigations are in progress in order to achieve a full comprehension of the degradation mechanisms for Al NPs, to better control the filament dynamics and to increase the device reliability.

5 TOWARDS PRINTED MEMORIES

Contents

5.1 Introduction

Nowadays, due to the growth in material consumption and population, two major concerns in the world are energy consumption and waste. A sustainable society is technically and economically feasible only with a drastic increase in the efficiency of material and energy use. Environmentally sustainable systems for the design, production, and handling of electronic devices should be developed to solve the dramatic increase in electronic waste. Moreover, industrial manufacturing processes should undergo a transformation with minimal impact on the environment. Emerging printable electronics technology has attracted considerable attention because it has the potential to drastically reduce ecological impact, energy consumed in manufacturing, and material wastage. Indeed, printing techniques allows performing simultaneously coating and patterning and enables the correct amount of the necessary material to be placed at the correct position with extremely high material efficiency. In particular, drop-on-demand technology in the form of inkjet printing has demonstrated a rapid growth during the last two decades: it turned

out to be a relatively cheap alternative for the production of electronic devices if compared to other micro- and nanopatterning techniques, like photolithography. With direct inkjet printing, patterns can be realized in one step, and therefore reduce the time, space and waste consumed in production. Moreover, this technique has the potential to be applied to organic electronic devices, to direct writing of electronics onto flexible substrates, and to biotechnology and biomedical materials. Organic materials offer a unique opportunity to guide electronics industry towards an environmentally safe direction. Printed organic electronic devices can be fabricated in freeform shapes on flexible substrates at extremely low costs. Therefore, these devices can be used in a number of novel consumer applications, such as large area displays, disposable sensor arrays, radiofrequency identification tags (RFIDs), and various smart packaging devices. Most of these electronic devices inevitably involve functions that require non-volatile memories with high switching speeds, ability to retain their states for relatively long periods and which can be programmed preferably by electrical signals. Organic memories are increasingly being considered as promising candidates for such applications as these memories can be mechanically flexible and can be processed at low temperatures using solutions, i.e inks.
During the PhD reasearch activity, the definition of technological processes for the reliable fabrication of high performances printed organic memory devices has been investigated. In particular, the possibility of completely transferring the technology developed for the memory devices presented in the previous chapter was contemplated. Indeed, materials like gold nanoparticles and N1400 could be easily treated by liquid phase in several organic solvents, thus being suitable for the development of inks to be employed in printing technologies. Moreover, among commercially available conductive inks, silver is the most widely used material. Consequently, a final goal of developing an entirely inkjet-printed organic memory devices can be surely foreseen, replacing step by step the preparation of the functional components (top and bottom electrode and the resistive layer) from evaporation based fabrication with inkjet-printing. Among these, the fabrication of an inkjet printed resistive layer is the most challenging activity. Indeed, the activity carried out so far (and described in the sequent sections) is related to the optimization of ink formulation and printing parameters for the deposition of the hybrid resistive layer. The optimization of the electrodes patterning is ongoing at the time of writing.

5.2 Structure and materials

The basic implemented structure is shown in Figure 5.1. Since the technology developed for glass substrates was transferred on flexible substrates without substantial variation of performances, all memory devices were fabricated on ITO coated PET substrates (Delta Technologies), in order to ensure transparency and mechanical flexibility. ITO and silver were employed as bottom and top electrodes, respectively, since this configuration allowed obtaining the best results for thermally evaporated devices. The main innovation is the resistive layer, which consist of a N1400 and gold NPs blend, i.e. an hybrid organic/inorganic ink. In particular, methoxybenzene (anisole) was employed as solvent for ink preparation. The implemented layout is the one designed for flexible memory devices (see section 4.3) and here reported in Figure 5.1 . Specifically, also in this case, the layout choice was driven by the prospect of integration with electrical sensors.

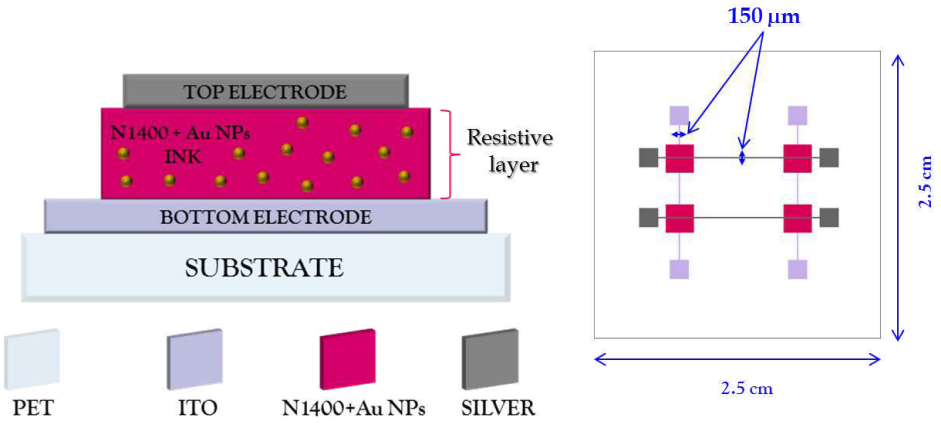


Figure 5.1: Schematic structure and layout of the printed memory elements.

5.3 Fabrication process

The fabrication process for a single memory element is schematically depicted in Figure 5.2. It starts from an ITO coated PET susbtrate, on which ITO bottom electrode is directly patterned. Then, the resistive layer is printed in one step. Finally, the procedure ends with the Ag top electrode deposition. If compared with the fabrication procedure of thermally evaporated memory devices (see

Figure 4.4), it is clearly evident that printing involves a reduced number of process steps, as three thermal evaporations are now replaced by a single printing process. ITO and silver electrodes were patterned with the same procedures already described in sections 4.4.2 and 4.4.4, respectively. As a consequence, in the following, only the details of resistive layer deposition will be provided.

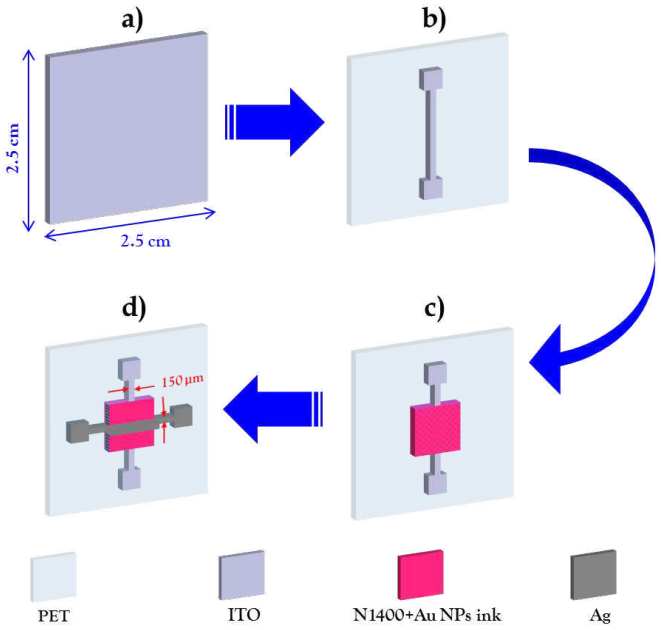
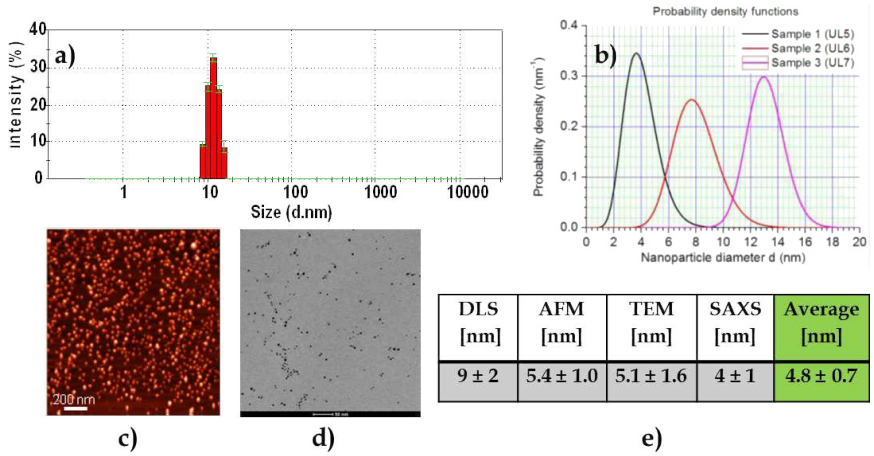


Figure 5.2: Scheme of the fabrication process: a) ITO coated PET substrate; b) ITO bottom electrode patterning; c) resistive layer printing and d) top electrode deposition.

5.3.1 Ink formulation

The ink is the core of the technology as all final material properties, as well as drawbacks, are dictated by its chemistry. For instance, evaporation, film homogeneity, electrical properties rely heavily on ink formulation. Currently, the most widely used are silver inks, where nanoparticles are dispersed in an appropriate carrier, allowing a proper ink ejection control. This suggests that the control on the nanoparticles synthesis is important for the ink development.
In order to be used in inks, nanoparticles should be small (less than 50 nm in diameter) enough to avoid clogging in the nozzles of the inkjet printhead during the printing process. In this work,

gold nanoparticles were synthesized according to chemical reduction method described in [129], as already explained in section 4.4.3. Figure 5.3 shows Dynamic Light Scattering (DLS), Atomic Force Microscopy (AFM), Transmission Electron Microscopy (TEM) and Small Angle X-ray Scattering (SAXS) characterizations of the Au NPs colloid in water. Measurements revealed that the aqueous colloid is highly monodisperse without any agglomerates or aggregates. The shape of the nanoparticles is spherical with an average size of (4.8±0.7) nm, which is suitable for fabrication of inks.



DLS [nm]	AFM [nm]	TEM [nm]	SAXS [nm]	Average [nm]
9 ± 2	5.4 ± 1.0	5.1 ± 1.6	4 ± 1	4.8 ± 0.7

Figure 5.3: a) Dynamic Light Scattering (DLS), b) mall Angle X-ray Scattering (SAXS), c) Atomic Force Microscopy (AFM), and d) Transmission Electron Microscopy (TEM) characterization of Au NPs; e) The Au NPs size in colloid obtained from AFM, DLS, TEM and SAXS techniques, and average value.

The use of NPs in organic memory elements requires to prepare stable and well-dispersed NPs in solvents commonly used in organic electronics. Most organic molecules are *non-polar*, i.e. they contain bonds between atoms with similar electronegativities (such as carbon and hydrogen), which lack partial charges. At molecular level, solubility is controlled by the energy balance of intermolecular forces between solute-solvent molecules. It is well known that polar molecules (containing bonds between atoms with very different electronegativities, such as oxygen and hydrogen) dissolve in polar solvents (e.g. water, alcohols) and non-polar molecules in non-polar solvents. This means that the use of NPs in organic memory elements requires organic non-polar solvents. There are different possible methods which allow obtaining stable and well-dispersed nanoparticles in non-polar solvents. The phase transfer method

of aqueous synthesized nanoparticles to organic solvents gives the possibility to disperse nanoparticles in non-polar solvents. The idea is to functionalize the NPs surfaces with an appriopriate modifier, which prevents agglomeration and/or aggregation of nanoparticles in the non-polar solvent or while being deposited on the substrate. In a phase transfer process, NPs are first prepared in water under optimized conditions and then subjected to the phase transfer from an aqueous solution to organic media. Although this method involves two steps and requires additional stabilizing agents, it provides great control of NPs size and of polydispersity in non-polar solvents. Moreover, all reagents (e.g., by-products of NP synthesis), which may have a negative impact on the electronics device functionality, remain in the aqueous phase after NPs transfer to organic media.
In this work, phase transfer of the Au NPs was performed using toluene, since it is an organic non-polar solvent for N1400. For the surface modification of Au NPs, a secondary amine, namely 1,1-dioctadecylamine, was used in a 0.01% toluene solution. The modifier amount corresponds to 25 modifier molecules/nm^2 of NP surface. Au NPs were transferred from water to toluene adding to the aqueous nanoparticles colloid acetone and toluene-amine solution with the ratio 2:1:1. Acetone was added to reduce the surface tension between water and toluene phases. The biphasic system was vigorously shaken for at least 1 minute. Subsequently, the system spontaneously separated into a toluene phase and a water phase: the water–acetone phase became yellow and the toluene phase turned into dark red due to the phase transfer of nanoparticles (`Figure 5.4`).

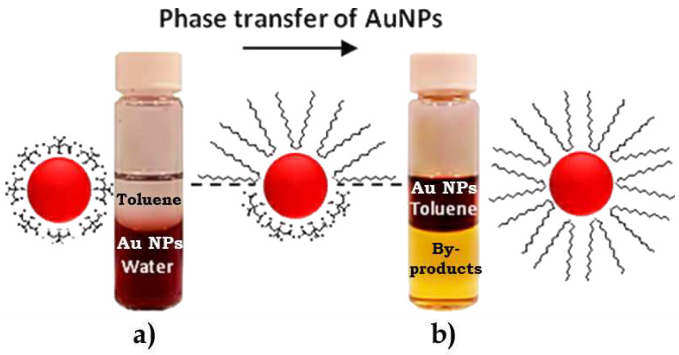


Figure 5.4: Color change of aqueous and organic phase before (a) and after (b) the phase transfer of Au NPs.

Au NPs colloid in toluene was characterized by DLS technique immediately after the phase transfer, and after 19 days. As shown

in Figure 5.5 a) and b), the size of Au NPs modified with 1,1-dioctadecylamine immediately after the phase transfer process is (9±2) nm, and after 19 days is (8±2) nm. Moreover, Au NPs colloid in toluene results monodisperse and stable, because no additional signal on the DLS statistic graph was observed even after 19 days. Au NPs colloid in toluene was also characterized by Scanning Transmission Electron Microscopy (STEM). The analysis of STEM images (Figure 5.5 c)) allows concluding that NPs are spherical and monodisperse with a mean size of 5 nm. This means that size of Au NPs does not change in relation to the water colloid and NPs distribution on the substrate is related to the solvent evaporation during the sample preparation procedure. The effectiveness of the phase transfer process was monitored by UltraViolet–Visible (UV-Vis) spectroscopy. Figure5.5 d) shows the UV-Vis spectra of Au NPs before and after transfer from water to toluene with 1,1-dioctadecylamine.

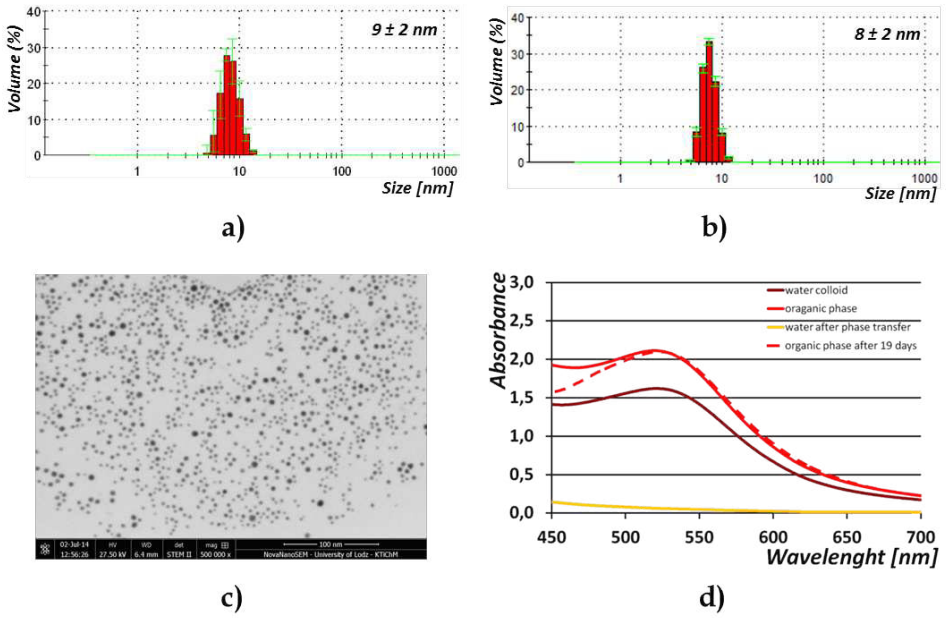


Figure 5.5: Size distribution of Au NPs in toluene measured by the DLS technique (a) immediately after the phase transfer and (b) after 19 days; c) STEM characterization of Au NPs in toluene; d) UV-Vis spectra of Au NPs in water, Au NPs in toluene immediately after the phase transfer, Au NPs in toluene after 19 days and water phase after phase transfer process.

The maximum plasmon resonance peaks of Au NPs in water and in toluene are at 521 nm and 520 nm, respectively. The respective spectrum of the aqueous phase shows a baseline without a characteristic signal of gold nanoparticles. Additionally, it can be

concluded that transfer of Au NPs from water to toluene does not lead to aggregation. The maximal plasmon peaks before and after phase transfer process remained unchanged, indicating that Au NPs are well dispersed also after the transfer process. Finally, the colloid was concentrated through toluene evaporation, in order to obtain different Au NPs concentrations, namely 200, 500, 1000, 2000 ppm. Although toluene is a N1400 solvent, it is not generally considered a valuable solvent for ink preparation, due to its low viscosity (0.59 cP at 20 °C). Among N1400 solvents, anisole shows a viscosity suitable for printing (1.05 cP at 20 °C); moreover, it is relatively nontoxic, especially if compared to other solvents with a viscosity feasible for printing (e.g. 1,2-dichlorobenzene). Therefore, a phase trasfer of Au NPs colloid from toluene to anisole was performed through toluene evaporation, under reduced pressure, from a mixture containing Au NPs in toluene and anisole mixed in 1:1 volume ratio. Au NPs colloid in anisole was characterized by DLS technique immediately after the phase transfer, and after 1 month (Figure 5.6 a)-b)). Results of DLS indicates that the size of Au NPs immediately after the phase transfer process and after 1 month is (9±2) nm. Au NPs colloid in anisole is monodisperse and stable, because no additional signal on the DLS statistic graph was observed even after 1 month. Au NPs were deposited on a copper grid and characterized by STEM (Figure 5.6 c)). Analysis of STEM images allows to conclude that the nanoparticles are spherical and monodisperse with a mean size of 5 nm. Size of Au NPs did not changed in relation to the water colloid and NPs distribution on the substrate is related to the solvent evaporation during the sample preparation procedure.
Finally, ink preparation was completed by determining the optimal N1400 concentration for its complete dissolution in both anisole and Au NPs colloid in anisole. Tested concentration ranged from 1 to 50 mg per 1 ml of anisole. The best concentration for the ink preparation was found in 2.5 mg of N1400 / 1 ml of anisole (or Au NPs colloid in anisole). In particular, N1400 incorporation in the colloid can be described as following:

- N1400 was weighed in a glass vial;
- the Au NPs colloid in anisole was added in the vial with the N1400;
- the mixture was stirred for one hour at 60 °C, allowing the complete dissolution of N1400.

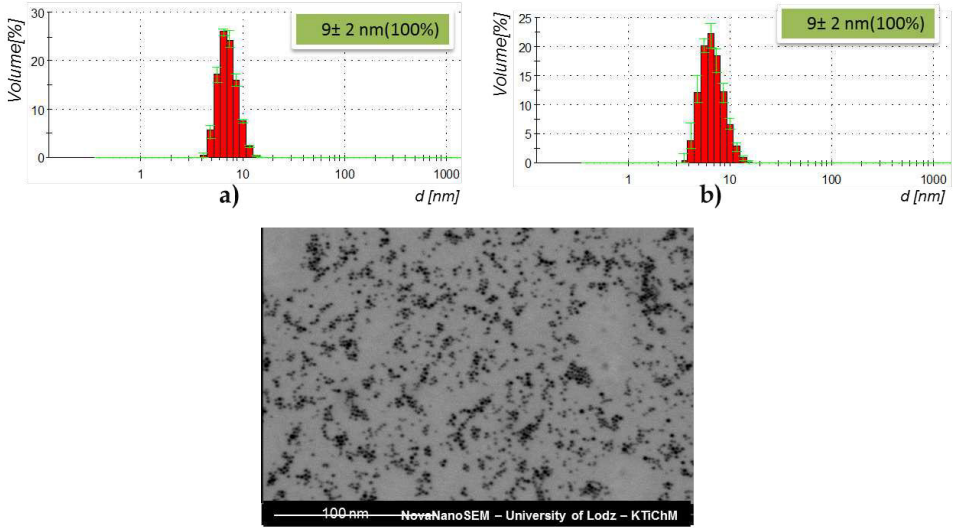


Figure 5.6: Size distribution of Au NPs in anisole measured by the DLS technique (a) immediately after the phase transfer and (b) after 1 month; c) STEM characterization of Au NPs in anisole.

5.3.2 Hybrid layer deposition

The hybrid layer was entirely inkjet printed in air by means of FujiFilm Dimatix Material Printer (DMP) 2800 using a DMC-11610 cartridge. This cartridge contains 16 nozzles with a diameter of 21.5 μm and each nozzle generates 10 pL drops of ink. The cartridge was filled with the not filtered anisole-based ink using a glass pasteur pipette. Immediately before printing, PET substrates with patterned ITO bottom electrodes were cleaned by a rinsing with acetone and then dried under nitrogen flux. In order to maintain the nozzles in optimal conditions, cleaning cycles were performed before and also during printing (approximately every 50 scans). The details of the cleaning cycle process performed before each printing and during printing are reported in `Table 5.1 and 5.2`, respectively. `Table 5.3` reports the optimized cartridge and printer main settings employed. During printing the cartridge and the platen (and thus substrates) were kept at room temperature. Indeed, keeping the platen at a lower temperature may avoid solvent evaporation at the nozzles meniscus which can cause clogging of nozzles. Since high resolution is not essential while film continuity is required, it was printed using three jetting nozzles with a firing voltage of 35 V and a drop spacing of 15 μm. The highest achievable jetting frequency (25

kHz) was set in order to avoid long lasting of the process, which could damage nozzles due to solvent evaporation at the nozzle meniscus.

Action	**Time**	**Frequency**	**Post delay**
Spit	500m s	1.5 kHz	2 s
Purge	1 s		2 s
Spit	500 ms	1.5 kHz	2 s

Table 5.1: Cleaning cycle procedure used before each printing.

Action	**Time**	**Frequency**	**Post delay**
Spit	100 ms	1.5 kHz	2 s
Purge	0.1 s		2.5 s
Spit	100 ms	1.5 kHz	2 s

Table 5.2: Cleaning cycle procedure used during printing.

Cartridge	10 pL
Cartridge temperature	RT
Platen temperature	RT
Cartridge Print Heigh	500 mm
Drop spacing	15 μm
Jetting nozzles	3
Firing voltage	35 V
Jetting frequency	25 kHz

Table 5.3: Main cartridge and printer settings.

The hybrid layer was always fabricated printing one single layer. As shown in Figure 5.7, the pattern consists in 4 rectangulars of 4 mm x 3 mm for each substrate of 2.5 cm x 2.5 cm, i.e 1 rectangular for each memory element. As already mentioned in the previous section, different inks with various Au NPs concentrations were prepared and tested (Table 5.4).

In order to achieve satisfactory printing performances, monitoring the quality of jets ejected is crucial. Jets are considered good-performing if: i) they are made of single, spherical drops,; ii) their direction is perpendicular to the nozzle plate and parallel one another; iii) drops have matched velocities. These features allow a high precision in droplets deposition and a minimal spreading on the

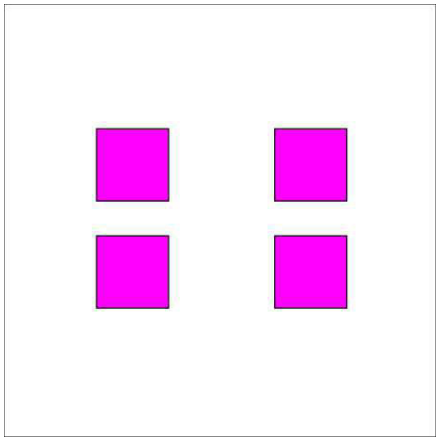


Figure 5.7: Schematic of the used pattern.

Ink	N1400 %	Au NPs
N1400 INK	0.2wt%	-
INK 1	0.2wt%	200 ppm
INK 2	0.2wt%	500 ppm
INK 3	0.2wt%	1000 ppm
INK 4	0.2wt%	2000 ppm

Table 5.4: Tested inks with different Au NPs concentrations.

substrate. Firing voltage, jetting frequency and the number of jetting nozzles are the parameters that can be set to obtain good-performing jets. Monitoring and adjusting the ink jets is possible by using the drop watcher camera system, which includes a digital camera with a magnification of 150x. Once the nozzles are positioned over the system, it allows direct observation of the jetting of the ink. Figure 5.8 shows drop watcher images corresponding to the jetting of the tested inks. It is noticeable that the higher is the Au NPs concentration the higher the possibility of clogging the nozzles. In all the cases jets appear perpendicular to the nozzle plate and parallel one another, while for higher Au NPs concentations drops velocities are not always matched.

Good printing performances were obtained for all the anisole-based inks with and without Au NPs, as shown in Figure 5.9. In particular, Figure 5.9 a) represents a generic printed film before solvent drying: no differences between printed films were observed. On the contrary, the printed films after solvent drying resulted to be clearly different in function of the Au NPs concentration. In all the

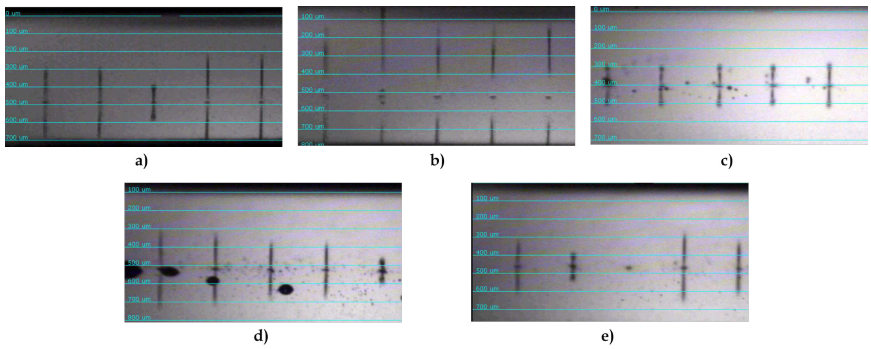


Figure 5.8: Jetting of the tested inks: a) N1400 INK; b) INK 1; c) INK2; d) INK 3; e) INK4.

cases, films were continuous and allowed the fabrication of devices without short circuits between top and bottom electrodes.

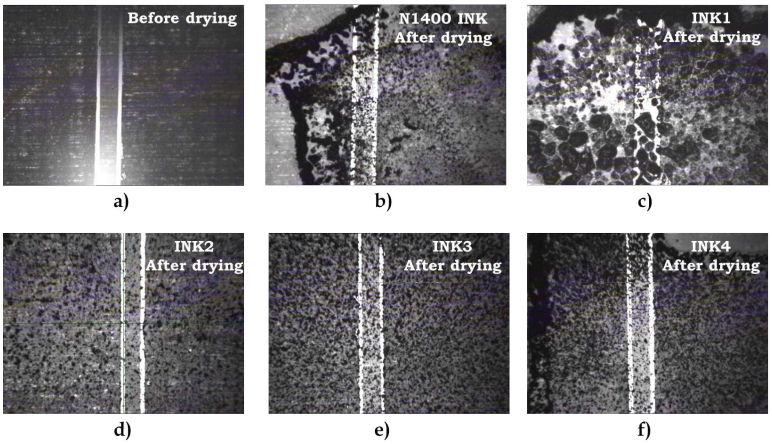


Figure 5.9: Images of printed film by means of the fiducial camera: a) generic printed film before drying; printed films after drying: b) N1400 INK; c) INK 1; d) INK2; e) INK 3; f) INK4.

5.4 Electrical characterization

Electrical measurements were performed in ambient conditions (temperature of about 22 °C, humidity in the order of 50%) with an Agilent B1500A Semiconductor Parameter Analyzer. Each memory element was probed with tungsten tips. Generally, the memory devices did not require electrical preconditioning in order to achieve

bi-stability. The typical measurement procedure is equal to the one described in section 4.6.1.
Several tests were carried out with the prepared inks, in order to study the influence of NPs concentration on electrical proprierties and to find the best combination which allows to replicate performances already obtained for thermally evaporated structures.
At first, structure with N1400 INK, i.e. without NPs, were fabricated and characterized. Figure 5.10 shows a typical I-V curve for this kind of devices, which never showed switching behaviours.

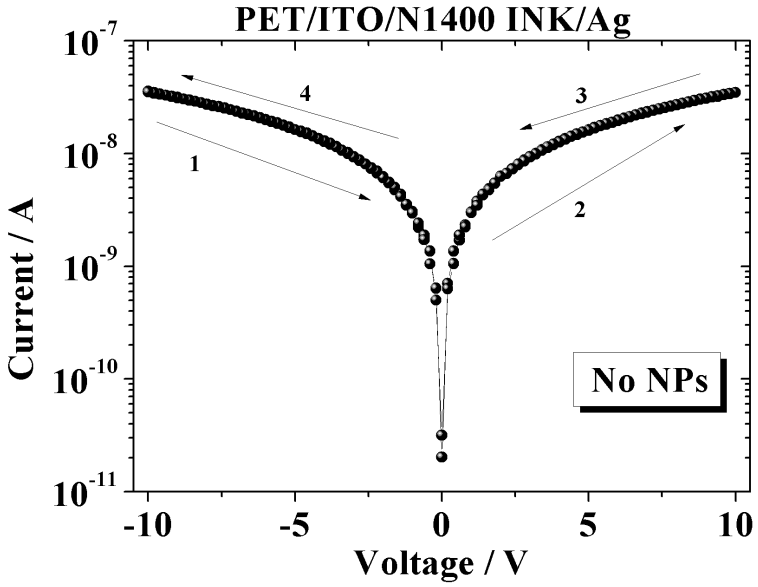


Figure 5.10: Rapresentative I-V characteristics for printed devices without NPs measured in air.

This first result is perfectly consistent to the one obtained for devices fabricated by thermal evaporation (see section 4.6.2). Indeed, it turned out that the presence of metal NPs seems to play a role in conditioning the switching behaviour of the devices. Figure 5.11 shows representative I-V characteristics of structure with different Au NPs concentrations. The introduction of Au NPs allows obtaining a noticeable and reproducible resistive switching effect. In particular, it was found that the two lowest concentration (Figure 5.11 a)-b)), i.e. 200 and 500 ppm, showed the best electrical performances. No significant switching behaviours were observed for the devices with the highest Au NPs concentration, i.e. 1000 and 2000 ppm (Figure 5.11 c)-d)).

Specifically, electrical results demonstrate that the higher is

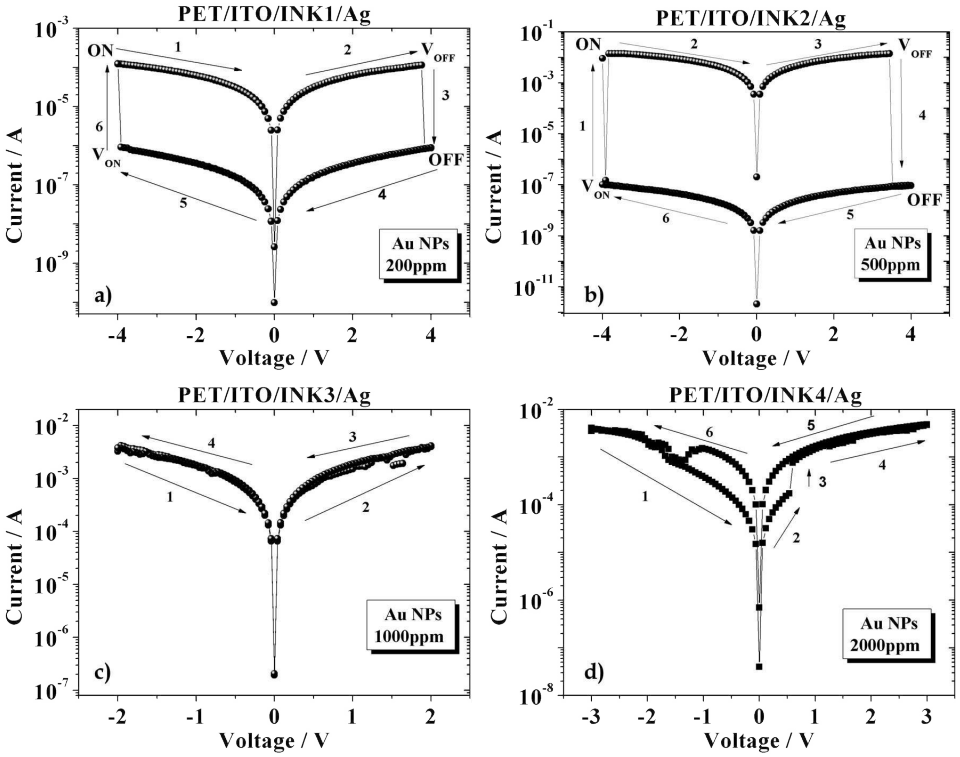


Figure 5.11: Rapresentative I-V characteristics for structures with different Au NPs concentrations measured in air: a) 200 ppm; b) 500 ppm; c) 1000 ppm; d) 2000 ppm.

the NPs concentration, the higher is the I_{OFF} current, and so less significant is the switching effect. This phenomenon is depicted clearly in `Figure 5.12 a)`, where average values of I_{ON} and I_{OFF} for all the structures are reported. `Figure 5.12 b)` illustrates a comparison between I-V characteristics: it can be noticed again that higher Au NPs concentrations result in higher currents, i.e. ON and OFF states are almost identical. Moreover, it is interestingly to observe that the current of the device without NPs is comparable with the I_{OFF} of the structures which show switching behaviour.

It is possible to conclude that Au NPs concentration of 200 ppm and 500 ppm represent the best range for achieving a good and reproducible resistive switching effect with good ON/OFF ratios. Importantly, higher I_{ON}/I_{OFF} ratios, in order of 10^5, were recorded for devices with a concentration of 500 ppm. However, 89% of devices with a NPs concentration of 200 ppm showed a reproducible switching behavior, with average writing and erasing voltages of (-3.8±0.2) V and (+3.7±0.4) V, respectively. On the other hand,

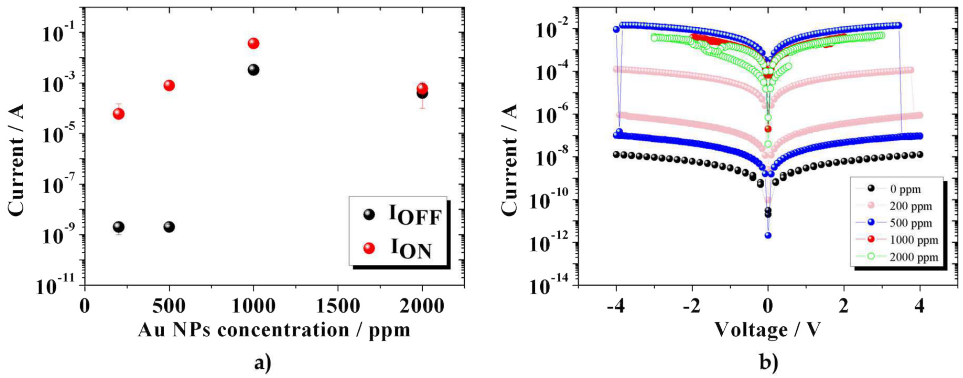


Figure 5.12: a) Average values of I_{ON} and I_{OFF} for all structures with different NPs concentrations; b) Comparison between I-V characteristics.

only 50% of device with a NPs concentration of 500 ppm showed a reproducible switching behavior, with average writing and erasing voltages of (-5±2) V and (+3.5±0.5) V, respectively. Statistic data for writing voltages, erasing voltages and I_{ON}/I_{OFF} ratios are reported in Table 5.5.

Parameter	**INK1**	**INK2**
V_{ON}	(-3.8±0.2) V	(-5±2) V
V_{OFF}	(+3.7±0.4) V	(+3.5±0.5) V
I_{ON}/I_{OFF}	(3±1) $\times 10^3$	4.2±0.6) $\times 10^5$

Table 5.5: Statistic data for writing voltages, erasing voltages and I_{ON}/I_{OFF} ratios.

It is important to highlight that INK1 and INK2 allowed to fabricate memory devices with very similar writing and erasing voltages. However, reliable resistive switching can be obtained only with appropriate current compliances. In particular, it turned out that the higher concentration of NPs (500ppm) require a higher current compliance. Table 5.6 reports current compliance values for the two structure. Specifically, during the set process (writing), devices with a Au NPs concentration of 200 ppm require a current compliance of 2.5 mA, while structures with higher Au NPs concentrations switch on only with a current compliance of 10 mA. Similarly, reset is possibile only setting current compliances of 10 and 12 mA for INK1 and INK2 based devices, respectively. Finally, a different current compliance has to be also set while sweeping the voltage, in order to obtain a typical resistive swithing in the current–voltage char-

acteristic. The actual relationship between Au NPs content in the resistive film and the required current compliance requires more sophisticated analysis. Nevertheless, it is possible to hypothesize that thicker filaments are determined by an higher NPs concentration, thus requiring higher power to be formed/interrupted.

Parameter	**INK1**	**INK2**
Sweep	10 mA	15 mA
Writing	2.5 mA	10 mA
Erasing	10 mA	12 mA

Table 5.6: Current compliance values required in sweeping, writing and erasing processes for memory devices with different Au NPs concentrations.

Finally, it can be noticed that the memory polarity resulted substantially the same of devices fabricated by means of thermal evaporation: the device is initially in its LRS or ON state and it turns off at the threshold voltage V_{OFF}. During the reverse voltage sweep, an abrupt current increase occurs at the threshold voltage V_{ON} and the device switches from the OFF state back to the ON state. The electrical performances are very similar to ones of thermally-evaporated memories (see Chapter 4 for more details), with writing, erasing voltages and ON/OFF current ratios in the same order of magnitude.

5.5 Conclusions and outlooks

In conclusion, it has been studied the possibility of fabricating memory devices based on a printed blend made out of N1400 and Au NPs in anisole. It has been analyzed the influence of Au NPs concentration in terms of resistive switching. In particular, 5 different Au NPs concentration were tested: 2 out of 5 structures showed promising results, comparable with the thermally evaporated N1400 based devices. As already found for these memory elements, the presence of NPs seems to be essential for determing the resistive switching. Moreover, electrical results demonstrate that the higher is the NPs concentration and the higher is the I_{OFF} current, and so less significant is the switching effect. This work clearly demonstrates the real possibility of fabricating high performaces printed memory elements. Further investigations are in progress in order to optimize the fabrication process towards a fully printed memory elements arrays. In particular, the inkjet printing of both bottom and top electrodes can be foreseen. Moreover, a thorough testing on endurance

and retention time is still missing, and will be carried out as soon as the fabrication process will be fine-tuned.

Part III

Integration of memory devices with electrical sensors

6 MEMORY-SENSOR SYSTEM

Contents

6.1 Introduction

The promise of ubiquitous computing has inspired researchers to integrate electronic circuits into everyday objects and biological tissues. The vision is for distributed sensors and processing devices to monitor and respond to the environment autonomously, enhancing the way humans interact with objects around them. Sensor applications have gained importance due to the increasing request for more and more intelligent and safe products. As the cost of sensor technology decreases the usage will spread to new products with functionalities that never before have been provided. For example, sensors incorporated into clothing or attached to skin can allow continuous monitoring of vital signs and alert people, both locally and remotely, if dangerous thresholds are exceeded. Currently, there is also a growing interest to develop sensor technology to be used for cellulose-based products for packaging, hygiene, or graphical use. The potential of smart packaging technology is far

reaching, from food safety and drug's use monitoring to postal delivery tracking and embedded security tags. The primary interest in the package application is to perform surveillance functions where the sensor technology enhances the primary function of the package, namely to protect the item it carries. Smart packaging applications usually involve large area integration of sensor functionality. Moreover, each package has its own design and message, and therefore electronic functions often have to be customized for a particular case. Thus, the system integration technique should both provide low-cost production and low-cost customization. This means that even small series should reach low cost. Here, organic electronics have the potential to provide such low-cost customization solutions. The fabrication of single electronic devices and entire electronic systems on lightweight, conformable and transparent plastic substrates can bring to a significant step forward towards a real smart packaging. Moreover, electronic devices and systems on textiles could determine a deeper integration of electronics and textile industries, towards e-textile and wearable electronics where the application of rigid electronic systems on garments is overcome. At the moment, organic devices are mainly employed as mechanical, physical and biochemical sensors; in this field, the employment of single devices is routinely diffused, while less has been done on electronic systems, where several devices are connected to perform a complex function. Among the reasons behind the limited diffusion of organic electronic systems, the substantial delay in the development of organic memory elements may be invoked. Overcoming the main limitations of organic memory elements may definitely contribute to the diffusion of organic electronic systems entirely fabricated on plastic substrates for the development of several kinds of applications. For instance, it is possible to conceive an integrated gas or acidity sensor to be integrated on food packages, able to memorize the preservation status of perishable goods. In the field of wearable electronics, the integration of biometric sensors and organic memory devices could make garments for sport performances monitoring independent of wireless communication systems, which can be solely fabricated with inorganic – thus bulky and rigid – electronics. To lead weight to the feasibility of the proposed technology to such applications, a significant effort has also been devoted, during the PhD research activity, to the development of basic memory/sensor systems entirely fabricated on plastic substrates. In particular, the suitability of organic non-volatile memory devices for the detection and the storage of external parameters was demonstated. As prototypical example, flexible arrays of mechanically switchable memory elements system were designed, fabricated and characterized.

6.2 Basic concept

As already explained in the previous chapters, RRAMs are characterized by a bi-stable electrical behaviour, which means that it is possible to change the electrical conductivity (resistance) of the resistive element by applying a certain external voltage (program voltage). This change in the conductivity remains constant even when the device is no longer biased and can be restored to its previous value by applying a different external voltage (erasing voltage). Therefore, since RRAMs respond to an applied voltage by a non volatile change of the conductivity, an external stimulus from a sensor element can be used to trigger the memory device to switch. In the simplest case, a sensor device can be connected in series with a two terminal device creating a novel sensor-memory system, as shown in Figure 6.1 a). Different devices (e.g. photo resistor, photodiode, thermistor, pressure sensor) can be used to trigger the switching event in the memory device, according to the scheme reported in Figure 6.1 b).

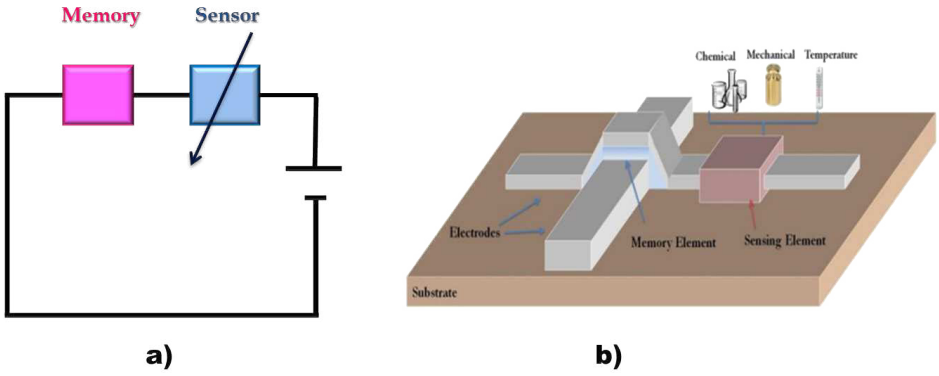


Figure 6.1: Schematic representations of a sensing system coupled with a resistive memory element.

During the Ph.D. research activity here described, the integration of a non-volatile memory element with a **piezoresistor** was developed as prototypical example of a *memory/pressure sensor system*. Indeed, if a memory element is integrated with a piezoresistor (connected in series), the resistivity change in the piezoresistor, induced by an external pressure, can be used for triggering the memory. The nominal resistance of the piezoresitive element in idle conditions (when no pressure is applied) must be much higher than the nominal resistance of the memory element. On the other side, when pressure is applied, the nominal resistance of the piezoresistive element must

be small enough to allow the addressing of the memory. In the following, a complete description of the structure and of the electrical characterization will be provided.

6.3 Materials and system structure

A pressure-triggered memory system was developed integrating a fexible memory element with a pressure sensor using the configuration reported in Figure 6.2 a). As previously mentioned, a resistive memory element is connected in series with the pressure sensor. In particular, a flexible device reported in Chapter 4, with the structure PET/ITO/N1400(120 nm)/Al NPs/N1400(120 nm)/Ag was employed (Figure 6.2 b)). The fabrication process and electrical characterization of such memory elements has been already described in Chapter 4. A commercially available piezoresistive rubber, namely ZL45.1 (ZOFLEX®), has been employed as pressure-sensitive element. Specifically, as shown in Figure 6.2 b)-d), a small square of this rubber was fixed between the Ag top electrode of the memory element and a thermally evaporated Au electrode on PET, which acts as top electrode of the memory-sensor system.

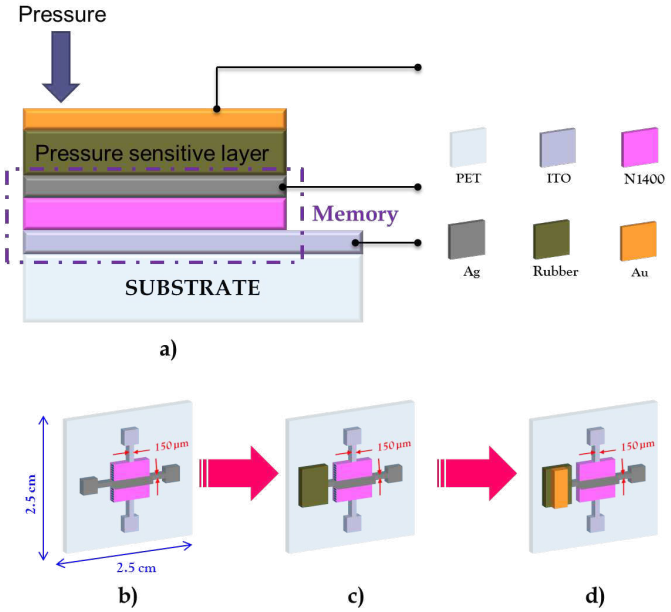


Figure 6.2: a) Schematic representation of the integration of 1 memory element and 1 pressure sensor; b)-c)-d) Integration of the piezoresistive rubber with the resistive memory element.

6.4 Working principle

It has been said that the nominal resistance of the piezoresistor must be much higher than the nominal resistance of the memory in idle conditions, and small enough to allow the addressing of the memory when pressure is applied. The piezoresistive rubber is characterized by a nominal resistance R > 100 MΩ without pressure, whereas, when a pressure higher than 50 kPa is applied, the resistance can be reduced to R < 1Ω. Figure 6.3 shows the typical response of this piezoresistive rubber film to an applied pressure of 10 kPa. As can be noticed, the resistance changes by more than 5 orders of magnitude. If opportunely connected to the memory element, this change in the resistance can be employed for connecting/disconnecting the memory element from the programming voltage, thus allowing the fabrication of a system where a shape insisting on the rubber is memorized.

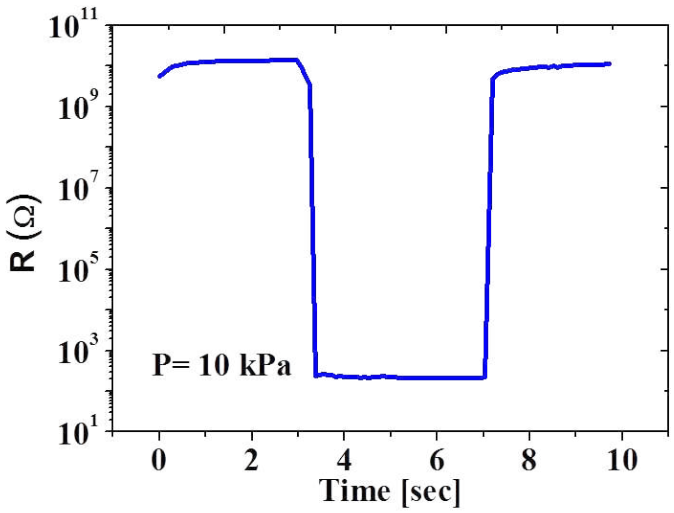


Figure 6.3: Resistance change in a typical piezoresistive rubber film, when an external pressure of 10 kPa is applied.

The working principle of the memory-sensor system can be easily described. If the piezoresistive rubber is connected in series with the memory element, according to the scheme reported in 6.2 a), the most of the programming voltage drops on the piezoresistor. Since the rubber is usually characterized by a very high resistance, in idle conditions only a very small voltage drops directly on the memory element, which will remain in its state. When an external pressure is

applied to the piezoresistor, its resistivity drops down, and the most of the voltage will be directly applied on the memory, thus leading to a state transition. The typical writing and erasing processes are schematically reported in Figure 6.4 and 6.5. Supposing that the memory is in its HRS (OFF state, Figure 6.4 a)). When the system is biased with an external voltage (equal to the programming voltage V_{SET} of the memory element), but pressure is not applied, all the voltage drops in the rubber element and the memory cannot be written. When programming voltage and pressure are simultaneously applied (Figure 6.4 b)), the resistance of the rubber drops down to few hundreds of Ohms and all the voltage is now applied on the memory element, which can be written (Figure 6.4 c)).

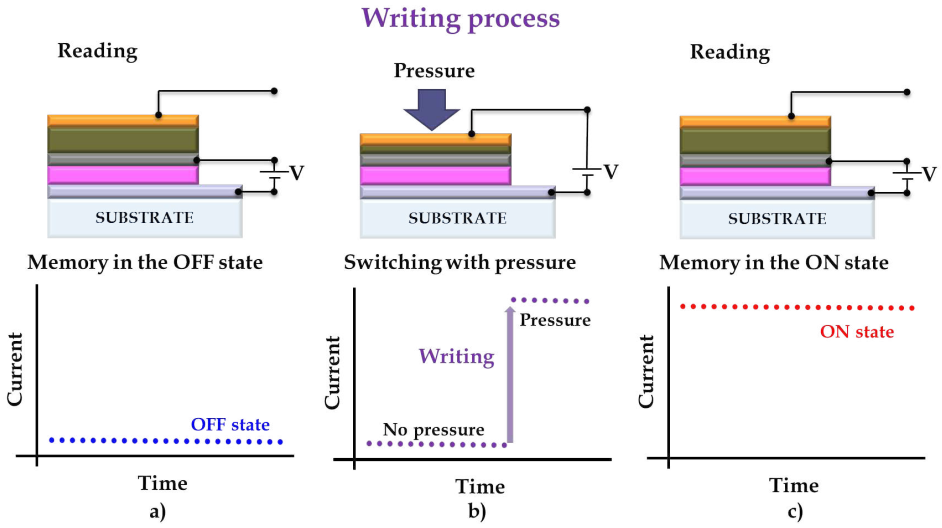


Figure 6.4: Schematic representation of the writing process.

An opposite voltage (equal to the erasing voltage V_{RESET} of the memory element) can be applied to the system in order to erase the memory. Again, if pressure is not applied, all the voltage drops in the rubber, thus not allowing the memory to be erased. When pressure and voltage are simultaneously applied (Figure 6.5 b)), the memory is switched again to the OFF state (Figure 6.5 c)).

6.5 Electrical characterization

Different tests have been carried out on fabricated memory/ sensor systems. In particular, at first, single memory elements have been integrated with a pressure sensor device (1M-1S system) in

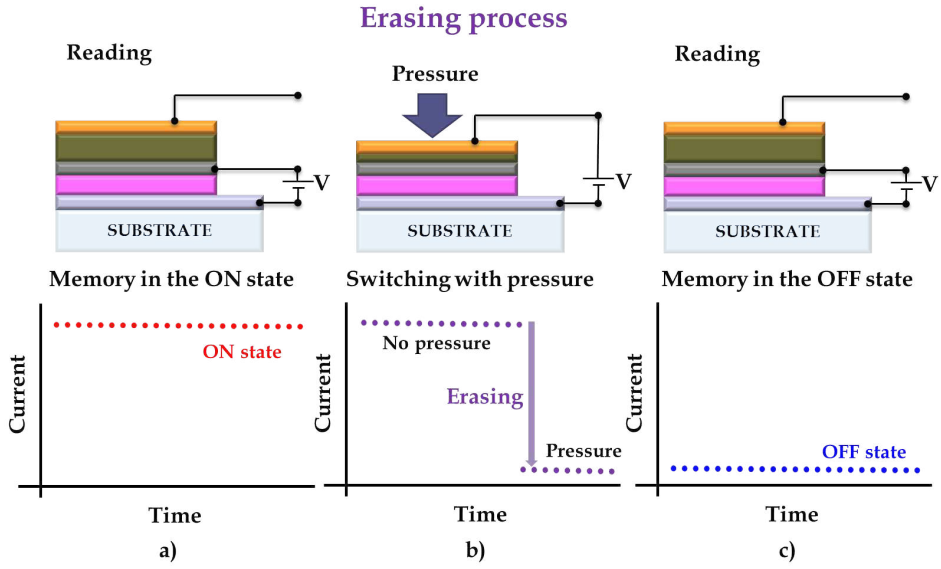


Figure 6.5: Schematic representation of the erasing process.

order to investigate and prove the integration feasibility and functionality. At a later stage, non-volatile memory arrays from 2x2 up to 4x4 bit storage capacity have been fabricated and tested in order to demostrate the possibility to integrate single memory elements to memory arrays in a crossbar wiring. Consequently, arrays of mechanically switchable memory elements system were designed, fabricated and characterized. In the following, a complete electrical characterization will be provided.

6.5.1 Experimental setup

Electrical measurements were performed in ambient conditions (temperature of about 22°C, humidity in the order of 50%) with a Keithley 2636 or an Agilent B1500A Semiconductor Parameter Analyzer. The measurement procedure for the memory elements arrays is equal to the one described in paragraph 4.6.1.
In the case of memory/sensor system, each memory element was contacted with tungsten tips only for the reading process, as shown in Figure 6.6 a). In order to write/erase the system, the ITO bottom electrode was contacted with a tungsten tip, while the Au top electrode was connected with a copper wire. As already explained in the previos sections, memory elements can be written (erased) only when writing (erasing) voltage and pressure are simultaneously applied to the system (Figure 6.6 b)).

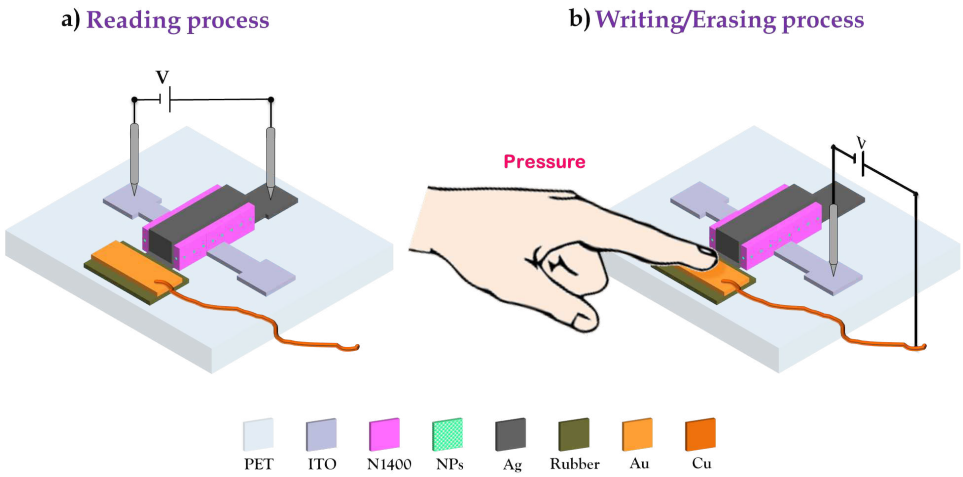


Figure 6.6: Schematic representation of (a) reading and (b) programming/erasing processes on a memory/sensor system.

6.5.2 1M-1S system

As already anticipated, first tests were carried out on a single memory element system. Figure 6.7 shows a typical example of electrical results. If the memory element is in its OFF state (Figure 6.7 a)), the simultaneous application of pressure and writing voltage (V_{SET}) to the system allows the programming of the memory element. In particular, Figure 6.7 b) shows clearly that the writing process starts as soon as the pressure is applied. The subsequent reading process at V_{READ} = 0.2 V, reported in Figure 6.7 c), proves that the memory is now in its ON state. This state is retained even after removing the bias. Aftewards, if the erasing voltage is applied to the series of devices, the memory element is erased only when pressure is applied on the pressure sensor (Figure 6.7 e)). The reading process confirms that the memory is switched again to the OFF state (Figure 6.7 f)).
In order to prove that the integration with pressure sensor does not affect memory performances, a statistical analysis was carried out on a number of single memory/sensor systems. Average writing and erasing voltages of (-2.1±0.5) V and (+2.2±0.6) V, respectively, were measured. The average I_{ON}/I_{OFF} ratio, at the reading voltage V_{READ} = 0.2 V, was $(1.6 \pm 0.7) \times 10^5$. If compared with statistics reported in paragraph 4.8, these results demonstrate that the electrical properties of the single memory element are not modified by the integration with a piezoresistor. Detailed statistics for writing voltage, erasing voltage and ON/OFF current ratio are reported in Figure 6.8.

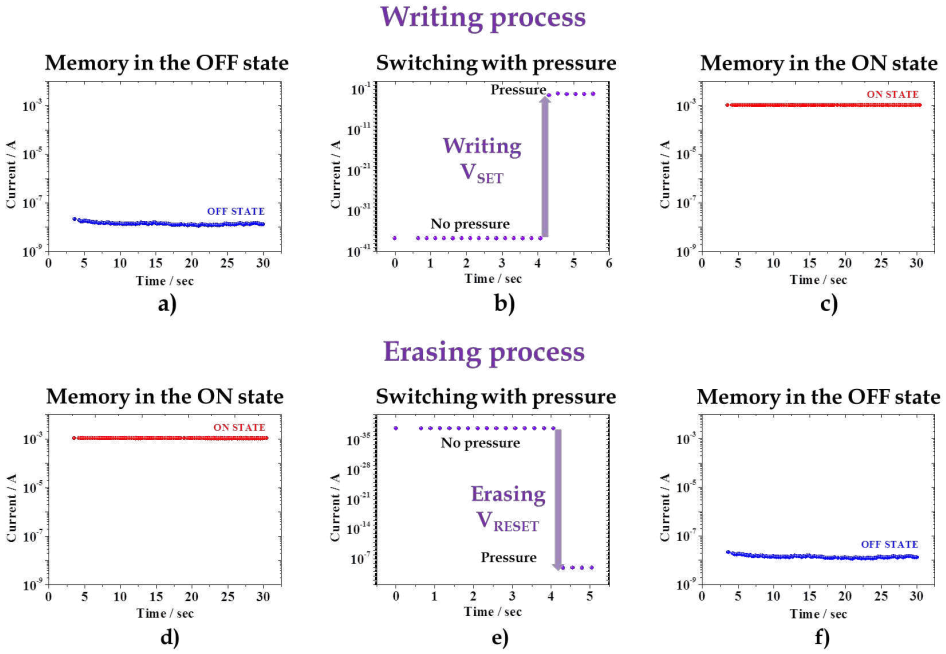


Figure 6.7: Example of a)-c) writing and d)-f) erasing processes on a single memory element system.

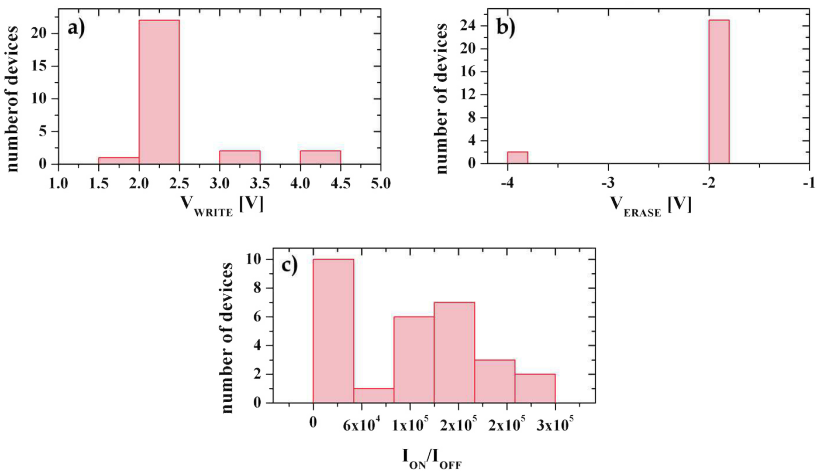


Figure 6.8: Histograms showing: memory/sensor statistics for (a) writing voltage, (b) erasing voltage, (c) current ratio.

6.5.3 2x2 array system

Starting from results obtained for the single memory/sensor system, a layout for the fabrication of a 2×2 array of memory elements

integrated with a pressure sensor was designed. As shown in Figure 6.9, four different devices are fabricated on the same substrate and arranged in a cross-bar configuration. Several tests were carried out on the memory/sensor array. In particular, the possibility of addressing (i.e. programming/erasing) a certain memory in the array, without affecting the status of the non-selected ones, was verified. Initially, all the memory elements are in the high resistance state, and a small current flows through them (Figure 6.9)).

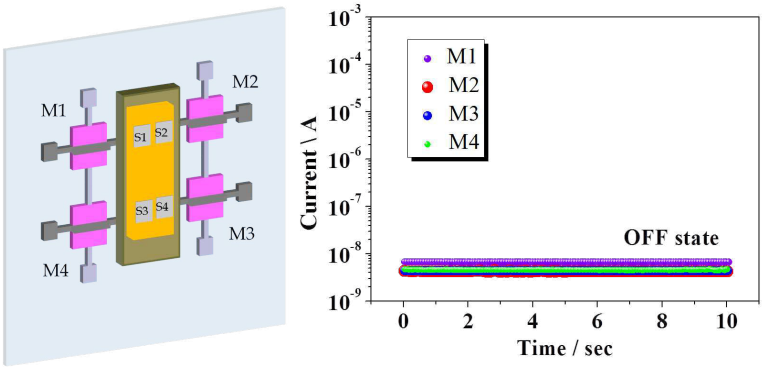


Figure 6.9: Schematic representation of the 2×2 array and electrical behaviour of the four memory elements in the OFF state. The current flowing in each ME has been measured at V_{READ} = 0.2 V.

Supposing that the programming voltage V_{SET} is applied to the whole system, when pressure is applied on a specific area (the dark pink one in Figure 6.10)) the resistance of the rubber film drops down only in the deformed area, which corrisponds to a specific memory (M1). Therefore, only M1 can be written during the process. Indeed, as it can be observed from electrical measurements, only M1 switches to the low resistive state (ON state), showing a much higher output current. Similarly, if pressure is applied only to the area S4 close to the memory M4, this element switches to the OFF state (Figure 6.11). M2 and M3, as well as M1, do not show any variation of their output current, indicating that the writing process took place only in the devices on which pressure was applied.

6.5.4 4x4 array and demonstrator

In order to demonstrate the feasibility of the proposed techonology to more complex applications, where spatial resolution and multi-bit storage are required, a 4×4 a pressure-triggered memory array has been designed, fabricated and tested. The layout, shown in

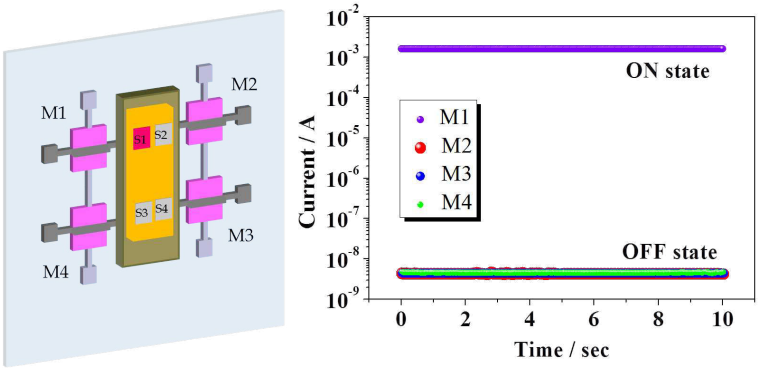


Figure 6.10: Electrical response of the memory element M1 induced by the application of an external mechanical stimulus (mechanical writing). The current flowing in each ME has been measured at V_{READ} = 0.2 V.

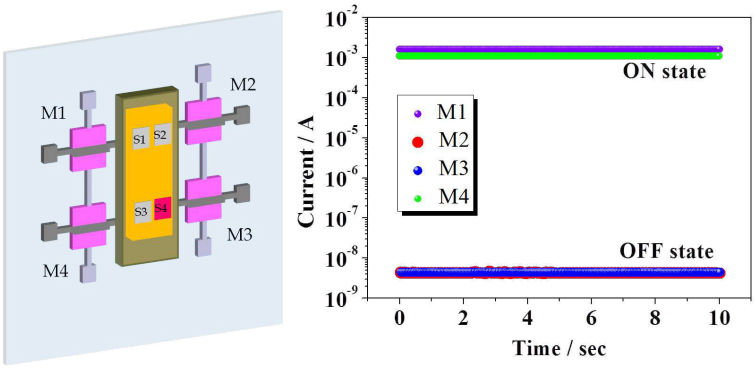


Figure 6.11: Electrical response of the memory element M4 induced by the application of an external mechanical stimulus (mechanical writing). The current flowing in each ME has been measured at V_{READ} = 0.2 V.

Figure 6.12, was mainly conceived for a system where a basic shape insisting on the rubber can be memorized.

The developed 16-pixel memory/sensor system has been successfully employed for the memorization of different shapes, like alphanumerical characters and geometrical figures. In particular, tests were carried out by means of custom-made letter shapes, fabricated with a 3D printer (Makerbot Replicator 2X). Each letter is made out of a common thermoplastic polymer, namely Acrylonitrile Butadiene Styrene (ABS). The shapes were designed with a protrusion in corrispondence of each pixel, thus acting as an indenter for the pressure application. For istance, Figure 6.13 reports the spatial map

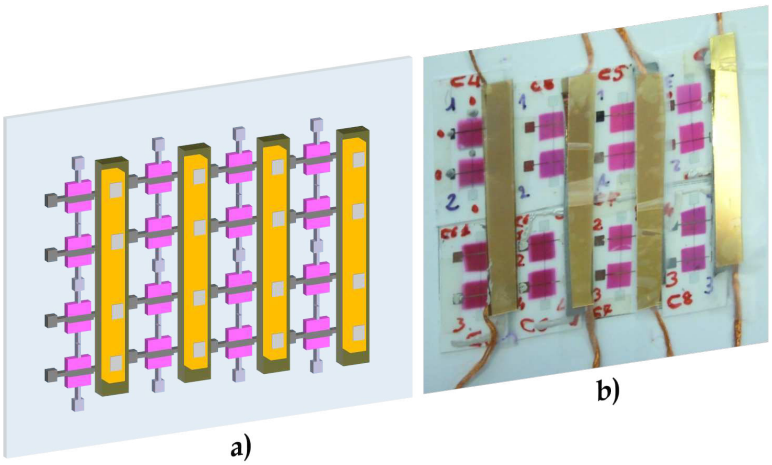


Figure 6.12: a) Layout and b) picture of the pressure-triggered memory array.

of system output showing the shape of the letter *N*. Specifically, 6.13 a) shows a schematic representation of pressure application: red squares correspond to the points where the protrusions of the shape insist on the rubber. In Figure 6.13 b) an actual picture of the *N* shape insisting on the system is reported. Finally, Figure 6.13 c) depicts the average current levels of each memory element according to the position in the array system, after the writing process. Importantly, all the memory elements were reset to their OFF state, before the programming. This operation was performed applying simultanously the V_{SET} and the pressure to the whole system. Only memories corresponding to the points where the indenter insisted were written, thus memorizing the *N* shape. Interestingly, although the pressure was applied by hand, i.e. with a relatively low force, memories switched to their ON state. Moreover, it was obtained a minimum I_{ON}/I_{OFF} ratio of 10^3, larger enough for a easy recognition of the shape, as clearly shown in Figure 6.13 c).

Finally, in order to evaluate the functionality of all the devices in the system, and to demonstrate that it can be programmed several times without any loss of functionality, the letters of the University of Cagliari acronym, UNICA, were memorized. Figure 6.14 reports a picture of the employed indenters and the corrisponding output of the system. Each shape was fabricated in the same way of the letter N employed in the previously presented characterization. Although each memory element was reset to the OFF state before every shape memorization, I_{ON}/I_{OFF} ratios larger enough for a unmistakable recognition of the letters were recorded (minimum of

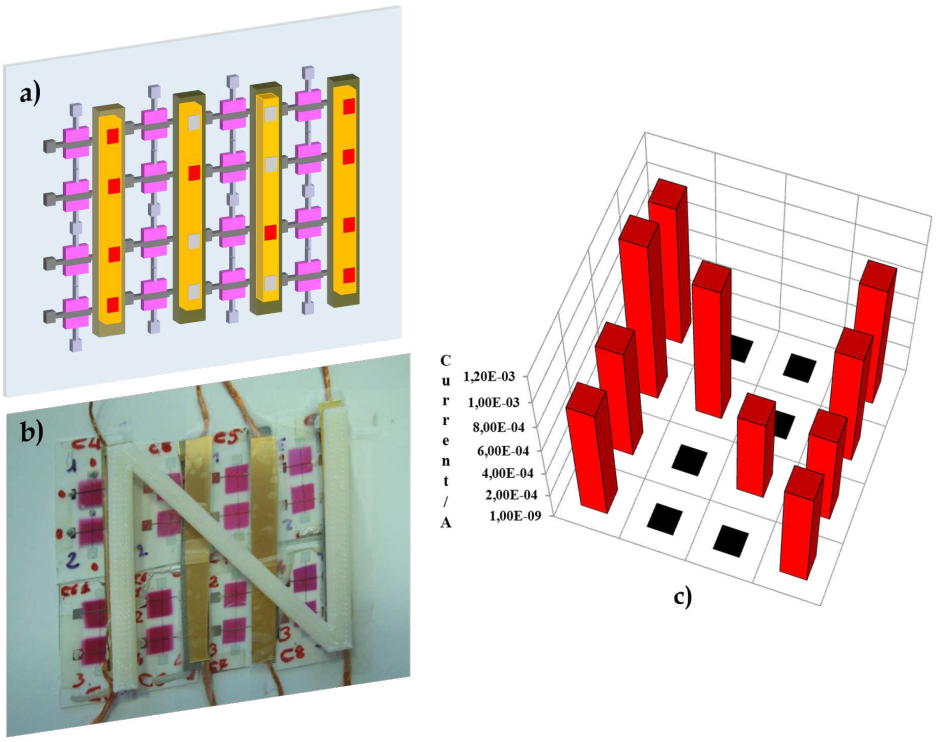


Figure 6.13: a) Layout and b) picture of the pressure-triggered memory array for the memorization of the character *N*. c) Representation of the current levels of the array, demonstrating the correct memorization of the shape.

10^3). Interistingly, the I_{ON} of each device involved in different writing processes during the experiments results substantially the same, demonstrating that the system is able to be cyclically employed for several tests without loss of functionality.

6.6 Conclusions

In conclusion, the suitability of organic non-volatile memory devices for the detection and the storage of external parameters was demonstrated. In particular, it was shown that if integrated with devices sensitive to an external stimulus, memory elements change their state depending on the presence of the stimulus. As prototypical example, flexible arrays of mechanically switchable memory elements system were designed, fabricated and characterized. These results definitely demonstrates the feasibility of the proposed technology for the fabrication of systems including organic memories

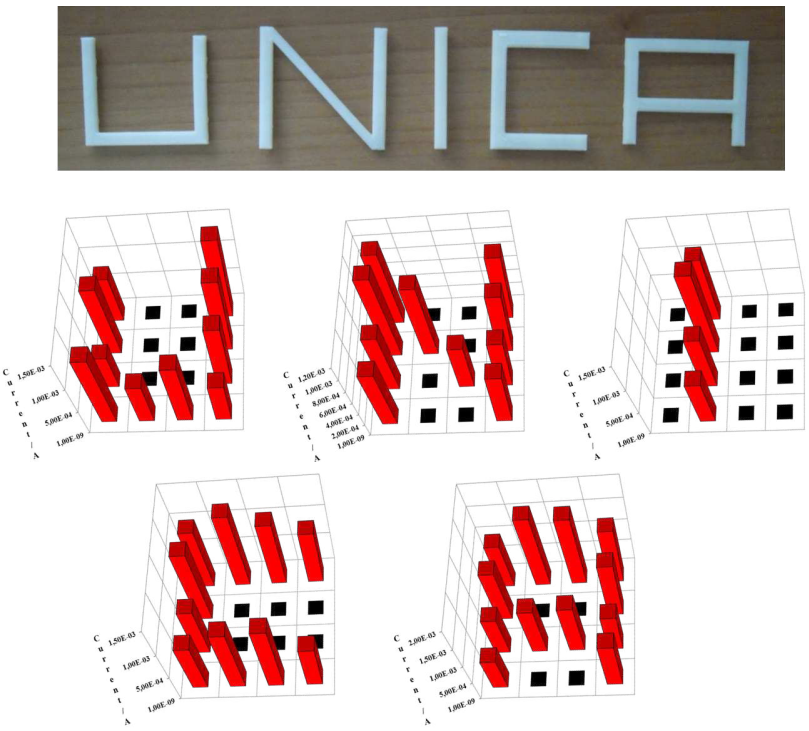


Figure 6.14: Application example: memorization of acronym UNICA. On the top a picture of employed indenters, on the bottom corrisponding output current levels of the memory elements in the system .

for their final application in different industrial processes, including e-textile and smart packaging.

Part IV

Non-volatile organic transistor memories

7 OFET-BASED MEMORIES

Contents

7.1 Introduction

As reported in Chapter 2, in the last years an increasing attention has been payed to OFET-based memories. Even if several significant step forwards have been recently reported in literature, organic transistor-based memory performances are still not satisfactory. This can be related to several aspects which need to be explored:

- organic transistor are generally high voltage devices, i.e. they need tens of volts to be operated; even if several examples of low voltage transistors have been reported so far in literature, a suitable fabrication process for flexible electronics and easily up-scalable to the industrial size are still missing;
- programming voltages required for a reliable data storage are generally high, even for low voltage transistor structure;
- memory performaces, such as retention time and endurance to

memory cycling, are still far for being satisfactory, and actually feasible for pratical applications.

As a consequence, nowadays, a significant effort is devoted to overcoming such limitations, thus paving the way to the employment of OFET-based memory devices in operational environment. As a part of the Ph.D. research activity here described, the design, fabrication and characterization of transistor-based memories has been carried out in collaboration with Dr. Piero Cosseddu, which was the main responsible for such task. In the following, a basic description of device structures and layout, working principle and performances will be reported.

7.2 Device structure: low voltage OFETs

In 2012, Cosseddu *et al.* [133] reported a novel, highly reliable procedure for the fabrication of low voltage OFETs, particularly conceived for an easy up-scalability to an industrial size. The core of such a novel device structure (`Figure 7.1 a)`) is represented by a ultra-thin, hybrid organic/inorganic dielectric layer, composed by the innovative combination of two well-known and highly diffused materials, namely aluminum oxide and Parylene C. Aluminum oxide is one of the most diffused inorganic oxides for the fabrication of OFETs: it can be directly grown in nanometrical films on aluminum layers by means of several techniques, including plasma, ozone or electrochemical oxidation, or deposited in different ways including sputter coating and atomic layer deposition. Thanks to the significantly high electrical permittivity ($8 \div 10$), aluminum oxide can be used for obtaining high gate capacitances, thus allowing the low voltage operation of the transistor. Nevertheless, the employment of aluminum oxide for the reliable fabrication of low voltage OFETs is not trivial: aluminum oxide is not pinhole free, thus impeding its employment for large area production. Moreover, chemical groups covering its surface acts typically as charge trapping centers, affecting seriously the device performances. Cosseddu *et al.* demonstrated that coating aluminum oxide with an ultra thin Parylene C layer allows obtaining a pinhole free insulating layer, where trap sites are completely buffered. Parylene C can be deposited in nanometrical films on relatively large areas by meas of Chemical Vapor Deposition (CVD), which can be performed at room temperature, thus being suitable for plastic electronics. Thanks to Parylene C coating, nanometrical aluminum oxide obtained by low cost techniques, such as direct oxidation of the aluminum gate by means of UV-produced ozone in ambient condition, can be used for the reliable fabrication

of low voltage OFETs. Figure 7.1 b) reports a Trasmission Electron Microscopy (TEM) cross section image, showing the aluminum oxide and the Parylene C layers composing the hybrid, nanometrical dielectric. Figure 7.1 c) and d) shows the output and transfer characteristic curves of a low voltage transistor, fabricated using 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS pentacene) as organic semiconductor. From these curves, quasi-ideal transistor performances can be observed: low leakage current (I_g), negligible hysteresis, threshold voltage lower than 1 V, significant field-effect and good saturation. Interestingly, the authors reported a process yield of about 90% in non optimized conditions, which is promising for future industrial scalability.

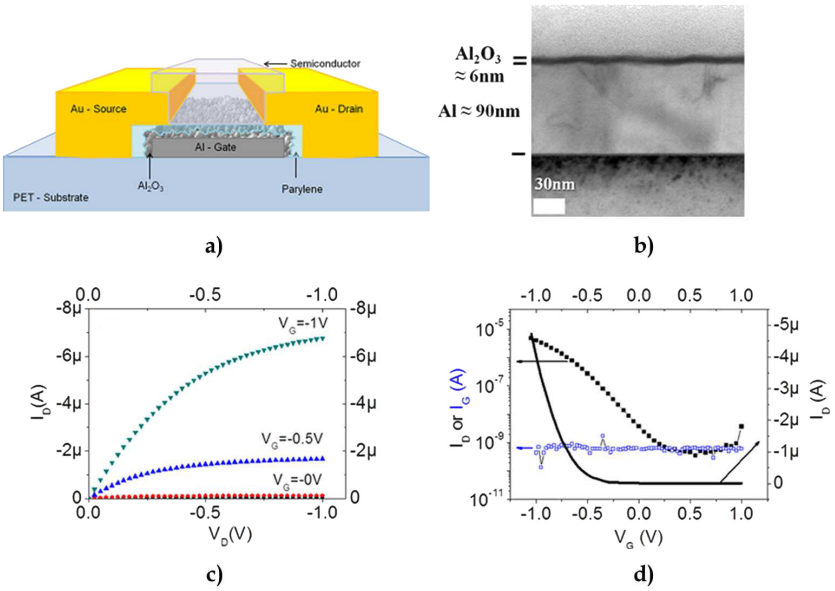


Figure 7.1: a) Basic structure of the low voltage OFET; b) SEM image of the aluminum oxide and Parylene C dielectrics, determining the ultrathin, hybrid gate insulator; c) output and d) transfer characteristic curves of the low voltage devices [133].

7.3 Low voltage OFET-based memories

The TEM image in Figure 7.1 b) shows how aluminum oxide and Parylene C form a substantially stacked structure. Therefore, these materials can theoretically act as blocking dielectric and electrect in a charge trapping memory device, being the electrical permittivity of Parylene C (3.15 at 60 Hz) lower than the one of aluminum

oxide. Since the basic device structure is bottom gate/bottom contact, in a hypothetical memory measurement, a sufficiently high gate-source voltage drop could allow charge carriers from the channel, or, alternatively, from source/drain contacts, to tunnel through the Paylene C layer. Such a charge would be consequently stored at the interface between Parylene C and aluminum oxide, thus acting as fixed charge in the hybrid dielectric and determining a shift in the theshold voltage.
In order to explore the actual functionality of the low voltage transistors reported in Cosseddu *et al.* as memory devices, and consequently determining their working principle and performances, a custom layout was designed, several devices has been fabricated and tested. In the following, the fabrication process will be reported, and a complete electrical characterization will be provided.

7.4 Device layout and fabrication

In order to provide a consistent platform for testing the OFET functionality as memory device, a custom layout, shown in `Figure 7.2`, was designed. Each substrate ($5 \times 3.5\ cm^2$) hosts six low voltage transistors, which can be independently biased, thus preventing any possible cross-talk during the measurements. In order to provide a reproducible probing of the devices during the characterization process, the layout was provided with a flat connector, to be inserted in an suitable connector. More details will be provided in the experimental setup description.

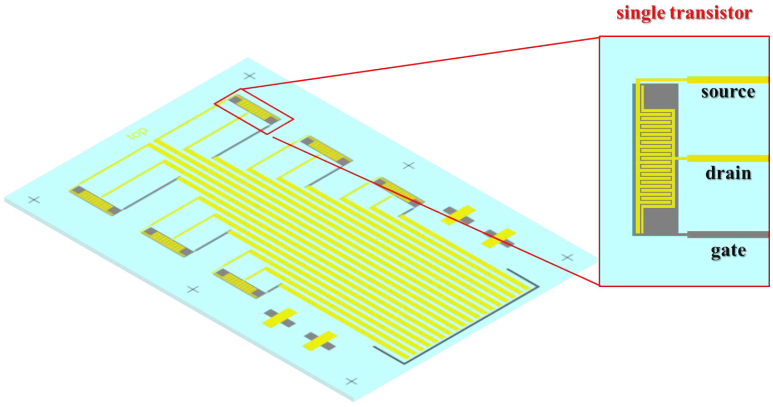


Figure 7.2: Layout of the fabricated devices. The inset shows a particular of the single transistor structure.

All the substrates have been fabricated on a 175 μm-thick PET foil.

Prior any fabrication step, a basic cleaning procedure (subsequentely rinsing with acetone, isopropyl alchool and deionized water) was carried out. The gate electrodes were obtained by photolithographic patterning of an unique aluminum layer, thermally evaporated onto the PET substrate. The pattern, consisting on the different gate structures and basic alignment marks necessary in the further steps, was reported using a positive photoresist, deposited by means of spin coating and dried in oven at 40 °C for half an hour. After the exposure to UV light and the development of the pattern by means of a 175 mM solution of sodium hydroxide in water, the excess of aluminum was removed by means of a 0.5 % in volume of hydrofluoridric acid. The result of the photolithographic procedure is reported in Figure 7.3 c). The surface oxidation of the aluminum gates was performed by 1 hour exposure to ozone, produced by a UV-lamp (UVP Penray) generating a 185 nm radiation. Afterwards, a 40 nm thick Parylene layer was deposited by CVD using a Parylene Deposition System Labcoater2 (Specialty Coating Systems). The final gate capacitance is of about 35 $nFcm^{-2}$. Source and drain electrodes were fabricated within the flat connector by a photolithographic process of an unique gold film, deposited by means of thermal evaporation. The process is the same described for the aluminum, except for the chemical etching, performed by a solution of potassium iodide and iodine in water (1 : 4 : 40 in weight). A picture of the completed device is shown in Figure 7.3 g). 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS Pentacene) was employed as organic semiconductor. In particular, it was deposited from liquid phase (0.5% in weight in toluene) by drop casting. After deposition, the substrate has been annealed for 30 minutes at 90 °C in order to remove any residual solvent and to improve the crystallinity of the film.

7.5 Electrical characterization

7.5.1 Experimental setup

As previously mentioned, the substrate hosting the low voltage transistors is provided with a flat connector which allows a reliable probing of the devices. The measurement setup is completed by a custom made Printed Circuit Board (PCB), hosting a 18-wire ZIF connector and 18 pins for allowing the connection with standard probes. A picture of the substrate connected to the PCB is shown in Figure 7.4. The characterization was carried out by means of Keithley 2616/2636 source meters, controlled by custom made Matlab® graphical interfaces.

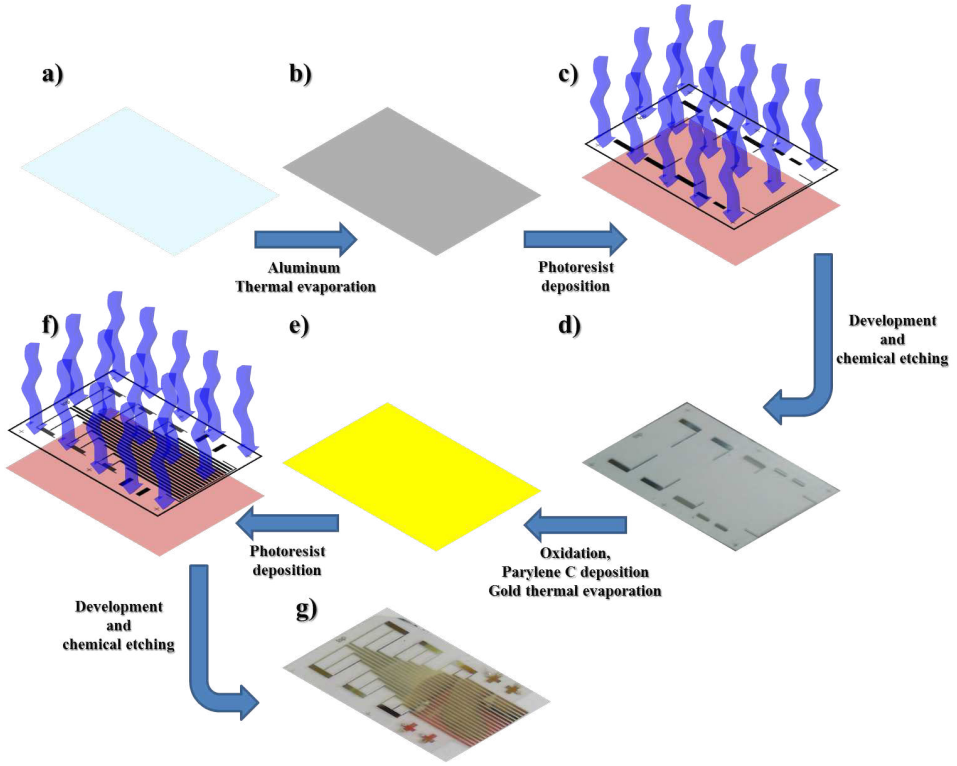


Figure 7.3: Schematic representation of the fabrication process.

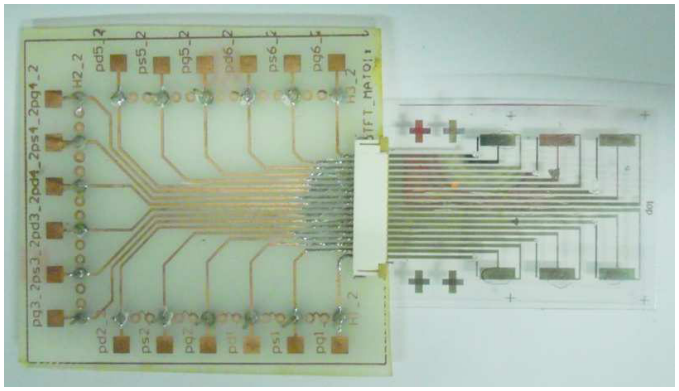


Figure 7.4: A completed device connected to the PCB fabricated for the electrical characterization.

7.5.2 Working principle and programming tests

In order to characterize the devices as memory elements, single V_{GS} pulses (in the following, V_{prog}) with a duration of 10 ms were

applied, keeping V_{DS} at 0 V. At first, negative V_{prog} of different amplitudes were employed, varying from -5 V to -25 V.
It is noteworthy that, thanks to its remarkable breakdown field (3 $MVcm^{-1}$), the ultra-thin dielectric layer can resist to significantly high gate voltages. For instance, V_{prog} = –25 V corresponds to an induced gate field of -7 $MVcm^{-1}$. The application of such high field for a very short time (10 ms) does not damage the hybrid dielectric, despite the fact that this value is higher than the recorded breakdown voltage. An irreversible breakdown of the dielectric was only observed for longer application of programming voltage pulses, usually giving rise to an irreversible breakdown of the dielectric.
Interestingly, a negative V_{prog} always induced a shift of the transistor threshold voltage towards more negative values. However, some marked differences have been observed with different V_{prog} amplitudes. Indeed, if $0 < V_{prog} < -10$ V, very small threshold voltage shifts has been observed (in the range of $-0.3/-0.4$), as shown in `Figure 7.5 a)`. Increasing the pulse amplitude up to -15 V (`Figure 7.5 b)`), a much more pronounced shift of the threshold voltage was induced (in average close to -1 V and).

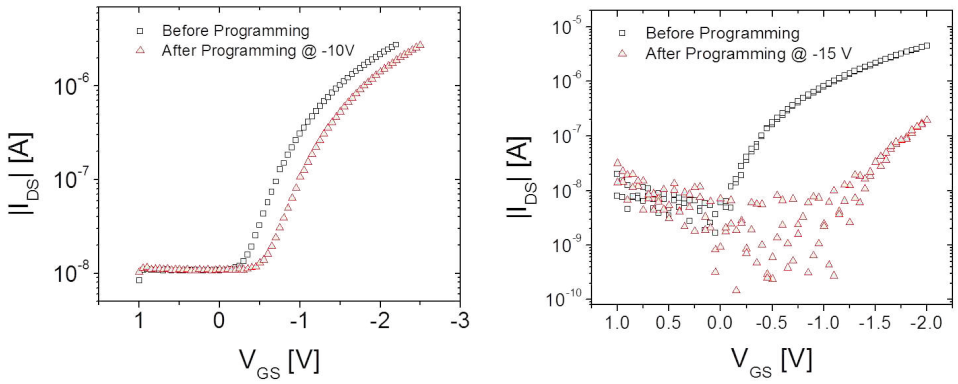


Figure 7.5: Threshold voltage shift obtained by the application of a single voltage pulse a) V_{prog} = -10 V and b) V_{prog} = -15 V.

When positive V_{prog} of the same amplitudes were employed on pristine devices (never programmed before), no significant shift of the threshold voltage has ever been observed. As previously observed by other groups [68, 69], this trend possibly demonstrates that, when a negative pulse is applied to the gate, positive charges are trapped within the Parylene C film or at its interface with the aluminum oxide (`Figure 7.6 b)`). In this case, the aluminum oxide film could act as a blocking layer, thus impeding the injected charges to move

towards the gate electrode. Consequently, the trapped charges could act as fixed charges, thus inducing a marked shift of the threshold voltage towards higher negative values. On the contrary, when a positive pulse is applied, due to the very poor concentration of free electrons in the p-type semiconductor, no significant amount of negative charge can be trapped. It is noteworthy that, as shown in Figure 7.6 d), when a high, positive V_{prog} is applied to a transistor previously programmed with a negative V_{prog}, the threshold voltage shifts back to its previous state. Again, this behavior supports the idea of a memory behavior induced by trapping and de-trapping of a positive charge: positive V_{prog} can push back the charges in the channel of the device, thus resetting the threshold voltage shift (Figure 7.6 c)).

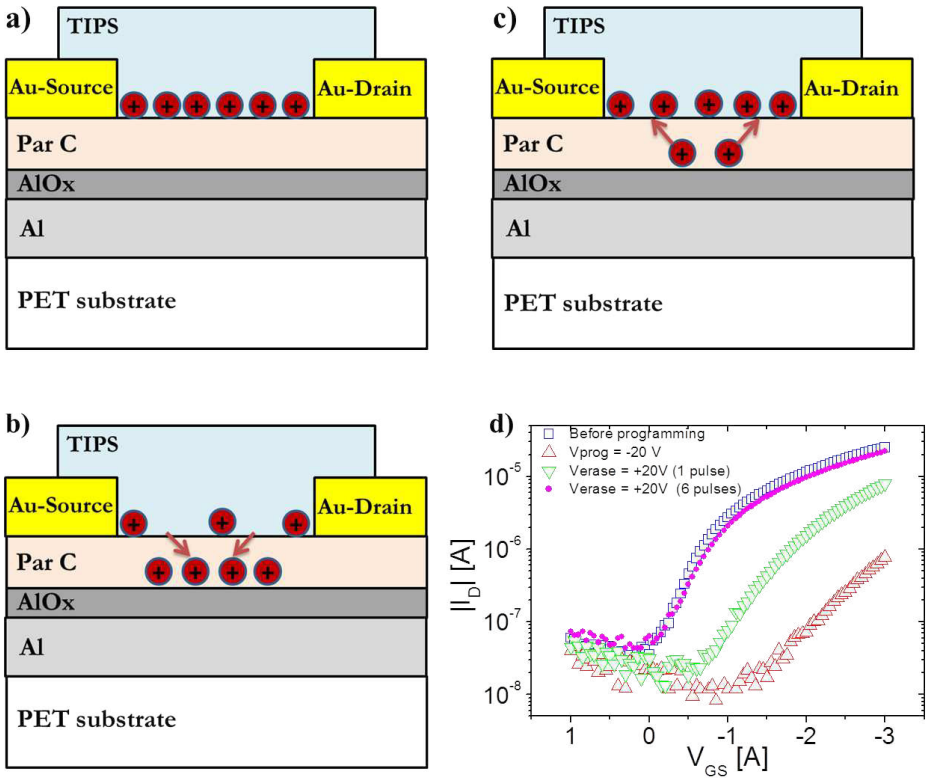


Figure 7.6: a) Charge distribution in the channel of a pristine device; b) programming (writing) process; c) erasing process; d) example of resetting of the threshold voltage by the application of positive V_{prog} pulse.

The reported tests demonstrate that the memory elements can be written (negative V_{prog}) or erased (positive V_{prog}) in a reproducible way.

However, the erasing process requires the application of at least 6 consecutive positive pulses (duration 10 ms) of the same amplitude in order to have a complete resetting of the memory.

7.5.3 Memory performances

As basic parameter for evaluating the actual functionality of non-volatile memory devices, the retention time of the low voltage OFET-based devices was investigated. In particular, the retention time was evaluated as function of the negative V_{prog} by monitoring the threshold voltage shift in time after the programming process. For instance, the progressive absorption of the threshold voltage variation is shown in `Figure 7.7 a)` for $V_{prog} = -15$ V and $V_{prog} = -25$ V. An exponential decay of the threshold voltage shift can be observed in both cases. No significant differences in the relaxation time can be derived for the curves, coherently with the fact that the charge de-trapolation is probably a function of the Parylene C layer thickness. Generally, the higher the initial threshold voltage shift, the higher is the retention time: this evidence is depicted in `Figure 7.7 b)`, where these two parameters are plotted as function of V_{prog}. As already observed in `Figure 7.5`, the higher V_{prog}, the higher $|\Delta V_{TH}|$; consequently, a higher retention time was obtained. In particular, a maximum of 3×10^5 s (83 hours) has been recorded for $V_{prog} - 25$ V, which determined a threshold voltage shift of about 1.7 V.

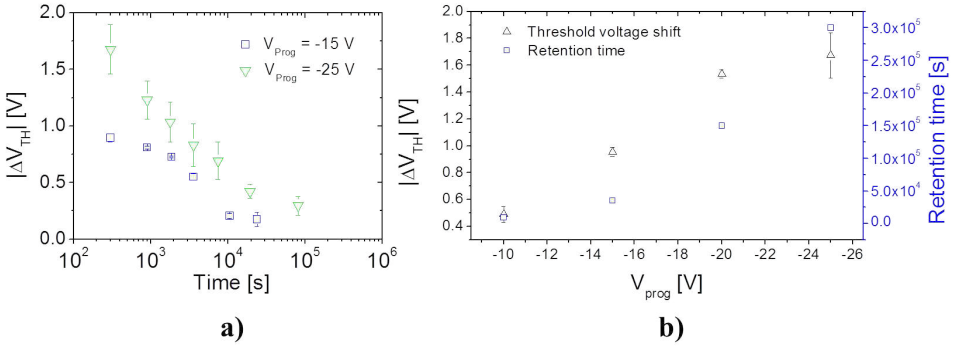


Figure 7.7: a) Relaxation of the threshold voltage shift in time for two different programming voltage, namely $V_{prog} = -15$ V and $V_{prog} = -25$ V; b) absolute value of the threhsold voltage shift and related retention time as a function of V_{prog}.

In order to test the durability of the fabricated memory elements, endurance cycles have been also performed. The following procedure was applied:

- the memory is written by applying a negative programming voltage;
- the memory is read by measuring the output current at a constant voltage $V_{DS} = -2$ V and $V_{GS} = -1$ V;
- the memory element is erased by applying a series of positive pulses;
- the memory is read by measuring the output current at a constant voltage $V_{DS} = -2$ V and $V_{GS} = -1$ V.

The results, reported in Figure 7.8, clearly demonstrate that the memory elements can be written/erased more than 100 times without significant loss.

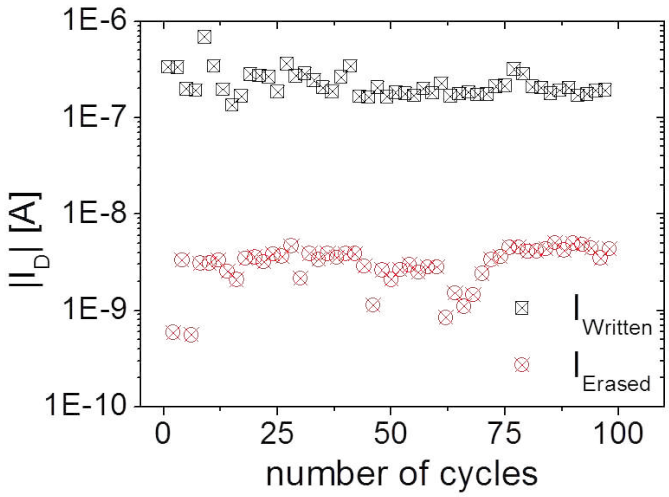


Figure 7.8: Write/erase endurance cycle test as a function of the number of programming cycles.

7.6 Ultra-flexible OFET-based memories

As already discussed in Chapter 4, the application of organic memory devices in flexible electronics represents a natural exploitation of the potentialities of organic technology. In the case of transistor based memories, the influence of mechanical deformation on the device performances must be taken into account. As demonstrated by several groups [134], the mechanical deformation of the flexible

substrate can bring to a surfacial strain and to a consequent variation of the charge carrier mobility in the active layer, related to the dislocation of the crystalline domains. The sensitivity to mechanical deformation can be related to several aspects, comprising active layer morphology [135] and substrate thickness. In particular, the thicker the substrate, the higher the sensitivity of the transistor to mechanical deformation. Obviously, a transistor-based memory device suitable for flexible electronics applications should be insensitive to surface strain.

According to these considerations, the possibility of fabricating ultra-flexible memory elements, using the previously described approach, was evaluated by transferring the fabrication process on ultra-thin substrates. In particular, the hybrid dielectric-OFETs was fabricated on a 13 μm thick Kapton® substrate. Since the induced surface strain is directly proportional to the thickness of the substrate, using such a thin substrate allows bending the devices to very small bending radii without reaching significant levels of strain [136]. The fabrication procedure is equivalent to the one reported before. The main difference is that single devices was fabricated on every substrate in order to allow an easier and more consistent mechanical characterization of the devices.
At first, the behavior of a non-programmed transistor was analyzed (Figure 7.9 a) and b)). This was done with the aim of identifying the minimum value of bending radius able to induce an effect in the transistor behavior. For this reason, the transfer characteristic curves were recorded before, during and after each bending step. Interestingly, the device electrical characteristics resulted very stable and reproducible even when the device is bent around a cylinder with a radius of 150 μm (see Figure 7.9 a)). Moreover, mechanical stress tests was performed by bending the devices at the smallest bending radius 1000 times. As it can be observed from Figure 7.9 b), the device characteristics are very stable during the first 500 cycles, with a very small reduction of the mobility (less than 10%) and a very slight shift of the threshold voltage towards more positive values (less than 0.1 V). A slightly higher degradation was observed after 1000 cycles, with a further reduction of the device mobility (around 15%) and more pronounced shift of the threshold voltage (around 0.5 V). We assume that this effect could be mainly related to an early degradation, and oxygen doping, during the whole device characterization, which was performed in ambient atmosphere with a duration of more than 5 hours. However, it is possible to notice that the transistor functionality is not compromised and that the threshold voltage shift induced by the mechanical stress is much smaller than that induced in the programmed memories. In order to further

prove this, the same procedure was then applied to programmed memory devices, and their retention capability was monitored during and after several bending cycles at $R = 150\ \mu m$, corresponding to a surface strain of 0.3%. This value was estimated by considering that, for such small bending radii, only a very small fraction of the device active area ($5 \times 5\ mm^2$, less than 10%) is deformed. Interestingly, even after 200 cycles the memory device is still quite stable in the programmed state (`Figure 7.9 c)`).

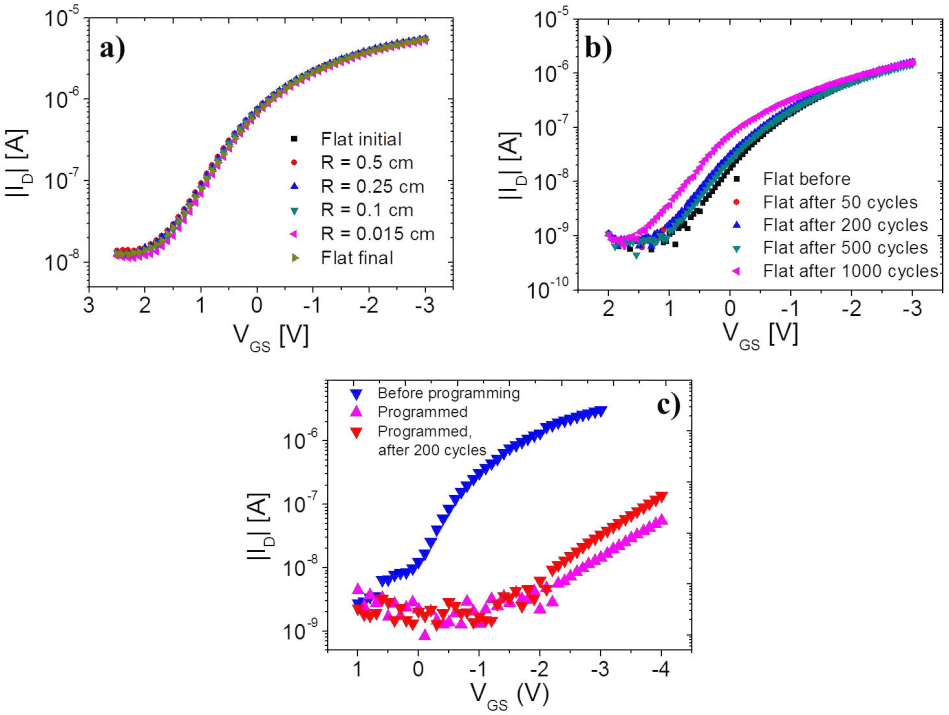


Figure 7.9: Transfer characteristics of OFETs fabricated on ultrathin Kapton® substrate a) recorded at different bending radii; b) after cycled mechanical deformation at $R = 150\ \mu m$; c) before, after programming and after cycled mechanical deformation at $R = 150\ \mu m$.

To better characterize the retention capability of the memory devices, a much higher surface strain was employed. Therefore, memory devices were fabricated on 175 μm thick PET films. These devices were firstly programmed and then bent 200 consecutive times at a bending radius of 0.5 cm, which corresponds to a surface strain of about 2%. This value was chosen because recently Cosseddu *et al.* demonstrated that this is the upper deformation limit sustainable by OFETs [135] fabricated with these architecture and materials, without causing an irreversible modification of the electrical properties.

The results reported in Figure 7.10 clearly show that the charges stored into the hybrid dielectric film are stably trapped and the data retention is not influenced by mechanical deformation.

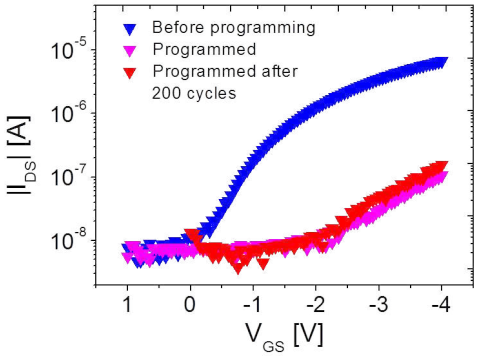


Figure 7.10: Transfer characteristics of OFET memories fabricated on a 175 μm thick PET substrate, before and after programming, and after cycled mechanical deformation for a strain of about 2%.

7.7 Conclusions and outlooks

In this chapter, a novel transistor structure to be employed as non-volatile memory devices has been presented. The main novelty of such a device is represented by a ultra-thin (around 40 nm), hybrid organic/inorganic dielectric, composed by aluminum oxide and Parylene C, which can be fabricated over relatively large area with a high reliable process easily up-scalable to an industrial size. The stacking of such dielectrics, which have a significantly different electrical permittivity, allows the exploitation of a charge trapping mechanism for a non-volatile data storage in terms of threshold voltage modulation in the transistor.
Several devices have been fabricated and tested over different substrates and employing different layouts. The reported tests show that, using a p-type organic semiconductor as the active layer, negative voltage pulse applied to the gate can determine a significant shift of the threshold voltage through more negative values, thus switching off the device. The initial threshold voltage can be restored by applying several positive voltage pulses to the gate. Since negative voltage pulses applied to pristine devices does not determine significant threshold voltage shifts, the trapping of positive charges was identified as working principle behind the memory effect. The retention capability was tested and correlated to the amplitude of the programming voltage pulses: retention times up to 3×10^5 s

were measured. Moreover, the memory devices were programed and erased several time without any significant loss of functionality.
Finally, several devices were fabricated on ultra-thin substrates in order to demonstrate the feasibility of the proposed technology to those application where conformability and high flexibility are required, such as smart packaging and wearable electronics. In particular, it was demonstrated the device capability of retain the memory even if it is bent at significantly low radii (as low as 150 μm).
The activity on transistor-based memory devices is still ongoing, as several aspects still need to be investigated. Indeed, even if the transistor structure can be operated at low voltages, programming pulses as high as -25 V are needed to have valuable retention time, thus significantly affecting the portability of the devices. Several optimization in the transistor structure can be hypothesized in order to reduce operating voltages and/or increase the retention time for a given programming voltages. Moreover, a deeper insight on the working principle is needed to determine further possible optimization of the device performances. To this aim, preliminary tests on the oxygen influence on the memory performances, and characterization of n-type transistor memories are currently ongoing.

Part V

Conclusions

The Ph.D. research activity described in this manuscript was focused on the study, design, fabrication and characterization of new non-volatile memory elements based on organic electronics. In particular, the activity was mainly carried out in the frame of the European project "HYbrid organic/inorganic Memory Elementsfor integration of electronic and photonic Circuitry" (HYMEC), which involved the University of Cagliari during the last three years. The project goal was to realize new hybrid inorganic/organic resistive memory devices with functionality far beyond the state of the art. Specifically, the research aimed at understanding and controlling all relevant properties of systems comprising inorganic metal nanoparticles embedded in matrices of organic materials. The electronic, optical, dielectric, structural, and morphological properties of systems were determined using state of the art experimental techniques in order to establish a reliable specific knowledge base for device fabrication and integration.
During the Ph.D. research activity, a novel non-volatile hybrid organic–inorganic memory structure has been developed. A commercially available, environmentally stable, n-type organic semiconductor, namely $ActivInk^{TM}N1400$, was employed for the first time ever as organic matrix in memory devices. The presented work clearly demonstrates the suitability of such a material in the fabrication of resistive memory elements. At first, devices fabricated on glass substrates were fabricated, employing two different metal NPs as intermediate layer. In Au NPs based memories, a retention time of at least ten months was reproducibly demonstrated for devices tested and stored in ambient conditions for sixteen months in total; in addition, after this time, the functionality of the devices in terms of writing, reading and erasing resulted perfectly maintained. These performances are the best reported so far in literature; it is also noteworthy that, to our knowledge, the statistic analysis is the largest ever reported for organic-based RRAMs. Devices employing Al NPs resulted less stable, showing a shorter retention time, but their performances are still absolutely competitive with the state of the art. These results suggest that environmental stability of both organic and inorganic materials is needed for obtaining reproducible and stable memory effects. The proposed structure was thoroughly characterized by morphological techniques, which clearly evidenced the top electrode material diffusion inside the organic layer. Resistive switching mechanisms in this material can thus be interpreted in terms of formation and rupture of metallic filaments inside the organic layer assisted by the metal NPs.
The developed technology was then successfully applied on flexible PET substrates. In particular, at the moment only devices incor-

porating Al NPs have been studied and results are very similar to the previous on glass substrates. Interestingly, higher retention times (1.5×10^7 s) were recorded with flexible Al NPs based memory. Further investigations are in progress in order to achieve a full comprehension of the degradation mechanisms for Al NPs and to increase the device reliability.

The definition of technological processes for the reliable fabrication of high performance printed organic memory devices was also investigated. In particular, it was studied the possibility of fabricating memory devices based on a printed blend made out of N1400 and Au NPs in anisole. The influence of Au NPs concentration in terms of resistive switching was thoroughly analyzed: 2 out of 5 ink recipes allow the fabrication of devices with promising results, comparable with the thermally evaporated N1400 based devices. As already found for these memory elements, the presence of NPs seems to be essential for determining the resistive switching. This work clearly demonstrates the real possibility of fabricating high performace printed memory elements. Further investigations are in progress in order to optimize the fabrication process towards a fully printed memory elements array. In particular, the inkjet printing of both bottom and top electrodes can be foreseen. Moreover, a thorough testing on endurance and retention time is still missing, and will be carried out as soon as the fabrication process will be fine-tuned.

A significant effort was also devoted to the development of basic memory/sensor systems entirely fabricated on plastic substrates. The suitability of organic non-volatile memory devices for the detection and the storage of external parameters was demonstrated. In particular, it was shown that if integrated with devices sensitive to an external stimulus, memory elements change their state depending on the presence of the stimulus. As prototypical example, flexible arrays up to 4x4 of mechanically switchable memory elements system were designed, fabricated and characterized. The results definitely demonstrated the feasibility of the proposed technology for the fabrication of systems including organic memories for their final application in different industrial processes, including e-textile and smart packaging.

Finally, a complementary activity on three-terminal organic memory devices was carried out. Specifically, highly flexible OTFT-based memory elements with excellent mechanical stability and high retention time were developed. The devices were fabricated using a combination of two ultrathin dielectric layers, namely aluminum oxide and Parylene C. The stacking of such dielectrics, which have a significantly different electrical permittivity, allows the exploitation of a charge trapping mechanism for a non-volatile data storage in terms

of threshold voltage modulation in the transistor. Retention times up to 3×10^5 s were recorded, and memory devices were programmed and erased several times without any significant loss of functionality. An electromechanical characterization demonstrated that such memory elements can be cyclically bent around a cylinder with a radius of 150 μm without losing the stored data. The activity on transistor-based memory devices is still ongoing, as several aspects still need to be investigated. Indeed, even if the transistor structure can be operated at low voltages, programming pulses as high as 25 V are needed to have reasonable retention times, thus significantly affecting the portability of the devices. Several optimizations in the transistor structure can be hypothesized in order to reduce operating voltages and/or increase the retention time for a given programming voltage. Moreover, a deeper insight on the working principle is needed to determine further possible optimizations of the device performances.

Part VI

Appendixes

A

Materials and Methods

Contents

A.1 Introduction

In this appendix, a deeper insight on materials and methods employed during the Ph.D. research activity will be provided. In particular, in the first section, the main physical and chemical properties of materials employed for fabricated devices are reported. To the reader convenience, materials will be divided into *substrates*, *conductors*, *semiconductors* and *insulators*. Moreover, for each material, a reminder about its actual usage in the fabrication of devices described in the manuscript will be also given. Afterwards, the second section comprises a description of the methods employed for the fabrication and characterization of the devices.

A.2 Materials

A.2.1 Substrates

Glass

Glass is an amorphous solid material, which is often transparent and has widespread usage in electronics, especially in optoelectronics. Glass provides good chemical resistance, form stability, even at increased temperatures and superior clarity. The specific properties of glass make it a suitable substrate for carrying electroconductive layers in electric or semiconductor devices such as flat panel displays, electroluminescent panels, cathode ray tubes (CRTs), photovoltaic cells, etc. However, its high specific weight, brittleness and low flexibility are the main problems associated with the use of glass as substrate in electric or semiconductor devices.
In the research activity described in the manuscript, ITO-coated glass substrates has been used for the fabrication of memory devices.

PET

Polyethylene terephtalate (PET) is a thermoplastic resin of the polyester family. It consists of polymerized units of the monomer ethylene terephthalate, with repeating $C_{10}H_8O_4$ units (`Figure A.1`). PET is dimensionally stable, presents a good chemical resistance (except to alkalis, which hydrolyse it), and it is highly transparent when in thin films. Thanks to these characteristics, it is widely used as substrate for organic electron devices.
In the research activity here reported, PET was employed for the fabrication of flexible memory devices, both resistive and transistor. In the specific case of RRAMs, ITO-coated PET has been employed.

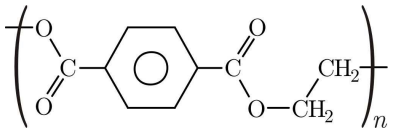


Figure A.1: Chemical structure of PET.

Kapton®

Kapton® (poly(4,4'-oxydiphenylene-pyromellitimide)) is the brand name of a polyimide film, which was first developed by DuPont. It is

widely used in flexible electronics as substrate for flexible printed circuits and in aerospace. It is well known for its excellent high temperature properties and radiation resistance, inherently low flammability and smoke emission, low creep and high wear resistance. Kapton films are usually transparent amber coloured if thinner than 125 μm, and can remain stable in a wide range of temperatures, from -270 °C to 320 °C.
During the research activity, 13 μm thick Kapton® substrates were used for the fabrication of conformable OFET-based memory devices.

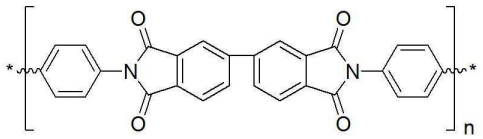


Figure A.2: Chemical structure of Kapton®.

A.2.2 Conductors

Indium Tin Oxide (ITO)

Indium Tin Oxide (ITO) is a compound of indium oxide (In_2O_3) and tin oxide (SnO_2). In particular, tin oxide acts as dopant for indium oxide; the compound (generally 90 % In_2O_3 : 10 % SnO_2) shows a good electrical and thermal conductivity. Moreover, ITO is transparent when deposited in thin films ($1000 \div 3000$ Å). The typical deposition and patterning procedures are compatible with several kind of substrates, both organic and inorganic. These properties made ITO a reference materials for electrodes fabrication in electronic and opto-electronic applications. For instance, it is normally employed as transparent and conductive packaging for different kind of screens, including liquid crystals, plasma and touchscreens, for the fabrication of solar cells and OLEDs.
During the Ph.D. activity, ITO was used as reference materials for patterning bottom electrodes in resistive memory devices. In particular, ITO coated substrates (glass and PET) were employed, and bottom electrodes were patterned by means of a photolithographic process specifically set up. More details about such processes are reported in Chapter 4.

Silver

Silver is a transition metal, highly ductile and malleable. Among metals, it is characterized by the highest thermal and electrical

conductivity. These properties make silver feasible for the fabrication of metal contacts. In the research activity described, it was employed for the fabrication of top electrodes in resistive memory devices.

Aluminum

Aluminum is the third most abundant material (and the most abundant metal) in the Earth's crust. It is ductile, malleable, lightweighted and shows good thermal and electrical conductivity. It is characterized by a low specific weight (of about a third of that of iron and copper alloys) and by a good plasticity. Thank to its low electronegativity, it is easily oxidized in ambient condition, thus being resistant to corrosion. Moreover, since it has a low melting point, it can be easily deposited by several phisical vapor deposition techniques, such as thermal evaporation.
During the research activity, aluminum was employed in both resistive and OFET-based memory devices. In particular, aluminum nanoparticles were deposited by thermal evaporation as metal interlayer in resistive memory devices. Aluminum films were also used as gate electrodes for OFET-based memory devices. In this last case, the tendency of aluminum to form nanometrical insulating films represented a key factor for reaching the low operating voltages.

Gold

Gold is a ductile, malleable transition metal, highly resistant to corrosion and oxidation processes. It is diffusely employed in electronic applications thanks to its high conductivity ($4.52 \cdot 10^7 Sm^{-1}$). Moreover, it is caracterized by a relatively low melting point (1064.43 °C), thus being suitable for thermal evaporation processes.
During the research activity described in the manuscript, gold was employed especially for the fabrication of resistive memory devices. In particular, gold nanoparticles were synthetized according to the chemical reduction method described in Chapter 4. In a first case, Au NPs were deposited by means of electrospraying in order to obtain nanoparticles interlayers in resistive memory devices fabricated by thermal evaporation (see Chapter 4). Moreover, Au NPs were employed for the formulation of an ink with the aim of developing printed resistive memory devices (see Chapter 5). Gold was also tested as material for top electrodes in resistive memory devices, but the obtained performances were worst than those obtained using silver (see Chapter 4). Finally, gold was employed for the fabrication of source and drain electrodes in OFET-based memory device, as its work function (5 eV) is suitable for easy hole injection in the most of

p-type semiconductors.

A.2.3 Semiconductors

ActivInk™ N1400

ActivInk™ N1400 is the commercial name of a perylene derivative, patented and distributed by Polyera. Its chemical structure is reported in Figure A.3 a). It looks like a red powder, with a melting point around 300 °C. This last feature makes it feasible for thermal evaporation. Moreover, it is soluble in several organic solvents, such as chloroform, anisole, dichlorobenzene, and if heated up to 80 °C, toluene, o-xylene and 1,4-dioxane. The HOMO/LUMO levels are 6.4/4.3 eV respectively, thus determining a bandgap of 2.1 eV. Thanks to its relatively high LUMO level, N1400 allows electrons to be easily injected by conductors like gold, aluminum and ITO (cfr. Figure A.3 b)). Charge carrier mobilities in the range of $(0.02 \div 0.2)\ cm^2V^{-1}s^{-1}$ can be easily obtained both in thermally evaporated and spin-coated films. It is noteworthy that, among n-type organic semiconductor, is surely the most stable in ambient conditions.
During the research activity described in the manuscript, ActivInk™ N1400 was employed as organic layer in resistive memory devices. Interestingly, as reported in Chapter 4, it is the first time that such a semiconductor has been used for this purpose.

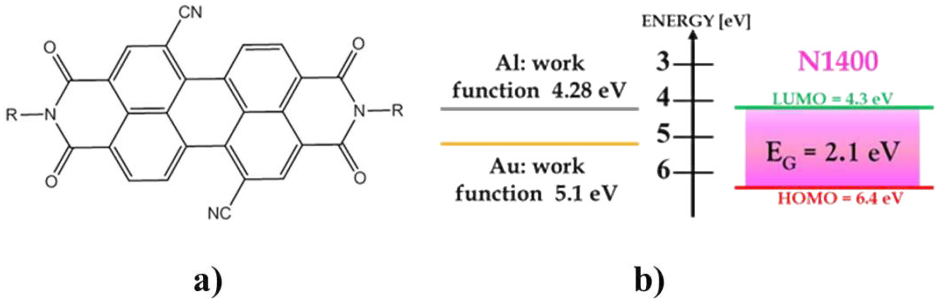


Figure A.3: a) Chemical and b) electronic structure of ActivInk™ N1400.

TIPS pentacene

6,13-Bis [(triisopropylsilyl)ethynyl] pentacene (TIPS pentacene, $C_{44}H_{54}Si_2$) is a p-type, solution processable organic semiconductor. It is diffusely employed for the fabrication of organic electronic devices by means of several techniques, including spin coating, spray coating,

dip coating and inkjet printing. It is a pentacene derivative: a single chain of pentacene ($C_{22}H_{14}$) is modified in position 6 and 13 by two silyl ethers, (triisopropylsilyl)ethynyl), composed by a silicon atom linking several methyl (CH_3) groups (see Figure A.4). Thanks to this modification, pentacene molecule becames soluble in different organic solvents (including toluene, anisole, chlorobenzene, dichlorobenzene). Moreover, the stability in air is improved, just as the charge carrier mobility. In particular, hole mobility up to 1.8 $cm^2V^{-1}s^{-1}$ has been obtained in literature. HOMO and LUMO levels are 5.3 eV and 3 eV respectively, thus allowing a good hole injection by several conductors, including gold, ITO and PEDOT:PSS. During the Ph.D. research activity, TIPS pentacene WAS employed as active layer in OFET-based memory devices.

Figure A.4: a) Chemical structure of TIPS pentacene.

A.2.4 Insulators

Aluminum oxide

Aluminium oxide is a chemical compound of aluminium and oxygen with the chemical formula Al_2O_3. It is the most commonly occurring of several aluminium oxides, and specifically identified as aluminium(III) oxide. Al_2O_3 is an electrical insulator but it has a relatively high thermal conductivity (30 $Wm^{-1}K^{-1}$) for a ceramic material. Aluminium oxide is an amphoteric substance, meaning it can react with both acids and bases, such as hydrofluoric acid and sodium hydroxide, acting as an acid with a base and a base with an acid, neutralising the other and producing a salt. Aluminium oxide is responsible for the resistance of metallic aluminium to weathering. Metallic aluminium is very reactive with atmospheric oxygen, and a thin passivation layer of aluminium oxide (4 nm thickness) forms on any exposed aluminium surface. This layer protects the metal from further oxidation. The thickness and properties of this oxide layer

can be enhanced using different processes, including annealing, plasma, ozone and electrochemical oxidation. Moreover, it can be deposited by several techniques, such as Atomic Layer Deposition (ALD).
Thanks to these features, and to the quite high dielectric constant ($8 \div 12$, according to the employed grown method), alumina was employed as key element in the hybrid organic/inorganic dielectric for the fabrication of low voltage, OFET-based memory devices (cfr. Chapter 7).

Parylene C

The name parylene is used for a family of polymers obtained from the polimerization of poly(paraxylylene). Such polymers, which can be deposited by vapor phase, show ideal features both as electrical and environmental insulator, thus being suitable both as dielectric and packaging layer in electron devices. The basic monomer of parylene is composed of a benzenic ring to which two $-CH_2-$ groups are connected in para position. In ortho position, a radical group is inserted, determining a specific type of parylene. In electronic applications, parylene C is surely the most widely used. As shown by the structure formula in `Figure A.5`, a chlorine atom is connected in ortho position. Parylene C is biocompatible, transparent if deposited in thin films, insoluble in organic solvents, resistant to acids and bases. A deposited parylene C layer is perfectly conformal to the underlying surface with a uniform thickness and good dielectric properties. Indeed, it is almost pinhole-free also if deposited in relatively thin films, showing a relative dielectric constant of 3.15 at 60 Hz and a electrical resistivity of $6 \times 10^{16} \Omega cm^{-1}$ at 20 °C.
In the research activity described in this manuscript, Parylene C was employed in combination with alumina for the fabrication of the ultra-thin, hybrid organic/inorganic dielectric layer for low voltage, OFET-based memory devices.

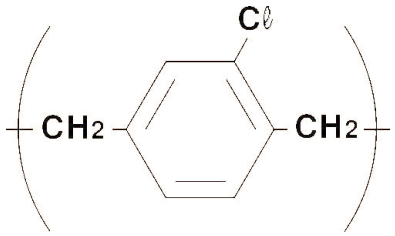


Figure A.5: Chemical structure of Parylene C monomer.

A.3 Methods

A.3.1 Thermal evaporation

Thermal evaporation is one of the most common physical vapor deposition techniques. It allows the deposition of several kind of materials, including metals and semiconductors, in thin films over moderately large areas. The basic working principle of thermal evaporation unit is reported in Figure A.6 a): the material to be deposited is inserted in a crucible inside a chamber where a high vacuum ($10^{-3} \div 10^{-9}$ Torr) or ultra-high vacuum ($10^{-9} \div 10^{-12}$ Torr) is created; in this condition, it is possible to sublimate the material by heating up the crucible. The obtained vapor condenses on the substrate, positioned over the crucible. Generally, the crucible is a tungsten filament, connected between two electrodes, which is heated up by Joule effect. A picture of the thermal evaporation unit used during the reported activity is shown in Figure A.6 b).

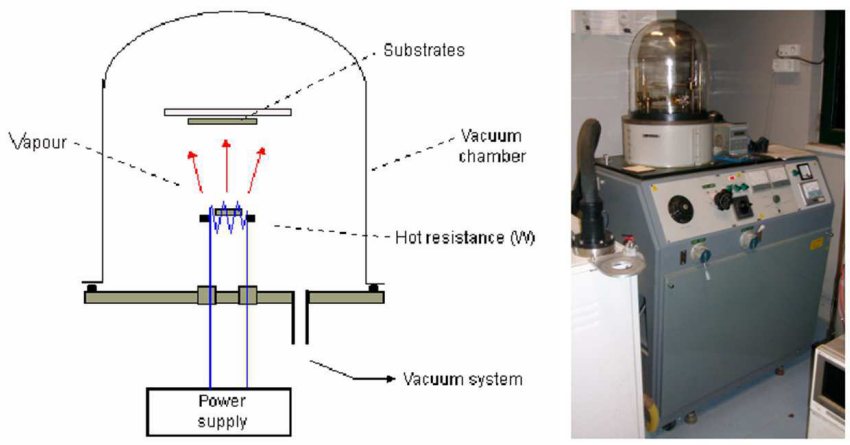


Figure A.6: a) General scheme of a Joule effect thermal evaporator; b) thermal evaporation unit employed during the research activity.

Important parameters in evaporation procedures are the evaporation speed, Φ_e, and the thickness of evaporated films, $d(x)$. The evaporation speed (as number of evaporated atoms per area unit and time unit) is a function of the vapor pressure of the material to be evaporated, P_e and to the pressure in the deposition chamber, P_h according to the relationship

$$\Phi_e = c \cdot \frac{P_e - P_h}{\sqrt{T}} \tag{A.1}$$

where c is a constant value, related to the specific material, and T the temperature of the crucible. As shown in `Figure A.7`, the thickness of the deposited film is not perfectly uniform, but it is a function of the distance l between the considered point x and the center of the film, i.e. the point perfectly perpendicular to the crucible, according to the relationship

$$d(x) = \frac{d(0)}{\left[1 + \left(\frac{l}{h}\right)^2\right]^{\alpha}} \tag{A.2}$$

where $d(0)$ is the film thickness at the center of the film, h the distance of such a point from the crucible, and α a constant related to the kind of source.

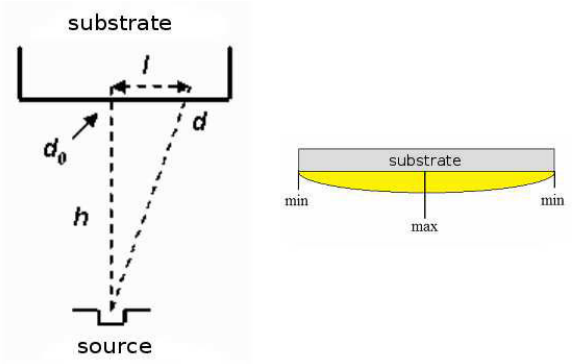


Figure A.7: Main geometrical parameter determining the thickness of the deposited film in a thermal evaporation unit.

Controlling the film thickness is generally crucial for the actual functionality of the fabricated devices. For instance, in the resistive memory devices fabricated during the Ph.D. research activity, the performances and actual functionality were strongly reliant on the thickness of the hybrid resistive layer, i.e. by the thickness of both the semiconductor matrix and the metal nanoparticles interlayer. In order to control the layer thicknesses, thermal evaporator unit are generally provided with a *quartz crystal microbalance* (QCM), which measures a mass variation per unit area by measuring the change in frequency of a quartz crystal resonator. The resonance is disturbed by the addition or removal of a small mass due to film deposition at the surface of the resonator. The change in the resonat frequency, Δf, is related to the mass deposited Δm by the Sauerbrey equation,

$$\Delta f - \frac{2f_0^2}{A\sqrt{\rho_q \mu_q}}\Delta m \tag{A.3}$$

where f_0 is the resonant frequency, A the piezoelectrically active crystal area, ρ_q the density of the quartz and μ_m the Shear modulus of quartz. Thanks to easy calibration procedure, to be performed by techniques such as Atomic Force Microscopy (AFM), Focused Ion Beam - Scanning Electron Microscopy (FIB-SEM) or profilometry, is it possible to associate a film thickness to a certain frequency variation.
As already mentioned, thermal evaporation and QCM were employed for the deposition of the hybrid resistive layers in the RRAM structures fabricated during the PhD activity. Moreover, thermal evaporation was employed for the deposition of each metal electrode, both in resistive and OFET-based memory devices.

A.3.2 Spin coating

Spin coating is a deposition techniques which allows the formation of thin, uniform films from liquid phase over a solid substrate. The deposition facility, generally referred as spin coater, is a rotating plate with a tunable angular speed ω. A small amount of a liquid is dropped in the center of the rotating plate (`Figure A.8 a)`; at a generic point P, far r from the center of the rotating plate, a centrifugal force

$$F_n = -kr\omega^2 \tag{A.4}$$

is applied to the liquid, thus determining the spreading of the liquid all over the substrate. The final thickness of the film, d, is defined by the relationship

$$d(\omega) = c_0 \cdot \left[\frac{\sqrt{\omega}}{2(1-c_0)K\omega^2}\right]^{\frac{1}{3}} \tag{A.5}$$

where c_0 is the solute/solvent ratio and K is a constant related to the viscosity and density of the liquid. The higher the angular speed, the thinner the film, until a saturation limit is reach. Obviously, also the total spinning time affects the actual characteristic of the deposited film. In particular, according to the material to be deposited, three time parameters must be carefully set (cfr. `Figure A.8 b)`).

- **acceleration time (t_a)**: time required to the rotating plate in order to reach the regime speed, ω_{max}; if the solvent is volatile, this time must be kept as small as possible;
- **spin time (t_{spin})**: time of constant, regime speed of rotation; for a given viscosity, the longer the spin time, the thinner the film; for a required thickness, the higher the viscosity, the longer the spin time required to reach it;

- **deceleration time (t_d)**: deceleration time of the rotating plate; generally it is chosen equal to t_a.

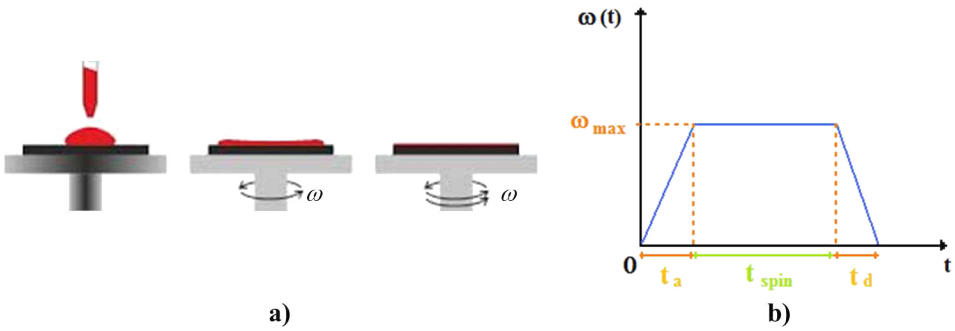


Figure A.8: a) Schematic representation of the spin coating process; b) characteristic time values in spin coating.

In the research activity here described, spin coating was employed for the deposition of uniform, thin photoresist films necessary to the photolithographic processes in the fabrication of resistive and OFET-based devices.

A.3.3 Photolithography

Photolithography is a top-down process that allows transferring a pattern from a mask to a substrate, covered by a thin film of an UV-sensitive material, called *photoresist*. Photoresist can be:

- **positive**: composed by a resin and a organic solvent, it becames soluble if exposed to the UV radiation; it is used to report on the substrate exactly the same pattern of the mask;
- **negative**: composed by polymers and photosensitive compounds, it is cross-linked by UV radiation; it allows reporting the negative of the pattern defined in the mask.

As already reported in Chapter 4, and summarized in `Figure A.9`, the basic steps of the photolithographic process are:

1. **coating** of the substrate with the photoresist; this operation is generally made by spin coating;
2. **exposure** of the coated substrate to UV radiation through a mask, reporting the pattern to be transferred;

3. **development** of the exposed film in an appropriate development solution, which dissolves (cross-links) the portion of the positive (negative) photoresist exposed to the UV radiation, while the one shadowed by the mask remains unsoluble (is dissolved);

4. **chemical etching** of the material not covered by the photoresist by means of an appropriate chemical solution.

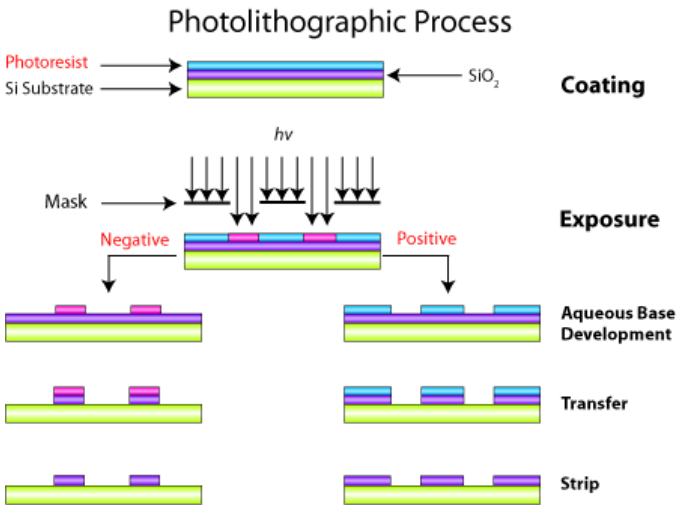


Figure A.9: Phases in the photolithographic process, according to the employed photoresist.

A.3.4 Fabrication of the ultra-thin, hybrid dielectric for low voltage OFETs

In Chapter 7, the research activity about OFET-based memory devices has been reported. Among the main innovation of the proposed device structure, a novel, ultra-thin, hybrid organic/inorganic dielectric has been presented. This insulator allows the devices to be operated at low voltages. It is obtained by the combination of two different materials, namely aluminum oxide and parylene C, which were obtained according to two different techniques, described in the following.

Aluminum oxidation

Aluminum oxide was directly grown on the aluminum surface by means of an easy, low cost, post-processing technique. UV-produced

ozone was used as oxidizing agent. In particular, a UV lamp (UVP Penray) was employed in ambient conditions, as shown in Figure A.10. Ozone is a not-stable form of oxygen, which rapidly decomposes in molecular oxygen (O_2) and radical oxygen (O^-). This latter element is the main responsible for the oxidation of the aluminum surface. Despite the fact that ultra-pure ozone in vacuum conditions is generally employed for oxydation, such a low cost, easy techniques turned out to be sufficient to obtain a thin (8 nm) aluminum oxide layer over relatively large areas.

a) b)

Figure A.10: Picture of the UVP Penray employed for ozone oxidation.

Parylene C deposition: Chemical Vapor Deposition

Parylene C can be deposited at room temperature in thin films over large areas by means of Chemical Vapor Deposition (CVD). In particular, a PDS2010 LabCoater (Specialty Coating Systems, Figure A.11) was employed. This system is composed by five parts:

- **Vaporizer**, where the di-parylene dimer is inserted and evaporated (*vaporization*);
- **Pyrolysis furnace**, where the *pyrolysis* process takes place, i.e. the chemical bonds between parylene molecules are broken by means of an high temperature (690°C), thus producing a parylene gas;
- **Deposition chamber**, where the gas is injected for deposition at room temperature (*polymerization)*;
- **Vacuum pump**, which creates moderately vacuum conditions necessary for the deposition;
- **Chiller**, a system used for the refrigeration of the cold trap (*thimble*) necessary for removing impurities by the deposition process.

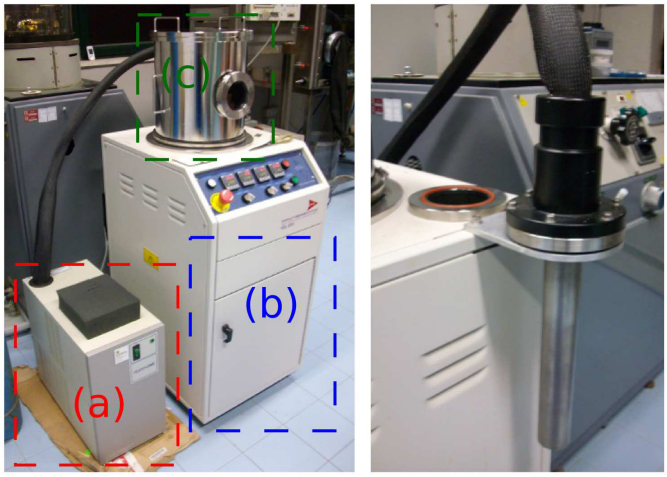


Figure A.11: Picture of the PDS2010 LabCoater used for CVD of parylene C: on the left, the chiller (a), the vaporizer (b) and the deposition chamber (c); on the right, the thimble.

The three phases (vaporization, pyrolysis and polymerization) are subsequently cycled until all the dimer in the vaporizer is consumed. In particular, the CVD unit works between two pressure values in the deposition chamber: when the pressure reaches the minimum value, the temperature in the vaporizer is increased, until the gas is produced and pumped into the deposition chamber. As a consequence, the pressure increases; when the maximum imposed pressure value is reached, the temperature drops down and the evaporation is stopped. The single cycle is depicted by the graph in Figure A.12.

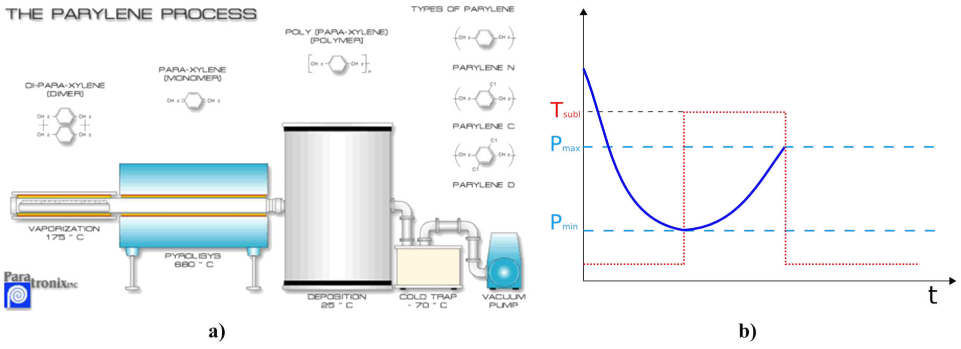


Figure A.12: a) Phases of the parylene C deposition process; b) deposition process as a function of the temperature and the pressure values set in the CVD unit.

A.3.5 Electrospraying

Electrospraying was employed in order to deposite gold nanoparticles over the first layer of N1400 in resistive memory devices. It was performed by University of Łódź. The electrospray setup, shown in Figure A.13 a), is composed of a capillary nozzle (Harvard Apparatus Ltd.) connected to the high voltage power supply (Applied Kilovolts Ltd). The applied voltage is in the rage from 0.1 kV to 15 kV. The positive potential is applied to the nozzle when the stainless steel plate electrode is earthed. The distance between the nozzle tip (small, blunt epidermic needle) and the substrate may be changed in the range from few millimeters up to 250 mm. The change of meniscus on the end of the nozzle to a jet form or multijet is recorded using a camera (Opta-Tech). The camera is connected to the computer, which permits observation of cone on the end of the nozzle. Examples of single and multijet operating mode are reported in Figure A.13 b) and c). The inlet of the needle is connected to a syringe pump (B.Braun Perfusor Secura) using a glass tube with ID 0.32 mm and 250 mm length (Supelco). The second end of the glass tube is connected to a 1ml glass syringe (Fortuna Optima). The flow rate of sprayed solution is also changed in wide range. For the illumination of the end of the nozzle a fibre optics light source (Cold Light L-15A Opta-Tech) is used. This equipment is used for deposition of gold nanoparticles from aqueous colloid onto memory elements without direct contact of colloid with the sample. The obtained coverage on the sample can be changed by controlling different parameters, e.g. flow rate (F), time (t), voltage (V), distance between nozzle and substrate (d), operation mode (single jet/ multi jet), nanoparticles concentration and solvent system in sprayed solution.

A.3.6 Inkjet printing

The inkjet printing process involves the ejection of a fixed quantity of a liquid phase material, called ink, in form of droplets from a chamber through a nozzle. The ejected drops fall onto a substrate under the gravity force and air resistance to form a pattern. The solidification of the liquid may occur through the evaporation of a solvent, chemical changes (for example the cross-linking of polymers) or crystallization. Often some post-processing treatments are required, as thermal annealing or sintering, i.e. the melting of metallic nanoparticles in metallic inks, achieved by heating to elevated temperatures. Among inkjet printing systems, Drop-on-Demand (DoD) is the most common. In this technology the system ejects an ink droplet from a reservoir through a nozzle only when a voltage pulse

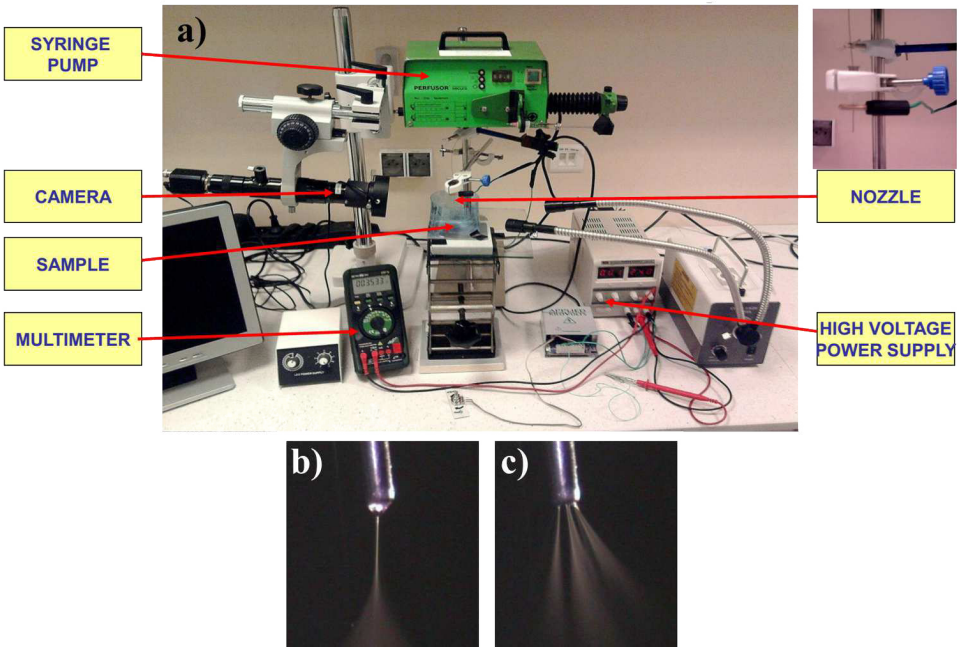


Figure A.13: a) Electrospraying apparatus; b) single and c) multi jet operating mode.

is applied to a transducer, i.e. only when the ejection is required. The DoD inkjet printing system employed in this research activity is a Dimatix Material Printer 2800 (DMP2800, FujiFilm), which is a *piezoelectric* printer. In this systems, the ejection of the droplet is caused by the mechanical deformation of a piezoelectric material under the application of an electric field. Before the printing process starts, the ink chamber is depressed by applying an appropriate bias to the piezoelectric crystal in order to prevent the ink from falling down from the nozzle (Start or Standby phase). A zero voltage is then applied to the piezo, which is thus undeformed in its relaxed position, leading to a flow of fluid in the ink chamber from reservoir. In the next phase, the chamber is strongly compressed causing the drop ejection from the nozzle. Finally, the chamber is brought back to the initial decompressed condition to pull back the ink and to prepare the system for the next ejection. The main component of the DMP2800 are:

- *print carriage*: it is the physical support of the cartridge and it represents the core of the printer itself;
- *platen*: it's the substrates' holder. It can be heated until 60 °C and it is provided with a vacuum system. The platen tempera-

ture is an important printing parameter. Indeed, it affects the drying time of the ink-jetted droplets on the substrate, and it can be one of the major causes of the undesired nozzle clogging. The vacuum system has the function of holding the substrate on the platen during the printing process;

- *cleaning station - blotting pad*: it is the cartridge maintenance station, where the cleaning cycles are performed;
- *drop watcher station*: this is the system which allows direct viewing of the jetting nozzles, the face plate surrounding the nozzles, and the actual jetting of the fluid.

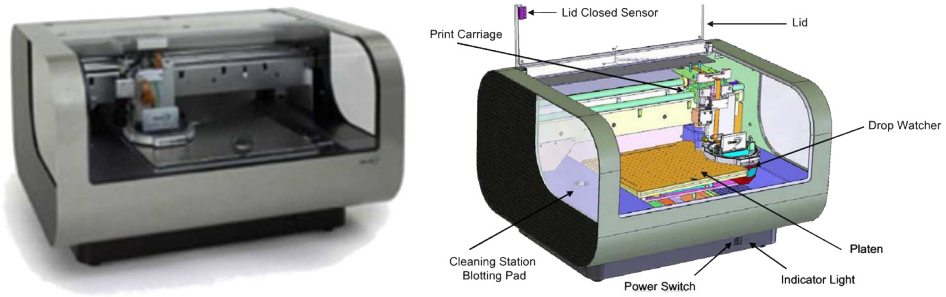


Figure A.14: Picture a) and scheme b) of a Dimatix DMP2800.

The print carriage (`Figure A.15 a)`) is the core of the printing system. It is the support for the cartridge and it includes the fiducial camera, a very useful tool for alignment procedures and for evaluation of the printed pattern quality. During printing, the carriage moves horizontally (X direction) above the substrate, while the vertical shift (Y direction) is achieved by means of the platen motion. In other words, the printing action proceeds through subsequent horizontal scans of the print carriage, and subsequent vertical shifts of the substrate. The cartridge (`Figure A.15 b)`) is composed of two main parts: a *fluid module*, which contains a plastic bag acting as ink reservoir, and a *jetting module*, where 16 jetting nozzles, at a distance of 254 μm, are located in a single row and each orifice size is about 21.5 μm. Dimatix supplies two models of piezo-driven jetting cartridges which differ for the nominal drop volume they can eject: DMC-11601 and DMC-11610 models are able to jet 1 pL and 10 pL droplets respectively. Determining the spot size of the ink on the substrate is a fundamental operation to set an appropriate *drop spacing* in order to achieve the desired resolution of the printed pattern. The

drop spacing is the distance between the center of two subsequent drops, both in X and in Y direction, which the printer deposits on the substrate to create the pattern. As shown in `Figure A.15 c)` and `d)`, in the X direction the printer manages the ejection of a drop from the correct nozzle according to an encoder signal and to the image resolution corresponding to the drop spacing set. In the Y direction the distance between two subsequent spots is determined by the cartridge mounting angle (angle between the scan direction of the cartridge and the nozzle plate), but also by the intrinsic resolution of the printer, i.e. the distance between two subsequent nozzles in the nozzle plate (254 μm). The cartridge mounting angle is set manually through a rotating system, which allows the operator to rotate the cartridge at the desired angle by means of two graduated scales (`Figure A.15 e)`). The drop spacing thus is adjustable between 5 μm and 254 μm.

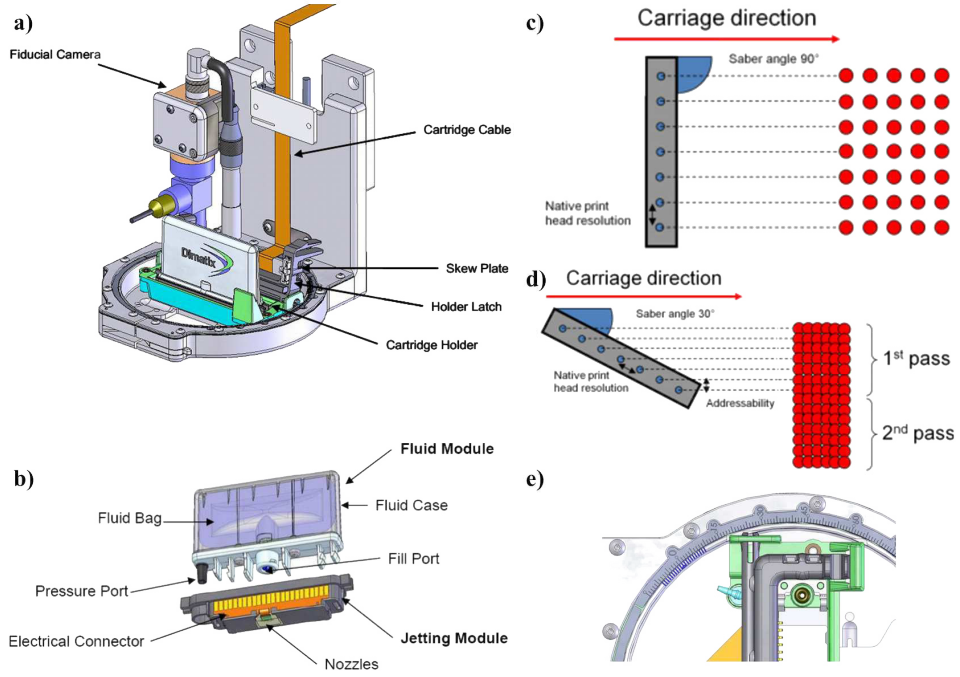


Figure A.15: a) Print carriage; b) cartdridge parts (fluid module and jetting module); c) and d) pattern resolution in X and Y directions as a function of the cartridge mounting angle e).

Controlling the quality of jets ejected is crucial in order to achieve the best print quality. It can be done in two different and complementary ways: caring for the cartridge maintenance and monitoring the ink droplets ejection. The maintenance operations are supported

both by software and hardware of the printer, and are designed in order to initialize and maintain the optimal jetting performances. In the cleaning station there is a replaceable adsorbing pad, which has the function of soaking up the ink from the nozzle plate. Four main functions can be combined to form Cleaning Cycles:

- **purging**: the fluid is pushed out of the nozzles by an application of air pressure to outside of fluid bag. Purging is required for the initial use of the cartridge to push air out of the fluid path, as air bubbles may cause nozzle clogging;
- **spitting**: a certain number of drops are jetted at a predetermined frequency in order to clean the nozzles and to keep fluid path surfaces wet;
- **blotting**: the nozzle plate is kept in contact with the cleaning pad (no wiping) to remove the excess of fluids that may be present in proximity of the nozzles;
- **meniscus control**: in order to prevent ink from flowing out of the cartridge nozzles, a low vacuum is applied to the ink reservoir.

The desired cleaning cycle can be performed before (almost mandatory to achieve satisfactory printing performances), during and after printing and also during resting time. Monitoring and adjusting the ink jets is possible by using the *drop watcher camera system*, including a replaceable *drop watcher pad* which collects the fluids ejected, and a digital camera with a magnification of 150x.
During jetting observation several parameters can be setted and/or modified:

- **firing voltage**: it corresponds to the bias applied to deform the piezoelectric crystal for the droplet's ejection. It can be adjusted for each nozzle independently. Obviously, different inks requires different firing voltages in order to reach the optimal jetting performances. Generally, a high firing voltage produces quite compact drops but with a long tail. Conversely, a low firing voltage permits reducing tails length, drop velocity and avoiding droplets scattering at the impact with the substrate (and, subsequently, obtaining a better print quality). On the other hand, a low firing voltage may bring to misdirected jets and increases the probability of clogging nozzles during printing;
- **jetting frequency**: it's the frequency of nozzles for ejecting droplets. It affects the print velocity, the print precision and

it is strictly dependent on the particular pattern as described afterwards;

- **number of jetting nozzles**: as the jetting frequency, also the choice of the number of used nozzles is strictly dependent on the specific pattern and precision. If high precision and definition of the printed pattern are required, using a few jets is suitable. On the contrary, when rough layers of material have to be printed, the use of many nozzles leads to a faster print process together with a good uniformity of the material deposited. It should be noticed that printing with more than one nozzle implies to use adjacent nozzles: choosing the group of nozzles with the overall best jetting performances is really critical and sometimes it could be quite difficult. Checking the good jetting performance of the chosen nozzles just before printing is absolutely advisable.

A.3.7 Electrical characterization

The electrical characteristics of the devices were measured employing several source meters provided by Keithley (Keithley 2616 and 2636 SourceMeter®), and by means of two Semiconductor Parameter Analyzer, namely HP4155A (Hewlett Packard) and B1500A (Agilent). Source meters of Keithley Series 2600A System Source Meter® instruments (`Figure A.16`) are source-measure instruments for use as either a bench-top I-V characterization tool or as a building block component of multi-channel I-V test systems. As voltage supply unit ($100\ \mu V \div 200V$), current ranging from 100 pA to 1.5 A can be recorded, with a 100 pA resolution. Thanks to several, custom-made Matlab® software, several kind of electrical characterization were performed, including output and transfer characteristic of transistors, I/V sweeps of organic memory devices, real-time measurements for constant and variable bias.

Figure A.16: Keithley 2616 and 2636 SourceMeter Systems.

HP4155 Semiconductor Parameter Analyzer (Figure A.17) is an electronic instrument for measuring and analyzing the characteristics of semiconductor devices. This instrument allows performing both measurement and data analysis. It has four highly accurate source/monitor units (SMUs), two voltage source units (VSUs), and two voltage measurement units (VMUs). It can perform three types of measurements: i) sweep measurement, ii) sampling measurement, iii) quasi-static C-V measurement. Moreover, it allows knob sweep for quick measurements executed by rotating the rotary knob on the front panel. Furthermore, it is provided with a pulse generator unit(PGU), which is installed in Agilent 41501A/B SMU/Pulse Generator Expander. The HP4155A supplies a marker and two lines for analyzing the measurement results. It also provides the automatic analysis function, which moves marker and lines at desired location and displays desired calculation results automatically after measurement is completed. Finally. it allows storing measurement setup information, measurement data, and instrument setting information on a 3.5-inchdiskette using the built-in flexible disk drive.

Figure A.17: HP4155A.

The Agilent B1500A Semiconductor Device Analyzer (Figure A.18) is a modular instrument with a ten-slot configuration, which supports both IV and CV measurements and also fast high-voltage pulsing. Its familiar, Microsoft® Windows® user interface supports Agilent's EasyEXPERT software, which provides a new, more intuitive task-oriented approach to device characterization. Thanks to its extremely low-current, low-voltage, and integrated capacitance measurement capabilities, the Agilent B1500A can be used for a wide range of semiconductor device characterization needs (IC-CAP supports the B1500A). It is also an excellent solution for non-volatile memory cell characterization and high-speed device characterization (including advanced NBTI and RTS noise (RTN) measurement).

Figure A.18: Agilent B1500A.

Main features and benefits of the B1500A are:

- superior IV measurement performance: 0.1 fA / 0.5 μV measurement resolution; measurement features include single and multi-channel sweep, time sampling, list sweep, quasi-static CV (using the SMUs), direct control and arbitrary linear waveform generation (ALWG) GUI for the HV-SPGUs;
- optional, integrated capacitance module supports CV measurements up to 5 MHz;
- optional positioner-based CV-IV switching solutions available with 0.5 μ V voltage measurement resolution and 10 fA, 1 fA or 0.1 fA current measurement resolution capability;
- easy test automation with built-in semiautomatic wafer prober drivers and test sequencing without programming via the Quick Test mode;
- optional high-voltage semiconductor pulse generator unit (HV-SPGU) available with 10 ns programmable pulse widths and /-40 V (80 V peak-to-peak) output;
- optional waveform generator/fast measurement unit (WGFMU) available with ALWG and fast current or voltage measurement capabilitieas;
- 10 ns pulsed IV solution is available for characterizing high-k gate dielectric and SOI (silicon-on-insulator) transistors;
- Classic Test mode is available to provide the look, feel, and terminology of the 4155/4156 interface while enhancing user interaction by taking full advantage of Microsoft®Windows®GUI features.

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List of Publications

1. **An organic, charge-modulated field effect transistor for DNA detection.**

   by: M. Demelas, S. Lai, **G. Casula**, E. Scavetta, M. Barbaro, and A. Bonfiglio.

   published in: Sensors and Actuators B: Chemical, **171-172**, 198-203 (2012)

   Abstract: A novel DNA sensor able to detect the DNA hybridization in liquids is presented. The device is a charge sensor, realized with an organic field effect transistor, sensitive to the negatively charged DNA phosphates groups. Compared to other examples of DNA sensors based on organic transistors, this device has two noticeable features: the probe area is completely separated from the transistor area and the sensing mechanism is not reliant on the choice of the device materials. Moreover, the device architecture has been designed in order to avoid any damaging treatment that may reduce the stability of the organic semiconductor. These features make this device especially suitable for the realization of portable and low cost sensors. Two devices (one used as reference and the other as sensor) are measured at the same time in order to get rid of current drifts which are due to organic semiconductor degradation or bias stress, and to enhance variations induced by the DNA sensing mechanism.

2. **Ultralow Voltage, OTFT-Based Sensor for Label-Free DNA Detection.**

by: S. Lai, M. Demelas,**G. Casula**, P. Cosseddu, M. Barbaro, and A. Bonfiglio.

published in: Advanced Materials, **25**, 103-107 (2013)

Abstract: An organic ultralow voltage field effect transistor for DNA hybridization detection is presented. The transduction mechanism is based on a field- effect modulation due to the electrical charge of the oligonucleotides, so label-free detection can be performed. The device shows a sub-nanomolar detection limit and unprecedented selectivity with respect to single nucleotide polymorphism.

3. **High performance, foldable, organic memories based on ultra-low voltage, thin film transistors.**

by: P. Cosseddu, S. Lai, **G. Casula**, L. Raffo, and A. Bonfiglio.

published in: Organic Electronics, **15**, 3595–3600 (2014)

Abstract: We report on the fabrication of highly flexible OTFT-based memory elements with excellent mechanical stability and high retention time. The devices have been fabricated using a combination of two ultrathin AlOx and Parylene C as dielectric, and TIPS-Pentacene as the semiconductor, obtaining high performing low voltage transistors with mobility up to 0.4 cm^2/V s, and I_{on}/I_{off} ratio of 10^5. Charge trapping in the Parylene C electret layer is the mechanism that allows employing these devices as non volatile memory elements, with retention time as high as 4×10^5s. The electromechanical characterization demonstrated that such memory elements can be cyclically bent around a cylinder with a radius of 150μm without losing the stored data.

4. **7.5 – 15 MHz organic frequency doubler made with pentacene -based diode and paper substrate.**

by: M.Virili, **G. Casula**, C. Mariotti, G. Orecchini, F. Alimenti, P. Cosseddu, P. Mezzanotte, A. Bonfiglio, and L. Roselli.

published in: Microwave Symposium (IMS), 2014 IEEE MTT-S International, 1-4 (2014)

Abstract: This work describes the realization of a fully organic "chip-less" tag, based on the harmonic RFID architecture, oper ating at 7.5 and 15 MHz. The tag is fabricated on paper substrate and includes an organic pentacene-based diode, as a non-linear component, to generate harmonics. The communication between reader and tag is provided by

coupled resonators operating at the fundamental and harmonic frequencies. A measure campaign of the complete reader-tag system has been performed and the results are here reported .

5. **Air-stable, non-volatile resistive memory based on hybrid organic/inorganic nanocomposites.**

   by: **G. Casula**, P. Cosseddu, Y. Busby, J. - J. Pireaux, M. Rosowski, B. Tkacz Szczesna, K. Soliwoda, G. Celichowski, J. Grobelny, J. Novák, R. Banerjee, F. Schreiber, and A. Bonfiglio.

   published in: Organic Electronics, **18**, 17-23 (2015)

   Abstract: A non-volatile memory element based on organic /inorganic nanocomposites is presented. The device can be operated in ambient conditions, showing high retention time and long-term life time. The formation/rupture of metallic filaments in the organic matrix is investigated by HR-XPS and ToF-SIMS analysis, and is demonstrated to be the driving mechanism for the resistive switching.

List of Figures

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