SiC-GaN-Based Universal DC-DC Converter for Plug-In Electric Vehicles

Milad Moradpour

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Department of Electrical and Electronic Engineering

University of Cagliari
Department of Electrical and Electronic Engineering

This is to certify that I have examined this copy of a doctoral dissertation by

Milad Moradpour

and have found it complete and satisfactory in all respects,
and that any and all revisions required by the final
examining committee have been made.

Supervisor:

_____

Prof. Gianluca Gatto

Reading Committee:

_____

Prof. Francesco Castelli

_____

Prof. Luigi Piegari

Date: _____

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by Milad Moradpour

Supervisor

Professor Gianluca Gatto

Abstract

In this thesis, a two-phase full-directional dc-dc converter is designed for the application of plug-in electric vehicles. It is a universal dc-dc converter in which two power electronic modules, the battery charger dc-dc converter and the power management dc-dc converter, are integrated in order to improve the power density, which is a crucial factor in plug-in electric vehicles. The state-of-the-art wide band gap silicon carbide (SiC) and gallium nitride (GaN) switching devices are used in the proposed converter. Especially the GaN device has the lowest switching loss among the power electronic devices causes higher efficiency and higher power density in the hard-switched applications. To cope the power rating limitation of the GaN device and evade the complexity and infeasibility of the multi-phase converters with excessive number of phases, a GaN phase is paralleled with a SiC phase in a half-bridge configuration. An asymmetrical current sharing is applied between the phases in such a way to maximize the utilization of the GaN device. Mathematical model of the proposed converter is derived and verified. A comprehensive power loss analysis investigates the superiority of the proposed converter. Dead-time loss analysis is performed with a new method of power loss calculation. A cascade PI controller is designed to provide satisfactory performance of the converter in the all modes of operation. Finally, a gate-driver multi-objective parameterization method is also presented to improve efficiency and EMI level of a GaN-based one inverter leg case study.

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DEDICATION

To my beloved family

Chapter 1. Introduction

Conventional vehicles with their combustion engines consume co-products of petroleum such as benzene and gasoline. There are two critical problems with these kinds of fuel. First, petroleum and its co-products are nonrenewable resources and will be finished sooner or later. As a result, the price of these types of fuel is increasing which is a negative effect on the vehicle market. Second, combusting nonrenewable resources produce toxic emission, which deteriorate the environmental pollution crisis such as global warming.

Renewable energy resources such as solar, wind, marine, thermal, etc. are the alternative of the nonrenewable resources to cope the critical problems of deficiency and pollution. In general, these kinds of energy are being harvested in different way and converted to electrical energy. The obtained electrical energy provides the demanded power for deconstructed power electrical systems (distributed grids, smart grids, etc.) or is saved in battery energy storage systems. In this way, in an updated transportation system with the use of the alternative renewable energy resources, electric vehicles are being replaced with the conventional ones with a growing demand in the market in the recent years.

An electric vehicle in precise words is a plug-in electric vehicle where the source of energy is purely electric energy. The vehicle should be plugged in an electric outlet facility to charge its battery (or its other energy storage system such as ultracapacitor, flywheel, etc.) or to be discharged in the case of vehicle-to-grid (V2G).

Among the different challenge such as the battery technology, the electromechanical compatibility, the reliability, etc., power electronics is a key factor to progress the penetration of the electric vehicles in the market. In the application of electric vehicles, from the power electronics point of view, the power density is a crucial factor. The power density is related to the both volume/weight and efficiency of the power electronic modules. Generally, there are four power electronic modules in an electric vehicle: ac-dc-dc battery charger, dc-dc power management, dc-ac traction inverter, and dc-dc light loads.

One innovative idea to compact the volume/weight of the power electronic modules in the electric vehicles is to integrate the dc-dc converter of the battery charger with the dc-

dc converter of the power management into a fully directional universal dc-dc converter. Such a universal converter is needed to work from the medium range of power in the plug-in mode to the high range of power in the drive mode.

On the other hand, the state-of-the-art wide band gap (WBG) switching device technologies such as gallium nitride (GaN) and silicon carbide (SiC) have superiority over the settled technologies such as silicon (Si) power MOSFETs and Si IGBTs in the switching converters. Especially the GaN devices have the lowest switching power loss in hard-switched applications. The current commercial GaN devices have a lateral structure with a limitation of power rating. Therefore, in the case of the electric vehicle applications, the GaN devices are being studied for the low-to-medium power electronic modules.

To have the advantage of the impact universal dc-dc converter and the efficient GaN device at the same time, in this thesis a new topology is proposed. The novelty of the proposed topology is to parallel the switching devices of different technologies in a multi-phase configuration and share the demanded power in an asymmetrical way. While in a conventional multiphase converter, all the switching devices are of the same technology, the proposed converter is a two-phase dc-dc converter with one GaN-based phase and one SiC-based phase. In the proposed converter, only the GaN phase conducts the current to provide the demanded power up to its power rating. For the amount of power higher than the power rating of the GaN device, the SiC phase will conduct as well to provide the rest of the demanded power.

In the application of electric vehicles, the power rating of the universal dc-dc converter can be even ten times more than that of the GaN device. To prevent the complexity and infeasibility of a multi-phase converter with excessive number of phases, the idea of paralleling the GaN device with the SiC device is proposed. While in a conventional multi-phase converter, the current sharing is needed to be symmetrical because of the safety problem resulted from the negative thermal coefficient of the diodes, in the proposed converter where there is no diode, the asymmetrical current sharing is possible.

The next chapters are organized as follow:

In chapter two, different types of the electric vehicles, their sub-systems, the role of power electronics in the electric vehicles, the universal dc-dc converter in the electric

vehicle application, WBG devices, and state-of-the-art SiC-based and GaN-based dc-dc converter are studied.

In chapter three, the proposed SiC-GaN-based universal dc-dc converter is studied. The topology and the design of the power stage are presented. The average model of the converter is derived and then verified through OrCAD simulations. A comprehensive power loss analysis is performed to show the superiority of the proposed converter in the term of the efficiency compared to a two-phase all-SiC dc-dc converter through OrCAD simulations using precise Spice model of the components. In addition, a new dead-time analysis method is presented to investigate dead-time loss. The effect of the OFF gate-source voltage on the dead-time loss is studied as well.

In chapter four, a cascade PI controller is designed for the proposed converter to regulate the dc bus voltage in the drive mode and the battery power in the plug-in mode as well as sharing the current between two phases asymmetrically in a way to achieve the maximum utilization of the GaN device, the minimum switching loss, and the maximum efficiency.

In chapter five, an innovative idea is proposed as gate driver multi-objective parameterization. First, different issues of the gate driver design in general and for the case of GaN devices in particular are discussed. Then, the application of optimization and multi-objective optimization in power electronics in general and in the gate driver design in particular is reviewed. Then, the proposed method is presented in which the high side (HS) gate resistor, the low side (LS) gate resistor, and the HS ferrite bead are parameterized in a multi-objective optimization problem with two objective functions of the efficiency and the electromagnetic interference (EMI) level for a GaN-based one inverter leg case study. The multi-variant regression functions and the multi-objective optimization Pareto Front of the gate driver design problem are obtained using MATLAB; based on OrCAD simulations data of the GaN-based one inverter leg case study.

Chapter 2. State-of-the-art DC-DC Converters for EVs

2.1 Electric Vehicles

In a conventional vehicle, an internal combustion engine (ICE) consumes petrol, oil, or other fossil fuel to provide propulsion for the mechanical motor. On the contrary, in an electric vehicle (EV), the propulsion is provided by renewable energy resources such rechargeable electrochemical batteries or fuel cells to drive an electric motor.

The main problems of the conventional vehicles are the environmental crisis such as pollution and global warming caused by burning fossil fuels, the limitation on the non-renewable fossil fuel resources, and consequently the rising prices of the fossil fuels. As a result, there is an increasing trend in the recent years by the governments, the organizations, the car manufacturers, and the costumers to replace the conventional vehicles the EVs. Unlike the conventional vehicles, EVs are emission free using the renewable energy resources. Beside the main advantages of EVs, there are two other superiorities of EVs over the conventional vehicles: the simpler and the cheaper maintenance issues and the ability of the regeneration power during the braking mode, which makes the vehicle more efficient.

Depend on the type of the energy sources of the vehicle, there are three types of EVs: pure electric vehicles or simply EVs, hybrid electric vehicles (HEVs), and fuel cell vehicles (FCVs). Therefore, when we say EVs, it may refer to electric vehicles generally or to pure electric vehicles particularly depends on the context.

The characteristics of all these energy storage systems (ESSs) are compared in fig. 2.1 on the base of energy density and power density. Higher energy density provides a higher driving range for a longer period of time while higher power density provides a high-power for a shorter period of time such as a fast acceleration of the vehicle. As it can be seen in fig 2.1, ultracapacitors and flywheels are high-power low-energy while fuel cells are high-energy low-power, and batteries are mid-power mid-energy. Based on different characteristics of the energy sources, a combination of different systems will provide a better power management and performance for the vehicle. The main features of EVs, HEVs, and FCVs are presented in table 2.1.

Table 2.1. *The main features of EVs, HEVs, and FCVs*

Type of EV	EVs	HEVs	FCVs
Propulsion	• Electric motor drives	• Electric motor drives • Internal combustion engines	• Electric motor drives
Energy Source	• Battery • Ultracapacitor • Flywheel	• Battery • Ultracapacitor • ICE generating unit	• Fuel cells
Energy Infrastructure	• Electric grid charging facilities	• Gasoline stations • Electric grid charging facilities (for plug-in hybrid)	• Hydrogen
Characteristics	• Zero emission • High-energy efficiency • Independence on fossil fuels • Relatively short driving range • High initial cost • Commercially available	• Low emission • Long driving range • Dependence on fossil fuels • Higher cost as compared with ICE vehicles • Commercially available	• Zero or ultra low emission • High-energy efficiency • Independence on fossil fuels • Satisfied driving range • High cost • Commercially available
Major Issues	• Battery and battery management • Charging facilities • Cost	• Multiple energy sources control, optimization, and management • Battery sizing and management	• Fuel cell cost, cycle life and reliability • Hydrogen Infrastructure

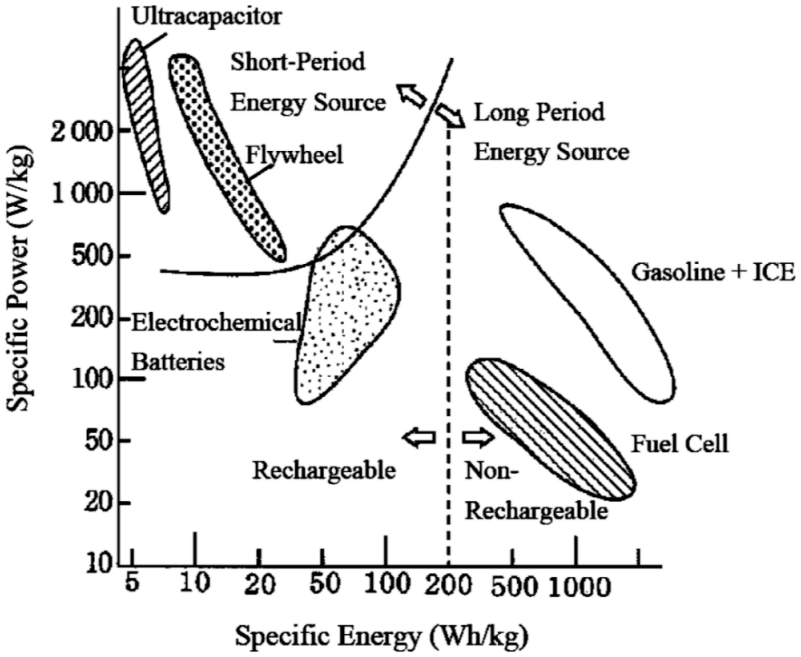


Figure 2.1. Characteristics of various energy resources

2.1.1 Energy Storage Systems

Batteries: For EVs, batteries are more commercial regarding their relatively higher energy density, compact size, and reliability. The different types of batteries are discussed as follow:

a) Lead-Acid Batteries: The advantages of lead-acid batteries are the low cost price of them and the maturity of their production technology. The disadvantages of lead-acid batteries are limited life cycle and low-power low-energy density due to the weight of the lead collectors.

b) Nickel Metal Hydride (NiMH) Batteries: The advantages of NiMH batteries are high energy density (two times more than lead-acid batteries), environment friendly materials, safe operation at high voltage, long life cycle, and wide operation temperature ranges. On the other hand, if repeatedly discharged at high load currents, the life of NiMH is reduced to about 200–300 cycles.

c) Lithium-Ion Batteries: Lithium-ion batteries are dominant in portable electronics and medical devices. They have high energy density of 100 Wh/kg, high power density of 300 W/kg, high temperature performance, and long battery life of 1000 cycles. Regarding

the advantages of lithium-ion batteries and the growing price of Nickel, they are the best candidates to be replaced with NiMH as the new generation of batteries for the EVs.

d) Nickel-Zinc (Ni-Zi) Batteries: The advantages of Ni-Zi batteries are high power density and high energy density, low cost materials, being environment friendly, and having high range of temperature operation (-10 to 50 Celsius). However, because of their poor life cycle, they are not developed for the EVs.

e) Nickel-Cadmium (Ni-Cd) Batteries: The advantages of Ni-Cd batteries are their long lifetime. Their specific energy density is 55 Wh/kg. They are recyclable, however, cadmium can be harmful for the environment if not be properly disposed of. They are also costly such as 20000 $ to be installed in an EV.

The characteristics of commercial NiMH, Li-Ion, and Lead-Acid batteries are presented in table 2.2.

Table 2.2. *Characteristics for commercial batteries [2]*

Type of Battery	Capacity (Ah)	Voltage (V)	Resistance ($m\Omega$)	Power Density (W/kg)
NiHM				
Panasonic	6.5	7.2	11.4	207
Ovonic	12	12	10	195
Saft	14	1.2	1.1	172
Li-Ion				
Saft	12	4	7	256
Shin-Kobe	4	4	3.4	745
Lead-Acid				
Panasonic	25	12	8	77

In EVs, state of charge (SOC) of batteries (or ultracapacitors) is a quantity to measure the amount of electrical energy stored in the battery. SOC in EVs is analogous to the fuel gauge in the conventional vehicles with ICE. SOC of a battery define as:

$$S(t) \triangleq \frac{Q_0 - \int_{t_0}^{t} I_b(\tau) d\tau}{Q_0} \times 100 \qquad (2\text{-}1)$$

where t_0 is the initial time in which the battery is fully charged, $I_b(t)$ is the discharging current, $\int_{t_0}^{t} I_b(\tau)\, d\tau$ is the charge delivered by the battery at the time t, and Q_0 is the total charge the battery can deliver (hold). It is desirable for batteries to keep their SOC in a limited range such as $20\ \% \leq S(t) \leq 95\ \%$.

Ultracapacitors: Ultracapacitors do not have chemical variations on the electrodes and for that reason have long cycle life but low energy density. On the contrary, the power density of ultracapacitors is considerably higher than that of the batteries. Ultracapacitors have low internal resistance. The advantage is to have high efficiency and the drawback is the possibility of a large burst of the output current in the case of very low SOC.

The technologies of ultracapacitors are under developing: carbon/metal fiber composites, foamed carbon, a carbon particulate with a binder, doped conducting polymer films on a carbon cloth, and mixed metal oxide coatings on a metal foil. Among these five types of technologies, a carbon composite electrode using an organic electrolyte has the highest energy density.

Low energy density and high power density of ultracapacitors make them suitable to be used at the EVs with batteries complementarily specially in urban drive where there are too many stop-and-go driving conditions. In stop-and-go driving conditions, the total required power is relatively low while the electricity should be regenerated very quickly during the braking. Therefore, ultracapacitors are the best candidate to be energy source of EVs in urban stop-and-go driving conditions to be used beside a battery energy source.

Table 2.3 compares the characteristics of a commercial battery with a commercial ultracapacitors. The total usable energy and the energy density of the battery are much higher than those of ultracapacitor while the maximum discharging current and the power density of ultracapacitor are much higher than those of the battery. Life cycle of ultracapacitor as well as its cost is considerably lower than those of the battery.

Fuel Cell: The main advantages of fuel cells are high conversion efficiency of fuel to electrical energy, noise-free operation, zero or very low emission, waste heat recoverability, fuel flexibility, durability, and reliability.

Table 2.3. *Comparison of a commercial battery with a commercial ultracapacitor [2]*

Parameter	Zebra Battery Pack	Thunderpack II Ultracapacitor pack
Usable Energy (kWh)	23.5	0.3
Max Discharge Current (A)	224	400
Specific Energy (Wh/kg)	113	4
Specific Power (W/kg)	174	1500
Life Cycle (year)	2.5-5	10-12
System Cost ($/kW)	400	100
Life Cycle Cost ($/kW)	1200	100

The ideal fuel for fuel cell is hydrogen since it is a clean fuel with a bi-product of water and it has also the highest energy density respect to any other fuel. Energy density of hydrogen (2.6 kWh/L) is lower than petrol (6 kWh/L). Also, unlike electrochemical batteries, the reactants of fuel cells must be refilled before finishing. Therefore, in EV applications, when a fuel cell is the source of energy, a relatively large fuel tank should be installed on board. The efficiency of fuel cells is higher when they are used at lower power. The main power loss contributor is related to the voltage drop on internal resistances. Time response of fuel cells is relatively longer than those of batteries and ultracapacitors. The cost of fuel cells is also five times more than ICEs. Table 2.4 compares typical characteristics of six different types of fuel cell: phosphoric acid fuel cell (PAFC), molten carbonate fuel cell (MCFC), alkaline fuel cell (AFC), solid oxide fuel cell (SOFC), direct methanol fuel cell (DMFC), and solid polymer fuel cell (SPFC).

Table 2.4. *Typical characteristics of fuel cells [2]*

Parameter	PAFC	MCFC	AFC	SOFC	DMFC	SPFC
Temp (℃)	150-210	600-700	60-10	900-1000	50-100	50-100
Density (W/cm^2)	0.2-0.25	0.1-0.2	0.2-0.3	0.24-0.3	0.04-0.23	0.35-0.6
Life (kh)	40	40	10	40	10	40
Cost ($/kW)	1000	1000	200	1500	200	200

Flywheel: A flywheel stores energy in the kinetic form using a rotating disk to be transformed into electricity by the use of a motor/generator coupled with the rotating disk. The role of the electric motor is to store energy to the rotating disk and the role of the generator is to provide energy from the rotating disk to the electric load. To overcome the mechanical power loss caused by the air resistance, flywheels need to be operated at a partial vacuum. Magnetic contactless bearing also should be used to eliminate the mechanical power loss of the friction. The power density of flywheels is very high and limited only by the size of the electric machine. They have also virtually infinitive number of charge-discharge cycles. Therefore, flywheels are very attractive to be an ESS of EVs.

2.1.2 Propulsion Motor

There are three types of electric motors for EVs, HEVs, and FCVs: 1) induction motors, 2) permanent magnet (PM) synchronous or brushless motors, and 3) switched reluctance motors. The required characteristics of motors for EV application are high torque density and power density, wide speed range including constant torque and constant power operations, high efficiency over wide speed range, high reliability, robustness, and reasonable cost.

Induction machines are simple, robust, and they have wide speed range. Similar to dc machines, induction machines are also field-oriented controlled. Because of the inherent rotor loss, the efficiency of induction machines is generally lower than PM machines. For the same reason, at a specified power and speed rating, the size of induction machines is generally larger than PM machines.

The main advantages of PM machines are high efficiency, high torque, and high-power density. Unlike induction machines that do not have back emf, the inverter must be able to withstand the maximum back emf generated by the stator winding for high speed range in the case of PM machines. In addition, if a stator-winding short circuit happens, the machine may run into problems because of the existence of a rotor PM field.

Switched reluctance motors have simple structure and simple control, ability of extremely high operation, and high reliability. The main drawback of switched reluctance machines is relatively high cost of them.

2.1.3 Configuration of HEVs and PHEVs

HEVs, as described before, have a combination of ICE and at least one electric source of energy to increase the efficiency of the vehicle. HEVs can be categorized as series configuration and parallel configuration. In a series configuration (fig. 2.2) the ICE is coupled to a generator in order to charge the battery. Then, battery provides the propulsion for the electric motor. In the series configuration, the vehicle has lower fuel consumption in the city driving by making the ICE operate at the highest efficiency point during the frequent stops/starts.

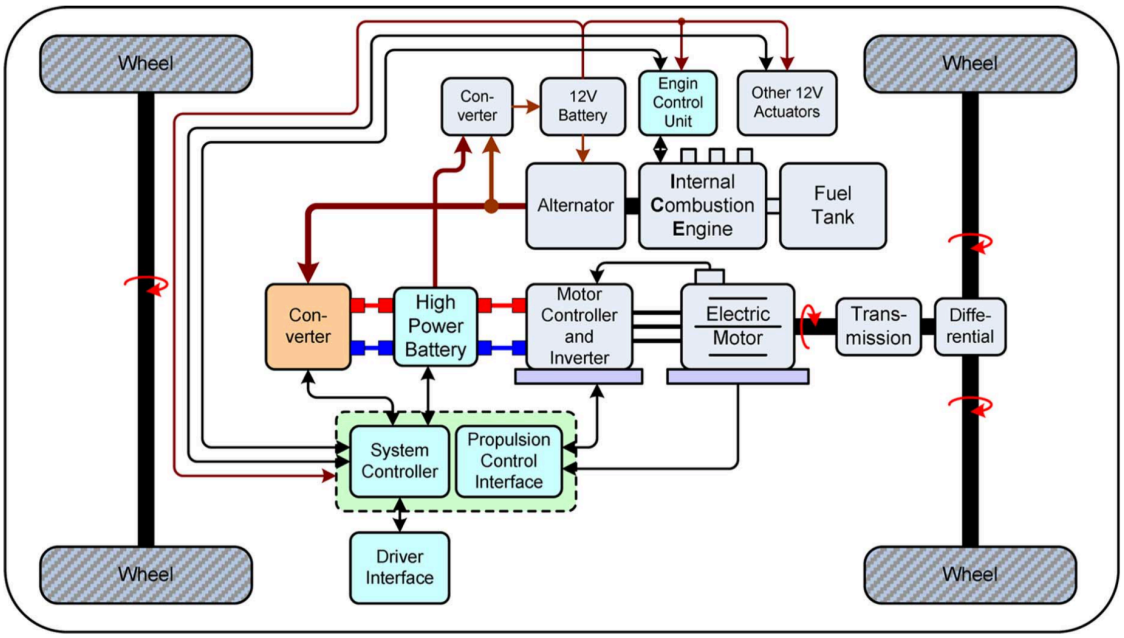


Figure 2.2. Series HEV configuration

In a parallel configuration (fig. 2.3), the engine and the electric motor can be used separately or together to propel the vehicle. A parallel HEV has lower fuel consumption in highway driving by making the ICE operate at highest efficiency point when the vehicle is running at a constant speed.

Plug-in hybrid electric vehicles (PHEVs) have a high energy density battery, which can be charged directly by an ac outlet in an urban station or a domestic garage. Therefore, PHEVs can drive on only electric power for a longer range than regular HEVs. Another advantage of PHEVs is the improved utilization of power since the battery can be charged during the nighttime when the demand for electric power and its cost are much

lower. Fig. 2.4 presents a parallel configuration for PHEVs where an ac utility and an ac-dc battery charger are considered in the configuration.

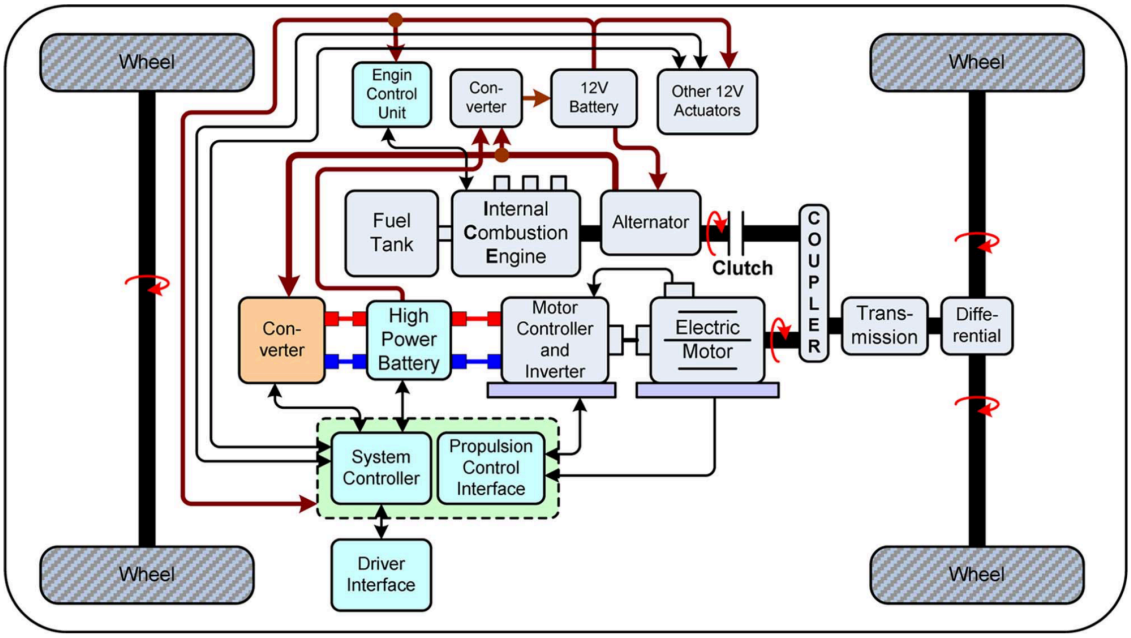


Figure 2.3. Parallel HEV configuration

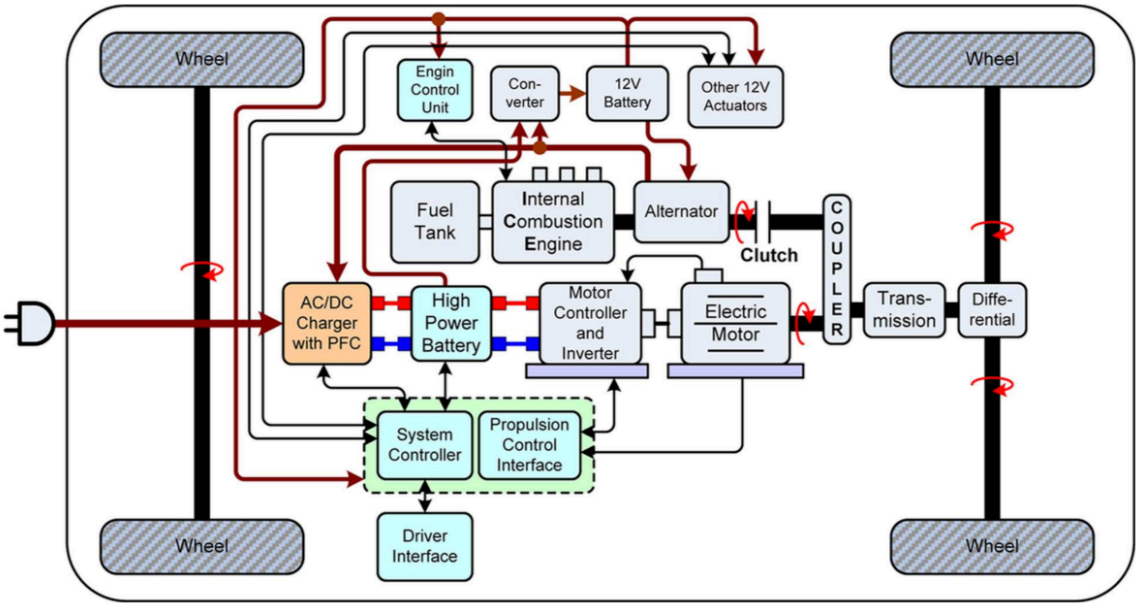


Figure 2.4. Plug-in hybrid electric vehicle (parallel configuration)

In the next section, power electronic requirements of EVs are discussed.

2.2 Power Electronics in EVs

There are three types of power electronic modules in an EV generally. The first power electronic module is a dc-dc converter in series with a dc-ac traction inverter. The input of the dc-dc converter is a battery, an ultracapacitor, a fuel cell, or a combination of them. The output of the dc-dc converter is a regulated dc bus, which is supposed to be the input of the inverter. In the case of batteries and ultracapacitors, the dc-dc converter must be bidirectional to be able to charge the ESS in regenerative braking mode. Since fuel cell cannot be electrically charged, the dc-dc converter is unidirectional in FCVs. The roles of the dc-dc converter are: 1) provide a regulated dc bus for the inverter, 2) discharge the ESS and provide power for propulsion in driving mode, 3) charge the ESSs (battery and/or ultracapacitor) in regenerative braking mode, and 4) power management between ESSs in the case of a combination of ESSs.

The second power electronic module is an ac-dc rectifier in series with a dc-dc converter as the battery charger of the EV. The EV in this case is called plug-in electric vehicle (PEV) since it can be plugged in an ac outlet and be charged. If the battery charger is installed in the EV, it is called *'on-board'*; otherwise, the battery charger is included in the ac outlet facility and is called *'off-board'*. In a vehicle-to-grid (V2G), the EV can also provide power to ac grid. In this case the dc-dc converter of the battery charger is bidirectional. In a V2G, the ESS (battery and/or ultracapacitor) will be charged during the nighttime when the demand for electric power (and its corresponding cost) is low. Then, the ESS can also give back or in a precise word sell the electric power to the ac grid in the peak electric power demand time of the electric network based on the EV owner's will.

The third electronic power module in an EV is a unidirectional dc-dc converter which provides electric power from the ESS for the low voltage electronic loads of the vehicle such as lights, accessories, heaters, control systems, etc.

The first main power electronic module in EVs is the dc-dc converter for drive and power management purposes and it has these characteristics:

1) Buck, Boost, Buck-Boost: If the voltage level of the ESS (the input of the dc-dc converter) is higher than the voltage level of the regulated dc bus (the output of the dc-dc converter and the input of the inverter), the dc-dc converter needs to have a buck

topology. If the voltage level of the ESS is lower than that of the regulated dc bus, the topology should be boost. However, if the input voltage has the same level of the output voltage, the topology should be buck-boost. Typically, the input voltage level of the inverter is around 600-650 V. On the other hand, the voltage level of the battery pack is not higher than 300 V. Therefore, a boost topology is needed for the dc-dc converter

2) Unidirectional and Bidirectional: In a unidirectional dc-dc converter, the power direction is only from the input energy source to the output load. In this case, each leg consists of one bidirectional transistor and one unidirectional diode, which is cheaper than a bidirectional transistor. In a bidirectional dc-dc converter when there is also regenerative power flow from the output load to the input energy source, such as the case of battery/ultracapacitor in braking mode, the both switching devices are bidirectional transistors.

3) Non-Isolated and Isolated: dc-dc converter isolation, provided usually by a transformer, adds more cost and loss. The isolation is necessary when low voltage (LV) and high voltage (HV) negative sides cannot be grounded together and the voltage ratio between LV and HV is high enough where the converter cannot deal with high current and high voltage at the same time.

4) Single-Phase and Multi-Phase: Single-phase dc-dc converter consists of one-leg high-side low-side switching devices. However, in high-power applications when power (current) rating of the switching device is not high enough to handle the high current, paralleled switching devices should be used as a multi-phase configuration to share the required load current.

5) Single-Input and Multi-Input: A single-input dc-dc converter has only one input source of energy. In the case of the multi-input, there is a combination of ESSs.

In the following figures, different configurations of power management dc-dc converter are presented. In fig. 2.5, the dc-dc converter is boost, bidirectional, non-isolated, single-phase, and multi-input. The two inputs of the dc-dc converter, the battery and the ultracapacitor, are paralleled directly without any additional power electronic modules. Therefore, the controllability of the ESSs is low and the configuration is called passive cascade. In fig. 2.6, the battery and the ultracapacitor are actively cascaded and have different voltage levels. In this case, controllability is higher but the dc-dc converter in

fact consists of two boost converters. One is unidirectional with the battery as the input and the other is bidirectional with the ultracapacitor as the input. In this configuration, in regenerative braking mode, only the ultracapacitor can be charged.

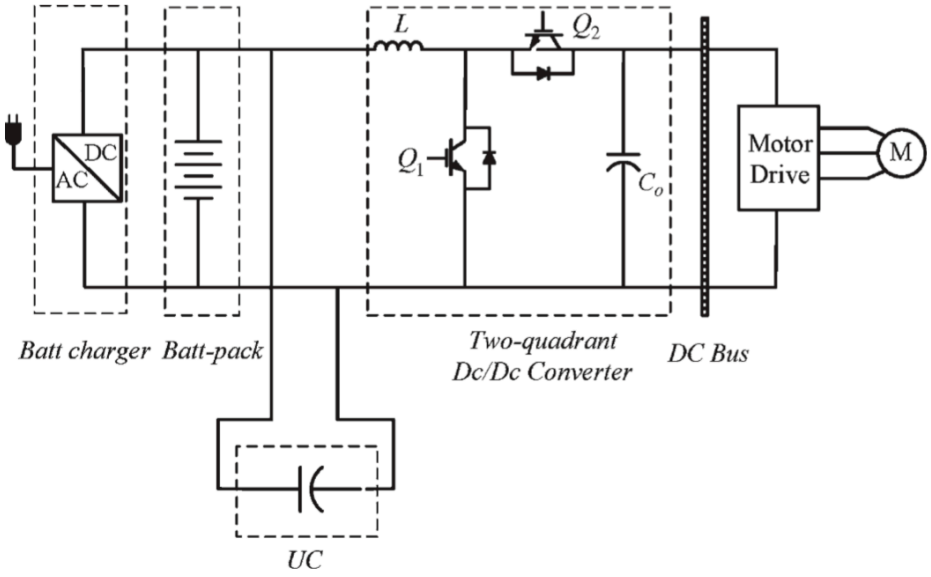


Figure 2.5. Passive cascade battery/ultracapacitor (UC) configuration

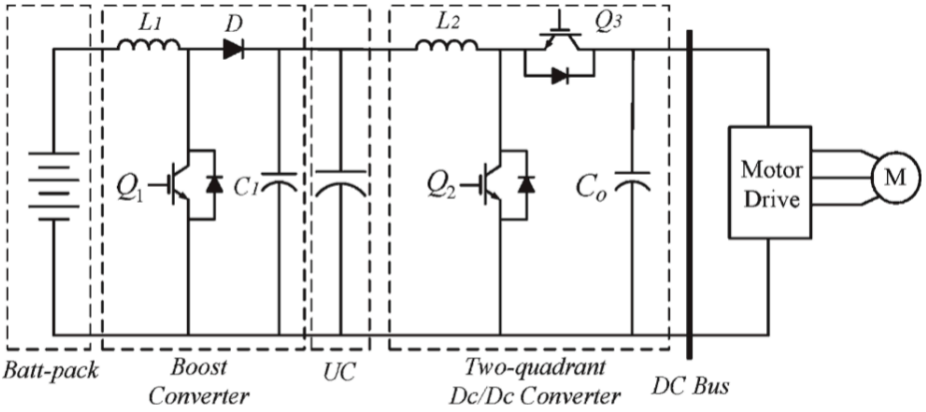


Figure 2.6. Active cascade battery/ultracapacitor (UC) configuration

In fig 2.7, a battery and a fuel cell are actively paralleled. Each of them has their own dc-dc boost converter and the controllability of the system is high. Since the fuel cell cannot be electrically recharged, its dc-dc converter is a unidirectional one. In all of these examples, the topology of the dc-dc converter was *'half-bridge'*. The typical topologies for the non-isolated dc-dc converters are: 1) half-bridge, 2) cascade buck-boost, 3) Cùk, and 4) SEPIC/Luo.

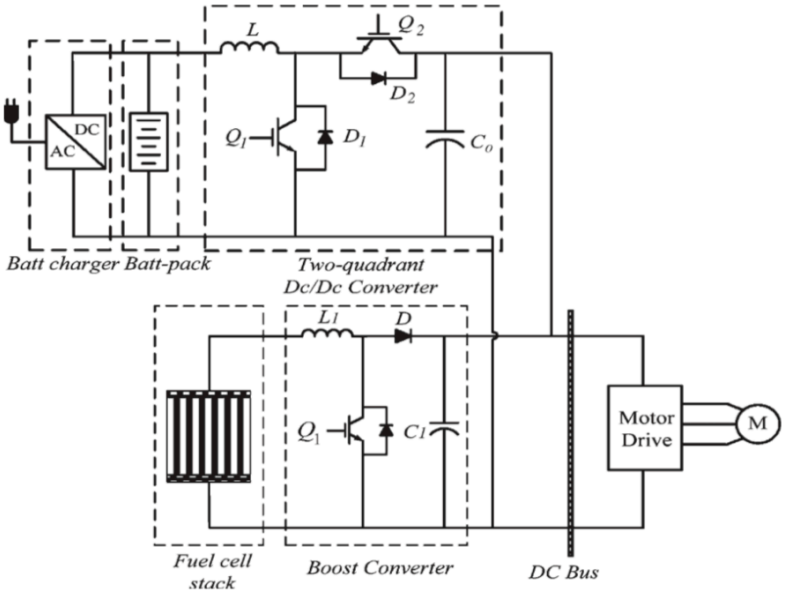


Figure 2.7. Active parallel battery/fuel-cell configuration

1) Half-Bridge: The topology of the half-bridge boost converter is shown in fig. 2.8. The advantage of the half-bridge is simplicity where it needs only one inductor instead of two in comparison with the Cùk and the SEPIC/Luo topologies. Beside, the size of the inductor in the half-bridge is only half the size of that in the Cùk and the SEPIC/Luo. Another advantage of half-bridge is its higher efficiency where the inductor conduction loss and the active components switching loss are lower respect to those of the Cùk and the SEPIC/Luo. The major disadvantage of the half-bridge converter is its discontinuous output current when operating in boost mode. This impacts the size of the output capacitor.

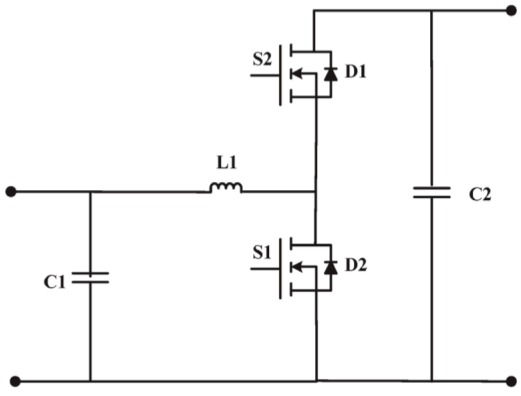


Figure 2.8. Half-bridge topology

2) Buck-Boost: The topology of the buck-boost (fig. 2.9) is similar to the half-bridge with double number of active components. As it was explained before, the buck-boost is needed when the input and the output of the dc-dc converter have the same voltage levels.

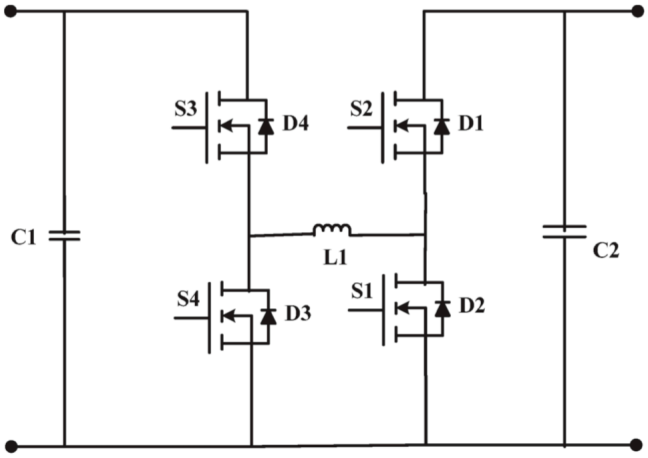


Figure 2.9. Buck-boost topology

3) Cùk: The topology of the Cùk is presented in fig. 2.10. The advantage of the Cùk is the lower input/output current ripple while its drawbacks are the large size of the inductors and the high voltage stress (input voltage plus output voltage) on the transfer capacitor (C_t).

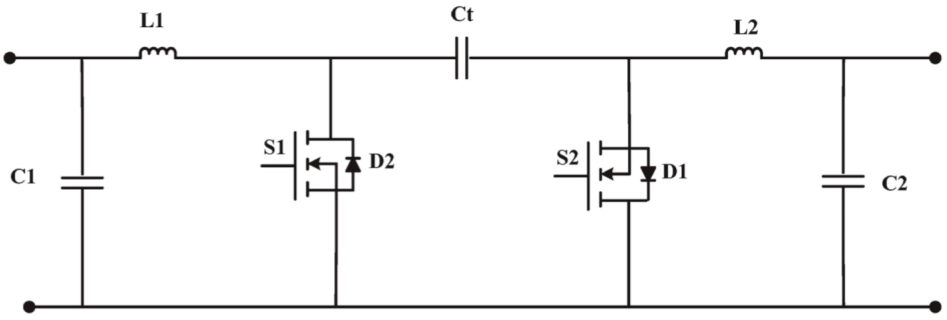


Figure 2.10. Cùk topology

4) SEPIC/Luo: The topology of the SEPIC/Luo is shown in fig. 2.11. The advantage of the SEPIC/Luo, in comparison with Cùk, is the lower voltage stress (only input voltage) on the transfer capacitor C_t while its disadvantages are the large size of the inductors, the same as the Cùk, the discontinuous output current, and the large size of the output capacitor.

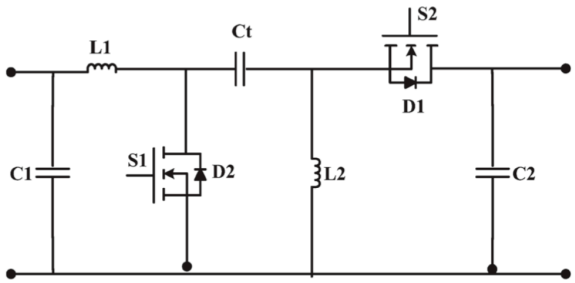


Figure 2.11. SEPIC/Luo topology

The second important power electronic module in EVs is the battery charger. Fig. 2.12 depicts the configuration of a PEV with its all power electronic modules: bidirectional power management dc-dc converter, ac-dc/PFC/dc-dc battery charger, dc-ac traction drive inverter, and unidirectional dc-dc converter. The battery charger consists of an ac-dc rectifier, a power factor correction (PFC), and a dc-dc converter. It can be on-board, which means installed in the vehicle, or off-board, which means included in the ac outlet facility. It can be also bidirectional in the case of V2G. In the configuration of fig 2.12, the output of the battery charger is connected to the regulated dc bus. The other common configuration is where the battery pack is directly connected to the battery charger.

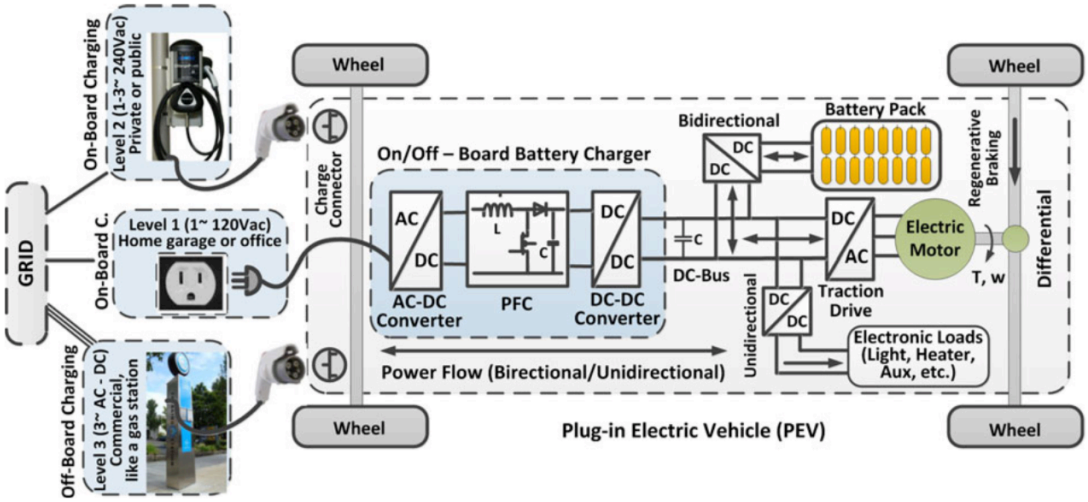


Figure 2.12. On/Off board charging system for PEV

There are three types of battery charger depends on power level, current rating, type of voltage (ac/dc and one-phase/three-phase), charger location, ac outlet facility, interface, and charging time. The characteristics of the three types of battery charging systems (level I, II, and III) are presented in table 2.5.

Table 2.5. *Characteristics of level I, II, and III battery charging systems [9]*

Type of Voltage	Charger Location	AC outlet facility	Supply Interfaces	Power Levels	Charging Times	Vehicle Types
Level I 230 Vac	On-board One-phase	Home garage or office	Convenience outlet	1.9 kW (20 A)	11-36 hours	PHEVs (5-15 kWh)
Level II 400 Vac	On-board Three-phase	Private or public outlet	Electric vehicle supply equipment	4 kW (17 A)	1-4 hours	PHEVs (5-15 kWh)
Level III 208-600 Vac or Vdc	Off-board Three-phase	Public station	Electric vehicle supply equipment	50 kW 100 kW	0.4-1 hour 0.2-0.5 hour	EVs (20-50 kWh)

2.3 Universal DC-DC Converter for PEVs

As it is mentioned in the previous section, there are different configurations in order to connect the battery to the battery charger. In the cascade configuration of fig. 2.13, the ac outlet is connected to the battery in series to the battery charger (included the rectifier, the PFC, and the dc-dc converter #1). Then, the battery is in series with the dc-dc converter #2 to transfer energy between the battery and the traction system.

The available space in a vehicle to be used for installing electrical and mechanical systems is limited. The weight of the vehicle also is an important issue. Therefore, power density (kW/l and kW/kg) is a crucial factor for power electronic modules in EVs. To improve the power density, one idea is to integrate two dc-dc converters: the dc-dc converter #1 of the battery charger and the dc-dc converter #2 of power management with traction system.

Figures 2.14, 2.15, and 2.16 show three state-of-the-art dc-dc converters with four modes of operation: charging/discharging the battery from/to the ac grid; power transfer between the battery and the traction system. Such a multi operational fully directional dc-dc converter in EVs can be named as *'universal'* dc-dc converter (fig. 2.17).

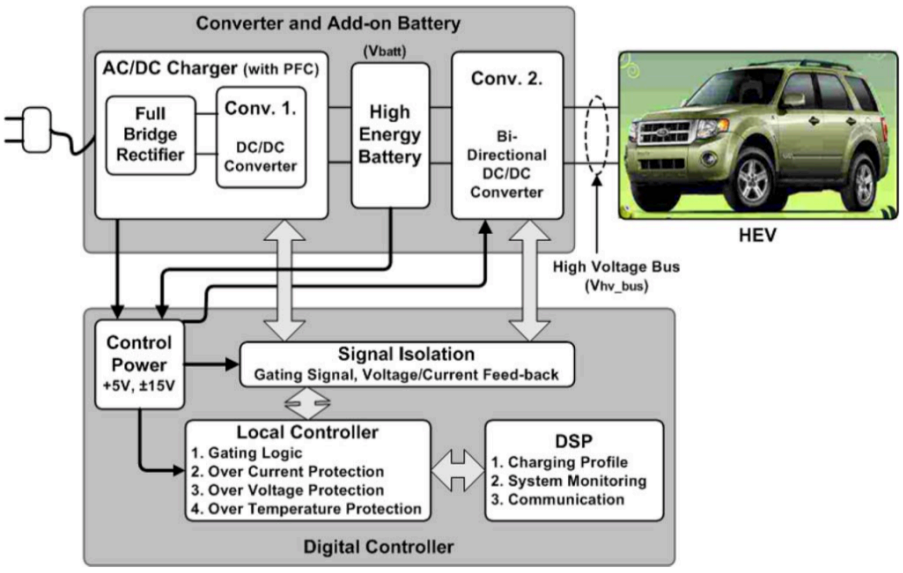


Figure 2.13. Cascade configuration of the battery charger, the battery, the power management dc-dc converter, and the traction system

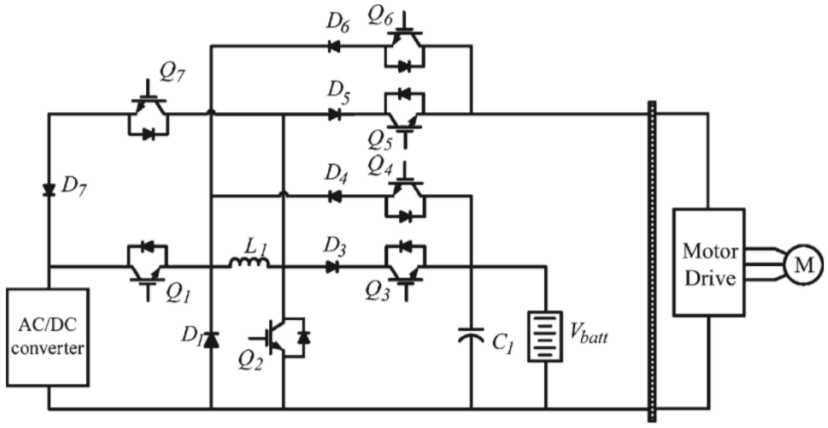


Figure 2.14. Universal dc-dc converter ([2] and [10])

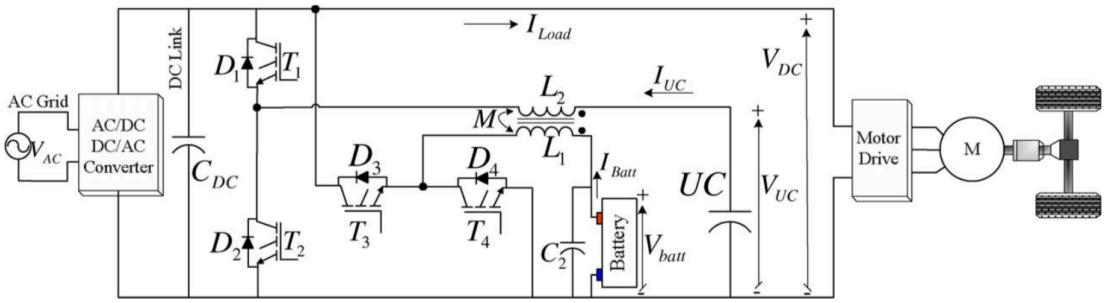


Figure 2.15. Universal dc-dc converter [11]

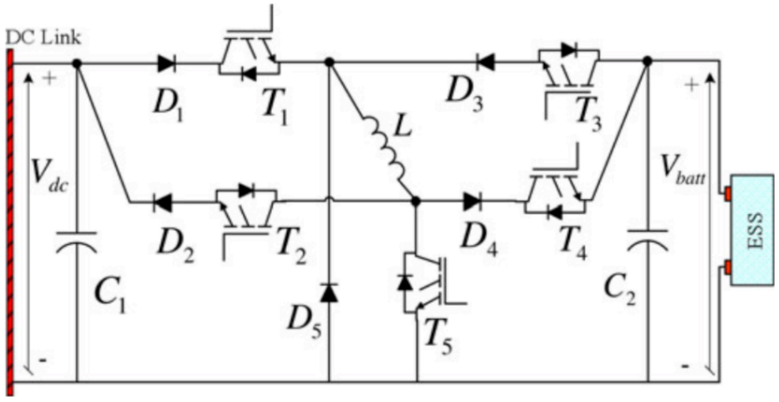


Figure 2.16. Universal dc-dc converter [12]

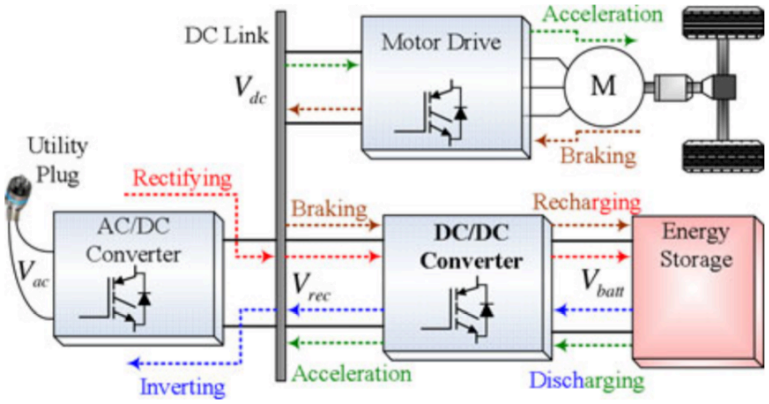


Figure 2.17. Configuration of EV with universal dc-dc converter

In fig. 2.15, the universal dc-dc converter is multi-input with two ESSs, a battery and an ultracapacitor. It has also coupled inductors (L_1 and L_2), which makes the converter more compact.

2.4 Wide Band Gap Devices

In power electronic converters, the most important component is the switching device. Most of the power losses are dissipated in the switching devices: switching loss and conduction loss. In addition, the size of the passive component (inductors and capacitors) is directly related to the characteristics of the switching devices such as switching speed (switching frequency). Operating at a higher switching frequency results in lower current and voltage ripples, which it makes the size of the passive components smaller. On the other hand, the lower ripples cause lower heat, which leads to a smaller heat sink.

Moreover, the operation temperature of the switching devices also defines the requirement for the thermal design. As a result, the switching device has the key role to determine the efficiency and the volume/weight of the converter, which both factors determine the power density of the power electronic converter.

For the last decades, Silicon (Si) switching devices are well established in power electronics. But, Si shows important limitations in blocking voltage capability, operation temperature, and switching frequency. In such a situation, wide band gap (WBG) semiconductors are an enabling technology for high frequency high efficiency power electronics. Among the possible semiconductor materials candidates, Silicon Carbide (SiC) and Gallium Nitride (GaN) represent the best tradeoff between theoretical characteristics (high blocking voltage capability, high temperature operation, and high switching frequency), real commercial availability of the initial material (wafers and epitaxial layers), and maturity of their technology.

The higher breakdown field of WBG semiconductors makes the drift regions of the device thinner, which it results in lower specific ON-resistance. The high mobility of GaN further reduces the ON-resistance. This allows a smaller die size to achieve a given current capability, and therefore lower input and output capacitances. Higher saturation velocity and lower capacitances enable faster switching transients and consequently lower switching loss. In short, the material properties of WBG semiconductors result in a device with lower ON-resistance and switching losses than a Si device with comparable voltage and current capabilities.

Fig. 2.18 compares the material characteristics of Si, SiC, and GaN devices. SiC excels in high temperature applications, while the material characteristics of GaN are superior in high efficiency and high frequency converters. Although GaN theoretically offers better high frequency and high voltage performances, the lack of good-quality bulk substrates needed for vertical devices and the lower thermal conductivity lend SiC the better position for high voltage devices. In fact, some SiC devices, such as Schottky diodes, are already competing with their Si counterparts.

In [15], a comprehensive study is done to investigate superiority of SiC over Si in inverters and dc-dc converters (isolated and non-isolated) for low, medium, and high voltage applications. Regarding to our application, the medium voltage non-isolated dc-

dc converter is of our interest. To perform the comparison, the dc-dc converter of fig. 2.19 is implemented with four switches of both Si and SiC devices.

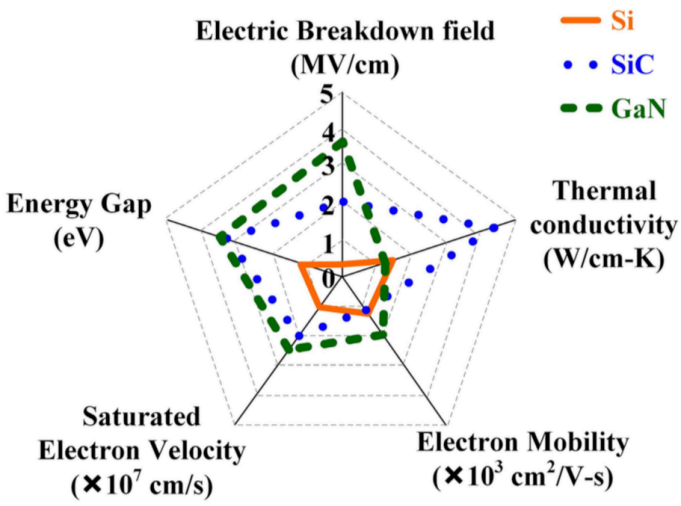


Figure 2.18. Comparison of the material characteristics of Si, SiC, and GaN devices

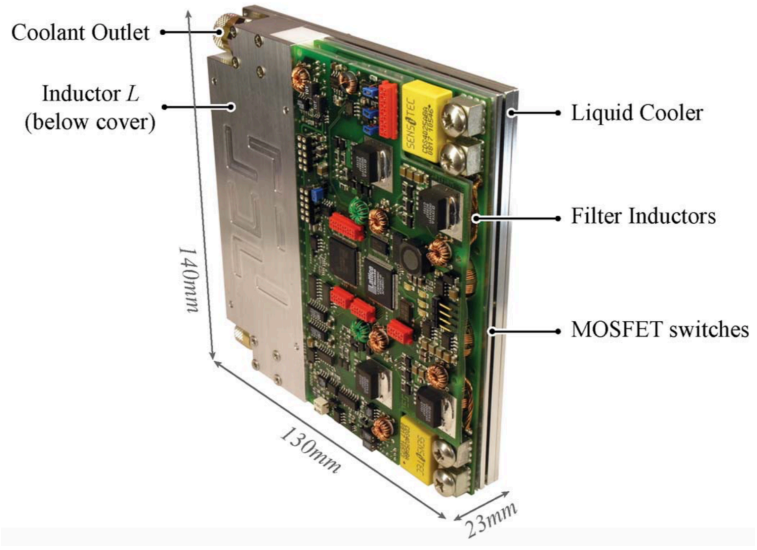


Figure 2.19. Bidirectional buck–boost converter with 150-450 V, 12 kW, and 100 kHz

The comparison of fig. 2.20 is based on chip area and not on current rating since chip area is proportional to cost, and current rating dependents on the application, the switching frequency, and the cooling condition.

For the SiC devices, both soft switching and hard switching are considered. In the case of hard switching, different amounts of peak-to-peak ripple current in the inductor are assumed. In all considered cases, the minimum efficiency is higher than 95%. In the

upper graph, the required chip areas of the switches are shown, and in the lower graph, the efficiency and the theoretical power density are shown.

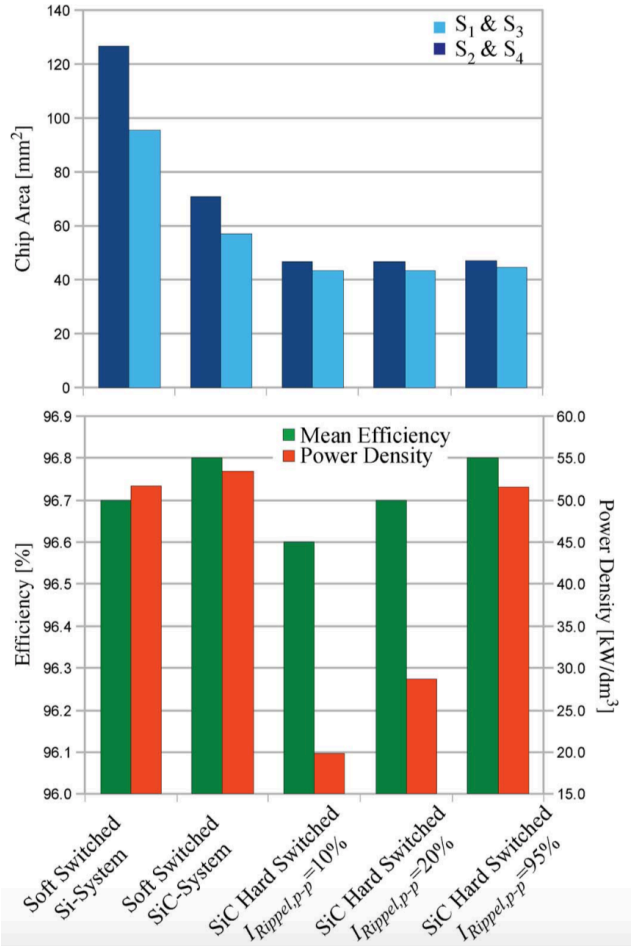


Figure 2.20. Calculation comparison for the non-isolated bidirectional buck–boost converter with Si and SiC [15]

As a conclusion, in medium voltage dc–dc converter, SiC devices offer the possibility of reducing the chip area for a desired efficiency especially for soft-switched applications. It could help to increase the power density as the case of the non-isolated bidirectional buck–boost converter, where the chip area approximately could be reduced to 50% for achieving the same performance with SiC devices.

In the future, SiC devices could show a significant advantage compared with Si devices if the output capacitance of the SiC switches could be reduced significantly, such as GaN devices. This would reduce the switching losses in hard-switched applications resulting in

a better efficiency and/or a more compact design. For this reason, GaN devices have superiority over SiC devices in hard-switched applications.

In [16], commercial GaN devices are studied. There are two structures for GaN devices: vertical and lateral. Vertical GaN devices, using structures similar to their Si and SiC counterparts, can take greatest advantage of the superior GaN material properties. However, the lack of availability of high-quality low-cost GaN wafers has limited these prospects. Vertical devices generally require homoepitaxial fabrication, meaning that the substrate and epitaxial layers are fabricated with the same type of semiconductor (i.e., GaN-on-GaN). However, MIT has developed a method of vertical MOSFET and diode fabrication using a heteroepitaxial GaN-on-Si structure. Because vertical GaN devices have not yet been produced on a commercial level, most of the GaN devices available today are lateral heterojunction field-effect transistors (HFETs), also known as high electron mobility transistors (HEMTs). These devices are typically limited at 600–650 V, and consequently have limitation on power rating unlike those with vertical structure. Because of the lateral heterojunction structure, these devices are fundamentally different from MOSFETs and have unique characteristics such as their reverse conduction behavior and their dynamic drain-source ON-resistance.

There is a current path layer between the drain and the source of the GaN HEMT. This layer, shown in the GaN HEMT structure of fig. 2.21, is called *"two-dimensional electron gas"* (2DEG). Because of the native 2DEG channel, the HFET is depletion-mode (normally-ON) device. This is not desirable for voltage-source converters, because of the potential for shoot-through during startup or loss of control power. One method to fabricate *"enhancement mode"* (e-mode) normally-OFF GaN HEMT is the cascode structure (ex. manufactured by Transphorm). A normally-OFF GaN device can be made using the cascode structure shown in fig. 2.22. Cascode device requires co-packaging of the depletion-mode GaN HEMT with a low-voltage e-mode MOSFET, typically Si. The two dies are connected in such a way that the output (drain-source) voltage of the MOSFET determines the input (gate-source) voltage of the HEMT. In general, controlling the ON/OFF state of the low voltage silicon MOSFET to control the ON/OFF state of the high voltage GaN HEMT makes the cascode GaN HEMT behave as an e-mode device that is compatible with the commercial driver.

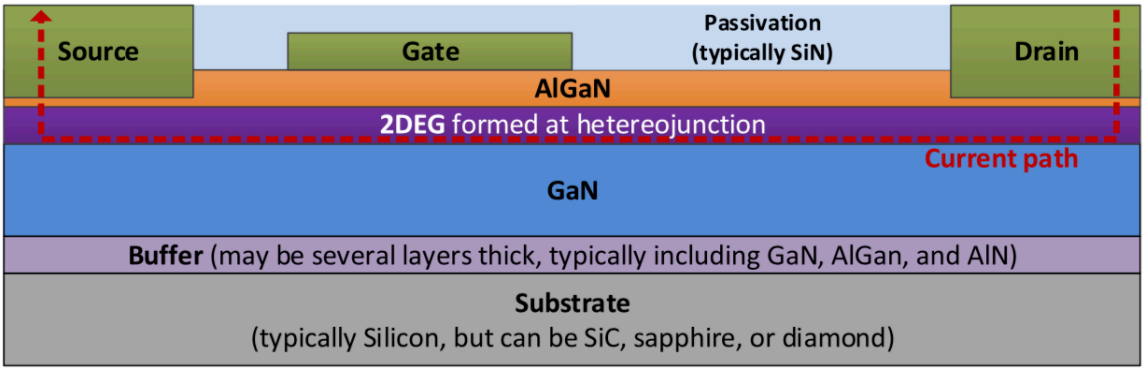


Figure 2.21. Basic structure of depletion-mode lateral GaN HEMT

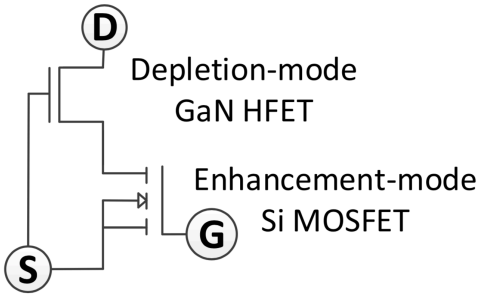


Figure 2.22. Basic structure of depletion-mode lateral GaN HEMT

Although the 2DEG makes the lateral GaN HEMT natively depletion-mode, the gate can be modified to shift the threshold voltage positively and thereby make an e-mode device There are e-mode GaN HEMT devices manufactured by EPC, GaNSystems, or Panasonic. In [18], commercial GaN (fig. 2.23) and SiC (fig. 2.24) devices are listed.

Manufacturers	Voltage Ratings	Current Ratings	Conduction Resistance	Configuration
EPC	15 V~450 V	0.5 A~90 A	1.3 mΩ~2800 mΩ	enhancement mode
Transphorm (Fujitsu)	600 V	9 A~17 A	150 mΩ~290 mΩ	cascaded
	600 V (module)	70 A	30 mΩ	cascaded (half bridge)
	650 V	21 A~47 A	35 mΩ~110 mΩ	cascaded
Infineon (IR)	100 V			cascode
	600 V			
Panasonic (Infineon)	600 V	10 A, 15 A	140 mΩ, 54 mΩ, 71 mΩ	enhancement mode
TI	80 V	10 A	18 mΩ	enhancement
	600 V	12 A	70 mΩ	cascode
GaN Systems	100 V	45 A, 80 A, 90 A	7 mΩ, 15 mΩ	enhancement mode
	650 V	7.5 A~60 A	25 mΩ~200 mΩ	

Figure 2.23. Commercial GaN devices

Manufacturers	Products	Voltage Ratings	Current Ratings
Cree	SiC Schottky diode	600 V, 650 V, 1200 V, 1700 V	1 A~50 A (100 °C)
	SiC MOSFET	900 V, 1200 V, 1700 V	2.6 A~71 A (100 °C)
	SiC power module	1200 V, 1700 V	20 A~325 A
ROHM	SiC Schottky diode	650 V, 1200 V	5 A~40 A (150 °C)
	SiC MOSFET	400 V, 650 V, 1200 V, 1700 V	2.6 A~49 A (100 °C)
	SiC power module	1200 V	80 A~ 300 A (60 °C)
Infineon	SiC Schottky diode	600 V, 650 V, 1200 V	2 A~40 A
	SiC JFET	1200 V	18 A, 25 A (100 °C)
	SiC module (IGBT or CoolMOS + SiC diode)	650 V, 1200 V, 1700 V	30 A~600 A
	SiC MOSFET	1200 V	
	SiC module (SiC MOSFET)	1200 V	
ST	SiC Schottky diode	600 V, 650 V, 1200 V	4 A~20 A
	SiC MOSFET	1200 V	16 A, 34 A, 85 A (100 °C)
Fairchild	SiC Schottky diode	1200 V	15 A, 20 A, 30 A, 40 A (148 °C)
	SiC module (IGBT + SiC diode)	650 V	40 A, 50 A (80 °C)

Figure 2.24. Commercial SiC devices

2.5 SiC-Based and GaN-Based DC-DC Converters for EVs

While SiC and GaN devices are being in to the use of power electronic converters in general, there are efforts at the same time to improve the EV industry using these new technology devices. Especially for the case of dc-dc converters, we review some state-of-the-art and prestigious literatures on SiC-based and GaN-based dc-dc converters in EV application here.

In [19], a dc-dc converter for the aim of power management in EV application is set up with all-silicon (conventional silicon IGBTs and silicon diodes), hybrid (silicon IGBTs with SiC Schottky diodes), and all-SiC (SiC MOSFETs with SiC Schottky diodes) to compare the power losses (switching loss, conduction loss, and inductor/capacitor loss). The specifications of the half-bridge dc-dc converter are presented in table 2.6 and the power loss experiment results are shown in fig. 2.25.

From fig. 2.25, it can be seen that the all-SiC converter has the lowest power losses compared to the hybrid Si/SiC, and the all-Si converters. By increasing the switching frequency from 20 to 200 kHz, the switching loss of the SiC device increases.

In [20], an on-board battery charger for EV application is introduced by APEI, Cree, and Toyota companies. The battery charger consists of two stages: ac-dc bridgeless boost converter and phased-shift full-bridge isolated dc-dc converter (fig. 2.26). In the battery charger, the applied MOSFET is 1200-S080B and the applied diode is 1200-S020B both by Cree with the voltage rating of 1200 V and the current rating of 20 A.

Table 2.6. *Specifications of the converter [19]*

Specifications	Value
Low side voltage	300 [V]
High side voltage	600 [V]
Power rating	20 [kW]
Switching frequency	20, 50, 100, 150, 200 [kHz]
Junction temperature	125 ℃
Inductor	225.6 [µH]
High side capacitor	900 [µF]

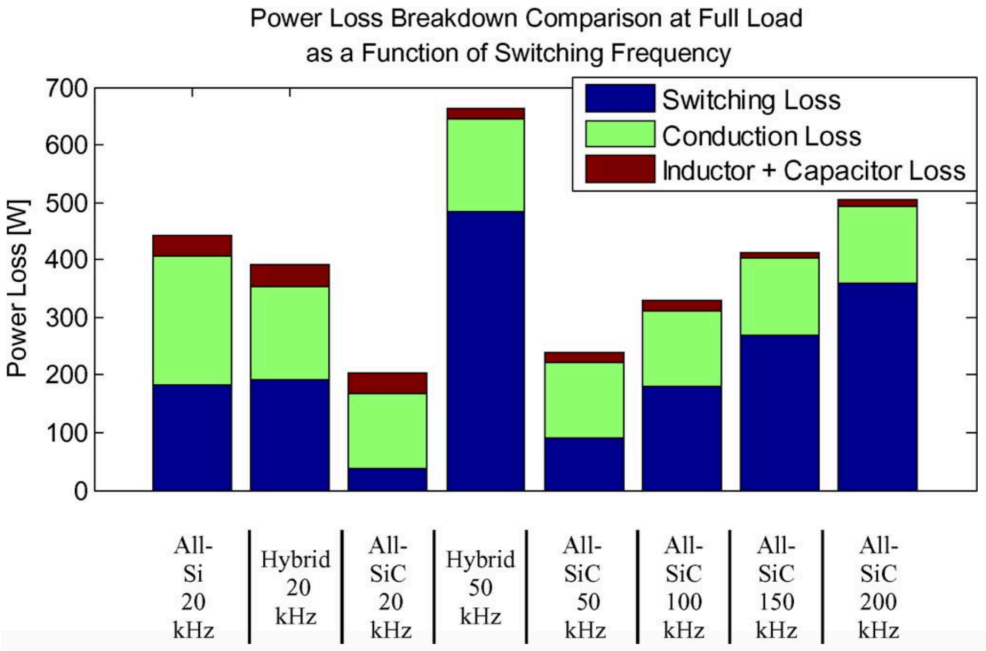


Figure 2.25. Power loss contributors for three type of converters with all-Si, hybrid Si/SiC, and all-SiC devices in different range of switching frequencies [19]

The experiment results of the battery charger show the efficiency of 95% with high volumetric power density of 5.0 kW/L and high gravimetric power density of 3.8 kW/kg where the power electronic module works at the maximum power of 6.1 kW and the switching frequency of 200 kHz.

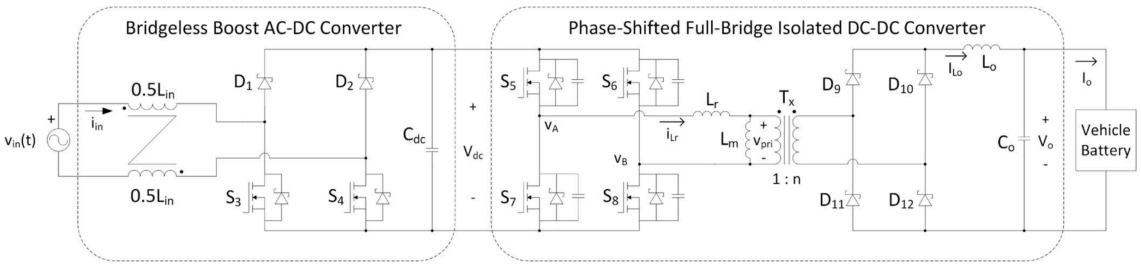


Figure 2.26. Two-stage battery charger

Power electronics research center of ETH Zurich is also working on SiC-based converter. Particularly in the application of EVs, there are examples in which high power density is reported such as a SiC-based power management converter [21] and a SiC-based battery charger [22].

In the case of the GaN-based converter in the application of EVs, there are still less efforts compared to the SiC-based converter. The main limitation is the low power rating of the current commercial lateral GaN devices, which make them suitable for low-to-medium power levels. On the other hand, vertical GaN devices don't have this limitation, however, they are not still commercialized. As a result, GaN devices normally can be applied for the low-to-medium power battery chargers and low-power electronic loads in EVs (fig. 2.27).

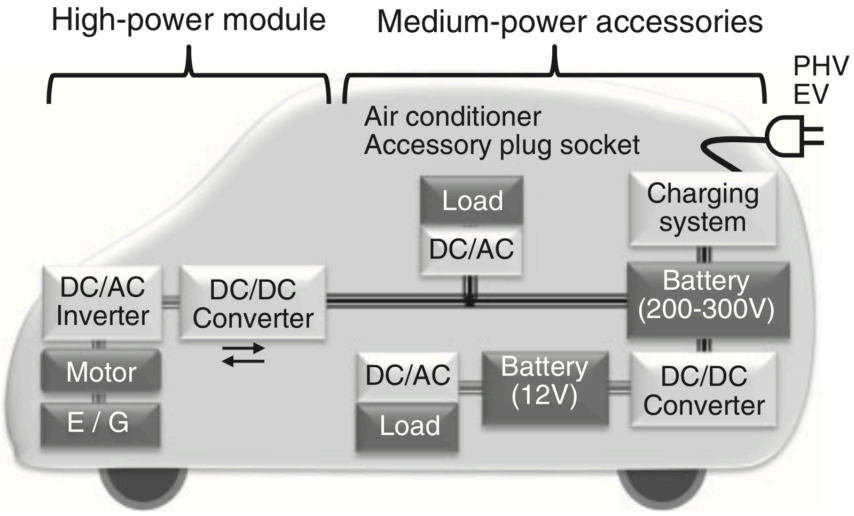


Figure 2.27. Power module categorizing in EVs based on the power level

To close this chapter and have a wider look on the present and the future of GaN devices on EV market, we can review the summary of the report of ABB magazine as follow

[24]. Large GaN power devices are currently at the introduction phase. Very rapid market growth is expected within the next five years leading to sales exceeding $500 million by 2020. Light EV/HEVs constitute the dominant the potential market area for GaN power switch devices. The EV/HEV penetration of the total automotive market is currently very small. The battery cost is the primary factor that determines the EV/HEV manufacturing cost. The growth potential for EV/HEV cars will be greatly improved as battery costs fall below $400/kWh. The EV/HEV combined sales are forecast to reach 30 million units annually by 2025.

Already SiC devices are expected to be introduced that are optimized for 900 V operation and GaN devices will also follow this path. The potential competitive threat offered by SiC is real because the SiC devices offer excellent thermal performance in terms the variation of on-resistance with temperature. It is however the Device Value in terms of performance versus system cost that is critical. The 6-inch starting wafer cost for a GaN-on-Si device is $25-50 while a SiC wafer cost can be $5,000. Even under extremely adverse thermal conditions, 175°C junction temperature, large area GaN devices can have lower ON-resistance than a that of SiC devices, smaller chip area, and far smaller switching losses. The lateral nature of current GaN devices allows for the inclusion of on-chip drivers, very low capacitance, and lower gate charge. However, The automotive market opportunity is possibly the largest that can be addressed by GaN devices. The current market is being served by IGBTs, which are low cost and well understood devices. Displacement of IGBTs will be achieved only when the efficiency improvements and reliability of GaN are well established.

Chapter 3. SiC-GaN-Based Universal DC-DC Converter

3.1 Problem Definition

In chapter 2, dc-dc converter for EVs is discussed. In the case of PEVs, two important dc-dc converters, the battery charger and the power management, are needed to be efficient and compact in order to accelerate the penetration of PEVs in the market. Universal dc-dc converters are a solution to increase the power density in which the two important dc-dc converters are integrated as one module. Such a universal dc-dc converter is full directional with four modes of operation. Here, the configuration of the universal dc-dc converter (fig. 3.1) and its operation modes are reviewed as follow.

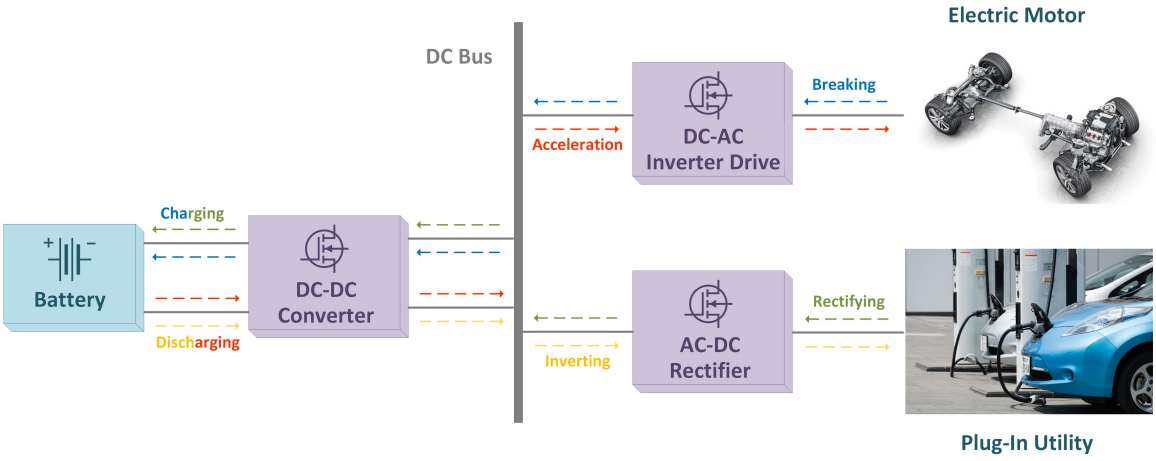


Figure 3.1. Universal DC-DC converter for PEVs

1) Generative/Acceleration Drive Mode: The battery provides the power for the electric motor. The input of the converter is the battery and the output is the regulated dc bus. Therefore, the converter works in boost mode.

2) Regenerative/Braking Drive Mode: The electric vehicle has a negative torque and regenerates the power. This power charges the battery. The input of the converter is the regulated dc bus and the output is the battery. Therefore, the converter works in buck mode.

3) Vehicle-to-Grid (V2G) Plug-In Mode: The battery provides energy to the grid while the electric vehicle is plugged in to the grid. The input of the converter is the battery and the output is the regulated dc bus. Therefore, the converter works in boost mode.

4) Battery Charging Plug-In Mode: The electric vehicle is plugged in to the grid. The grid provides power for the battery. The battery is under charged. The input of the converter is the regulated dc bus and the output is the battery. Therefore, the converter works in buck mode.

A universal dc-dc converter in the application of PEVs should be able to charge the battery. The power rating of a battery charger depends on the ac utility. For an on-board home/office 230 V_{AC} one-phase level I battery charger, the power rating is up to 1.9 kW. For an on-board private/public outlet 400 V_{AC} one- or three-phase level II battery charger, the power rating is up to 19.2 kW. For an off-board filling station 208-600 V_{AC} or V_{DC} three-phase level III battery charger, the power rating is up to 100 kW.

Therefore, if the universal converter is supposed to work as a level I battery charger, it should be able to work at low 1.9 kW power. On the other hand, the universal dc-dc converter should provide the power for the regulated dc bus of the traction inverter. The power rating for drive purpose is at least 30-40 kW for a small PEV. In the case of a large sedan it could be around 150 kW. As a result, the universal converter should be able to work in the range of 1-30 kW for the case of a small PEV and 1-150 kW in the case of a large sedan.

Another solution to progress PEVs in the market is to apply WBG devices such as SiC and GaN in power electronic modules in order to improve the efficiency and the power density. WBG devices have superiority over Si devices in the term of the switching frequency and the power losses.

The nominal voltage of the regulated dc bus in the application of PEVs is 600 V. Table 3.1, presents the main characteristics of two state-of-the-art GaN (GS66516T) and SiC (SCT3017AL) devices. The GaN device has a very low gate charge ($Q_{G(tot)}$) and consequently a very lower switching power loss in hard-switched applications. However, the available lateral structure GaN devices in the market have limitation on the rating power (unlike the expected GaN devices with a vertical structure in the future). The drain current (I_D) rating of the GaN GS66516T is 60 A. Consequently, GaN devices are suitable only for low-to-medium power applications such as on-board battery charger for PEVs (up to 15 kW). In fact, lateral GaN devices cannot be used for high power applications such as dc-dc power management converter neither in the dc-dc universal

converter; the both cases for PEV application. However, if we want to have the advantages of the compact universal dc-dc converter and the efficient lateral GaN devices at the same time for PEVs, we need to find a way to use the lateral GaN in the universal dc-dc converter.

Table 3.1. Characteristics of the GaN and the SiC devices

Parameters	GaN GaNSystems (GS66516T)	SiC ROHM (SCT3017AL)
V_{DS} [V]	650	650
$R_{DS(on)}$ [$m\Omega$]	25	17
I_D [A]	60	118
$Q_{G(tot)}$ [nC]	12.1	172
Q_{rr} [nC]	0	206
C_{iss} [pF]	520	2884
C_{oss} [pF]	130	148
$V_{GS(th)}$ [V]	1.1 – 1.3	2.7 – 5.6

In power electronics, when the switching devices have lower current rating than the demanded load current, the solution is to use multi-phase topology in which the switching devices are paralleled to share the demanded load current. For the case of a small PEV in which the universal dc-dc converter needs to provide 1-30 kW range of power, using multi-phase topology with GaN devices is practical. But, this is not the case for a large sedan in which the universal dc-dc converter needs to provide 1-150 kW of power. In this case, a multi-phase topology with ten legs of paralleled GaN devices are needed which is not feasible because of the complexity.

The innovative idea of the thesis, to have the advantage of using the lateral GaN in the universal dc-dc converter, is to parallel different devices in a multi-phase topology. The example of this idea in the thesis is a universal two-phase SiC-GaN-based dc-dc converter with a power rating of 40 kW in which one GaN-based leg (to provide up to 15 kW) is paralleled with one SiC-based leg (to provide up to 25 kW). The idea of paralleling different devices can be modified for any specific application (not only PEVs)

and any specific power rating. In this way, for another application and another power rating, the designer can optimally find the best number of phases and the best combination of different devices to reach the maximum efficiency and/or the maximum power density.

Paralleling different devices has not been applied in the past. In a conventional multi-phase converter, one of the objectives is to have the same current sharing for all the phases. The main reason is about safe operation of the converter. Generally, the resistance of the diodes has a negative temperature coefficient. It means the resistance of the diodes becomes smaller with a higher temperature. Therefore, if the converter has a mismatched current sharing, the diode with the higher current will face a higher temperature and consequently a smaller resistance. The smaller resistance leads to even higher current sharing. Finally, the feed-forward situation may cause instability for the converter. Fortunately, in our case, there is no switching diode. Because, in a bidirectional topology, both high side (HS) and low side (LS) switches are transistors and there is no unidirectional diode. Moreover, in the proposed two-phased SiC-GaN-based dc-dc converter, there is no anti-parallel diode. First, GaN transistors have no body diodes and are naturally capable of reverse conduction. Therefore, they have no need for anti-parallel diodes as an important advantage of this technology. Second, the SiC power MOSFET used in the proposed converter (SiC SCT3017AL) has a body diode with a very similar characteristic of a typical anti-parallel diode. Therefore, it is possible to avoid the use of the anti-parallel diodes also for the SiC SCT3017AL. All together, the safety operation issue related to unbalanced current sharing is not a matter in our case.

In the next section the configuration of the proposed converter and the power stage design is discussed.

3.2 Configuration and Power Stage Design

Based on what is reviewed and discussed till now, we need a universal two-phase dc-dc converter for the application of PEVs in which one phase is GaN-based and the other phase is SiC-based. In our application of a PEV, the voltage of the battery is considered to be 300 V and the voltage of the regulated dc bus is considered to be 600 V. When the universal dc-dc converter works in generative/acceleration drive mode or in V2G plug-in

mode, the input of the converter is the battery and the output is the regulated dc bus. Therefore, for these two modes of operation, the converter needs to have a boost topology. Considering a two-phase boost converter in which both HS and LS devices are bidirectional transistors, the converter inherently is a buck converter when it works in regenerative/braking drive mode and in battery charging plug-in mode as its input is the high voltage regulated dc bus and its output is the low voltage battery. As a result, the proposed dc-dc converter has a two-phase boost topology, while we are aware of its bidirectional nature. Referring to the context of PEVs, we call the proposed converter as "universal". All together, the configuration of the proposed converter can be designed as the presented converter in fig. 3.2.

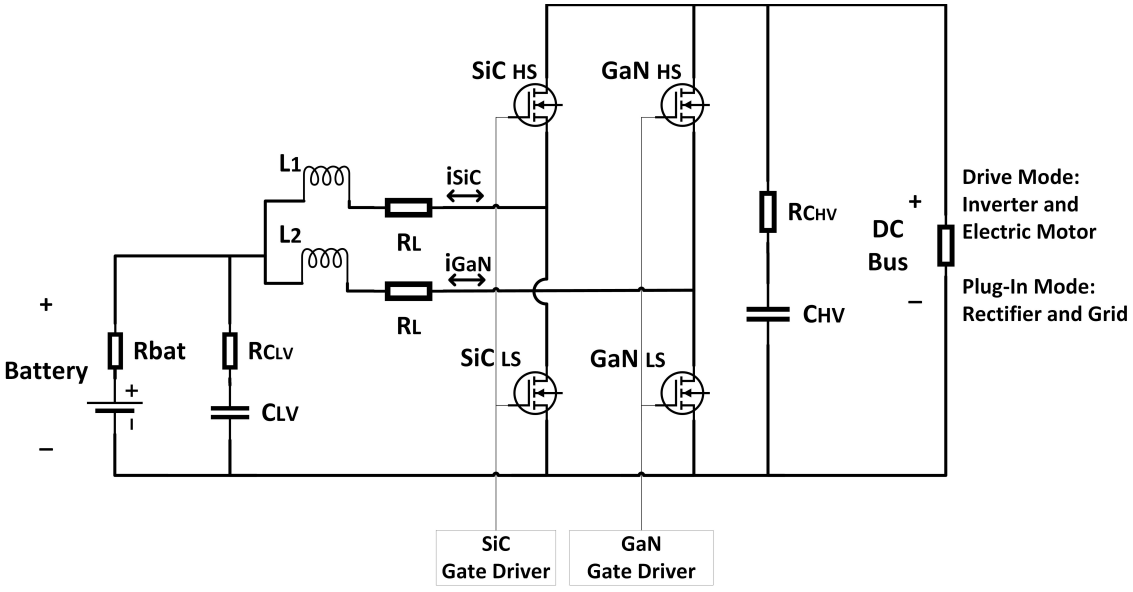


Figure 3.2. Configuration of the SiC-GaN-based converter

Active devices (SiC SCT3017AL and GaN GS66516T) are already selected. Now, we need to calculate passive components L_1, L_2, C_{HV}, and C_{LV}. To design the inductances, first, it should be decided if the converter is going to operate in continuous conduction mode (CCM) or discontinuous current mode (DCM). In one of the main references of this thesis on the universal dc-dc converters for PEVs, CCM is considered for all range of power [11]. Here, we follow the same method of designing the inductances, so that the minimum current is considered in the formula 3.1:

$$L = \frac{V_{HV} \times \left(1 - \frac{V_{LV}}{V_{HV}}\right) \times \left(\frac{V_{LV}}{V_{HV}}\right)^2}{\Delta I_{L(P.U.)} \times I_{L(min)} \times f_{sw}} \qquad (3.1)$$

where V_{LV} is the battery voltage, V_{HV} is the regulated dc bus voltage, f_{sw} is the switching frequency, and $\Delta I_{L(P.U.)}$ is the per unit current ripple of the inductors. In addition, $I_{L(min)}$ is the minimum inductor currents and should be calculated considering the minimum demanded power. As it is discussed in section 3.1, the minimum power for the converter is 1 kW. For a demanded power up to 15 kW, only the GaN phase is supposed to provide the power. Therefore, the minimum inductor current of the GaN phase ($I_{L2(min)}$) will be obtained as:

$$I_{L2(min)} = \frac{P_{(min)}}{V_{LV}} = 3.3\ [A], \quad P_{(min)} = 1\ [kW], \quad V_{LV} = 300\ [V] \qquad (3.2)$$

To calculate the minimum inductor current of the SiC phase ($I_{L1(min)}$), we consider a minimum power of 1 kW as well. Then, we will have $I_{L1(min)} = I_{L1(min)} = 3.3\ [A]$. As it is described in section 3.1, it is the case when the demanded power is more than 15 kW (the power rating of the GaN phase) and the SiC phase needs to provide the rest of the demanded power.

All together, the inductances of the both phases and their corresponding parameters are summarized in table 3.2.

Table 3.2. *Inductor Design*

Parameter	Value
$\boldsymbol{V_{LV}}$	$300\ [V]$
$\boldsymbol{V_{HV}}$	$600\ [V]$
$\boldsymbol{\Delta I_{L(P.U.)}}$	0.3
$\boldsymbol{P_{(min)}}$	$1\ [kW]$
$\boldsymbol{I_{L(min)}}$	$3.3\ [A]$
$\boldsymbol{f_{sw}}$	$10\ [kHz]$
$\boldsymbol{L_1 = L_2}$	$7.5\ [mH]$

The capacitance of the high voltage capacitor can be calculated as follow:

$$C_{HV} = \frac{I_{out(max)} \times \left(1 - \frac{V_{LV}}{V_{HV}}\right)}{\Delta V_{HV} \times f_{sw}} \qquad (3.3)$$

where $\Delta V_{HV} = \Delta V_{HV(P.U.)} \times V_{HV}$ and $\Delta V_{HV(P.U.)}$ is the per unit output voltage ripple which considered as 0.05. In addition, $I_{out(max)}$ is the maximum current of the output in a boost configuration. Therefore, to calculate $I_{out(max)}$, we need to know the current at the high voltage side of the converter at the rating power (40 kW):

$$I_{out(max)} = \frac{P_{(rating)}}{V_{HV}} = 66.7\ [A] \qquad (3.4)$$

Replacing the parameters in formula 3.3 results in $C_{HV} = 111\ \mu F$.

The capacitance of the low voltage capacitor can be calculated as follow [22]:

$$C_{LV} = \frac{\left(\frac{V_{LV}}{V_{HV}}\right)}{8 \times L \times \Delta V_{LV} \times f_{sw}} \qquad (3.5)$$

where $\Delta V_{LV} = \Delta V_{LV(P.U.)} \times V_{LV}$ and $\Delta V_{LV(P.U.)}$ is the per unit output voltage ripple which is considered as 0.05.

Replacing the parameters in formula 3.5, it results in $C_{LV} = 27.7\ \mu F$.

3.3 Modeling

To obtain the mathematical model of the converter, first we need to investigate the time intervals. Here, we analyze the boost mode where a voltage ratio equal to 2 is needed ($V_{in} = 300\ [V]$ and $V_o = 600\ [V]$). The duty cycle of a boost converter and its voltage ratio are formulated as follow:

$$D = 1 - \frac{V_{in}}{V_o} \times \eta \qquad (3.6)$$

where η is the efficiency of the converter. Since, efficiency is always less than 1, the duty cycle of the converter in boost mode is always more than 50 percent.

On the other hand, a fixed frequency PWM modulation is considered for the proposed converter. The PWM modulation of the phases is supposed to have a time shift of 180° to realizes the interleaved inductor currents. In an interleaved two-phase converter, the switching commands of the phases have a time shift of $T_{sw}/2$ where $T_{sw} = 1/f_{sw}$ is the time period.

Considering these two facts, the possible inductor currents are depicted as fig. 3.3:

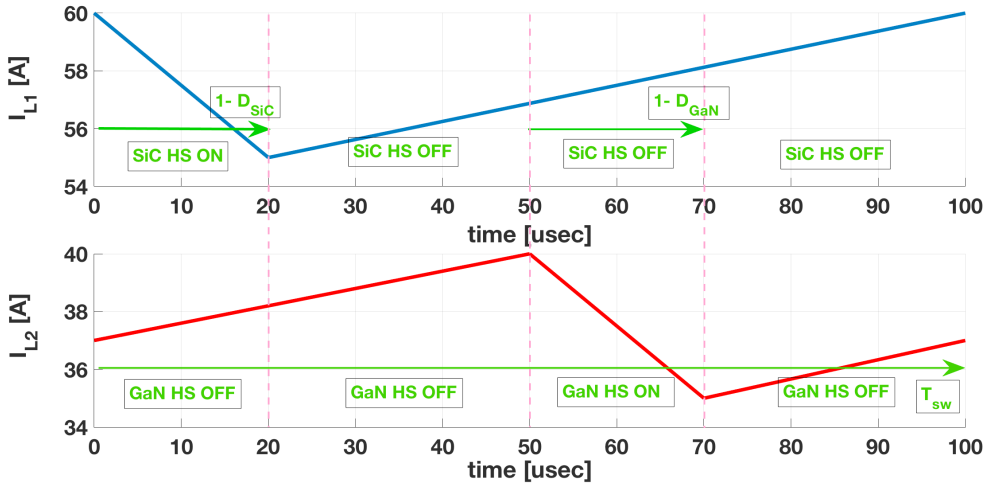


Figure 3.3. Investigation of the time intervals: inductor currents

As we can see in fig. 3.3, there are three time intervals for the converter:

1) The HS SiC is switched-ON and the HS GaN is switched-OFF (fig. 3.4) where the inductor current of the SiC phase (I_{L1}) is discharging through the HS SiC and the output load; while the inductor current of the GaN phase (I_{L2}) is charging through the LS GaN.

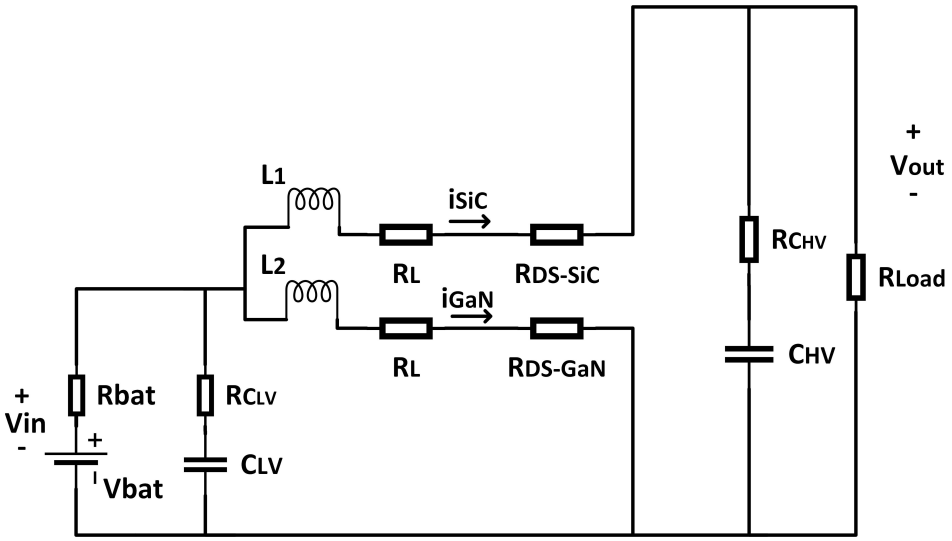


Figure 3.4. The circuit topology of the first time interval

2) The HS SiC is switched-OFF and the HS GaN is switched-ON (fig. 3.5) where the inductor current of the SiC phase (I_{L1}) is charging through the LS SiC; while the inductor current of the GaN phase (I_{L2}) is discharging through the HS GaN and the output load.

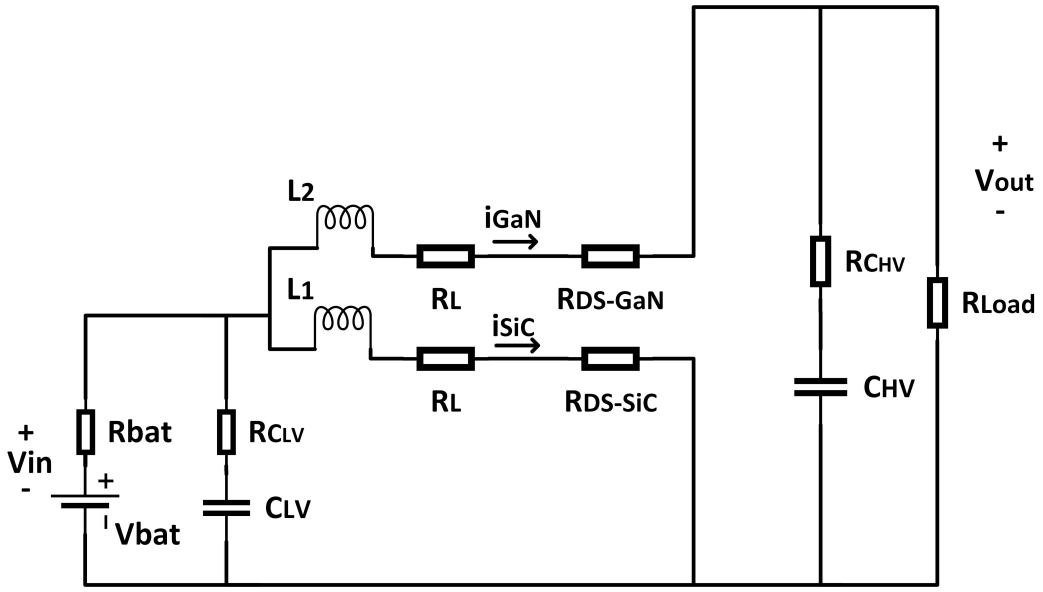


Figure 3.5. The circuit topology of the second time interval

3) The HS SiC and the HS GaN are both switched-OFF (fig. 3.6) where both the inductor current of the SiC phase (I_{L1}) and the inductor current of the GaN phase (I_{L2}) are charging through the LS SiC and the LS GaN respectively.

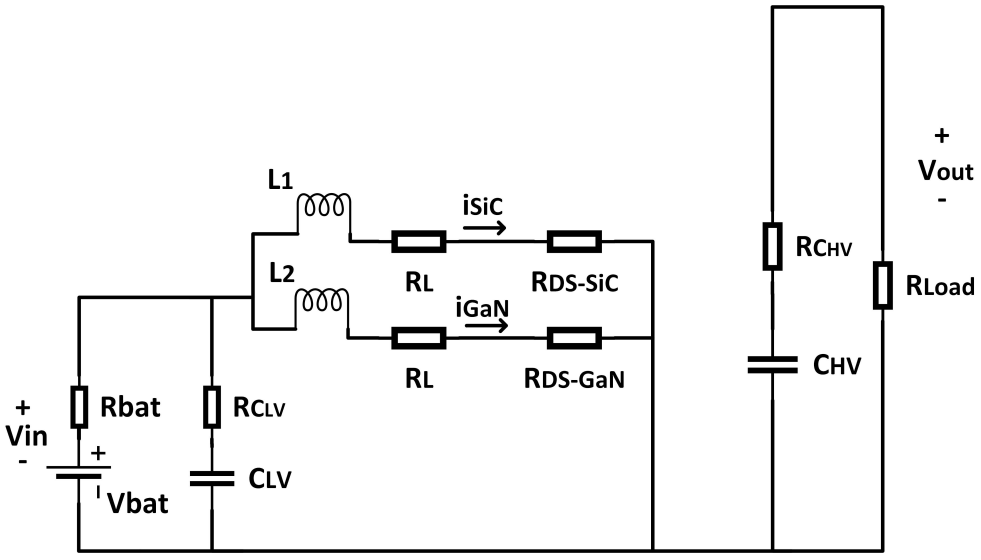


Figure 3.6. The circuit topology of the third time interval

Based on the circuit analysis theory, the differential equations of the first time interval can be obtained as (3.7) in which the time duration of $T_{sw}\times(1-D_{SiC})$ where D_{SiC} is the duty cycle of the SiC phase:

$$a)\ L\frac{di_{SiC}}{dt} + i_{SiC}(R_L + R_{DS-SiC}) = v_{in} - v_{out}$$

$$b)\ L\frac{di_{GaN}}{dt} + i_{GaN}(R_L + R_{DS-GaN}) = v_{in}$$

$$c)\ C_{LV}\frac{dv_{C_{LV}}}{dt} = \frac{V_{bat} - v_{in}}{R_{bat}} - (i_{SiC} + i_{GaN})$$

$$d)\ v_{in} = v_{C_{LV}} + R_{C_{LV}}C_{LV}\frac{dv_{C_{LV}}}{dt} \qquad (3.7)$$

$$e)\ C_{HV}\frac{dv_{C_{HV}}}{dt} = i_{SiC} - \frac{v_{out}}{R_{load}}$$

$$f)\ v_{out} = v_{C_{HV}} + R_{C_{HV}}C_{HV}\frac{dv_{C_{HV}}}{dt}$$

where $i_{SiC} = i_{L1}$, $i_{GaN} = i_{L2}$, and R_{DS-SiC} is the drain-source ON-resistance of the SiC device, and R_{DS-GaN} is the drain-source ON-resistance of the GaN device.

The differential equations of the second time interval can be obtained in the same of those of the first time interval analogously while SiC indicators should be replaced with GaN indicators and vice versa. The time duration of the second time interval is $T_{sw}\times(1 - D_{GaN})$ where D_{GaN} is the duty cycle of the GaN phase.

The differential equations of the third time interval are obtained in (3.8) with a time duration of $T_{sw}\times(D_{SiC} + D_{GaN} - 1)$:

$$a)\ L\frac{di_{SiC}}{dt} + i_{SiC}(R_L + R_{DS-SiC}) = v_{in}$$

$$b)\ L\frac{di_{GaN}}{dt} + i_{GaN}(R_L + R_{DS-GaN}) = v_{in}$$

$$c)\ C_{HV}\frac{dv_{C_{HV}}}{dt} = -\frac{v_{out}}{R_{load}} \qquad (3.8)$$

$$d)\ v_{out} = v_{C_{HV}} + R_{C_{HV}}C_{HV}\frac{dv_{C_{HV}}}{dt}$$

To simplify the equations, the series resistances of the battery (R_{bat}), the low voltage capacitor ($R_{C_{LV}}$), and the high voltage capacitor ($R_{C_{HV}}$) can be neglected. In this way, the *"state space equations"* of the converter in the boost mode will be obtained as (3.9):

$$A)\ \frac{di_{SiC}}{dt} = i_{SiC}\left[-\frac{(R_L + R_{DS-SiC})}{L}\right] + V_{bat}\left[\frac{1}{L}\right] + v_{out}\left[-\frac{(1 - D_{SiC})}{L}\right]$$

$$B)\ \frac{di_{GaN}}{dt} = i_{GaN}\left[-\frac{(R_L + R_{DS-GaN})}{L}\right] + V_{bat}\left[\frac{1}{L}\right] + v_{out}\left[-\frac{(1 - D_{GaN})}{L}\right]$$

$$C)\ \frac{dV_{C_{LV}}}{dt} = 0 \tag{3.9}$$

$$D)\ \frac{dv_{C_{HV}}}{dt} = i_{SiC}\left[\frac{1 - D_{SiC}}{C_{HV}}\right] + i_{GaN}\left[\frac{1 - D_{GaN}}{C_{HV}}\right] - v_{out}\left[\frac{1}{C_{HV}R_{load}}\right]$$

To linearize the state space equations of (3.9), *"small signal method"* is applied. Then, the linear equations of the converter will be obtained as (3.10):

$$I_{SiC} = -V_{out}.\frac{(1 - D_{SiC})}{R_L + R_{DS-SiC}} + V_{in}.\frac{1}{R_L + R_{DS-SiC}}$$

$$I_{GaN} = -V_{out}.\frac{(1 - D_{GaN})}{R_L + R_{DS-GaN}} + V_{in}.\frac{1}{R_L + R_{DS-GaN}} \tag{3.10}$$

$$V_{out} = I_{SiC}.(1 - D_{SiC}).R_{load} + I_{GaN}.(1 - D_{GaN}).R_{load}$$

where I_{SiC}, I_{GaN}, V_{in}, and V_{out} are the steady state values of the inductor current of the SiC phase, the inductor current of the GaN phase, the input voltage, and the output voltage respectively.

Replacing the steady state values of the voltages $V_{in} = V_{LV} = 300\ [V]$ and $V_o = V_{HV} = 600\ [V]$ in (3.10), the duty cycles of the SiC phase (D_{SiC}) and the GaN phase (D_{GaN}) in steady state will be obtained as (3.11):

$$D_{SiC} = 0.5 + (R_L + R_{DS-SiC}).\left[\frac{1}{R_{load}} - \frac{1}{R_{GaN-ratting}}\right]$$

$$D_{GaN} = 0.5 + \frac{(R_L + R_{DS-GaN})}{R_{load}}, \quad R_{load} \le R_{GaN-ratting} \tag{3.11}$$

$$D_{GaN} = 0.5 + \frac{(R_L + R_{DS-GaN})}{R_{GaN-ratting}}, \quad R_{load} > R_{GaN-ratting}$$

where $R_{GaN-ratting}$ is the output load resistance at the GaN phase power rating and can be calculated as (3.12):

$$R_{GaN-ratting} = \frac{P_{GaN-ratting}}{V_o} = 24\ [\Omega],\ \ P_{GaN-ratting} = 15\ [kW],\ \ V_o = 600\ [V] \tag{3.12}$$

In the next section, a comprehensive power loss analysis will be performed with Spice-based OrCAD simulations. In the simulations, steady state equations of (3.11) are applied to obtain the amounts of the duty cycles for low to full load. As we will see, the simulation results verify the accuracy of the modeling as well.

3.4 Power Loss Analysis

In this section, we are going to investigate all the power loss contributors for the proposed converter in different amounts of the demanded power. In addition, in order to show the advantage of the proposed converter in the term of the power losses and the efficiency, it should be compared with the possible alternative for the same application. As it is discussed in the previous sections, the superiority of the SiC and the GaN technologies over the Si technology has already been proved in the literatures. Besides, the main idea of the thesis is to the GaN, although its low power rating, in the high power universal dc-dc converter for PEVs, with an innovative two-phase SiC-GaN-based topology. As a result, the possible alternative for the same application can be a two-phase all-SiC topology where there is no GaN technology.

To this aim, Spice-based OrCAD simulations are performed for the both SiC-GaN-based and all-SiC converters in which the Spice model of SiC SCT3017AL and GaN GS66516T are used.

There are different methods for the power loss calculations:

1) Spice Circuit Simulation:

The most straightforward method is to use Spice software (such as OrCAD, PSpice and LTSpice) to simulate the whole circuit and obtain the loss values directly from the resulted waveforms with the computational functions embedded in the software.

Spice simulations are very convenient and accurate. The Spice device models take most underlining physical parameters into account and build semiconductor devices with accurate equations, rather than lumped linear circuit elements (L, R, and C). When Spice simulations are conducted, all the losses are accounted for automatically, even the losses associated with leakage currents and gate drives.

However, the accuracy of this kind of simulation largely depends on the accuracy of the Spice model of the devices used. Those Spice models are typically created by the device manufacturers where the models are fitted with the performance curves measured experimentally, which may not be accurate for all operation points. In addition, many devices do not even have a Spice model to use.

2) PLECS Circuit Simulation with Datasheet Extrapolation:

Some simulation tools like PLECS and MATLAB/Simulink treat semiconductor devices simply as combinations of linear circuit elements. For example, a diode is modeled as a constant voltage drop in series with a resistance.

In this case, switching loss is handled separately. First, the parameters of the circuit components needed for the simplified model, (such as the threshold voltage and the ON-resistance), are obtained at a suitable operating point by referring to the performance curves on datasheets. The parameters are put into simulation software, and operation waveforms can be obtained with ideal switching transients. Hence, the conduction loss of the switches as well as the losses from the inductor and capacitor will be obtained directly from the simulation. The switching loss can then be accounted for by reading the switching energy figures on the datasheet of the switches. The numbers may need to be scaled by some factor to match the operating conditions assumed, and should be multiplied by frequency to yield the switching loss.

3) Analytical Calculation Using Device Datasheets:

If discrete semiconductor devices are used and reliable Spice models of these devices do not exist, it is better to calculate their losses with equations presented in the following parts of this section by completely depending on the datasheet information.

In this thesis, the method of power loss calculation is a combination of the both Spice circuit simulation method and the analytical calculation using device datasheets method. For instance, for the switching loss calculation, the values of the turn-ON/turn-OFF switching times are obtained from the simulations; while for the conduction loss calculation, the reverse recovery loss calculation, and the gate loss calculation, the values of the drain-source ON-resistance ($R_{DS(on)}$), the reverse recovery charge (Q_{rr}), and the total gate charge ($Q_{g(tot)}$) are obtained from the device datasheets.

Here, the power losses contributors are formulated as follow:

1) Switching Loss:

$$P_{sw} = V_{DS(max)} \times I_{D(max)} \times f_{sw} \times \frac{T_{on} + T_{off}}{2} \qquad (3.13)$$

Referring to table 3.1, the amount $Q_{G(tot)}$ and consequently the amounts of T_{on} and T_{off} are smaller for the GaN device in comparison with those of the SiC device. For this reason, the GaN device has a smaller switching loss.

2) Conduction Loss:

$$P_{Cond} = R_{DS(on)} \times {I_{D(rms)}}^2 \times D \qquad (3.14)$$

where D is the duty cycle of the corresponding device. Referring to table 3.1, $R_{DS(on)}$ is smaller for the SiC device in comparison to the GaN device. For this reason, the SiC device has a smaller switching loss. As we will see later, the efficiency of the proposed SiC-GAN-based converter is still higher than the all-SiC converter since the main contributor of the power losses is the switching loss.

3) Reverse Recovery Loss:

$$P_{Qrr} = V_{DS(max)} \times f_{sw} \times Q_{rr} \qquad (3.15)$$

where Q_{rr} is the reverse recovery charge of the corresponding device. Referring to table 3.1, Q_{rr} is zero for the GaN device, however, as we will see later, it is not a big advantage for the proposed converter, as this contributor of the power losses is a very small portion of the total power loss.

4) Gate Loss:

$$P_G = V_{GS} \times f_{sw} \times Q_{G(tot)} \qquad (3.16)$$

where V_{GS} and $Q_{G(tot)}$ are the gate-source voltage, and the total gate charge of the corresponding device respectively. This term of the power loss contributors is neglected in this study after the power loss calculations because of its too small portion of the total power loss.

5) Inductor Loss:

There are three terms of the inductor loss: the dc resistive loss, the ac resistive loss, and the core loss. In this study, we only take the dc resistive loss into account. This term of power losses can be calculated as:

$$P_L = R_{L(dc)} \times {I_{L(dc)}}^2 \qquad (3.17)$$

where $R_{L(dc)}$ (or simply R_L) and $I_{L(dc)}$ are the dc resistance and the dc current of the inductors respectively.

6) Capacitor Loss:

$$P_C = R_{C(ESR)} \times {I_{C(rms)}}^2 \qquad (3.18)$$

where $R_{C(ESR)}$ and $I_{C(rms)}$ are the equivalent series resistance and the *rms* current of the capacitor respectively. As we will see later, this contributor of the power losses has roughly the same value in the both converters.

To verify the steady state model of the proposed converter (3.10) in boost mode, the circuit of fig. 3.2 is simulated in OrCAD using Spice model of SiC SCT3017AL and GaN GS66516T. The duty cycles are obtained from the equations 3.11 at rating power of 40 kW. Fig. 3.7 (with two different Y axes) and fig. 3.8 present the inductor currents (i_{L1} and i_{L2}) and the HS SiC and the HS GaN drain currents (i_{SiC-D} and i_{GaN-D}) respectively.

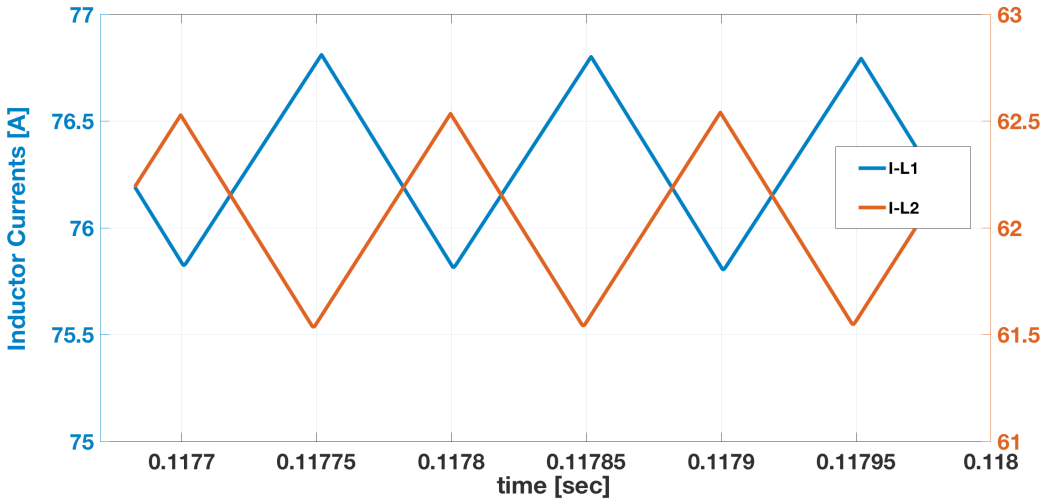


Figure 3.7. Inductor currents for the proposed converter in P_{out} = 40 [kW]

Based on the simulation results, the average amounts of the HS drain currents are 39.45 A and 26.34 A for the SiC and the GaN devices respectively. In an ideal current sharing for the proposed converter, the GaN device provides 25 A (15 kW); and the SiC device provides 41.67 A (25 kW) in the rating power of 40 kW. Comparing the simulation results with the ideal current sharing, the model has an error of 5 % approximately. However, as long as the current ratings of the devices are not violated, non ideal current sharing resulted by the modeling error is not a problematic issue in our application.

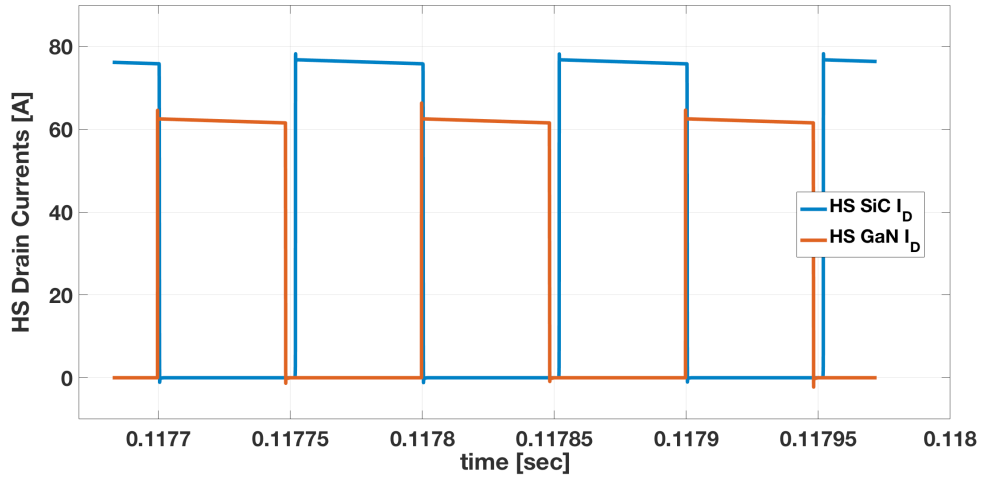


Figure 3.8. The HS drain currents for the proposed converter in P_{out} = 40 [kW]

Referring to table 3.1, the drain current ratings of the SiC and the GaN devices are 118 A and 60 A respectively. As it can be seen in fig. 3.8, the drain current ratings of the devices are respected.

In fig. 3.9, the power loss contributors are compared for the proposed SiC-GaN-based converter and the two-phase all-SiC converter at the rating power of 40 kW. As it can be seen, the main contributor of the power losses is the switching loss (P_{sw}). The conduction loss is lower for the case of all-SiC converter because of the smaller drain-source ON-resistance of the SiC device in comparison with that of the GaN device.

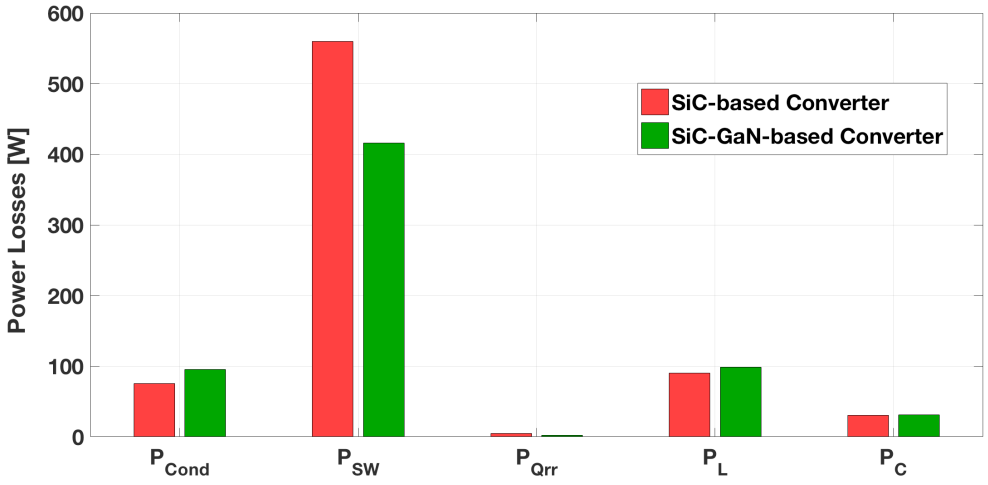


Figure 3.9. Power loss contributors for the both converter in P_{out} = 40 [kW]

Reverse recovery loss is a very small portion of the total power loss for the both SiC-GaN-based and the all-SiC converters. Inductor and capacitor losses have roughly the same amounts for the both converters. The gate loss (P_G) is not shown in fig. 3.9 because its portion of the total power loss is too small to be accounted.

Finally, in fig 3.10, the efficiency of the both converters is compared in different amounts of the output power. In P_{out} = 40, 30, 15, 5 kW, the GaN device provides 37.5, 50, 100, and 100 percent of the total output power respectively. The higher percentage of the GaN usage in light loads results in lower switching power loss. Consequently, the difference in the efficiency is higher in light loads between the proposed SiC-GaN-based converter and the all-SiC converter.

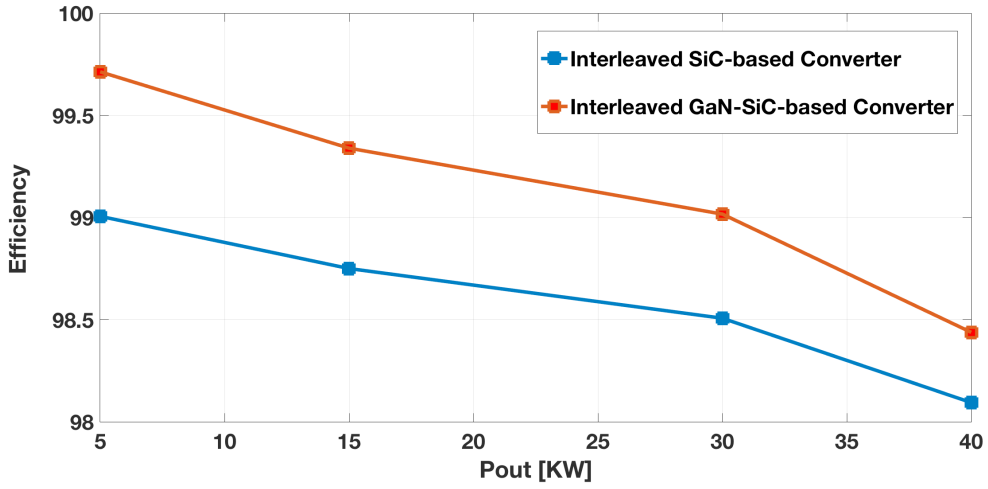


Figure 3.10. Efficiency investigation for the proposed SiC-GaN-based converter and the all-SiC converter in P_{out} = 40, 30, 15, 5 [kW]

3.5 Dead-Time Analysis

In the recent years, parallel to the growth of the GaN devices in power electronics, some studies are performed specially on the analysis and the optimization of the dead-time in the GaN-based converters [32-41]. In [32], the dead-time optimization is studied for a flyback converter using GaN EPC 1009 with voltage and current rating of 60 V and 6 A respectively. In [35], the dead-time optimization is studied for a 600 W full-bridge dc-dc converter using a 650 V, 15 A, GaN device by RFMD Company. In [36], the effect of the

dead-time on the switching behavior and the power losses of a boost converter, using a GaN device, is presented. This work is followed and completed in [37] by deriving a dead-time optimization model for the GaN device in order to select the optimum value of the dead-time. In [38], an analog dead-time generator circuit is presented for a GaN-based synchronous boost converter. This work is followed and completed in [39], where the analog circuit is enabled to predict the switching behavior of the GaN device during the dead-time interval to dynamically control the value of dead-time in order to minimize the dead-time power loss. In [40-41], the effect of the negative OFF gate-source voltage ($V_{GS-off} < 0$) on the dead-time power loss is investigated. A negative OFF gate-source voltage increases the drain-source forward voltage ($V_{DS-forward}$) and consequently increases the dead-time power loss.

Expect [19] and [22], in all other mentioned literatures, GaN EPC 2001 (100 V and 25 A) is the switching device of the converter. In addition, the reported output power is always less than 200 W. On the contrary, in this thesis, the power rating of the converter is 40 kW and the state-of-the-art GaN device (GS66516T by GaNSystems) with voltage/current ratings of 650 V and 60 A is used. Therefore, it is important to investigate the effect of the dead-time power loss in the SiC-GaN-based proposed converter, with its new GaN and SiC devices, in the high power application of universal dc-dc converter for PEVs. To this aim, in the section, a new Spice circuit simulation method is introduced to calculate the dead-time power loss in a more precise way. To compare the dead-time power loss of the GaN and the SiC devices, the simulations are performed with equal power sharing (15 kW for each phase). The effect of the negative V_{GS-off} on the dead-time power loss is also investigated.

In a dc-dc converter with bridge topology, the dead-time is defined as a switching time interval in which the gate-source voltages (V_{GS}) of the both HS and LS devices are in the OFF situation. Such a time interval is considered by the designer to prevent the possibility of short-circuit caused by the simultaneous switched-ON situation of both the HS and LS devices. During this time interval, in the boost mode, the HS device still conducts the inductor current while its resistance or its drain-source forward voltage is different from the drain-source ON-resistance during the conduction time interval. As a

result, the power loss during the dead-time interval is different from that of the conduction time interval.

In fig. 3.11, the switching loss, the conduction loss, and the dead-time loss are defined graphically with their corresponding time intervals. The curves of fig. 3.11, are obtained from OrCAD simulation of the proposed SiC-GaN-based converter at $P_{out} = 30\,kW$ using Spice model of the devices. The curves present the drain-source voltage (V_{DS}) and the drain current (I_D) of the HS GaN device. As it can be seen, during the dead-time interval, the negative *drain-source forward voltage* ($V_{DS-forward}$) is not constant and the resistance of the device is not equal to that constant $R_{DS(on)}$ of the steady-state conduction time interval.

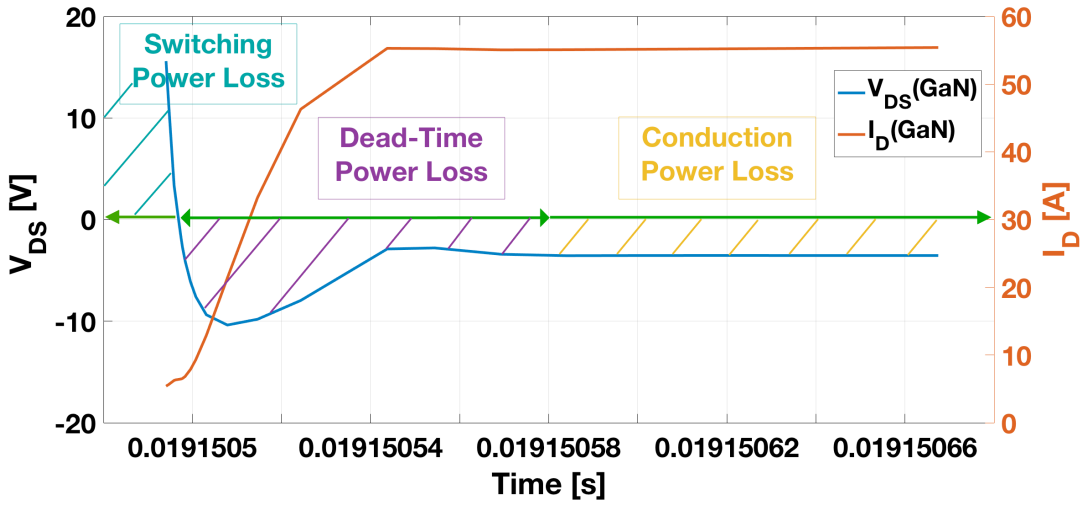


Figure 3.11. Power Loss Definition (P_{out} = 30 kW)

In the literatures, such as [42-44], the formula (3.19) is used to calculate the dead-time loss ($P_{dead-time}$). In this formulation, $V_{DS-forward}$ is the negative forward drain-source voltage and I_o is the output current respectively. To calculate $P_{dead-time}$, $V_{DS-forward}$ is obtained from the datasheet of the device and I_o is equal to the steady state I_D, practically, during the conduction time interval.

$$P_{dead-time} = V_{DS-forward} \times I_o \times f_{SW} \times T_{dead-time} \qquad (3.19)$$

In (3.19), $T_{dead-time} = T_{dead-time-on} + T_{dead-time-off}$ where in the ON dead-time interval, the HS device is going to be switched-OFF and the LS device is going to be switched-ON, and in the OFF dead-time interval, the HS device is going to be switched-

ON and the LS device is going to be switched-OFF. Based on this definition, fig. 3.10 presents an OFF dead-time interval.

The problems of the dead-time loss calculation method of (3.19) are: a) $V_{DS-forward}$ is not a constant value (obtained from the datasheet) during the dead-time interval b) $V_{DS-forward}$ during the dead-time interval has not the same transient trajectory for different values of the dead-time, and c) I_o, the corresponding current to $P_{dead-time}$, is not a constant value during the dead-time interval, equal to the steady-state I_D of the conduction time interval.

To modify the formulation of (3.19), another formulation is proposed where the term $V_{DS-forward} \times I_o$ is changed as:

$$P_{avg-on} = \frac{1}{T_{dead-time-on}} \int_{t_{0-on}}^{t_{0-on}+T_{dead-time-on}} |V_{DS}(t).I_D(t)|\, dt \qquad (3.20)$$

In this formulation, average power loss of the device during one ON dead-time interval (P_{avg-on}) is calculated by considering the instantaneous absolute values of $V_{DS}(t)$ and $I_D(t)$. Absolute value is used since $V_{DS-forward}$ of the device is negative during the dead-time interval for the HS device in the boost mode of bridge topology. Average power loss during OFF dead-time ($P_{avg-off}$) can be also calculated easily by considering the corresponding time interval and replacing ON with OFF in the indexes of the formula (3.20).

Now, the formula (3.19) can be rewritten as:

$$P_{dead-time} = f_{SW} \times \left(P_{avg-on} \times T_{dead-time-on} + P_{avg-off} \times T_{dead-time-off}\right) \qquad (3.21)$$

The values of $V_{DS}(t)$ and $I_D(t)$ will be obtained from OrCAD simulations in this method. Since the simulation results are discrete, (3.20) should be rewritten as:

$$P_{avg-on} = \frac{1}{n} \sum_{i=1}^{n} |V_{DS}(i).I_D(i)| \qquad (3.22)$$

where n is the number of the available samples during the dead-time interval, obtained from the simulations.

Fig. 3.12 compares $P_{dead-time}$ of the both GaN and SiC devices in the proposed converter for different values of the dead-time in the range of 0 to 100 nanoseconds. The simulations are performed at P_{out} = 30 kW. In this case, the both SiC and GaN phases share equal amount of power (15 kW for each phase) and conduct the same amount of

current ($I_D = 50\ A$). Therefore, the resulted $P_{dead-time}$ of the SiC and the GaN devices, a function of I_D, are comparable.

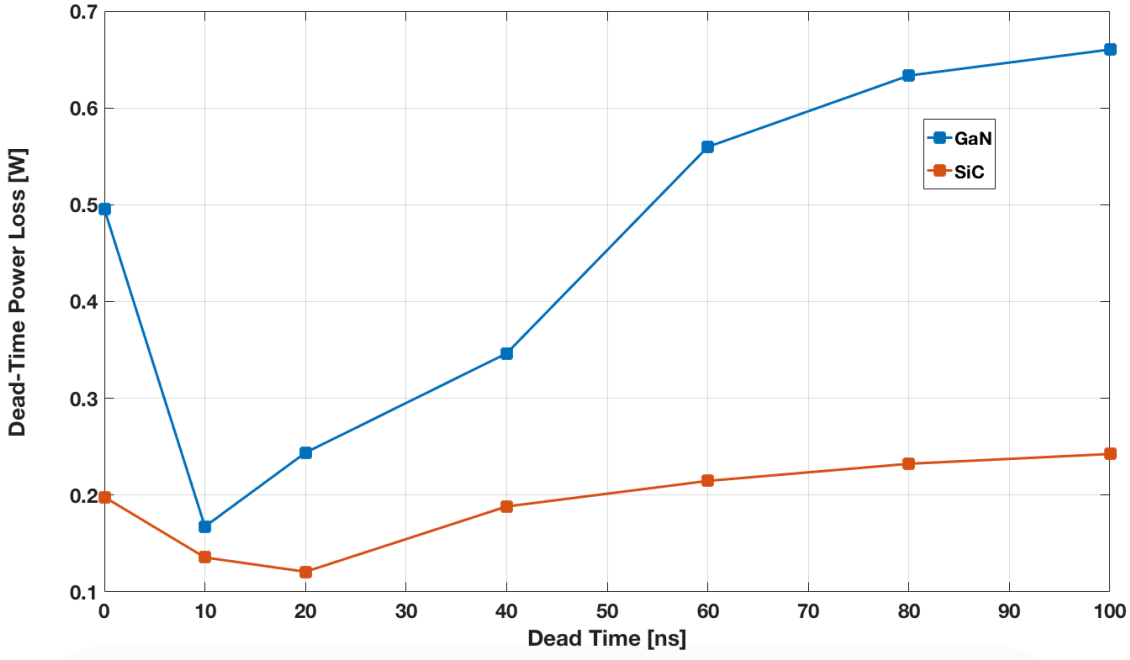


Figure 3.12. Dead-time loss of the GaN and the SiC devices

It should be noticed that, in fig. 3.11, $I_D = 55\ A$ at the steady state. This value is in fact the maximum current of the inductor ($I_{L-max} = I_{L-average} + I_{L-ripple} = 50 + 5 = 55\ A$) at the beginning of the conduction time interval. Considering the time scale of fig. 3.10 which is something around 100 ns, the visible steady state I_D corresponding to $P_{dead-time}$ is equal to 55 A.

At $T_{dead-time} = 0$ ns, the $P_{dead-time}$ is even higher than $T_{dead-time} = 10$, 20, and 40 ns. This higher amount of power loss is resulted from the high current spikes of the device. Therefore, a very low value of the dead-time not only increases the possibility of shoot-through problems, but also increases $P_{dead-time}$ and for these reasons should be avoided. In our case, the minimum $P_{dead-time}$ happened at $T_{dead-time} = 10$ ns for the GaN device and at $T_{dead-time} = 20$ ns for the SiC device. However, in [45], a minimum value of $T_{dead-time} = 30$ ns is recommended for the GaN device due to the propagation delay of the gate driver. A zero value of $T_{dead-time}$ is not applicable to calculate $P_{dead-time}$ using the formula (3.21). In fact, the settling time of $V_{DS}(t)$ is considered for the case $T_{dead-time} = 0$ ns. The settling time in the simulations is the time in which $V_{DS}(t)$

reaches its steady state value of the conduction time interval. In other words, in the settling time, the drain-source resistance of the device reaches its constant value of $R_{DS(on)}$.

In the dead-time range of 10-100 ns for the in the GaN device and 20-100 ns for the SiC device, $P_{dead-time}$ increases. The rate of the increase is higher in the case of the GaN device. For both devices, the rate of the increase is not linear and approximately reaches a saturation level for the very high values of the dead-time. It means that the settling time of $V_{DS}(t)$ does not increase linearly with the increase of $T_{dead-time}$. This behavior can be observed also in the calculated P_{avg-on} of the GaN device shown in fig. 3.13.

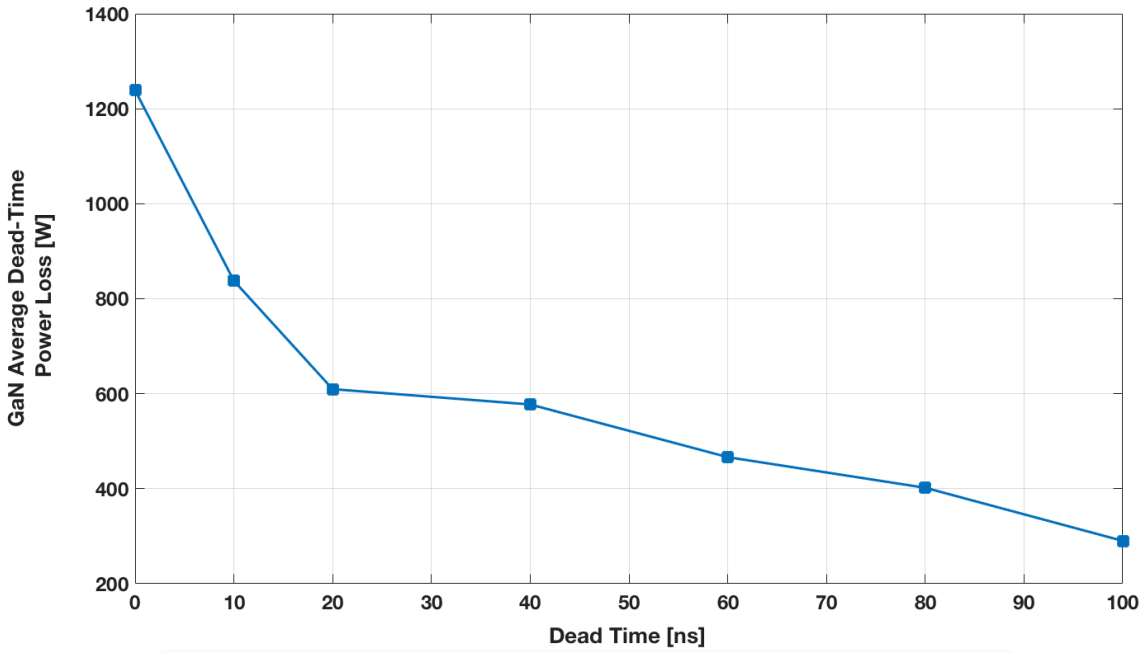


Figure 3.13. Average ON dead-time loss of the GaN device

As it is explained before, using $V_{DS-forward}$ values obtained from the datasheet is not a precise method. For example, $V_{DS-forward}$ is equal to 4.3 V for the GaN device at $I_D = 55\,A$ and $V_{GS-off} = 0\,V$. Therefore, the term $V_{DS-forward} \times I_o$ in (3.19) is calculated as $V_{DS-forward} \times I_o = 4.3 \times 55 = 236.5\,W$. This is the value of P_{avg-on} of the GaN device at $T_{dead-time}$ around 100 ns. But, this value is not valid for other values of dead-time as we can see in fig. 3.13. In fact, the datasheet does not provide $V_{DS-forward}$

for different values of dead-time. In some datasheets, $V_{DS-forward}$ is not provided even for different amounts of current.

Here, the effect of V_{GS-OFF} on $P_{dead-time}$ is analyzed as well. In [45], V_{GS-OFF} is modeled as a drop voltage added to $V_{DS-forward}$. A negative value of V_{GS-off}, results in higher amount of $P_{dead-time}$ as we can see in fig. 3.14 (simulated at P_{out} = 30 kW and $T_{dead-time} = 40\ ns$) for the case of the GaN device. Therefore, such a negative gate-source voltage applied during the switched-OFF interval is unpleasant. However, because of the low threshold voltage of the GaN device ($V_{GS(th)} = 1.1 - 1.3\ V$), there is the risk of unwanted switched-ON of the device during the switched-OFF interval with a zero gate-source voltage command. In [45], $V_{GS-OFF} = -3\ V$ is recommended.

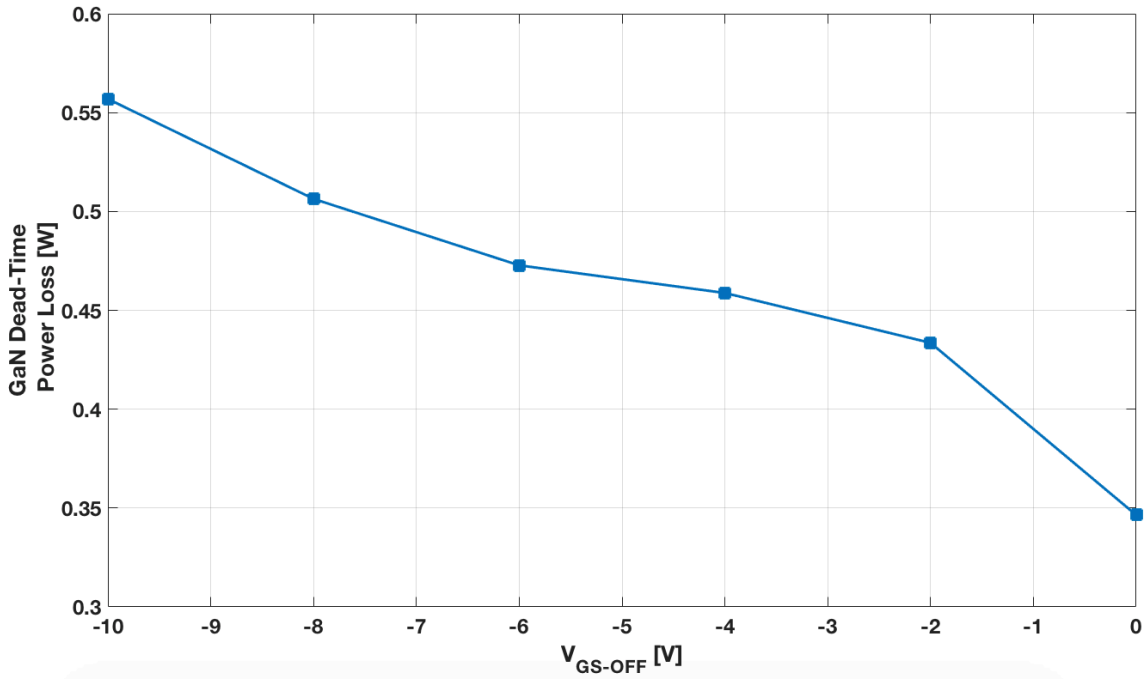


Figure 3.14. Dead time loss of the GaN device for different negative values of V_{GS-OFF} ($P_{out} = 30\ kW$ and $T_{dead-time} = 40\ ns$)

As a conclusion, considering the output power of 30 kW and the total power loss of 300 W (efficiency of the converter is around 99 % at P_{out} = 30 kW refers to fig. 3.9), the dead time loss ($P_{dead-time} < 1W$) has a very low amount and does not influence the efficiency effectively.

Chapter 4. Controller Design

In this section a cascade controller is designed for the proposed converter to achieve the active asymmetrical power sharing between the SiC and the GaN phases. The aim of active asymmetrical power sharing is the maximum utilization of the GaN device to minimize the power losses and reach the maximum possible efficiency.

The proposed converter is a universal fully directional one as it is shown in fig. 3.1 and its four modes of operation are explained in section 3.1:

1. *Generative/Acceleration Drive Mode*
2. *Regenerative/Braking Drive Mode*
3. *Vehicle-to-Grid (V2G) Plug-In Mode*
4. *Battery Charging Plug-In Mode*

Such a dc-dc converter with multi-mode of operation has different control objectives. In drive modes (modes 1 and 2); the first goal is to regulate the dc bus voltage with a reference of 600 V. In addition, in order to minimize the switching power loss by the maximum utilization of the GaN device, it is needed to have different inductor current references. It is also very important to respect the current rating of the both SiC and GaN devices and avoid high overshoots. Therefore, inductor current control is also necessary in our case. All these considerations lead to a cascade controller in which the inner loop controls the inductor currents of the both SiC and GaN phases and shares the current asymmetrically and the outer loop controls the voltage of the dc bus.

In plug-in modes (modes 3 and 4), the first goal is to control the power conversion of the battery. However, because of the aforementioned needs for the inductor current control in the proposed converters, also in plug-in mode a cascade structure is applied. Like the drive mode, the inner loop consists of the inductor current controller. The difference is the outer loop where the battery power is the reference of the controller instead of the voltage of the dc bus.

Using PI controllers is very common in dc-dc converters. We also use PI controllers for all controller blocks. The control scheme of the converter is shown in fig. 4.1. As it can be seen in the figure, in drive mode, where the control objective is to regulate the bus voltage, the outer loop reference parameter is $V_{bus}{}^{*}$. Moreover, in plug-in mode, where

the control objective is to regulate the battery power, the outer loop reference parameter is $P_{batt}{}^{*}$.

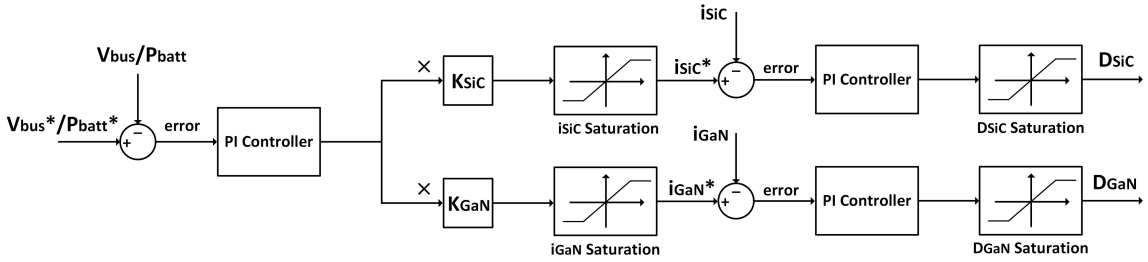


Figure 4.1. Cascade control scheme for the universal SiC-GaN-based converter

To obtain an active asymmetrical current sharing in order to maximize the utilization of the GaN device, the output of the outer loop PI controller is multiplied by the coefficients K_{SiC} and K_{GaN} to produce current references for the both SiC and GaN phases. Based on the power rating of the GaN device (15 kW), the coefficients should be calculated as:

$$K_{GaN} = \begin{cases} 1 & for\ P^* \leq P_{GaN-ratting} \\ \dfrac{P_{GaN-ratting}}{P^*} & for\ P^* > P_{GaN-ratting} \end{cases}$$

$$K_{SiC} = \begin{cases} 0 & for\ P^* \leq P_{GaN-ratting} \\ \dfrac{P^* - P_{GaN-ratting}}{P^*} & for\ P^* > P_{GaN-ratting} \end{cases} \quad (3.23)$$

where P^* is the demanded power (output load power in boost mode and battery power in buck mode) and $P_{GaN-ratting}$ is the maximum power which GaN transistors can provide. In our case, $P_{GaN-ratting} = 15\ kW$.

In fig. 4.1, the inductor current references and the duty cycle references are limited using the saturation blocks. For the inductor currents, the current ratings of the SiC and the GaN devices are considered as the limits of the saturation blocks. In the boost mode, the saturation limits are [0,118] and [0,60] for the current references, $i_{SiC}{}^{*}$ and $i_{GaN}{}^{*}$, respectively. In the buck mode, the saturation limits are [-118,0] and [-60,0] for $i_{SiC}{}^{*}$ and $i_{GaN}{}^{*}$ respectively. For the duty cycles, a saturation limit of [0.1,0.8] is considered. In a dc-dc converter, the voltage ratio is proportional to the duty cycle, however, there is a saturation limit for the duty cycle depends on the power loss of the converter. For the amount of the duty cycle higher than the saturation limit, the voltage ratio decreases. That is what we are going to avoid because it leads to a feed-forward instability in the control

system. Based on the open-loop simulations, the value of 0.8 is considered for the upper limit of the duty cycle.

To manually regulate PI parameters, the close-loop converter (power stage with control blocks) is simulated in MATLAB Simulink. Then, two steps are performed as follow.

a) Inner Loop Regulation:

In the cascade controllers, first, the parameters of the inner loop should be regulated. The inner loop response should be much faster than that of the outer loop. In this way, the inner loop can be approximated as a unit block from the outer loop's point of view. To perform such an idea, the inner loop is separated from the outer loop; a deliberate sinusoidal input is applied to the inner loop; and the PI parameters are regulated manually to observe a fast tracking of the sinusoidal input by the inductor currents.

b) Outer Loop Regulation:

Once the inner loop PI parameters are regulated, we connect the outer loop as the input of the inner loop. To regulate the PI parameters of the outer loop, we can use PID Tuner App of MATLAB. PID Tuner App needs a linear model of the system. PID Tuner App performs the linearization of the system automatically, however, in the case of the switching converter, the app is not able to perform the linearization. In this case, first, a linear model is estimated for the system using System Identification Toolbox. Then, the estimated linear model is used by PID Tuner App to regulate the PI parameters of the outer loop.

In fact, we have more than one system in the simulations and the PI parameter regulation steps. In the generative/acceleration drive mode and the V2G plug-in mode, when the converter works in the boost mode, a resistive load is connected to the dc bus while in the regenerative/braking drive mode and battery charging plug-in mode, when the converter works in buck mode, a dc voltage source is connected to the dc bus. Practically, the simulations and the regulation steps are performed only in the boost modes. For the buck mode, we take the advantage of the intrinsic robustness of the PI controllers to still have satisfactory results.

To examine the performance of the controller, the proposed converter is simulated in the both drive mode and plug-in mode. Each simulation has three phases, which are described as follow:

1) Start-Up Low Power Boost:

The converter is supposed to work in the boost mode, where $P_{out} = P_{GaN-ratting} = 15\ kW$. Since, the output power is equal to the power rating of the GaN device, only the GaN phase conducts the current. However, in the start-up phase, where the initial state of the dc bus voltage is zero, if only the GaN phase conducts the current, there will be current overshoot. This overshoot (around 5 percent of the rating current) may harm the devices. To avoid the current overshoot, the both SiC and GaN phases conduct the current to allow the dc bus voltage reaches its nominal value. Then, the SiC phase will be switched-OFF smoothly and only the GaN phase conducts the current to provide the demanded output power.

2) High Power Boost:

The converter is working in the first phase when $P_{out} = P_{rating} = 40\ kW$ is applied to the converter. The SiC phase switched-ON to impose more current to the output load and provide the rest of the demanded power. In this phase of operation, the outer control loop tries to keep the dc bus voltage regulated.

3) High Power Buck:

The converter is working in the boost mood at the rating power when the output load is replaced with a voltage source to evaluate the converter in a transition of boost-to-buck. In this phase, the demanded power of the battery is equal to the rating power of the converter.

In figures 4.2, 4.3, and 4.4, the drive mode results are presented. In $t = [0\ 0.03]\ s$, the *start-up low power boost* phase of operation is simulated. The dc bus reaches the regulated voltage of 600 V properly. The SiC phase conducts current in $t = [0\ 0.01]\ s$ to contribute with the GaN phase and avoid i_{GaN} to face an overshoot. For $t = [0.01\ 0.03]\ s$, where V_{bus} is close to the regulated voltage, only the GaN phase conducts to provide $P_{out} = P_{GaN-ratting}$ without violating the current rating of the GaN device which is 60 A. The battery is discharging to provide the demanded power to the load so that its voltage is decreasing.

In $t = [0.03\ 0.07]\ s$, the second phase of operation, *high power boost*, is simulated where the output demanded power is changed from 15 kW to 40 kW. It takes around 0.03 s for the dc bus to pass the oscillations and reach the regulated voltage again. The steady state

ripple is higher respect to the first phase but still below the allowable ripple ($\Delta V_{HV} = \Delta V_{HV(P.U.)} \times V_{HV} = 0.05 \times 600 = 30\ V$). The inductor current of the GaN phase (i_{GaN}) remains at the rating current of the GaN device (60 A). On the contrary, the inductor current of the SiC phase (i_{SiC}) starts to increase and reach the rating current of the SiC device (118 A) without any overshoot. In the steady state, the current sharing is perfectly divided respect to the formula (3.23). Like the first phase, the battery voltage is decreasing in this phase of operation as well.

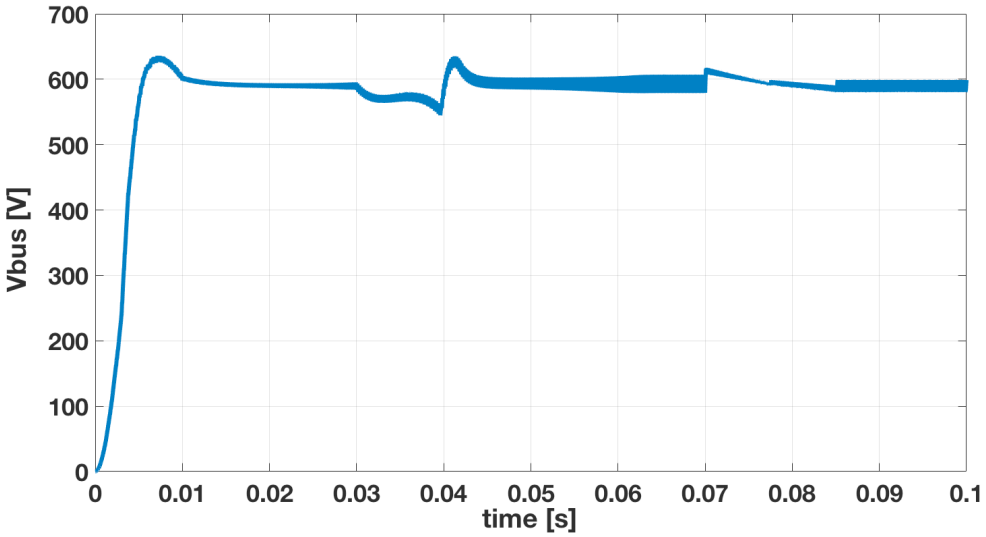


Figure 4.2. Drive mode: the dc bus voltage V_{bus}

In $t = [0.07\ 0.1]\ s$, the third phase of operation, *high power buck*, is simulated where a voltage source is applied to the dc bus. Within 0.015 s, the dc bus passes the oscillations and reached its regulated voltage again. Inductor currents of the both SiC and GaN phases reach their rating currents, in the opposite direction of the first and the second phases of operation, to charge the battery at the rating power of the converter (40 kW). The battery is charged in this phase and its voltage is increasing.

In figures 4.5, 4.6, and 4.7, the plug-in mode results are presented. In $t = [0\ 0.025]\ s$, the start-up low power boost phase of operation is simulated. The battery power reaches the power reference of 15 kW properly. The inductor currents have the same shape of the drive mode, however, the steady state of i_{GaN} is lower. Since the battery power reference ($P_{batt}{}^{*}$) is 15 kW, due to the power losses of the converter, the output power is lower than 15 kW. As a result, the GaN phase can provide the demanded output power at a

lower rate of current (around 50 A). The battery is discharging to provide the demanded power to the load and its voltage is decreasing as well.

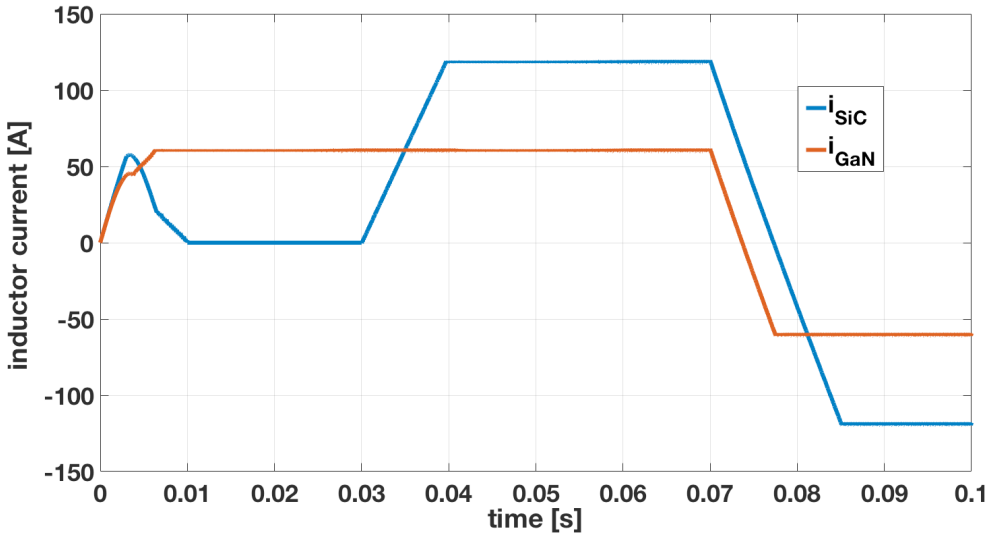


Figure 4.3. Drive mode: the inductor currents I_{SiC} and I_{GaN}

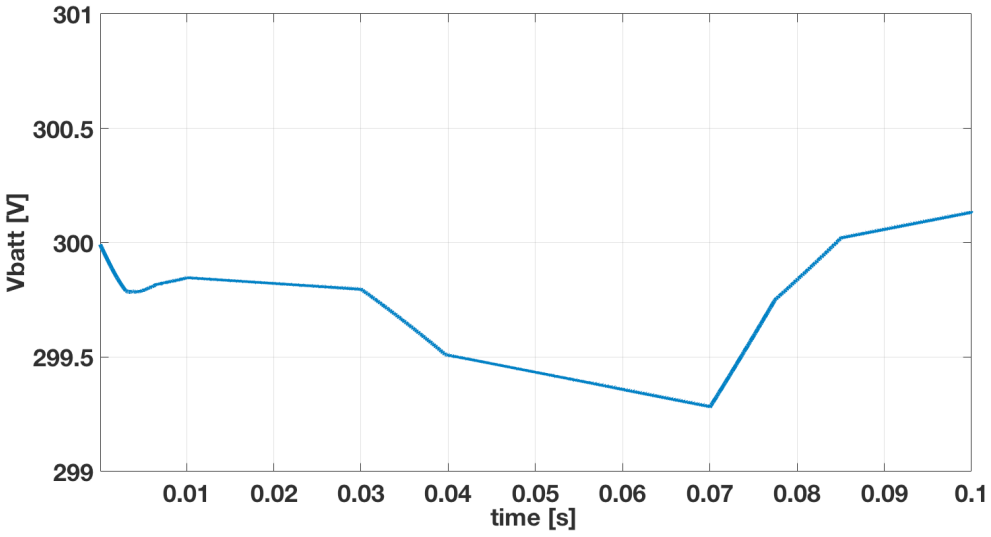


Figure 4.4. Drive mode: The battery voltage V_{batt}

In $t = [0.025\ 0.05]\ s$, the second phase of operation, high power boost, is simulated where the reference battery power is changed from 15 kW to 40 kW. It takes around 0.01 second for the battery to pass the oscillations and reach the new power reference. The inductor currents have no overshoot and the current sharing follows the formula (3.23). The battery voltage is decreasing in this phase of operation as well.

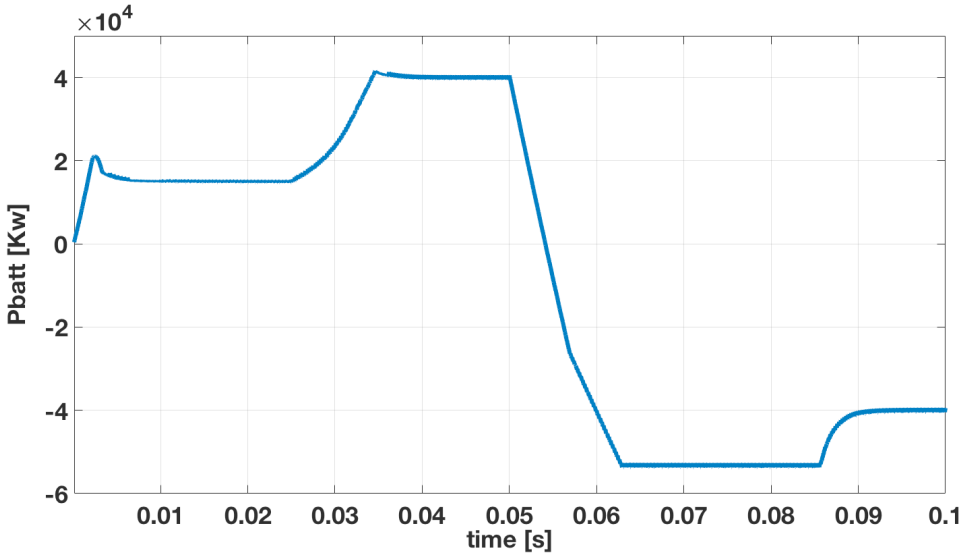


Figure 4.5. Plug-in mode: The battery power P_{batt}

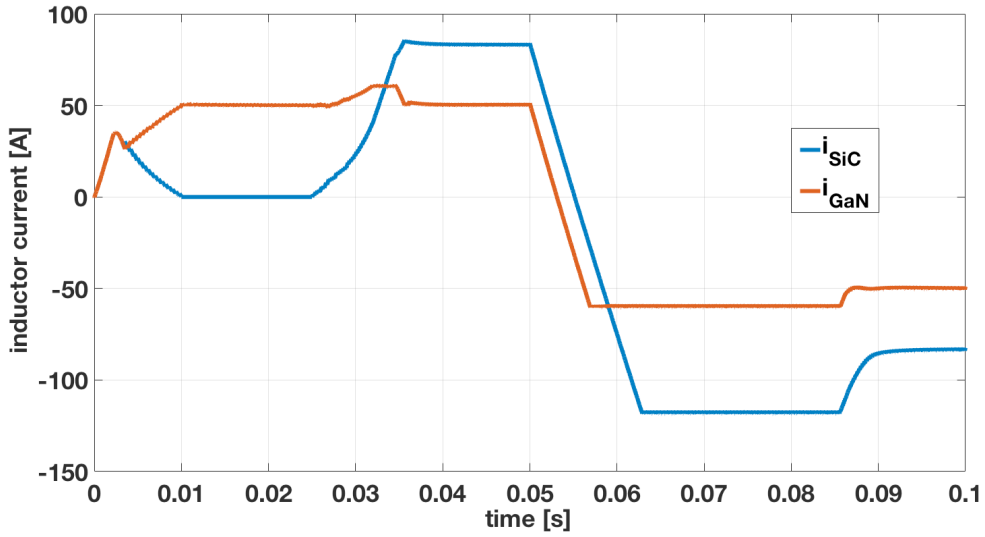


Figure 4.6. Plug-in mode: inductor currents I_{SiC} and I_{GaN}

In $t = [0.05\ 0.1]$ s, the third phase of operation, high power buck, is simulated where a voltage source is applied to the bus voltage. The battery power is supposed to reach its reference of -40 kW. At the beginning of this simulation, there is a large error between the measured power ($P_{batt} = 40\ kW$) and the reference power ($P_{batt}{}^{*} = -40\ kW$). It leads to a very large output of the first PI controller. This large amount, as the reference current, forces both i_{SiC} and i_{GaN} to reach their saturation levels (-118 A and -60 A respectively) immediately. It causes an overshoot in the battery power. Within around

0.023 s (roughly for $t = 0.063\,s$ to $t = 0.086\,s$), the output of the first PI controller decreases to such a level in which also inductor currents start to decrease. Then, the battery power reach the reference power very soon and the inductor currents reach their steady states. The battery is charged in this phase and its voltage is increasing as well.

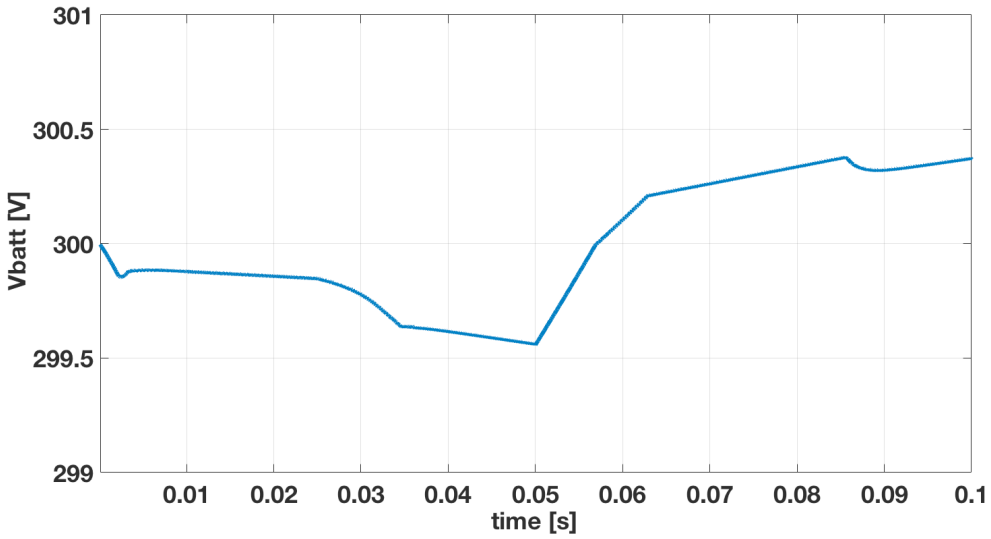


Figure 4.7. Plug-in mode: The battery voltage V_{batt}

As a conclusion, in both drive mode and plug-in mode, the performance of the controller is very well where there is no overshoot for the inductor currents, the settling time is quite fast, there are no steady state errors, and the current sharing follows the formula (3.23).

Chapter 5. Gate Driver Multi-Objective Parameterization

5.1 Gate Driver Design

To achieve higher performance of the switching devices, there are many considerations. In [46] the effect of the anti-parallel diodes, the current capability of the driver IC, the source inductance, the gate driver circuit topology, the packaging and the PCB layout on the performance of the switching devices have been addressed. In [47], the gate resistor and the bootstrap resistor design, optimized design of the PCB layout, applying the RC snubber, and using of the common source inductance are described as the methods to reduce the ringing.

In the case of the GaN devices, there are some different considerations rather than those of the Si MOSFETs and the Si IGBTs. For instance, the gate driver must comply with the component voltage/current ratings, the ON/OFF gate-source voltage, and the threshold voltage to operate properly and with high performance and reliability. In [48], low gate-source maximum voltage ($V_{GS(max)}$ of 6 V for the GaN FET in comparison to 20 V for the Si MOSFET) and ultra low threshold voltage (V_{th} of 1.2 V for GaN FET in comparison to 2-4 V for Si MOSFET) are addressed as characteristics of the e-mode GaN FET respect to the gate driver issues. Then, practical solutions are considered: a) applying a regulated gate driver bias voltage of 5 V to achieve the minimum $R_{DS(on)}$; b) separating the sourcing (turn-ON transition) and the sinking (turn-OFF transition) paths to avoid the unintended turn-ON related to the parasitic ringing that induce the device with an ultra low V_{th}; c) The use of the high-side bootstrap voltage clamp to provide a safety margin related to $V_{GS(max)}$. As it is described in section 2.4, rather than e-mode GaN device, there is another type of GaN FET named “cascode” in which the drain-source of a low voltage normally-OFF Si MOSFET is connected in series to the gain-source of the high voltage normally-ON GaN FET to ensure the safe operation. The e-mode GaN has a simple structure but needs integrated driver to take care about the ultra low V_{th} and very low safety margin (only 1 V) between the drive V_{GS} (5 V) and the $V_{GS(max)}$ (6 V). The cascode GaN is more complicated than e-mode GaN, however, it has higher V_{th} and higher safety margin of the gate-source voltage [49].

One of the *figure of merits* (FOM) of the switching devices is $R_{DS(ON)} \times Q_G$. Lower $R_{DS(ON)}$ leads to lower conduction losses and lower Q_G allows faster switching transient and consequently lower switching losses. Lower power losses, conduction and switching, results in higher efficiency. However, sharp transient in voltage and current causes high frequency noises and deteriorate *electromagnetic compatibility* (EMC) performance of the converter. Regarding performance of the switching devices, some efforts improve both efficiency and *electromagnetic interference* (EMI) level, such as PCB/layout optimal design or offering an innovative gate driver circuit design. Some other efforts such as parameterization of the gate resistor (R_G) have conflictive effect on the design objectives (efficiency, EMI level, etc.): higher/lower R_G results in higher/lower switching losses and lower/higher oscillations. In addition, there is also another term of losses: "*ringing losses*". During the switching transition of the device, the resonance among parasitics lead to high overshoot voltage that worsens the *cross talk*, leading to large *shoot-through* current and excessive switching losses [50]. Therefore, a lower amount of R_G decreases switching losses while increases ringing losses. There is a critical amount of R_G in which lowering R_G increases total losses (sum of both switching and ringing loss). Moreover, there might be a special amount for the gate drive circuit parameters such as R_G in which an increase/decrease of the amount leads to a small improvement in one objective but a high degradation in the other objective. Make all of these into the account; it seems attractive to determine the gate circuit parameters with a multi-objective optimization approach. It has no additional cost for the converter, and it needs only mathematical calculations while it can provides a Pareto Front for the designer in order to achieve the best possible efficiency and EMI level.

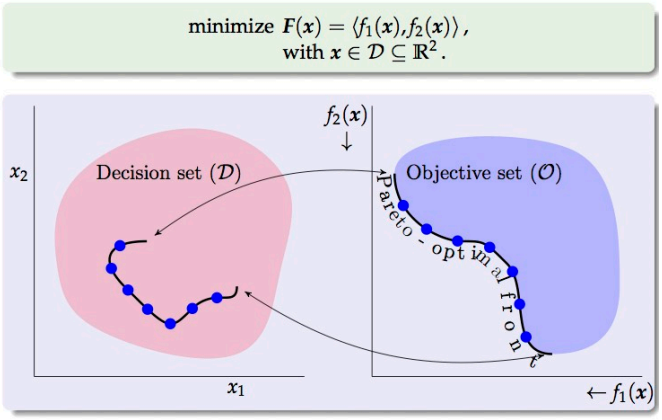
Another gate parameter of the gate driver circuit is the gate inductance (L_G), which is called also "*ferrite bead*". A ferrite bead is often used on MOSFET gate to provide stable operation by suppressing parasitic oscillation, while minimizing switching losses. In fact, adding a ferrite bead is more effective than using the gate resistance alone because the impedance of the ferrite bead is dependent of the value of the frequency. In [51] a ferrite bead is selected for a half-bridge configuration by measuring the ringing frequency to achieve the highest resistance at the ringing frequency. A resonant (refers to using of a ferrite bead) gate driver circuit is also proposed in [52]. In this circuit there are two

different paths for turn-ON and turn-OFF transitions. It is a very useful way to lower power losses since there are different required driver V_{GS} for the transitions. Also, the voltage and the current transients are much faster during turn-ON, as they need higher gate resistor to be damped. Therefore, having only one path for both transitions let more power loss during turn-OFF to dissipate unsatisfactorily. The design procedure in [52] is based on the circuit analysis and solving the differential equations where the objective is to satisfy the demanded peak voltage for the external gate-source capacitor. Circuit analysis is interesting, however, because of the high nonlinearity of the device equations, those are totally neglected. Since there is an external gate-source capacitor in the circuit topology with a value much larger than the GaN FET parasitic capacitor, such an approximation is considered. On the contrary, in this section, an OrCAD simulation method is investigated in which nonlinearity of the device equations are practically considered in the Spice model of the device.

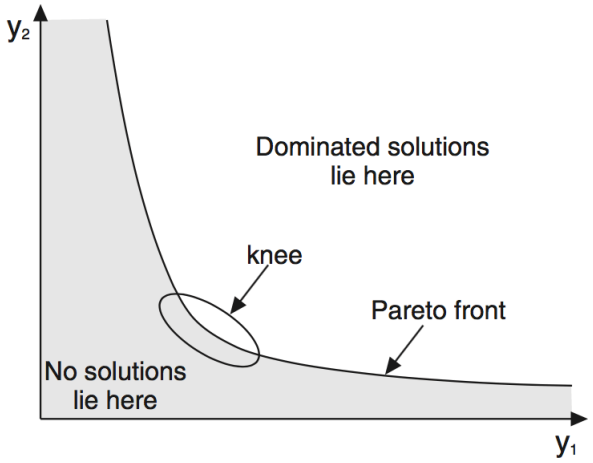
5.2 Multi-Objective Optimization

In power electronic design, the number of the variables is more than that of the constraints. Therefore, there are infinite sets of design solutions, which make the design an optimization problem with one or more objectives. In [53], the application of the optimization algorithms to design the power converters is introduced for the first time by F. C. Lee in which all the non-optimized/optimized/practical design methods are discussed. To make the optimization practical and simplify its complexity, usually different parts of the system, such as the gate driver, the power stage, the filters and the transformers, and the controller are designed separately. The main reason to such a separated design method is that some of the power converter objectives, such as the efficiency, the power density, and the EMI level are related to the circuitry; some of them such as the stability and the load tracking are related to the controller, and some other such as THD are related to the power quality of the system. Moreover, the separated design method is reasonable since the capability of the computer-aided design (CAD) optimization is limited to find too many optimum numerical solutions. Such an optimization design is followed in [54] to design the power stage and the transformer of an isolated half-bridge dc-dc converter separately. In [55] and [56] the gate driver circuit

optimization is studied using the analytical power loss modeling where the only objective is the efficiency. In [55], the HS ON/OFF gate resistors are considered as the variables while in [56], the gate driver supply voltage and the load current are also considered as the design variables. Both literatures consider a symmetrical design for the HS and the LS switching devices of the bridge configuration.



a. Mapping the feasible region to the performance region



b. Knee point

Figure 5.1. Pareto Front

Unlike the optimization problem with only one objective, in a multi-objective optimization, a *Pareto Front* will be provided. Pareto Front is a trade-off curve of optimal designs for the objectives. In fact, Pareto Front (or Pareto-Optimal) is the performance space mapped from the feasible region of the design variables in which an improvement of each objective comes at the detriment of the others resulting in a trade-off. In [57-58],

J. W. Kolar *et al.* have been designed the power stage of a power converter by multi-objective optimization with the efficiency and the power density as the objectives. Most of the time, there is a "*knee*" point at the Pareto Front curve in which a movement in any direction causes a small improvement in one of the objectives while leads to a large detriment in the others. Therefore, the knee point is a natural choice for the design problem. The mapping and the knee point concepts of the Pareto Front optimization is shown in fig. 5.1.

5.3 Gate Driver Optimization

In an optimization problem, the objectives are mathematical functions of the variables and the constants. In the case of the power electronic optimization, such functions are obtained by the circuit analysis or directly from the data sheets of the components. For instance, to maximize the efficiency, the total loss of the converter can be modeled as the sum of the winding loss, the magnetic loss, the capacitor ESR loss, and the device power loss (the both conduction and switching losses). Then, the total loss can be minimized where the mathematical model of each power losses is obtained from datasheet as a function of the circuit parameters and the constants.

In this section, the objectives of the gate driver optimization are the efficiency and the EMI level while the decision variables are the HS/LS gate resistors. Regarding the EMI level, cutting off the EMI paths to mitigate its influence on other parts of the converter needs bulky and costly filters. Therefore, it is better to attenuate the EMI by attending the source of it: the high dv/dt and the high di/dt of the switching device. That is why in the gate driver optimization; it is very interesting to consider the EMI level as one of the objectives. The EMI level is defined as the peak of the *ground* common mode (CM) current in μAdB scale in the frequency range of 150 kHz to 30 MHz in the thesis.

Regarding the decision variables, R_G and L_G are discussed in section 5.1 as the candidate of the decision variables. In the bridge configuration (fig. 5.2), to lessen the losses of the turn-OFF intervals, OFF-path, preferably with no gate resistor, should be separated from ON-paths. Moreover, the CM current path of the HS device has different parasitics from that of the LS device. Consequently, the high dv/dt (and the high di/dt) of the HS device imposes different EMI level to the circuit from that of the LS device. As a result,

an asymmetrical design of the HS and the LS gate resistors is more effective than a conventional symmetrical method. To perform an asymmetrical design, the both HS and LS turn-ON gate resistors (R_{GH} and R_{GL}) are selected as the decision variables. Moreover, the ferrite bead normally added in series with the HS gate resistor since in a half-bridge configuration, the HS switch is the main contributor in the term of the oscillations rather than the LS switch. Therefore, the other decision variable is L_{GH}.

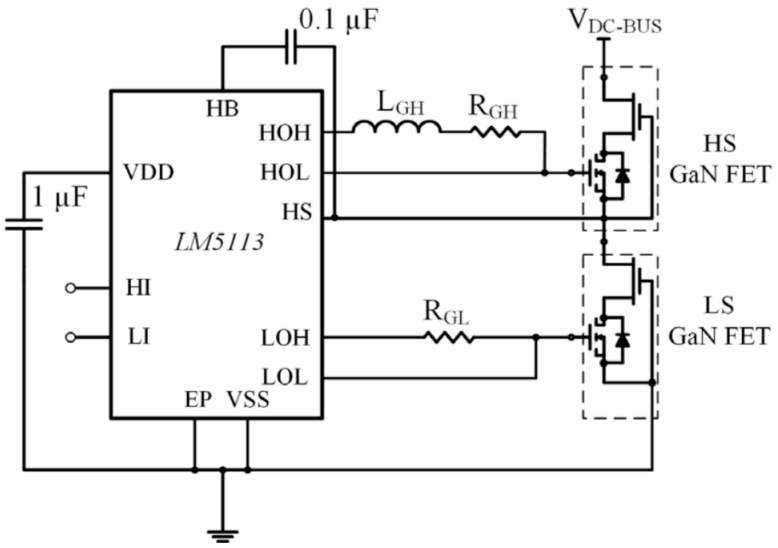


Figure 5.2. GaN FET bridge configuration gate driver circuit

Another issue in the optimization problem is the modeling. Since the EMI level is related not only to the component characteristics but also to the circuitry, the layout, and the heat sink, there is no mathematical expression of the EMI level as a function of the variables in the datasheet of the components. To obtain the mathematical expression analytically, the switching devices should be modeled as current/voltage sources and then a circuit analysis should be performed. In such a modeling method, the nonlinearity of the devices is not considered. To obtain a more precise mathematical expression of the EMI level, an OrCAD simulation approach is suggested in the thesis in which the nonlinearity of the devices is considered in Spice model of the devices. The idea of the suggested method is to perform a numbers of OrCAD simulations in the feasible region of the decision variables, collect all the input (R_{GH} and R_{GL}) - output (EMI level and efficiency) pairs, post-process data and obtain the *regression functions* for the objectives. Since there are two decision variables, the data regression is a *multi-variable* one. The post-processing

multi-variable regression is done using Statistics and Machine Learning Toolbox of MATLAB. The sufficient number of inputs-output pairs to achieve the regression functions with acceptable modeling error rises radically with the increase in the number of variables. That is why only R_{GH} and R_{GL} are considered as the variables in the first phase and then the HS ferrite bead (L_{GH}) is added in series with R_{GH} to improve the objectives in the second phase of the design.

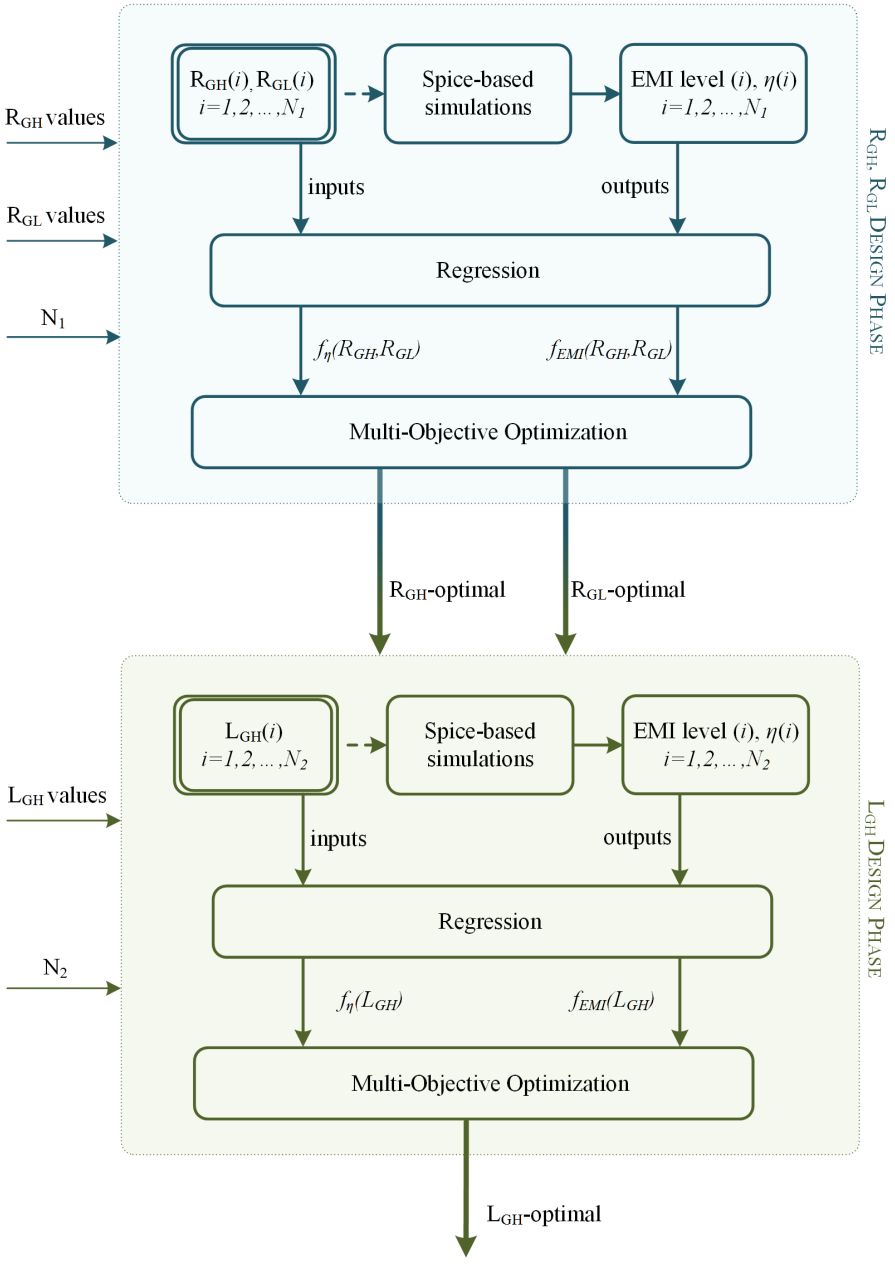


Figure 5.3. Flow chart of the proposed design approach

Once the regression models of the EMI level and the efficiency as functions of R_{GH} and R_{GL} are obtained, a multi-objective optimization can be performed to obtain Pareto Front of the design problem. Pareto Front can be obtained using non-linear multi-objective optimization solvers such as *fgoalattain* and *fminmanx* in Optimization Toolbox of MATLAB or using heuristic multi-objective optimization solver *gamultiobj* in Global Optimization Toolbox of MATLAB. In this study, we used the later one.

After first phase of the parameterization of R_{GH} and R_{GL}, to improve the objectives, L_{GH}will be added in series with R_{GH}. In the second phase of the proposed approach, OrCAD simulations should be performed for L_{GH} as the input of the optimization problem in the feasible region and the corresponding outputs (the EMI level and the efficiency) should be calculated from the simulation results. Then, a regression function is fitted to data using *fit* solver of Curve Fitting Toolbox of MATLAB. The two-phase proposed approach of the gate driver optimization is shown in the flowchart of fig. 5.3.

5.4 Case Study

a) Simulation Set-up

To design the gate driver circuit parameters based on the explained approach; a number of OrCAD simulations are performed for a *one-inverter leg* set-up. For this purpose, reference has been made to [65], where a one inverter leg circuit is studied in which the parasitics are experimentally measured, as represented in fig. 5.4. The parasitic elements $L_1 - L_4$ are inductances of the dc bus cable and foil, $C_1 - C_3$ are the coupled capacitances of the switching devices and the heat sink, $C_{DC1} - C_{DC2}$ represents the film capacitors connected to the dc bus, $L_{DC1} - L_{DC2}$ are the self-equivalent series inductances of the film capacitors, and R_{GR} and L_{GR} are the resistance and the inductance of the ground path respectively. The circuit is modified by replacing the switching device and its corresponding gate driver IC. The power switch is Transphorm 600 V Cascode GaN HEMT FET (TPH3206PD). A half bridge gate driver for GaN FETs by Texas Instruments (LM5113) is selected as well. Duty cycle of the switching devices is related to the steady state operation of the circuit and should are determined to provide the reference in the output. Since the aim of this work is to optimally design those parameters that affect the transient behaviors of the switching devices, the duty cycle is not

considered as the variables in the design approach and is remained constant for all the simulations. In this case, the duty cycle is set to 0.6 for the HS switch and 0.3 for the LS switch, while 0.1 of the period is considered as the dead time to provide 500 W as the output power for a RL load equal to $R = 300\ \Omega$ and $L = 100\ \mu H$.

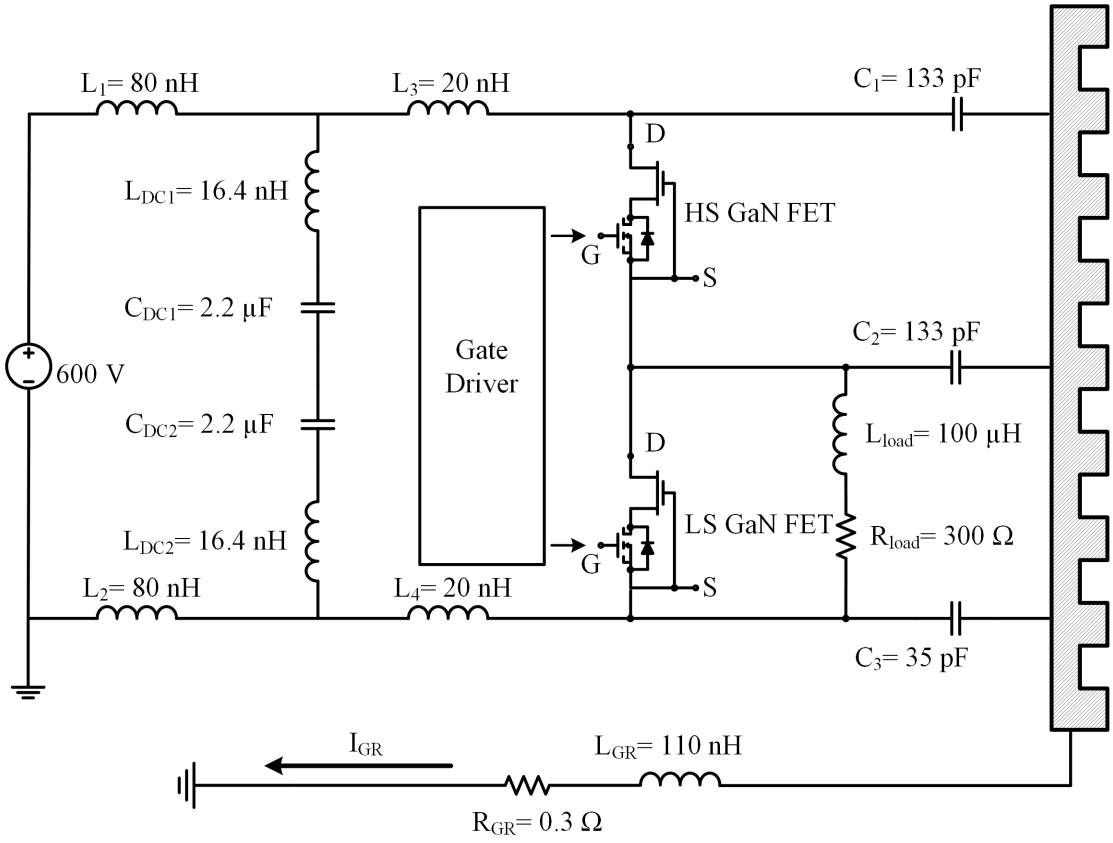
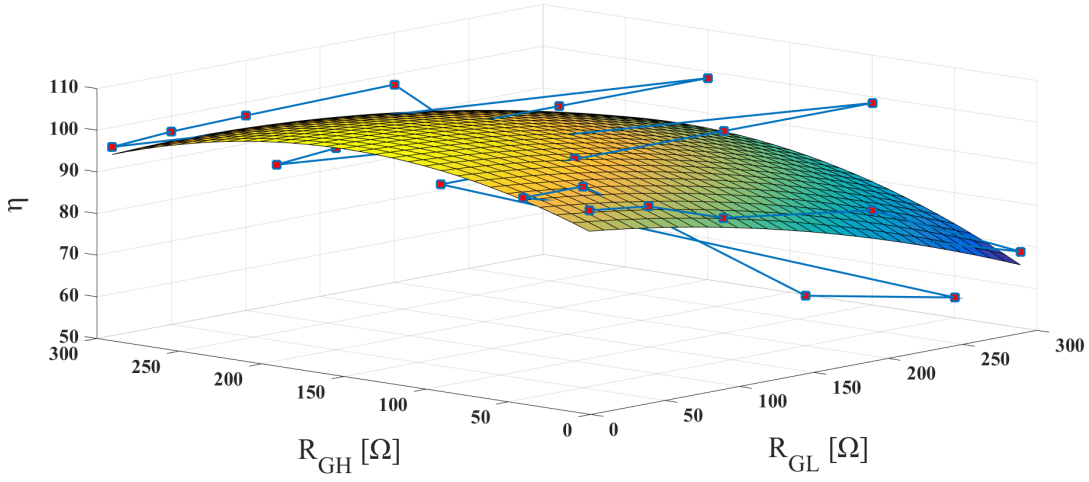


Figure 5.4. One leg inverter with extracted circuit parasitics [65]

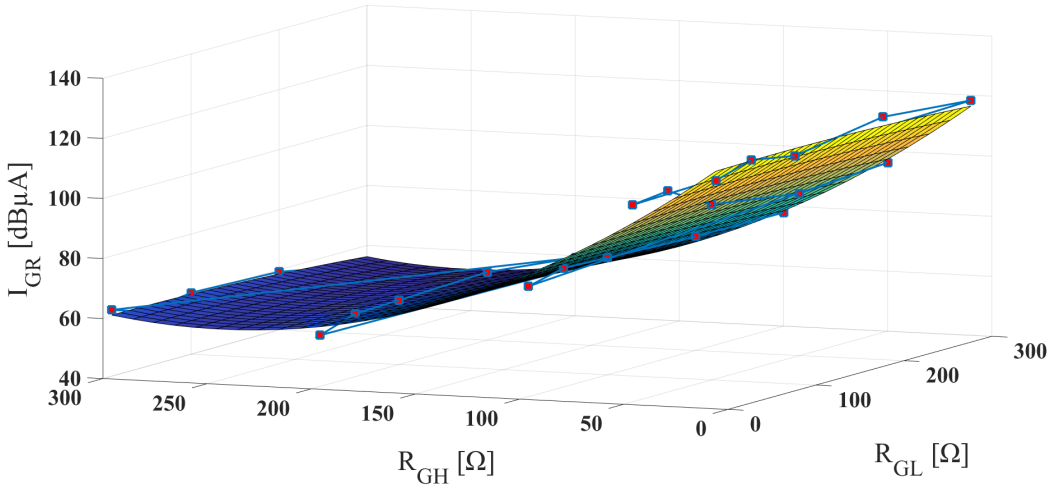
b) Results

In the first phase of the proposed design approach, the one inverter leg set-up is simulated 25 times for different values of R_{GH} and R_{GL} in the range of 10 Ω – 300 Ω, as the lower and upper bands. Particularly, the lower band is selected regarding to the gate current rating of the device, while for the upper band there is no practical constraint. However, efficiency is quite low and impractical for the range of hundreds of Ohms. Therefore, there is no need to consider a wider range of resistance. At the end of each simulation, efficiency is calculated in OrCAD considering the total input and output power of the one inverter leg. In addition, CM current spectrum is calculated by *Fast Fourier Transform*

(FFT) analysis of CM ground current in OrCAD as well. Then, EMI level is defined as the peak of the spectrum, in μAdB scale, in the frequency range of 150 kHz – 30 MHz.



a. Efficiency



b. EMI level

Figure 5.5. OrCAD simulation results (red points) and their corresponding regression functions (mesh grid surfs)

As it is shown in fig. 5.5, for the both efficiency and EMI level, a regression function is fitted using *Statistic and Machine Learning Toolbox* of MATLAB, to be the objective functions of the multi-objective optimization problem in the next phase of the design

approach. They may not be very accurately fitted to the input-output pairs, but linear and polynomial of the second order to be successfully converged in the optimization problem. The solver *fitlm* is used to obtain the quadratic regression functions as it is presented in formula (5.1), whose corresponding coefficients are presented in table 5.1.

$$f_{\eta}(x_1, x_2) = a_0 + a_1 x_1 + a_2 x_2 + a_3 x_1 x_2 + a_4 {x_1}^2 + a_5 {x_2}^2$$
$$f_{EMI}(x_1, x_2) = b_0 + b_1 x_1 + b_2 x_2 + b_3 x_1 x_2 + b_4 {x_1}^2 + b_5 {x_2}^2 \quad (5.1)$$
$$x_1 = R_{GL}, \quad x_2 = R_{GH}$$

Table 5.1. *Fitted objective function coefficients*

i	a_i	b_i
0	91.622	123
1	-3.835×10^{-2}	8.8362×10^{-3}
2	0.15262	−0.53186
3	2.0793×10^{-4}	-2.6687×10^{-5}
4	-1.8997×10^{-4}	-4.7908×10^{-5}
5	-4.9047×10^{-4}	1.0733×10^{-3}

In the second step of the first phase of design approach, the Pareto Front of the optimization problem is obtained as depicted in fig. 5.6 using the solver *gamultiobj*, which is a *metaheuristic* multi-objective optimization solver from Optimization Toolbox of MATLAB. Regarding to fig. 5.6, since the solver minimizes both objective functions, while the maximum of the efficiency is needed, f_{η} is considered with the minus sign. It means the negative amount of f_{η} should be minimized in order to maximize the efficiency.

There are some optimal design points in the Pareto Front with efficiency higher than 100%. For instance, at the optimal design point in the Pareto Front with the maximum efficiency of 103.4%, the corresponding values of R_{GH} and R_{GL} are 157.7 Ω and 10 Ω respectively. Selecting these values for the gate resistors in the one inverter leg set-up, the maximum efficiency are still obtained in spice-based simulation, however, the resulted amount of efficiency is 98.47%. It means in the Pareto Front, the amount of the objective

functions are obtained with a shift error from the spice-based simulation results, however, it doesn't affect the proper optimal points of the design variables.

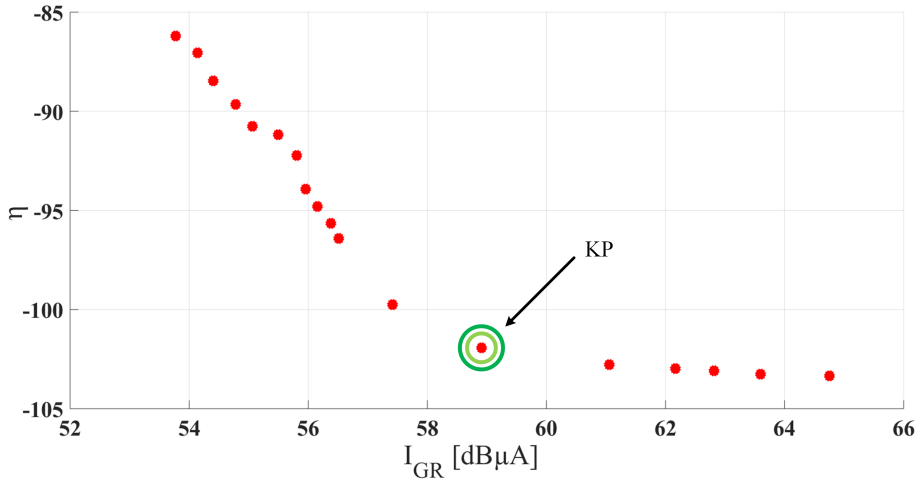


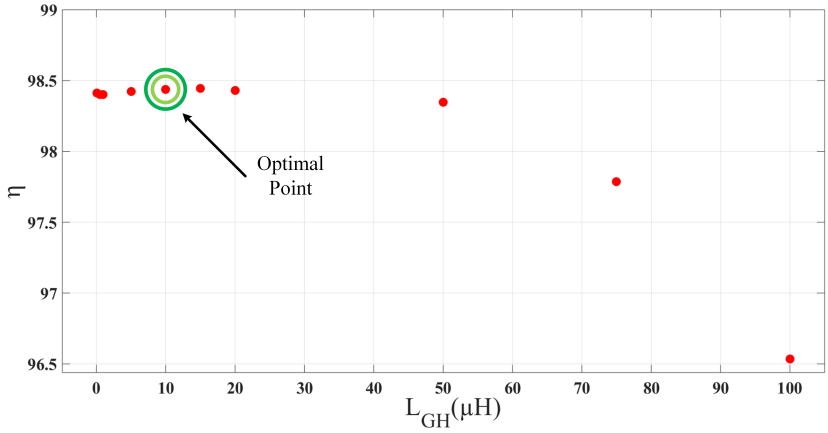
Figure 5.6. Pareto Front of the first phase of the multi-objective optimization process

As discussed before, the knee point (KP) is chosen as a reference for the optimal design. In this way, the corresponding design variables of the knee point are $R_{GH} = 199.8\ \Omega$ and $R_{GL} = 36.3\ \Omega$. Since the HS device is the main contributor in the term of the oscillations and the HS CM current path is more critical because of the higher values of the parasitic coupled capacitances compared to the LS one, an asymmetrical design points are obtained with a higher value for R_{GH} as it is expected.

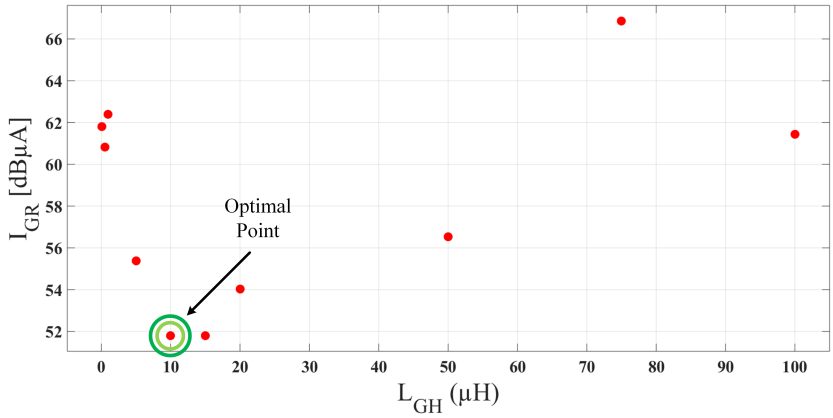
The aim of the second phase of the design approach is to improve the objective functions by optimally design of the HS gate inductance. L_{GH} is added in series with R_{GH} and then OrCAD simulations are carried out for ten different values of L_{GH} in the range of [0.1,100] μH. The same as the first phase, for each simulation, input-output pairs are collected, as shown in fig. 5.7. In our case, even without performing the regression and the optimization steps, it can be observed that the both objective functions reach their optimal points in $L_{GH} = 10\ \mu H$. Therefore, this value is selected for the second phase of the design approach.

In order to evaluate the effectiveness of the proposed design approach, a simulation study is performed. The GaN-based one inverter leg with three different gate driver circuits is simulated: a conventional symmetrical gate driver circuit with a gate resistor of 10 Ω

(case a), the optimal designed gate driver circuit without the ferrite bead (case b), and the optimal designed gate driver circuit with the ferrite bead (case c).



a. Efficiency



b. EMI level

Figure 5.7. OrCAD simulation results (red points) of the converter at the knee point of the gate resistors for different amounts of L_{GH}

Time-domain simulation results are shown in figures 5.8, 5.9, and 5.10 where HS drain-source voltage (V_{DS}) and CM ground current (I_{GR}) of the three cases are compared. As it is discussed before, the high transients dv/dt and di/dt occurred during turn-ON and turn-OFF switching intervals. These high frequency voltage/current interact between parasitics and result in CM ground current I_{GR}. It can be seen in fig. 5.9 that the high frequency ripples of V_{DS} and I_{GR} are significantly reduced in comparison with those of fig. 5.8 as it is expected because of the optimal design of the gate resistors. Adding the optimal gate inductance L_{GH}, further reduction of the ripples obtained during the turn-ON

switching interval of the HS device compared to case a and case b (fig. 5.10). For each of the three cases, the frequency spectrum of I_{GR} is depicted in fig. 5.10. It can be observed that the maximum amplitude of I_{GR} decreases from case a to case c. The corresponding frequency of the peak amplitude is equal to 20.4 MHz for the both case a and case b while it is equal to 20.1 MHz in the case c. It is because L_{GH} adds a phase change in the gate driver circuit impedances as well as I_{GR}.

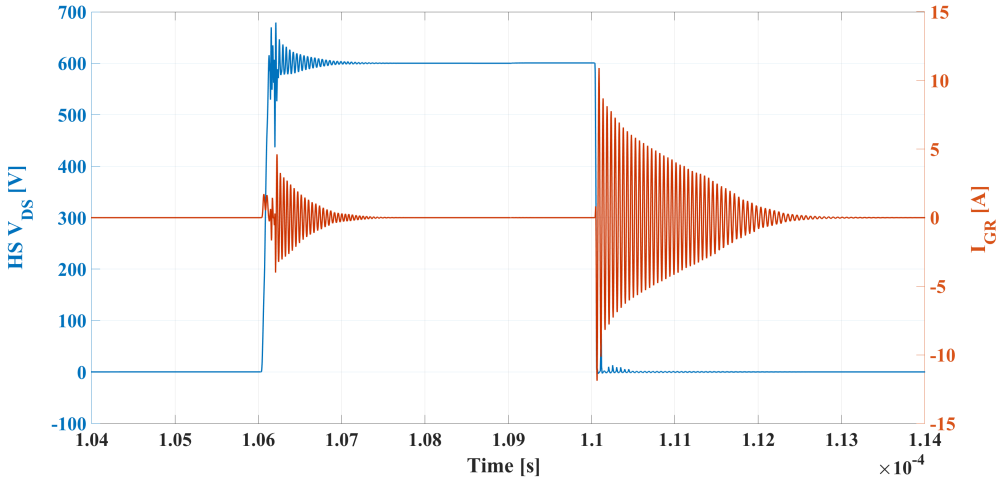


Figure 5.8. CM current and HS drain-source voltage (V_{DS}) evolutions: case a

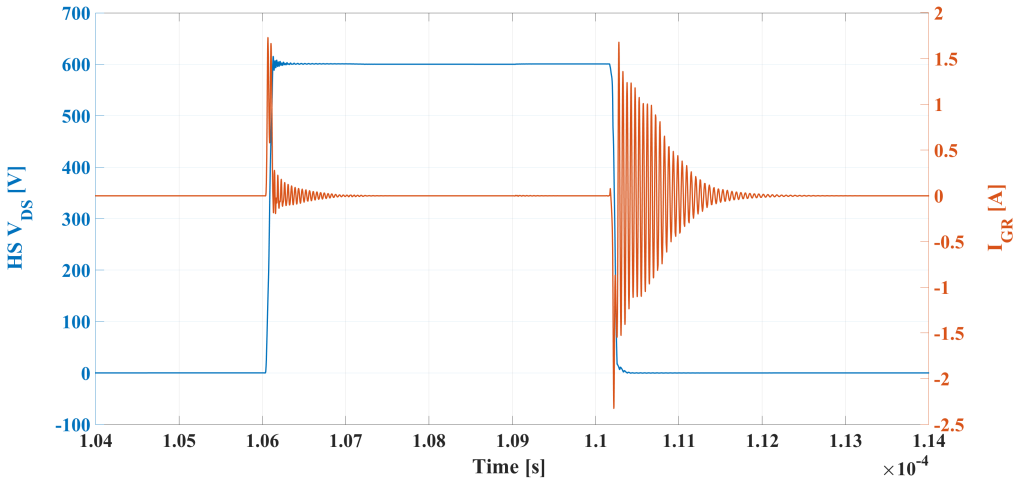


Figure 5.9. CM current and HS drain-source voltage (V_{DS}) evolutions: case b

Simulation results are summarized in table 5.2 in which a slight increase of the efficiency and a considerable reduction of EMI level are obtained for case a, case b, and case c, highlighting the effectiveness of the proposed design approach.

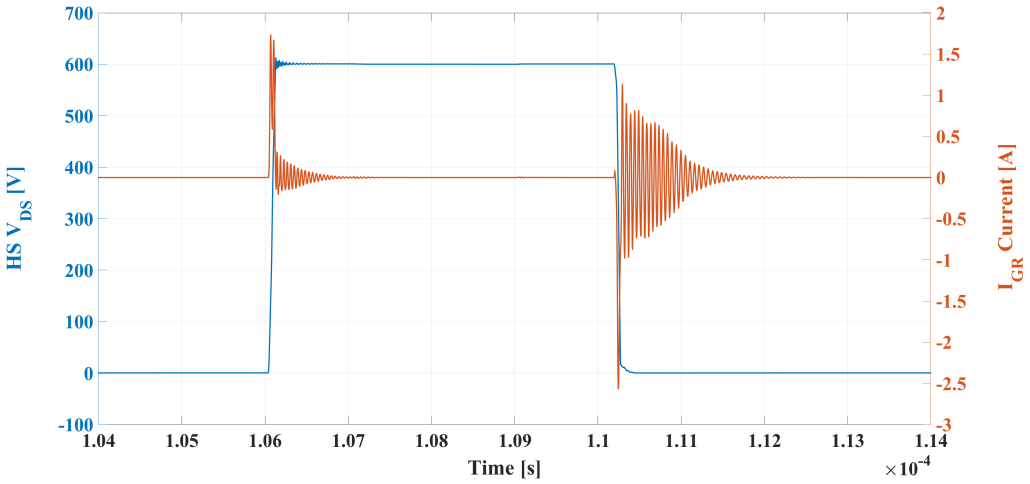


Figure 5.10. CM current and HS drain-source voltage (VDS) evolutions: case c

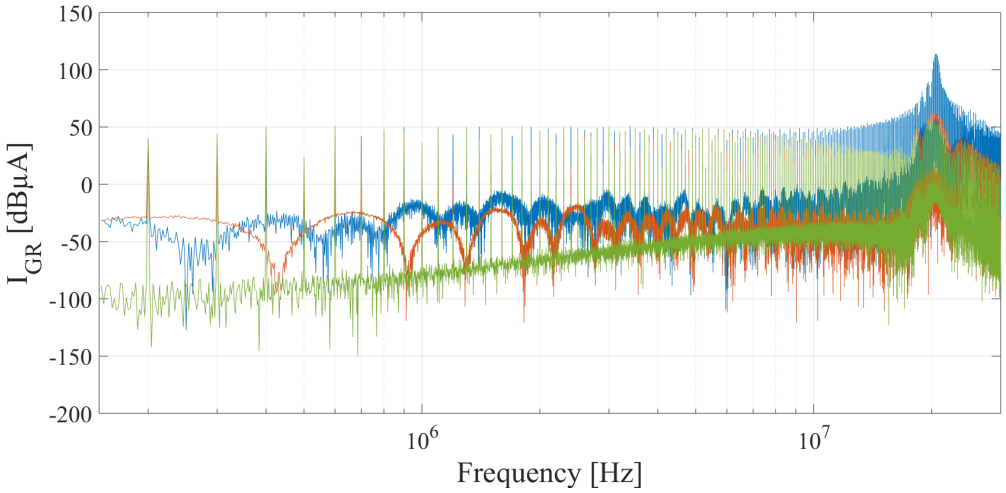


Figure 5.11. Frequency spectrum of I_{GR}: case a (blue), case b (red), case c (green)

Table 5.2. *Performance investigation of the converter with different gate driver*

Case	R_{GH} [μΩ]	R_{LH} [μΩ]	L_{GH} [μH]	η	I_{GR} [$dB\mu A$]
a	10	10	–	97.72 %	115
b	36.3	199.8	–	98.40 %	61.7
c	36.3	199.8	10	98.44 %	51.8

Conclusion and Future Works

In this thesis, the main goal was the improvement of the power density of the power electronic modules in the application of plug-in electric vehicle. The motivations were the benefit of electric vehicles because of their renewable and clean source of energy, prospective growth of electric vehicles in the future market, and the paradigm shift in power electronics from Silicon devices to the sate-of-the-art wide band gap devices such as Gallium Nitride and Silicon Carbide devices. In chapter two, the different types of the electric vehicles, their sub-systems, the role of power electronics in the electric vehicles, the wide band gap devices, and the both GaN-based and SiC-based dc-dc converters were studied.

To follow the goal of power density improvement in PEVs, first the universal dc-dc converter was acknowledged as an innovative solution of designing compact power electronic modules for PEVs. In the universal dc-dc converter, the dc-dc battery charger converter is integrated with the dc-dc power management converter. The universal dc-dc converter has four modes of operation: 1) Generative/acceleration drive mode (boost); 2) Regenerative/braking drive mode (buck); 3) Vehicle-to-Grid (V2G) plug-in mode (boost); and 4) Battery charging plug-In mode (buck). Such a universal converter should work from medium to high range of power. Second, the usage of the wide band gap devices for universal dc-dc converters was followed. The GaN device was found more attractive respect to its low switching power losses, however, its power rating is limited to the medium range of power.

Where in a multi-phase dc-dc converter, switching devices of the same technology are paralleled to share the current symmetrically between phases and provide the demanded power; in this thesis a two-phase SiC-GaN-based dc-dc converter was proposed. In the proposed converter, to evade the complexity and infeasibility of the multi-phase dc-dc converter with excessive number of phases, a SiC phase was paralleled with a GaN phase in a half-bridge boost topology. In the proposed converter, unlike a conventional multi-phase converter, switching devices of different technologies were paralleled and the current was shared between the phases asymmetrically in order to maximize the utilization of the GaN device, minimize the switching loss, and maximize the efficiency.

In chapter three, the topology, the power stage design, and the modeling of the proposed converter were studied. Then, a comprehensive power loss analysis was performed through OrCAD simulations using precise Spice model of the components to show the superiority of the proposed converter in comparison with a two-phase all-SiC dc-dc converter with a conventional topology of a multi-phase converter. In addition, a dead-time analysis of the GaN devices was studied in which a new method for dead-time loss calculation was suggested.

In the proposed converter, the current sharing between the phases are asymmetrical in a way to maximize the utilization of the GaN device based on the amount of the demanded power. Moreover, in the drive mode, the voltage of the dc bus should be regulated while in the plug-in mode; the power of the battery should be controlled. As a result, a cascade PI controller with an inner loop current control and an outer loop voltage control was designed in chapter four. The simulation results showed the satisfactory performance of the controller in the all modes of operation.

Finally, in chapter five, a gate driver multi-objective parameterization method was presented and applied for a GaN-based one inverter leg case study in which efficiency and EMI level of the circuit were the objectives to be optimized. The high side gate resistor, the low side gate resistor, and the high side ferrite bead (inductor) were parameterized through two phases design approach. The simulation results proved the effectiveness of the method to reach the optimized values of efficiency and EMI level for the circuit at the same time.

The proposed SiC-GaN-based dc-dc converter is currently under prototyping. The plan of the future work is to complete the hardware and verify the simulation results of the thesis (the comprehensive power loss contributors investigation and the dead-time power loss analysis method) in an experimental way. Once the hardware is prototyped and tested, the parasitics of the circuit can be extracted. Then, the gate driver multi-objective parameterization method can be applied for the proposed converter as well.

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Vita

Milad Moradpour received the B.S. and M.S. degree in electrical engineering from K. N. Toosi University of Technology, Tehran, Iran in 2007 and 2010 respectively. He presented the thesis “SiC-GaN-Based Universal DC-DC Converter for Plug-In Electric Vehicles” to receive the PhD degree at University of Cagliari, Italy in October 2018. His research interest includes power electronic switching converters, wide band gap devices, electric vehicles, and renewable energy resources.