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Organic Thin-Film Transistors: an Investigation of Device Properties, Applications and Market Perspectives

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XX Ciclo

Sommario

Dopo la metà degli anni ‘70 e la scoperta delle proprietà semiconduttive dei polimeri si aprì in modo definitivo per l’elettronica convenzionale una nuova era, quella dell’elettronica organica. Nei confronti di quest’ultima l’interesse sia scientifico che commerciale è cresciuto enormemente in questi ultimi dieci anni.

Infatti, la possibilità di creare dispositivi tramite processi realizzativi semplici e low-cost è solo uno degli aspetti peculiari dell’elettronica organica. A questi infatti si aggiunge la capacità di realizzare dispositivi su larga area con conseguente abbattimento di costi di produzione, di riduzione di tempi e di introduzione di un rapid-protyping dei dispositivi prodotti che rendono ancora più attraente questo nuovo mercato in crescita.

Nonostante questi notevoli vantaggi, la scienza dei materiali in questo campo si trova a fronteggiare ancora problemi quali la bassa mobilità dei portatori di carica, che richiede pertanto delle tensioni operative ancora troppo alte e, ancora, la forte interazione di questi materiali con l’ambiente (umidità, ossigeno, luce) che ne altera le proprietà di base. Tuttavia questa marcata sensibilità può essere impiegata proprio in quelle applicazioni dove il monitoraggio di variabili ambientali può’ diventare un vantaggio o dove la bassa velocità di risposta a segnali da monitorare ha tempi dell’ordine di quelli in gioco in quella data applicazione (es. particolari reazioni biologiche o biochimiche).

Questa tesi parte dallo studio delle proprietà dei materiali del transistor organico a film sottile (OTFT), ne propone un’applicazione al mondo della sensoristica studiandone infine le reali prospettive di mercato.

In particolare,

- Il primo capitolo parte con una introduzione ai materiali organici ed ai meccanismi di trasporto che li governano, per poi passare alla descrizione del principio di funzionamento ed alle equazioni dei transistor organici a film sottile (OTFT); vengono inoltre trattati aspetti come la definizione della tensione di soglia e l’effetto delle resistenze di contatto, concetti già sviluppati per l’elettronica del silicio ma che acquistano un significato differente nel mondo dei transistor a semiconduttore organico. Il capitolo si chiude con la descrizione delle principali tecniche di realizzazione dei dispositivi impiegate nel corso di questo lavoro.

- Il secondo capitolo presenta diverse tecniche per la caratterizzazione sia dei dispositivi che delle interfacce.

- Il terzo capitolo è focalizzato sulla descrizione di alcuni tra i principali effetti di non idealità che affliggono gli OTFT quali quello dello stress da polarizzazione (bias stress), dell'invecchiamento (aging) dei materiali organici in seguito all'effetto dell'ossigeno, della luce e dell'umidità; infine vengono studiati gli effetti di canale corto. Il primo lavoro, uno studio sull'effetto del bias stress e dell'aging è stato effettuato in collaborazione con il Dipartimento di Fisica dell'Università di Bologna. La parte relativa all'elaborazione di un modello che tenesse in conto gli effetti di canale corto per la caratterizzazione di transistor polimerici nasce da una collaborazione con l'azienda Konarka Austria GmbH sita a Linz (Austria).

- Il quarto capitolo prende in esame transistor a semiconduttore organico non piu' a geometria planare ma aventi rispettivamente geometria cilindrica e a doppio gate.
  Nel primo caso è stato realizzato e caratterizzato un transistor a partire da un filo di rame commerciale ricoperto da un sottile strato di isolante su cui è stato evaporato del semiconduttore organico e successivamente realizzati i contatti di source e drain. I transistor a doppio gate sono stati realizzati e caratterizzati durante un periodo di ricerca come *visiting research scholar*, sotto la supervisione del Prof. Christoph Brabec, presso Konarka Austria GmbH a Linz, (Austria) azienda leader mondiale per la ricerca nel campo delle celle solari organiche.

- La comprensione del ruolo dell'interfaccia semiconduttore/dielettrico nel transistor organico è oggetto di intensa ricerca e dibattito nella comunità scientifica mondiale. Il quinto capitolo prende in esame la relazione tra il dielettrico e l'influenza sulla morfologia del semiconduttore fatto crescere sopra di esso su un ampio campionario di dielettrici organici testati durante il lavoro di dottorato. Lo studio di questa interfaccia da un punto di vista chimico-fisico e dell'influenza di questa sul trasporto e quindi sulle performance elettriche dei transistor organici a film sottile è oggetto della parte finale del capitolo.

- L'impiego del transistor a film sottile in un dispositivo piu' complesso detto Charge-Modulated Organic FET (CMOFET) utilizzato come sensore di pH è l'oggetto del sesto capitolo.

- Il settimo capitolo, dedicato all'analisi delle reali prospettive di mercato dell'elettronica organica con particolare attenzione al caso degli OTFT usati come sensori, nasce in seguito all'assegnazione di una borsa J. W. Fulbright nell'ambito di un progetto pilota denominato BEST (Business Exchange for Student Training). Questo progetto, finanziato dall'Ambasciata americana in Italia, ha come obiettivo la promozione delle doti imprenditoriali di giovani ricercatori e lo studio della reale fattibilità economica di un'idea derivante dalla ricerca scientifica. Pertanto della consapevolezza maturata durante 6 mesi di corsi (Gennaio-Luglio 2007) del Master in Business Administration (MBA) presso la Leavey School of Business della Santa Clara University, Santa Clara, California nascono i contenuti proposti nella parte finale di questo lavoro di tesi.

Outline

Organic materials based on small molecules, polymers and composites have received a great deal of attention over the past years. When in 1977 Heeger, Shirakawa and MacDiarmid got a conductive polymer by doping polyacetylene with arsenic pentafluoride (AsF_5) a new era for Electronics arose: since then both n-type and p-type semiconductors based on organic molecules have been created and employed.

The possibility for printing circuits completely made of plastics and polymers is paving the way for exploiting both innovative and challenging applications that one could never have thought about only a few years ago. In addition, the low fabrication costs of the devices make them appealing for the market place. Thus, both scientific community and investors focus on the synthesis of new materials able to achieve better and better performances so that they can be marketable very soon. In fact, it is widely believed that organic electronics will be able to compete to inorganic devices for applications which need mechanical flexibility, large-area coverage and inexpensive mass production.

Unfortunately, organic materials are still too sensitive to ambient conditions such as oxygen, moisture and light that degrade and consequently change their pristine properties. Though many steps forward have been done, still a better control on the performances is needed for aiming to realistic applications of organic electronics.

However, this marked environmental sensitivity can be exploited in those applications where it can represent a plus rather than a minus such as gas, humidity or temperature sensing or in low speed switching circuits.

The first part of this thesis deals with organic thin-film transistors (OTFTs) and successively proposes their application as chemical sensors. It finally ends with an overview of the real market perspectives for organic-based sensors.

In particolar,

- Chapter 1 mainly deals with organic materials properties and the related transport mechanisms. Then the OTFT equation and working principles as well as the threshold voltage and the parasitic resistances role are discussed. Finally, the main device fabrication techniques used throughout this work are presented.

- Chapter 2 describes several techniques used to characterize both device and interfaces.

- Chapter 3 is focused on the non-idealities in OTFTs such as bias stress, aging and finally short-channel effects. Studies on bias stress and aging effects in the electrical performances of OTFTs were carried out in collaboration with the Physics Department of the University of Bologna, Bologna, Italy. Short-channel effects were modeled and simulated in collaboration with Konarka Austria GmbH based in Linz, Austria.

- Chapter 4 examines non-planar geometry OTFTs, more specifically the cylindrical as well as the double-gate case. In the former case, a transistor was made starting from a commercial wire on which a semiconductor layer and successively source and drain contacts were deposited. In the latter case, double-gate transistors were realized and characterized inside Konarka Austria GmbH (Linz, Austria) laboratories under prof. C. Brabec supervision (I was a *visiting research scholar* there from January to May 2006)

- The interface between an organic semiconductor/dielectric pair plays a decisive role in the functional performance of the Organic Thin-Film Transistors (OTFTs). First in this chapter an overview of the main organic dielectrics employed as the gate insulator in OTFTs fabrication will be presented; then the dielectrics we have been testing throughout this thesis work as well as the role of the interfaces will be discussed together with the trapping mechanisms occurring when dealing with organic materials, and finally how semiconductor morphology and chemical-physical nature of the interface can influence the OTFTs electrical performances.

- In Chapter 6, a brief overview of what is in literature on organic-based chemical sensors will be given. Starting from a deep insight into the Ion-Sensitive FET (ISFET) and its organic version, namely the Ion-Sensitive Organic FET (ISOFET). We will then examine the Charge-Modulated FET working principles useful to understand the Charge-Modulated Organic FETs which have been part of this thesis work and whose experimental results will be eventually shown and discussed.

Finally, Chapter 7 is dedicated to the analysis of the real organic electronics market perspectives focusing then on OTFTs used as sensors. This study was possible thanks to a J. W. Fulbright I was awarded in 2007. In fact the American Embassy in Italy created a pilot program called BEST (Business Exchange for Student Training) that is intended to foster entrepreneurship skills in young researchers having a smart scientific-based entrepreneurial

idea to bring to the market place. Therefore, most of the contents included in this chapter come from market analysis research and classes taken during the MBA (Master in Business Administration) program attended at the Leavey School of Business University of Santa Clara, Santa Clara, California (from Jan to July 2007).

Papers included in this thesis:

Detection of Chemical and Physical Parameters by means of Organic Field Effect Transistors

Bonfiglio, I. Manunza, P. Cosseddu, E. Orgiu

Book Chapter to appear in "Organic Semiconductors in Sensor Applications", *in press*.

Transparent dielectric films for organic thin-film transistors: a perspective for low cost, low size technologies

E. Orgiu, I. Manunza, M. Sanna, P. Cosseddu, and A. Bonfiglio

Thin Solid Films 516 (2008) 1533

An Analytical Model for Cylindrical Thin-Film Transistors

S. Locci, M. Maccioni, E. Orgiu and A. Bonfiglio

IEEE Transactions on Electron Devices 54 (2007) 2352

Photocurrent studies of stress and ageing in Pentacene Thin Film Transistors

B. Fraboni, A. Matteucci, A. Cavallini, E. Orgiu, A. Bonfiglio

Applied Physics Letters, 89 (2006) 222112

Investigation on different organic semiconductor/organic dielectric interfaces in pentacene-based thin-film transistors

E. Orgiu, M. Taki, S. Locci, B. Fraboni, A. Bonfiglio

Proceedings of *Material Research Society Fall 2007* (2008) in press

Short channel effects in organic thin-film transistors

S. Locci, M. Morana, E. Orgiu and A. Bonfiglio

Submitted to *IEEE Transactions on Electron Devices* (unpublished data)

Soft Lithography Fabrication of Fully Flexible and Transparent all Organic FETs for Large Area Applications

P. Cosseddu, E. Orgiu and A. Bonfiglio

Proceedings of *Material Research Society Fall 2006* 965 (2007) S07-02

Towards the textile transistor: assembly and characterization of an Organic Field Effect Transistor with a cylindrical geometry

M. Maccioni, E. Orgiu, P. Cosseddu, S. Locci and A. Bonfiglio

Appl. Phys. Lett. 89 (2006) 143515

(selected for publication on the Virtual Journal of Nanoscale Science and Technology of the American Institute of Physics and the American Physical Society).

On the efficiency of electron trapping at the insulator/semiconductor interface of organic field effect transistors

E. Orgiu, B. Fraboni, A. Cavallini and A. Bonfiglio

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The textile transistor: a perspective for distributed, wearable networks of sensor devices

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Producing Smart Sensing Films by Means of Organic Field Effect Transistors

I. Manunza, E. Orgiu, A. Caboni, M. Barbaro and A. Bonfiglio

Proceedings of *28th IEEE EMBS Annual International Conference*, Sept. 2006, New York City, New York, USA

Device Physics of Organic Thin Film Transistors Operating in Saturation Regime

M.Morana, E. Orgiu, S. Locci, A. Bonfiglio, M. Scharber, D. Waller, C. Brabec

Manuscript in preparation, to be submitted to *Physical Review B*

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Chapter1

Organic Thin-Film Transistors

Organic materials based on small molecules, polymers and composites have received a great deal of attention over the past years. When in 1977 Heeger, Shirakawa and MacDiarmid got a conductive polymer by doping polyacetylene with arsenic pentafluoride (AsF_5) a new era for Electronics was opened: both n-type and p-type semiconductors based on organic molecules have been created and employed since then.

The possibility for printing circuits completely made of plastics and polymers is paving the way for exploiting both innovative and challenging applications that one could never have thought about only a few years ago. In addition, the low fabrication costs of the devices make them appealing for the market place. Thus, both scientific community and investors focus on the synthesis of new materials able to achieve better and better performances so that they can be marketable very soon. In fact, it is widely believed that organic electronics will be able to compete to inorganic devices for applications which need mechanical flexibility, large-area coverage and inexpensive mass production [1].

Unfortunately, as it will be shown in the following, organic materials are still too sensitive to ambient conditions such as oxygen, moisture and light that degrade and consequently change their pristine properties. Though many steps forward have been done, still a better control on the performances is needed for aiming to realistic applications of organic electronics.

1.1 Generalities on organic semiconductors

Organic semiconductors are unsaturated carbon based materials. When the four electrons in the outer shell of the carbon atom are taking part in strong covalent bonds, the material is called saturated and has insulating properties. Instead, the unique property of Carbon of hybridizing its electronic orbitals, which in the ground state are found in the $1s^2$ $2s^2$ $2p^2$ configuration, allows to modify the s and p orbitals to form hybrid 3 sp^2 orbitals. These orbitals form an angle of 120°, defining a triangle coplanar to the carbon atoms. They form the stronger bonds with other atoms (s bond) while the fourth orbital is the p_z orbital, which is perpendicular to the plane of the atoms. The overlap of the p_z electrons from neighbor carbon atoms allows the formation of a delocalized electron density above and below the molecule plane, the so-called π-orbitals.

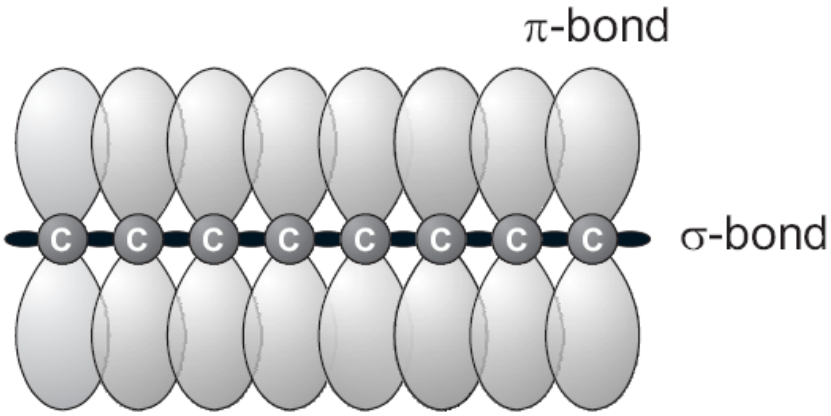

Figure 1.1 Schematic representation of the electronic bonds between carbon atoms

When an electron couple is bonded through a π-bond it has a higher special freedom degree which gives conductive properties to the molecule. In other words, the presence of alternating single and double bonds between carbon atoms, called conjugation, gives semiconducting properties to these materials.

The system may be expected to behave as a one dimensional metal, however, symmetry breaking reduces the energy of the system, resulting in an energy gap that separates two delocalized energy bands, the highest occupied molecular orbital (HOMO) and the lowest occupied molecular orbital (LUMO). Since the band gap is normally from one to a few eV, the transport band is normally unoccupied and the conductivity very low. The value of the energy gap depends on the structure of the material, and decreases for an increasing number of repeat units composing the molecule [2] [3] [4]. The repetition of many single units

(monomers) can define an oligomer (till five monomers) or, more commonly, a polymer (more than five monomers) that therefore presents normally a lower bandgap and energy bands with closer energy levels with respect to the analogous small molecule (oligomer). Along the molecule backbone the monomer units are bound by strong covalent forces, but the interaction between different molecules, however, consist of weaker Van der Waals forces. This feature, responsible for the characteristic physical properties of polymers like flexibility and elasticity and many others that make polymers today universally applied, represents however an intrinsic limitation for their use in electronics especially in those applications that require high- switching frequencies and others as better explained further.

1.2 Charge transport in organic materials: models and theories

Inorganic semiconductor crystalline lattices (Si, Ge etc.) are characterized by three dimensional long range order and strongly coupled atoms. The charge transport happens therefore generally rather isotropically in delocalized energy bands separated by a forbidden energy gap where charge carriers (intrinsic or extrinsic) can move with a relatively large mean free path limited usually by scattering of the carriers at thermal lattice vibrations, i.e. phonons. Consequently the mobility of the charge carriers decreases with increasing temperature. In conjugated polymers the charge transport happens within a single chain (*intrachain*) and between different molecules (*interchain*) or even from a domain, commonly called grain, to another. Along the molecule, the HOMO and LUMO energy bands are generally narrow and can easily be modified by molecular disorder. The electric charge is delocalized along the π-conjugated segments of the polymer backbone for rather short distances (typically around 5 nm), separated by chemical defects, such as a non-conjugated sp^3-hybridized carbon atom on the polymer backbone, or by structural defects, such as chain kinks or twists out of coplanarity. A current conduction over longer distances implies therefore the possibility for the carriers to move from chain to chain. When the π-orbitals of different molecules overlap this process becomes easier due to a degree of delocalization between different polymer chains. Oppositely, a reduced interchain charge transfer process turns out in strong reduction of the charge mobility in the material compared to the one associated to the intrachain transport. The efficiency of the interchain conduction process strongly depends on the molecular structure that determines the way chains arrange respect to one another. Planar molecules show in principle an easier stacking

and better electronic coupling via the π-orbitals. With respect to this issue, films made of solution-processed conjugated polymers and films made from sublimation of analogous oligomers may present very different transport characteristics, correlated to the interchain spacing and degree of order. Consequently, due to disorder, the semiconductor cannot be regarded simply as having two delocalized energy bands separated by an energy gap. Instead, the charge transporting sites, which are the segments of the main chain polymer, give generally rise to a Gaussian Density of States (see Fig.1.2), implying that all states are localized [5].

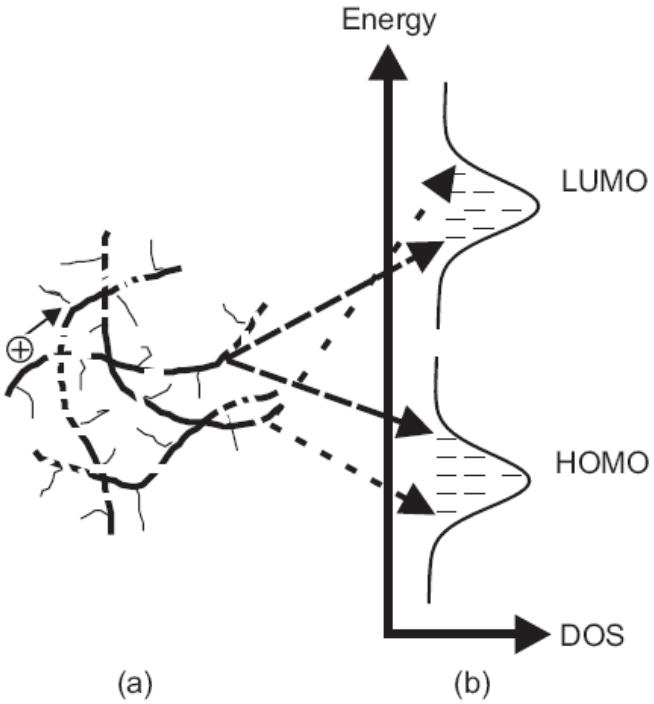

Figure 1.2 (a) Schematic view of polymer chain segments broken by defects, kinks between which the charge carriers hop and consequent representation of (b) Density Of States (DOS) and energy distribution of the localized states, approximated by a Gaussian distribution for the LUMO and HOMO levels.

The shape of the density of states (DOS) is suggested to be Gaussian, because of the observed Gaussian shape of the optical spectra [5]. The shape of the DOS, which is a manifestation of the disorder of the system, is however important for the description of charge transport. In conclusion, the charge transport and semiconductor properties of polymeric semiconductors are rather sensitive to the morphology of the polymer chains and the local structural order within the film. Structural and energetic disorder in conjugated polymer systems are therefore of importance in the description of charge transport involving different mechanisms and electronic processes.

Several transport models have been proposed for organic semiconductors over the past decades, but despite the fast progress in organic electronics an univocal model has not been developed yet.
Hereinafter are reported the most famous and valid models that refer to different behavior of the charge carriers in organic semiconductors.

1.2.1 The polaron model

First introduced in the case of inorganic semiconductor, the polaron model has been used later for describing transport in conjugated polymers [6]. This model relies on the interaction phonon-electron. A polaron can be described as a quasi-particle generated by the lattice deformation due to the charge of the carrier. The hopping rate of carriers from occupied *i* to unoccupied *j* localized donor state depends on the height of the energetic barrier E_j-E_i and can be expressed as

$$v_{i\to j} \propto \frac{1}{\sqrt{E_r T}} \exp\left[-\frac{\left(E_j - E_i + E_r\right)^2}{4E_r kT} \right] \qquad (1.1)$$

where E_r is the intramolecular reorganization energy. The charges moving by thermally activated hops between adjacent sites have a mobility which is field (F) and temperature (T) dependent:

$$\mu = \mu_0 \exp\left[-\frac{E_r}{4kT} - \frac{(aF)^2}{4E_r kT} \right] \frac{\sinh\left(\frac{aF}{2kT}\right)}{\frac{aF}{2kT}} \qquad (1.2)$$

where μ_0 is slightly temperature dependent. However, using Marcus theory the polaron contribution to the activation of the mobility is insignificant. The activation of the mobility using this model amounts to 25-75 meV [7], while using the disordered model the activation energy amounts to 420 meV [8].

1.2.2 Multiple Traps and Release (MTR) model

Another model used to account for the low mobility in amorphous organic materials is the multiple trapping and release model. Traps are levels localized at lattice defects or impurities in which the charge carriers are immobilized. These traps can be deep traps, which are located near the center of the band gap, or shallow traps, which are located close to the conduction or valence band as shown in Fig. 1.3

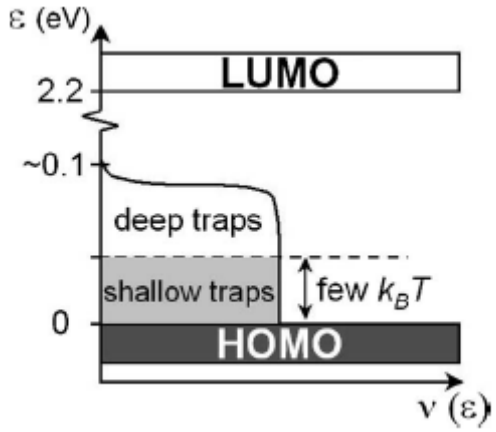

Figure 1.3 Schematic diagram of the energy distribution of localized electronic states in the energy gap between HOMO and LUMO bands

The effect of these states on charge transport depends on their energy. If the energy of a localized state is separated from the mobility edge by more than a few k_B T, the state acts as a deep trap: the charge, once trapped in a deep trap, cannot be released by thermal excitations. Developed for hydrogenated amorphous silicon (a-Si:H) by Le Comber and Spear [9], the multiple trapping and release model has been used more recently by Horowitz et al. [10] to explain the transport in sexithiophene FETs. This model assumes an exponential distribution of gap states. The charges injected or the charges which are already present in the organic semiconductor are trapped into localized states with a probability close to one and then released through a thermally activated process. The drift mobility μ_D is given by:

$$\mu_D = \mu_0 \alpha \exp\left[-\frac{E_T}{k_B T}\right] \qquad (1.3)$$

where μ_0 is the mobility at the band edge, α is the ratio between the effective density of states at the transport band edge and the density of traps, and E_T is the energy of the trap state. It has been demonstrated that the transport of carriers depends on the energy level of the trap states, the temperature and the voltage applied [10].

1.2.3 Variable Range Hopping (VRH) model

In the previous model, as stated above, the assumption made is that most of the charge carriers are trapped in localized states. Then the amount of released charge carriers to an extended-state transport level (a concept close to the valence band for *p*-type semiconductors) depends on the temperature, the gate voltage and obviously the energy level of the localized states. However, while extended-state transport may occur in highly ordered vacuum-evaporated molecular films as stated by Horowitz, we do not expect such behavior in amorphous organic films where the charge carriers are strongly localized. In 1998, Vissenberg and Matters [11] developed the concept of variable-range hopping (VRH), i.e., a carrier may either hop over a small distance with a high activation energy or hop over a long distance with a low activation energy. The temperature dependence of the carrier transport in such a system is strongly dependent on the density of localized states. In the case of a field-effect transistor (this model was by the way developed in order to explain transport in polymeric FET) , an applied gate voltage gives rise to the accumulation of charge in the region of the semiconducting layer that is close to the insulator. As these accumulated charge carriers fill the lower-lying states of the organic semiconductor, any additional charges in the accumulation layer will occupy states at a relatively high energies. Consequently, these additional charges will – on average- require less activation energy to hop away to a neighbor site. This results in a higher mobility with increasing gate voltage.
Let us consider the percolation criterion for the system

$$B_c \approx \pi\left(\frac{T_0}{2\alpha T}\right)^3 N_t \exp\left(\frac{\varepsilon_F + s_C k_B T}{k_B T_0}\right)$$

(with N_t the number of states per unit volume, k_B the Boltzmann's constant and T_0 a parameter that indicates the width of the exponential distribution) where we have assumed that the site positions are random, that most of the hopping takes place between tail states

and that the maximum energy hop is large. The expression of the conductivity as a function of the occupation δ and the temperature T is obtained:

$$\sigma(\delta,T)=\sigma_0\left(\frac{\pi N_t\delta(T_0/T)^3}{(2\alpha)^3 B_c\Gamma(1-T_0/T)\Gamma(1+T_0/T)}\right)^{T_0/T}$$

where the conductivity increases superlinearly with the density of carriers ($\sigma \propto \delta^{T_0/T}$). This is due to the filling of localized states: an increase in the carrier density gives rise to an increase in the average energy, thus facilitating an activated jump to the transport energy mentioned above.

In this model the field-effect mobility was found to follow the relationship:

$$\mu_{FE}=\frac{\sigma_0}{e}\left(\frac{\pi(T_0/T)^3}{(2\alpha)^3 B_c\Gamma(1-T_0/T)\Gamma(1+T_0/T)}\right)^{T_0/T}\left[\frac{(C_iV_g)^2}{2k_BT_0\varepsilon_s}\right]^{T_0/T-1} \quad (1.4)$$

where we have assumed that the thickness *t* of the semiconductor layer is sufficiently large such that V(*t*) = 0. Then the field-effect mobility is independent of the thickness *t* as well as the bulk carrier occupation δ_0. We note that the N_t dependence of the charge distribution in the accumulation layer is exactly canceled by the N_t dependence of $\sigma(\delta,T)$.

1.3 OTFTs: generalities and equations

Organic thin-film transistors (TFTs) have made an impressive progress over the past ten years, and the first electronic applications are now beginning to appear. Different research groups have demonstrated integrated circuits [12] [13] [14] [15], active-matrix displays [16] [17] [18] [19] and chemical sensors [20] [21] [22] using organic TFTs, while the Plastic Logic group has reported organic integrated circuits fabricated in part with the use of inkjet printing. [23] [24].

Instead of competing with conventional Si/GaAs technologies, OFETs may find niche applications in low-performance radio-frequency technologies as well as light emission. The main advantages of using OFETs rely on vapor/solution phase fabrication and good compatibility with different substrates, including flexible plastics [25] [26], and opportunities for structural tailoring [27] [28] [29].

1.3.1 Working principles and equations of organic FETs

An organic field-effect transistor (Fig. 1.4) is basically a three terminal device where the device output current flowing between the source and drain electrodes and collected at the drain terminal (I_{DRAIN} current) is modulated and controlled by applying input voltages to the drain (V_{DRAIN}) and gate (V_{GATE}) electrodes both referred to the source electrode (V_{SOURCE}). The metal-insulator-semiconductor (MIS) structure formed by respectively the gate electrode, the gate dielectric and the active layer constitutes the core structure for the whole device. All the charges collected at the interface between the semiconductor and the dielectric by applying a voltage to the gate electrode (field effect) can be then drifted along the channel when a voltage is applied to the drain terminal.

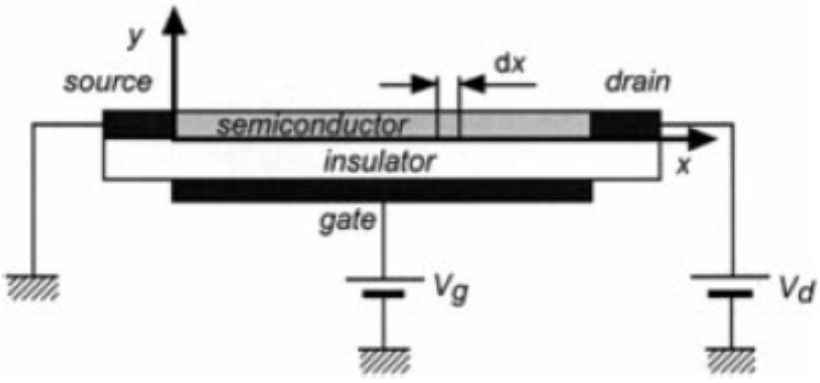

Figure 1.4 Schematic view of an Organic Field-Effect transistor (OFET)

A peculiarity of the organic FETs is that, differently from the inorganic devices, that work in inversion mode, they work in accumulation mode, i.e., their conduction mainly occurs, in the on-state, thanks to the layer of charge carriers which forms in the semiconductor, within few angstroms from the insulator/semiconductor interface, upon application of a gate bias and these charges are of the same type of the majority charge carriers that flow into the device in the off-state. A small fraction of the total drain current is therefore determined by the free carriers in the semiconductor, which can be thermally generated or are due to unintentional doping. Despite this fundamental difference, the characteristic equations of the devices resemble those of the inorganic MOSFET transistors [30] and can be, in first approximation, applied to the Organic FET:

$$I_{DS} = \mu\ C_i \frac{Z}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{1.5}$$

in the linear zone, where $V_{DS} \leq (V_{GS} - V_{TH})$ and

$$I_{DS} = \frac{1}{2}\mu C_i \frac{Z}{L}(V_{GS} - V_{TH})^2 \tag{1.6}$$

in the saturation zone, where $V_{DS} \geq (V_{GS} - V_{TH})$. The carriers mobility depends on the transversal electric field (gate-source) because of physical phenomena mostly related to the charge transport nature in the semiconductor and usually follows the relationship

$$\mu = \mu_0 (V_{GS} - V_{TH})^{\alpha} \tag{1.7}$$

that is in accordance with both Multiple Trapping and Release and Variable Range Hopping transport models presented above.

When an OFET is active, upon the application of negative V_{GS} and V_{DS}, the organic material is said to be *p*-channel or *p*-type and holes are the majority charge carriers (Fig. 1.5). On the other hand, when a (positive) S-D current is observed upon the application of positive V_{GS} and V_{DS}, the semiconductor is *n*-channel or *n*-type since the electrons are mobile.

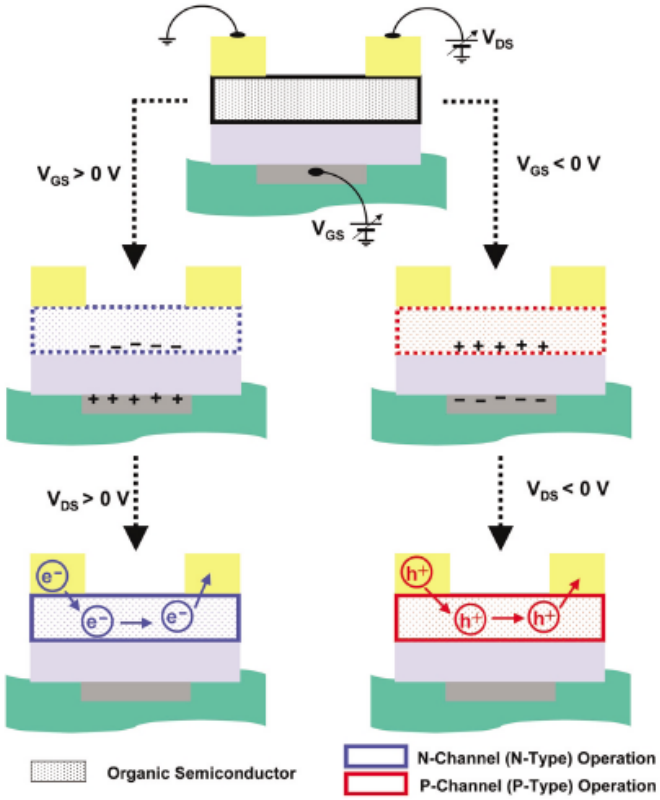

Figure 1.5 Schematic operation of a n-type and p-type Organic Field-Effect transistor (OFET)

In a few cases, OFETs operate for both V_{GS} and V_{DS} polarities and the semiconductor is said to be ambipolar. Note that the fundamental difference between n-/p-organic and n-/p-inorganic semiconductors is that in the latter case, the majority charge carrier types is determined by (chemical) doping process while in the case of organics, the transported charge depends on which carrier type is injected/extracted by the contact. Therefore it is important to stress that in organic materials the classification of organic semiconductors as 'p-'or 'n-'type has no absolute meaning but is strongly related to the FET device structure/material combination on which the transport characteristics are measured [31]. However, for ease of comparison and following common practice in the organic materials community, most of people usually describe p-/n-channel structures as well-separated semiconductor classes.

An OFET can be assembled in several configurations (Fig. 1.6). The source and drain contacts are deposited on the semiconducting layer in the top-contact configuration or staggered geometry whereas they lay under the semiconductor in the bottom-contact configuration. Regarding to the gate, it can be deposited either over the substrate with the dielectric layer on top (bottom-gate configuration) or the gate dielectric at the top of the

whole structure (top-gate configuration). Consequently we can have top-contact bottom-gate configuration (Fig.1.6a), bottom-contact bottom-gate configuration (Fig.1.6b), bottom-contact top-gate configuration (Fig.1.6c) and finally top-contact top-gate configuration (Fig.1.6d).

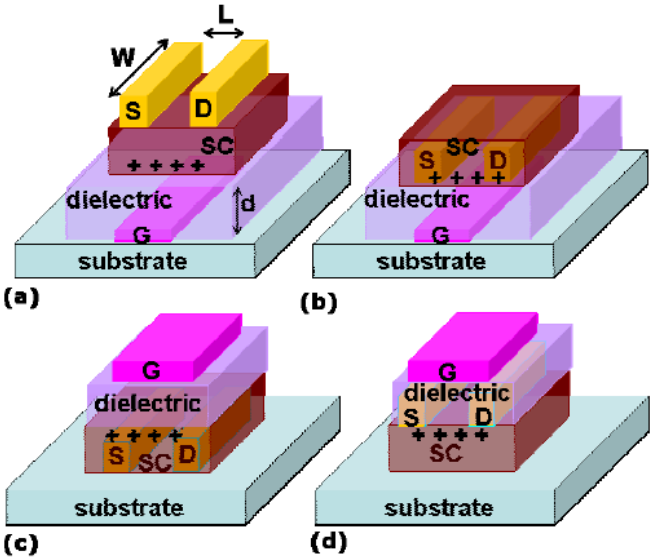

Figure 1.6 All of different OFET configurations: (a) top-contact bottom-gate, (b) bottom-contact bottom-gate, (c) bottom-contact top-gate and (d) top-contact top-gate

1.3.2 The concept of threshold voltage in OTFTs

Since we used the concept of threshold voltage in the previous paragraph and this concept appears in the OFET equations a digression on this topic is needed.

In fact this concept is rather different than it is for MOSFET devices. In such devices when the gate is biased to positive (negative) for an n-type (p-type) channel, an inversion layer is induced at the insulator/semiconductor interface, thus forming a conducting channel between source and drain. This has two consequences: first, the source and drain regions, along with the conducting channel between them, are isolated from the substrate by a depletion layer. Next, the conducting channel only forms after the gate voltage is beyond the so-called *threshold voltage*, that is, the onset voltage for the inversion regime. In first approximation, the threshold voltage can be defined as the gate bias where the Fermi level at the insulator/semiconductor interface crosses the middle of the gap [30]. The inversion regime is very specific to crystalline silicon. Instead, OTFTs operate in the accumulation

regime, where the gate voltage is polarized positively (negatively) versus the n-type (p-type) substrate. Accordingly, the source and drain consist of simple ohmic contacts on a thin semiconductor film. In such a geometry, there is no depletion layer to isolate the conducting channel from the substrate, and a very low conductivity is therefore required. Another consequence of the absence of a depletion layer is that in principle, when no traps are present the threshold voltage should be nil, in accordance with [32].

1.3.3 Contact Resistance Effect

In the above discussion it was assumed that the carriers injection is not a limiting factor. In other words the contacts were considered low-ohmic. However, the contacts can form a severe barrier for the injection of carriers [33] [32]. The most obvious one is when at the electrodes a high-resistive region is formed. This causes the current to grow sub-linearly in the linear region. This can be easily shown for instance in a simulation.

For strong currents, the contact resistance can become the limiting factor and the current saturates and becomes independent of V_G;

We have to imagine that the FET is made up of two contact resistances ($2R_c$) and the channel resistance, connected in series, make the current grow linear with V_G (as explained by the text above). The channel resistance is thus proportional to 1/ V_G. For large V_G the channel resistance disappears and the current settles at V_{ds} / 2 R_c.

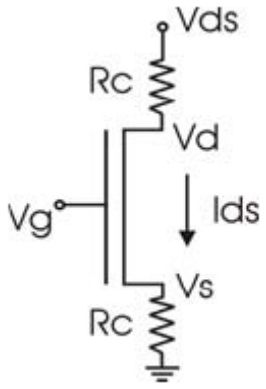

Figure 1.7 Equivalent circuit if an OTFT with the contact resistance effect included

Thus, when the current is increasing, the contact resistance induces a voltage drop at the source, $V_s = I_{ds} R_c$, the field at the source (V_G) is reduced and the current drops.

1.4 Fabrication Techniques

Organic semiconductors are usually obtained as thin films; accordingly, OFETs often present an inverted architecture (bottom-gate configuration), in which the gate electrode is laid down first, the deposition of the semiconducting film usually being the last step. At the beginning of the organic electronics era, the gate was constituted by a highly doped silicon wafer, on which a silicon oxide layer was thermally grown but over the past years the gradual substitution with polymeric dielectrics is spreading out being that the latter are flexible, solution-processable and have higher dielectric permittivity. The source and drain can be deposited by either conventional microlithographic techniques when gold made or microcontact printing technique [26] when conductive polymers such as PEDT:PSS substitute gold.

Over this thesis work thermal vacuum evaporation, photolithography and spin-coating techniques have been employed to realize respectively gold electrodes and semiconductor films with an almost controlled thickness as well as dielectric and semiconducting films of polymers.

1.4.1 Vacuum evaporation

Spin-coating, which requires high viscosity solutions, is not usually applicable to small molecules. These are more appropriately deposited by vacuum evaporation, which consists of heating the material under reduced pressure. The process is conducted in a very high or ultra high vacuum chamber. The organic material is put into a metal brace, normally a crucible, which is heated by Joule effects, or sometimes with an electron gun, and the substrate placed a few centimetres above the crucible.

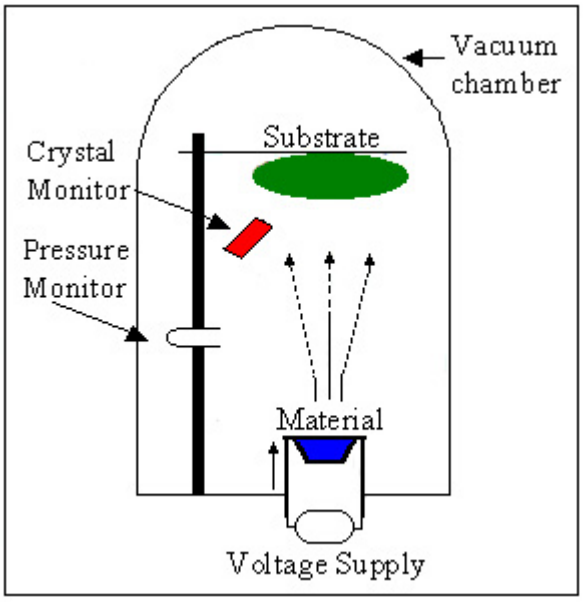

Figure 1.8 Schematic of an evaporation chamber: a large voltage drop between the electrodes generates a current that flows through the crucible filaments that, heating the crucible according to Joule effect, and gives place to a material evaporation on the sample placed a few centimeters far from it.

We note that, in principle, this technique cannot be used for polymers, which tend to decompose by cracking at high temperatures. Its main advantages are the easy control of the thickness and purity of the film, and the fact that highly ordered films can be realized by monitoring the deposition rate and the temperature of the substrate.

Its primary drawback is that it requires sophisticated instrumentation, in contrast to the simplicity and low cost of spin-coating.

1.4.2 Spin-coating

One of the most elegant ways to realize a nice polymer film is spin-coating. A machine used for spin coating is called spin coater, or simply spinner. When the technique is well handled, it allows the production of very homogeneous films with perfect control of their thickness over relatively large areas.

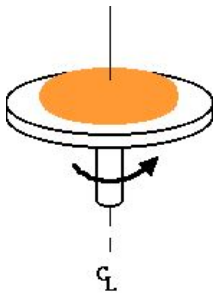

Figure 1.9 Spin-coating process: a certain amount of solution is placed on the spincoater plate that rotating spreads uniformly the polymer making uniform films with a very good control on their thicknesses.

A requirement for this technique is a good solubility of the polymer. Spin coating is a procedure used to apply uniform thin films to flat substrates. A certain amount of the material in solution is placed on the substrate, which is then rotated at high speed in order to spread the fluid by centrifugal force. Rotation is continued while the fluid spins off the edges of the substrate, until the desired thickness of the film is achieved. The applied solvent is usually volatile, and simultaneously evaporates. So, the higher the angular speed of spinning, the thinner the film. The thickness of the film also depends on the concentration of the solution and the employed solvent.

1.4.3 Photolithography

Photolithography is a very common technique widely used in Semiconductor industry for the patterning of the devices. The goal of this technique is to transfer a certain pattern on a substrate. For this purpose two elements are required: i) a mask which reproduces the image to transfer on the substrate and it must be opaque to ultraviolet light; ii) a photosensitive material, called photoresist, which is exposed to ultraviolet light during the process by interposing the mask between the UV source and the surface. There are two types of resists, namely, positive and negative photoresist. Positive resist is 'softened' by exposure to the Ultra-Violet (UV) light and the exposed areas are subsequently removed in the development

process, the resist image will be identical to the opaque image on the mask. Negative resist is 'hardened' by exposure to ultra-violet light and therefore it is the unexposed areas that are removed by the development process, the resist image will be a negative image of the mask. Photoresists are sensitive to a wide range of wavelengths of light, typically 200 - 500 nm, this range of wavelengths includes the visible blue and violet contained in normal white light. For this reason, photolithography fabrication usually employs a special filtered light to remove all of the wavelengths to which the resist is sensitive.

Starting from a thin metal film, usually a gold film, deposited over the surface through thermal evaporation a thin positive photoresist film is deposited onto the sample surface; generally this process is made by spin coating. Before the exposure process, a soft baking process of the sample is usually required in order to dry the deposited photoresist and the duration of this dry process depends on the substrate where the photoresist has been deposited. When this substrate is for instance a thin PET film (Mylar®, that we will sometimes employ in this work) an ordinary dry process of the photoresist at high oven temperature is possible due to the poor thermal resistance of this film. However, when the substrate is silicon dioxide a fast and at high temperature oven baking is possible.

Then, during the exposure process, the photoresist layer is exposed to UV light through an opaque mask; in this way it is possible to define the mask pattern on the resist film. After exposure, the sample is developed in order to remove the unwanted resist, thus leaving only the defined pattern on the substrate. Usually, a post baking step is made to increase resist adherence to the substrate and in particular to increase its resistance to etch process. Taking advantage of the presence of the patterned resist film, it is then possible to etch the metal in the undesired areas. Once the etching process is performed we can remove the photoresist by using an organic solvent, generally acetone, and the basic structure for the realization of the final device is assembled

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Chapter2

Device and Interface Characterization Methods

Organic materials are characterized by a poor degree of crystallinity due to weak intermolecular Van der Waals forces. Consequently the charge carriers mobility is quite lower if compared to that of Si or GaAs and this requires high voltages operation mode. At the same time being not properly crystalline materials makes it difficult to "interface" them to metals or polymers (conductive, insulating or even semiconducting). Therefore, characterizing all the device interfaces is absolutely needed: dielectric/semiconductor as well as source and drain contacts/semiconductor interface are both responsible for charge carriers trapping. In addition to that, there are many major aspects that have to be taken into consideration. First, how the charge injection mechanism through the contacts occurs is still on debate because it turns out that even the Mott-Schottky model is not always valid when dealing with either organic semiconductor/metal or organic semiconductor/conductive polymer interfaces. Nevertheless, the chemical-physical nature of the dielectric/semiconductor pair is also thought to be directly related to the ambipolar behavior of charge carriers therefore playing a major role on the device operation.

For these reasons, this chapter is focused on the description of the characterization techniques we used during this thesis in order to correlate interfacial and transport properties of materials to the electrical device performance.

In particular we used:

1. *Current-Voltage (I-V)* characterization of FET structures for extracting parameters such as threshold voltage (V_{TH}), I_{ON}/I_{OFF} ratio and mobility of the charge carriers under the application of an electric field (μ_{FET}).
2. *Capacitance vs. Frequency (C-f)* characterization of Metal-Insulator-Metal (MIM) capacitors for evaluating the gate dielectric capacitance and consequently (given ε_{ins})

the insulating layer thickness as well as *Capacitance vs. Voltage (C-V)* characterization of Metal-Insulator-Semiconductor (MIS) capacitors at different frequencies for a deeper insight into the trapping mechanisms occurring at the semiconductor/dielectric interface.

3. *Photocurrent (PC) Spectroscopy* for gathering information on the bias stress or aging process going on in the semiconductor layers (see Chapter1) and more generally as a tool for understanding trapping dynamics through excitation of matter states.
4. *Electro-chemical Impedance Spectroscopy (EIS)* for understanding how specific thio-aminic groups chemically bounded on gold can protonize and how efficient is this process because it is the base working principle for pH detection in aqueous solutions as shown in a further chapter.

2.1 Current – Voltage characterization

All the characterizations carried out on the TFTs structures, i.e., output characteristics (I_D-V_D) and trans-characteristics curves (I_D-V_G), were performed by using the Agilent 4155 [www.agilent.com] which is an electronic instrument for measuring and analyzing the characteristics of semiconductor devices. This one instrument allows you to perform both measurement and analysis of measurement results. Following is a summary of Agilent 4155 features:

• *Measurement Capabilities*

The 4155 has four highly accurate source/monitor units (SMUs), two voltage source units (VSUs), and two voltage measurement units (VMUs). The 4156C is designed for Kelvin connections and has high-resolution SMUs (HRSMUs), so the 4156C is especially suited for low resistance and low current measurements. You can measure voltage values with a resolution of 1 μV by using the differential measurement mode of VMUs. The 4155 can perform two types of measurements, sweep measurement and sampling measurement. The 4155 also provides knob sweep measurement function for quick sweep measurements executed by rotating the rotary knob on the front panel. The 4155 can perform stress testing. That is, it can force a specified dc voltage or current for the specified duration. Also, you can force ac stress by using pulse generator units (PGUs), which are installed in Agilent 41501A/B SMU/Pulse Generator Expander.

• *Analysis Function*

The 4155 provides a marker and two lines for analyzing the measurement results. The 4155 also provides the automatic analysis function which moves marker and lines at desired location and displays desired calculation results automatically after measurement is completed.

• *Data storing*

The 4155 allows you to store measurement setup information, measurement data, and instrument setting information on a 3.5-inch diskette using the built-in flexible disk drive, or on a NFS server via LAN. The allowable disk formats are MS-DOS and HP LIF. You can

also use internal memory for temporary data storage. You can save up to four files in internal memory. You can quickly move information between the internal memory and the 4155 working memory.

Here is shown a cartoon of the main building blocks for the FET characterization tests:

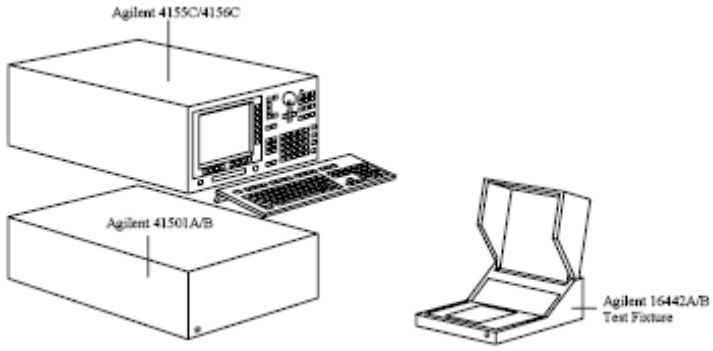

Figure 2.1 Complete FET characterization set: on the left, 4155 and pulse unit generator; on the right the Text Fixture

The access to the device electrodes is given by a microprobe station provided with sharp gold tips.

2.2 Capacitance vs. Frequency/ Capacitance vs. Voltage measurements

Information on the variation of the dielectric permittivity of the gate insulating layer with varying frequency can be obtained by performing Capacitance vs. Frequency measurements on Metal-Insulator-Metal capacitors. Once the capacitance variation is measured the deposited dielectric thickness of the polymeric dielectric can be estimated. In fact, being C_i the capacitance per area unit of a parallel plates capacitor, d the dielectric layer thickness, ε_0 and ε_r respectively the vacuum dielectric permittivity and the insulator dielectric permittivity, the following relationship is valid:

$$C_i = \frac{\varepsilon_r \varepsilon_o}{d} \tag{2.1}$$

And consequently we can calculate d as

$$d = \frac{\varepsilon_r \varepsilon_o}{C_i}$$

The thickness *d* depends on the deposition parameters (spin-speed, spin-time, acceleration-time and deceleration-time of the spincoater), on the solution viscosity and consequently on the kind of solvent in which the polymer is dissolved. Evidently we estimate *d* by C-f when we use a solution-processable dielectric rather than a PET thin film (Mylar®) or Bioplastic films (Mater-Bi®) which are provided with their nominal thickness reported onto the datasheet.

From C-f measurements it is possible to extract value of C_{ins} which is fundamental for the FET parameter extraction and also on the performance of the gate insulating layer.

However, C-f measurements alone are not sufficient to declare that the dielectric is capable of being employed for the realization of transistors. In fact, another prerequisite condition that the gate dielectric must have is that it must be able to allow a measurable charge carrier accumulation at the interface with the semiconductor layer because this attracted charge will be responsible for the current into the channel area. For the purpose of investigating also this aspect of the problem, quasi-static capacitance C (with varying the voltage bias) measurements on metal-insulator-semiconductor (MIS) structures have been done.

In the MIS structure, the capacitance is modeled as a serial connection of the dielectric capacitance and the capacitance of the semiconducting layer. The measured capacitance approaches the capacitance of the pure dielectric whenever charges are attracted to the interface between the semiconductor and the dielectric. In this case we can observe hole accumulation, as evident from the increase of capacitance at negative voltages that attracting holes to the interface with the insulator increase the semiconductor capacitance that being much higher becomes negligible compared to the capacitance of the dielectric. As a result, the total capacitance formed by the capacitance of the dielectric and the capacitance of the semiconducting layer approaches the value of the dielectric capacitance for negative values of the voltage applied. In fact, considering a series of two capacitors, the value of the series of the capacitors approaches that one of the smallest capacitance, that in case of negative voltages applied is the capacitance of the dielectric. Further details on what kind of information we can get from the C-V measurements are discussed in chapter 5.

To perform both the C-V and the C-f measurements we employ the Agilent 4284A LCR-meter which measures a complex impedance (or admittance) of the device under test (DUT) according to an equivalent model selectable by the user when setting the measurement.

A common capacitance (C) can be thus modeled as a capacitor with a resistance in parallel (R_p) in order to model leakage effects through the dielectric plus a resistance in series (R_s) that accounts for the ohmic voltage drop due to the contacts. This model is shown in the following figure:

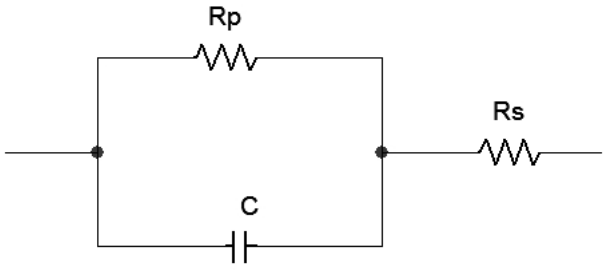

Figure 2.2 Equivalent capacitor circuit employed by the 4284A

When low capacitance values are to be measured (meaning high reactance values) at a certain frequency the major contribute comes from R_p and the most accurate instrumental model is the one called "C_p - R_p" that considers a capacitance and a resistance in parallel.
On the other hand, when we deal with high capacitance values the "C_s - R_s", referring to a capacitor in series with a resistance R_s.
The empirical criterion to be adopted is then

- if $\frac{1}{\omega C} \geq 10k\Omega$, then select C_p- R_p configuration
- if $\frac{1}{\omega C} \leq 10\Omega$, then select $C_s - R_s$ configuration

As it can be easily seen, the model selection depends on both the frequency and the expected capacitance value. Considering that it does not make sense to measure organic materials at high frequencies values (due to low mobility of charge carriers), let us say under 100KHz, and since capacitance values are in the range of nanoFarad, the model selected over this thesis work was always the C_p- R_p configuration..

2.3 Photocurrent Spectroscopy measurements

In order to better understand what kind of information is possible to obtain through photocurrent (PC) spectroscopy measurements some notes on the interaction between light and semiconductor are needed.

In fact, considering the conductivity due to only one type of charge carrier in dark conditions can be written as:

$$\sigma_0 = q\, n_0\, \mu_0 \tag{2.2}$$

Under light exposure an increasing $\Delta\sigma$ in conductivity is expected

$$\sigma_0 + \Delta\sigma = \left(n_0 + \Delta n\right) q \left(\mu_0 + \Delta\mu\right) \tag{2.3}$$

The relationship (2.3) indicates that an increase in conductivity can be generated by both a transport properties increasing (Δμ) and a charge carriers increase (Δn). In particular, being $n = G\tau$ the equation that states that Recombination rate must be equal to the Absorbance rate at the equilibrium , we can write

$$\Delta\sigma = q\mu_0 G\tau_n + n_0 q\Delta\mu \tag{2.4}$$

where G is the so-called photoexcitation rate ($m^{-3}s^{-1}$) and τ_n the average carrier lifetime.

That being said, a conductivity increase can be due to:

(a) density increase Δn of the charge carriers whose average lifetime can depend on the illumination $\tau_n = \tau_n(G)$.

(b) mobility increase Δμ that can be correlated with either scattering attributed to ionized defects whose concentration may vary or lowering of the barrier height among grains. Last but not least, this can be due to charge carriers promotion to a higher mobility band.

To generate a photocurrent, light must be absorbed: that is why we have a strong correlation between absorption spectrum with varying the incident wave length (α vs $\hbar\omega$) and the consequent photocurrent variation ($\Delta\sigma$ vs $\hbar\omega$).

2.3.1 Photocurrent in Polycrystalline materials

Grain boundaries can be usually assimilated to potential barriers that strongly limitate the current flowing from one grain to another.
Light can affect charge carriers transport in three different ways [R.H. Bube, Photoelectronic Properties of Semiconductors, page 36.]:

1. Increasing the global charge concentration over the whole material and consequently enhancing the transit over the barrier according to the thermoionic theory.
2. Lowering the barrier height by changing the charge concentration into the intragrain localized energetic states .
3. Increasing the tunneling probability through the barrier by lowering the depleted region close to the grain borders.

Anyway Bube's theory fits perfectly with the inorganic semiconductors (by the way, at that time it was fully referred to Silicon and GaAs), but still a perfect matching of the same theory with the organic materials has to be found.
Nevertheless, PC Spectroscopy have been used since a few years when dealing with organic materials and its application to this new world can be considered anyway successful.
In order to promote an electron from HOMO to LUMO, the system should acquire energy equal to the difference between the two levels, namely the energy gap E_G. Therefore, when the energy of the incident radiation is comparable to E_G the absorption signal as a function of the wavelength will rapidly increase (see peak E_1 in Figure 2.3). The other peaks detectable in the spectra can be due to the presence of deep or shallow traps, when the energy of the incident radiation is lower than E_G, or to transition between higher energy levels when it is higher than E_G. In fact, in an organic molecule several anti-bonding orbitals are present (LUMO representing the lowest one) and the higher energetic peaks can be explained with higher energetic transitions.

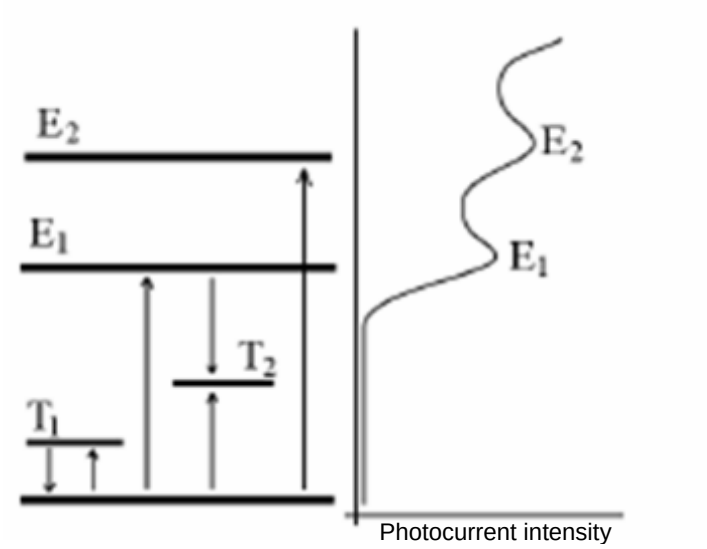

Figure 2.3 Simple sketch of photocurrent spectra generation by an energetic diagram

2.3.2 Experimental set-up

The experimental set-up employed for the PC spectroscopy measurements is completely designed and built up by "semiconduttori e semisolanti di fisica della materia" group from the Physics Department, University of Bologna, Bologna. A block diagram is shown in Fig. 2.4. The main constituent parts are:

a. The optical part which is composed of:

- A white light source: 300 W Xenon lamp by Oriel Instruments.
- A chopper, that have been used to make light flashing the illumination on the sample at a certain frequency.
- One monochromator (blazing diffraction) to select a specific wave lenght from coming from the white light source.
- A coaxial mirror, for collecting light coming out from the white light source and focusing it onto the sample.

b. The electrical part which is composed of:

- Electrometer current amplifier that supplies a small bias voltage (max 5V) for extracting the charge carriers generated by photoexcitation and for amplifying the ouput current and then send the signal to the Lock-in.

- The Lock-in, splits the input signal (through Fourier transform) and extracts the frequency component corresponding to the frequency that is instantaneously sent by the chopper supply. Data are then sent to the PC through an IEEE 488 interface.
- A PC that records the Lock-In signal and (through a control board) rotates the monochromator grid with a user-defined speed.

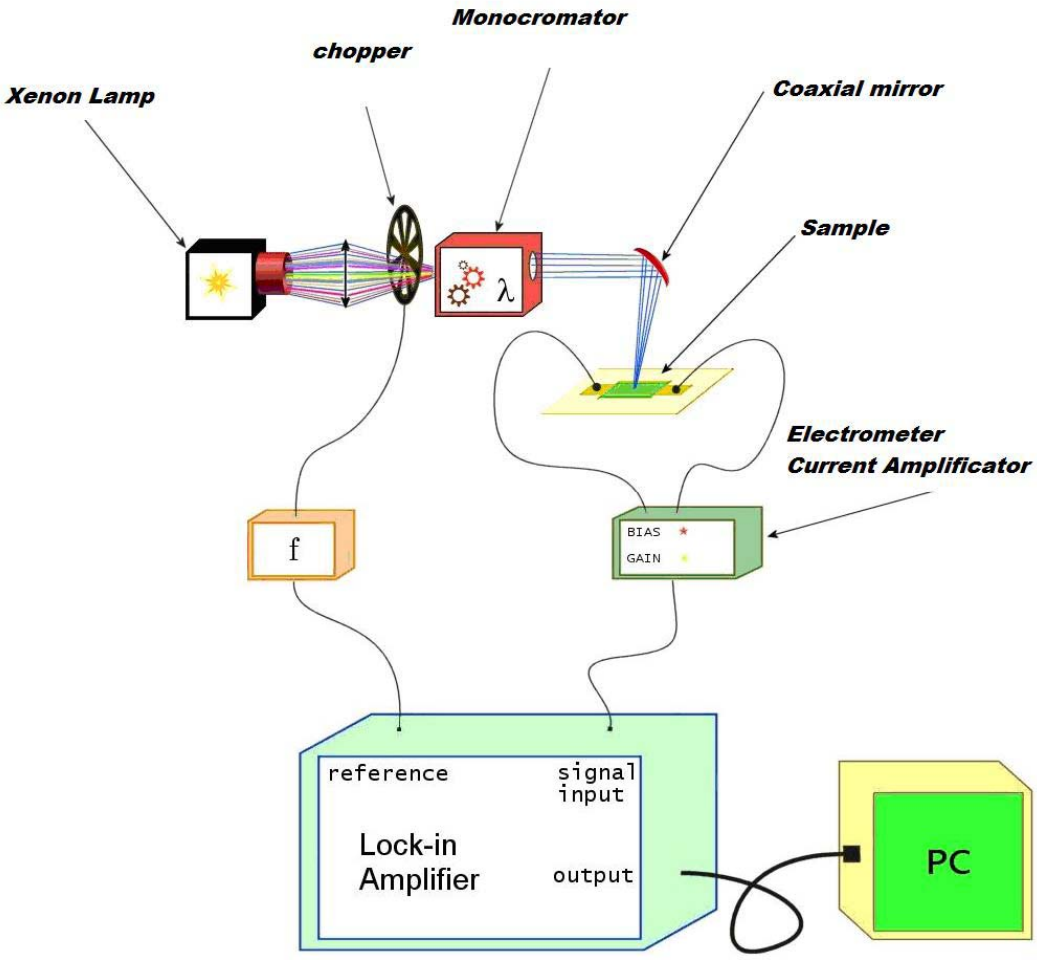

Figure 2.4 Experimental set-up for the PC spectroscopy measurements (block diagram)

2.4 Electro Chemical Impedance Spectroscopy (EIS) measurements

Electrochemical impedance spectroscopy (EIS) is a powerful method of probing the features of surface-modified electrodes and has been here employed to gain information on the behavior of the gold modified surfaces.

The complex impedance can be presented as the sum of the real, Z', and imaginary, Z'', components that originate mainly from the resistance and capacitance of the cell, respectively. In order to obtain more information from EIS results, the working electrode behavior can be simulated using an equivalent circuit, which consists of an electrolyte solution resistance R_s in series with a parallel double layer capacitance C_{dl} and a Faradaic resistance R_f. It is assumed that the Faradaic resistance R_f consists of two parts, which are the charge-transfer resistance R_{ct} and the Warburg impedance W resulting from the diffusion of ions.

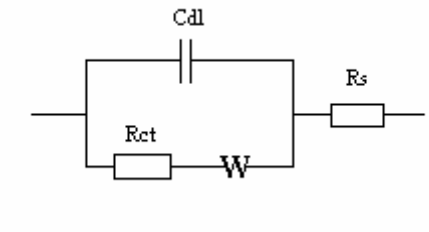

Figure 2.5 Randle's equivalent circuit used to simulate the experimental data

Representing bulk properties of the electrolyte solution and diffusion features of the redox probe in solution, R_s and W are not affected by chemical transformations occurring at the electrode surface. On the other hand, depending on the dielectric and insulating features at the electrode/electrolyte interface, the parallel combination of R_{ct} and C_{dl} gave rise to a semicircle in the Nyquist plots. The charge-transfer resistance R_{ct} can be obtained by measuring the diameter of the semicircle in the impedance spectrum via simulation.

The interfacial charge of the modified electrode changes by changing the pH value of the solution, due to the presence of amino group. We expect to observe a decrease in R_{ct} value as the we move towards more acid solutions (because we are using a negative redox probe).

Chapter3

Deviation from Ideality

Despite their promising features, organic materials and consequently OFETs still suffer from either the environmental conditions that strongly affect the devices' performances and other non-idealities such as the poor charge injection from the electrodes, the not always well-saturated output curves and the bias stress due to either chemical and physical reasons depending on the intrinsic nature of the organic materials.

To optimize the device characteristics of OTFTs it is very important to understand the transport mechanism and how they depend on the operating environment. In fact, many problems related to the understanding of the transport phenomena and the aging effects of the organic semiconductor [1] [2] are still open. Exposure to air is, in general, detrimental to the performance of the OTFTs [3] and the solution of this problem is still a major open issue for such devices to be marketable.

3.1 Aging and Bias stress

Over this work we carried out different kind of measurements in order to have a deeper insight on both bias stress and aging effects on the performance of TFTs. In particular, we studied the charge transport of pentacene-based thin film transistors that have been stressed either by repetitively biasing the device between V= +100 V and V= –100 V or by testing their electrical parameters at room temperature and in atmosphere over a long period of time (up to 80 days). To do that, we carried out photocurrent measurements whose experimental set-up will be better described in the following chapters. The mechanism of photocarrier generation is still an open question and no theoretical model has been appropriately developed to account for the whole process occurring in polycrystalline thin films [4] [5].

Most studies suggest that primary step of photocurrent generation in organic thin film devices is the creation of excitons even if recent reports indicate that free carriers can also be directly photoexcited [6] [7] [8] [9]. The charge transport process is then controlled by the diffusion of excitons and by their trapping and dissociation at the grain boundaries and metal/organic interface. Since an organic active layer exposed to atmosphere or to bias stress can modify its structure and affect the electronic transport process, the focus of this work is to investigate to what extent such alterations influence the charge carrier trapping and transport mechanisms.

Two-terminal devices have been obtained by patterning on a thin film of polyethilene terephtalate (Mylar, Du Pont) gold contacts separated by a channel 30 μm long and 5 mm wide. Then a pentacene layer (average thickness 50 nm) was thermally evaporated through a shadow mask in order to cover the channel and, partially, the gold contacts. The gate layer was then formed on the opposite side of the Mylar film by thermal evaporation of either gold or aluminum. In this way, identical bottom contact organic thin film transistor structures were formed. Aside each OFET structure, an identical two-terminal structure without any gate was fabricated (source and drain gold contacts covered by the pentacene layer with the same geometry of channel and contact coverage), in order to compare performances of three-terminal devices with those of two-terminal devices. The current-voltage characteristics of the fabricated devices were measured with a semiconductor parameter analyzer. The photocurrent spectroscopy analyses were carried out in air at room temperature by biasing the drain of the sample (with the source at ground) with a low bias

(>7 V, leaving the gate unbiased) and by measuring the current through a load resistance of 200 kΩ. As a light source we used a 150 W Xe arc lamp and a quartz-tungsten-halogen lamp coupled to a Jarrel monochromator and mechanichally chopped at low frequency (<20 Hz). The photocurrent was then measured as a function of wavelength (varied in the range λ=400–750 nm) using a current amplifier connected to a digital lock-in amplifier (Stanford Research 850). The photon flux was measured with a calibrated Si photodiode to normalize the photocurrent (PC) spectra. Figure 3.1 reports the photocurrent spectra obtained for pentacene TFTs that only differ in the presence or in the type of metal gate contact evaporated on the back of the polyethylene terephtalate thin film that acts both as the dielectric and the device support layer. Several peaks can be identified and the main ones are located at 1.86, 1.98, and 2.13 eV.

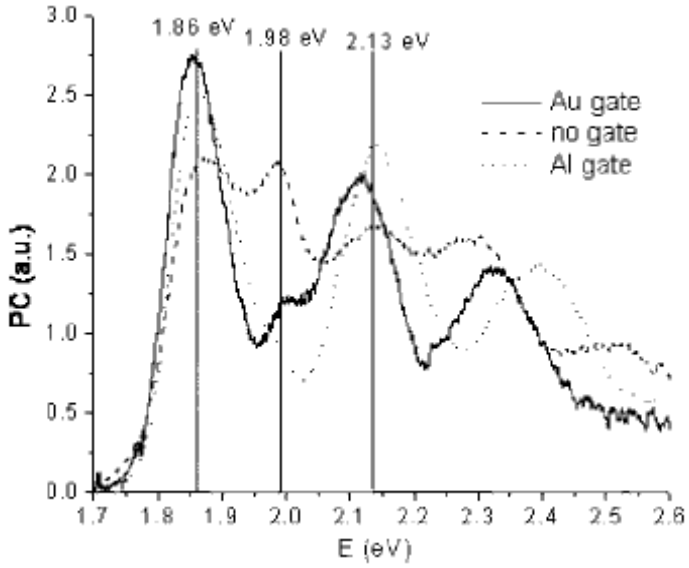

Figure 3.1 PC spectra taken under identical experimental conditions of different TFTs with Al, Au, and no gate, fabricated with pentacene deposited at the same time on the same Mylar substrate.

Absorption spectra reported in the literature on pentacene indicate the presence of intense peaks located at similar energy values, even if there is no general consensus on the nature, energy location, and physical origin of these transitions. The peaks around 1.85 and 2.1 eV have been recently attributed to Frenkel excitons, but still there is no reliable information on the exact energy gap of pentacene. One noteworthy observation is that spectra obtained from devices that have been prepared by evaporating pentacene at the same time on the same substrate, and that only differ in the presence of the metal gate or in the metal used to fabricate it (Au or Al), are significantly different. In particular, the devices with Al or Au

gate show similar spectra while the spectrum of the device without gate is characterized by a markedly lower 1.86 eV peak.

Two possible explanations could account for this observation:

(1) The presence of a metal contact at the back of the thin film structure may affect the reflection and the following interference effects of the impinging light beam. Light generation in the bulk pentacene layer exposed to multiple reflections could, in fact, be stronger in the gated devices and selective interference could take place and enhance the response at certain wavelengths [6][9]. To test for such effects we have carried out the measurements at different tilting angles, varying from −45° to +45° (with respect to the normal direction of indence), but we could not observe significant variations.

(2) The presence of a metal gate can also affect the charge distribution of a metal-dielectric-semiconductor structure by altering the concentration of charge carriers at the dielectric-semiconductor interface. In fact, even if the metal contact is floating (i.e., not intentionally connected to an external voltage source) its equipotential surface may be assumed to have a nonzero value. This could induce the presence of a higher density of charge carriers at the dielectric-semiconductor interface that, following the absorption of the incident light, result in the formation of a larger number of excitons [4]. By applying a positive gate bias (V_{GS}= +20 V) the peak intensity decreases, thus confirming that the channel carrier density has a role in determining the photocurrent intensity (data not shown). Therefore, this explanation seems at the moment to be the most plausible one. The effect of bias stress on these devices has been studied by repetitively measuring the current-voltage curves I_{DS}-V_{DS} with V_{DS} varying between +100 and −100 V. The I_{DS}-V_{DS} measurements have been carried out in air but in the dark, at room temperature over a whole day. Figure 3.2 shows how no variations are induced in the PC spectra of both gated and ungated devices after prolonged bias stress, while the I_{DS}-V_{DS} characteristics indicate a strong decrease in the current values.

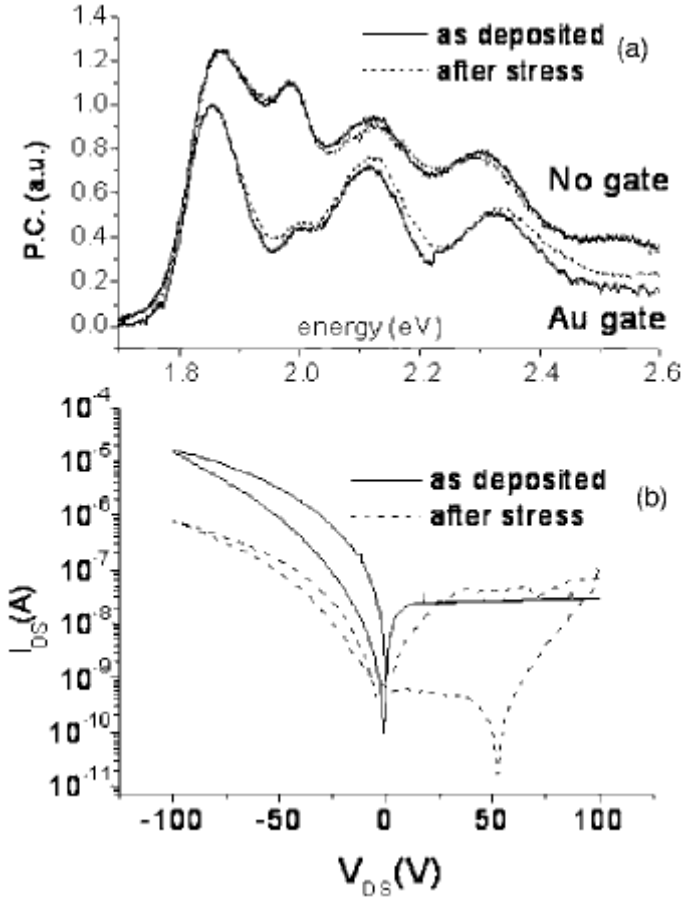

Figure 3.2 Effects of repetitive I_{DS}-V_{DS} scans: (a) PC spectra and (b) *I-V* curves.

These results suggest that the observed degradation of the macroscopic transport properties cannot be ascribed to alterations of the structure and of the electrical properties of the excited states, rather it could be associated with polarization effects that locally redistribute the density of trapped charge.

We have also studied the effects of aging, i.e., of a combination of prolonged bias stress and exposure to air and room light and temperature, on similar devices. We tested the devices up to 80 days after fabrication. The results of PC analyses are reported in Fig. 3.3 and indicate a marked evolution of the relative intensities of the peaks with elapsed time. The presence of a peak at about 1.91 eV is highlighted by the redistribution of the amplitudes of the other peaks. The most evident variation is observed for the lowest lying excited state, the one at 1.85 eV that gradually decreases in intensity leaving the dominant role to the transition at 1.98 eV.

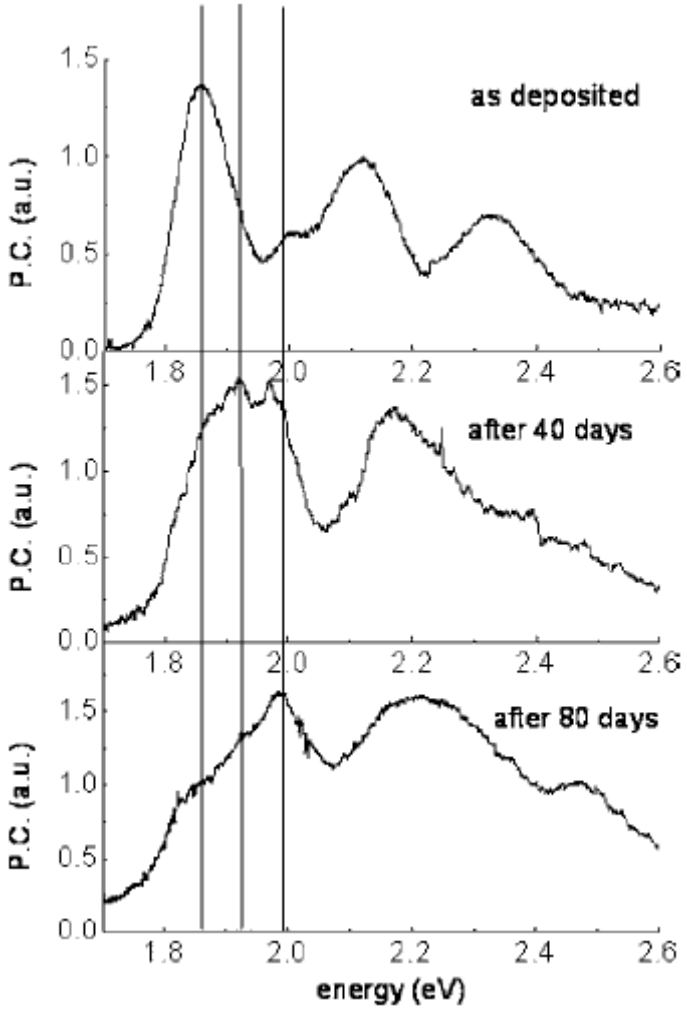

Figure 3.3 Evolution with time of PC spectra of the same pentacene TFT with a Au gate taken under identical experimental conditions after exposure to light and air while tested with I_{DS}-V_{DS} measurements

These observations indicate that the exposure to air and light has a significant effect on the excited state structure and energy distribution, on the contrary to what we have observed in the case of pure bias stress (Fig. 3.2). The effect of aging on the I_{DS}-V_{DS} characteristics is reported in Fig. 3.4 for the same Au gated devices whose PC spectra are shown in Fig. 3.3. After 40 days the current intensity has decreased while the hysteresis observed between the 0 to−100 V curve and the −100 to 0 V curve has increased. These effects could be understood in terms of an increased charge carrier trapping efficiency possibly caused by the formation of trapping sites. The hysteresis, in particular, could be associated with a quite long charge carrier emission time constant peculiar to the trapping sites. Again, as highlighted by PC analyses, I_{DS}-V_{DS} characteristics show how the effects of aging are quite different from those observed after long bias stress.

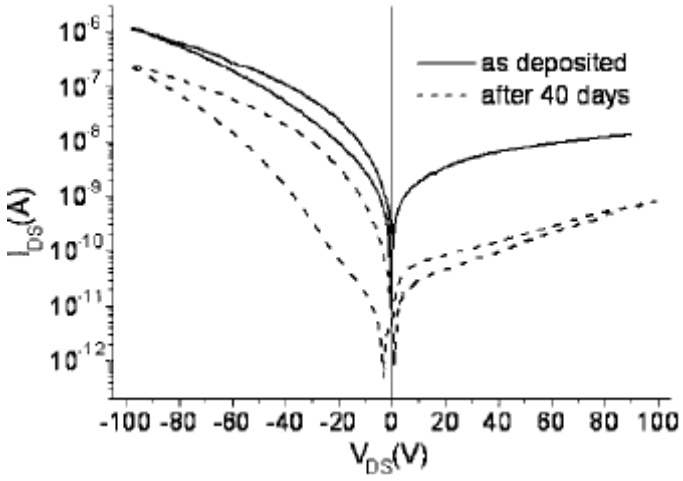

Figure 3.4 I_{DS}-V_{DS} measurements on the same pentacene TFT with a Au gate whose PC spectra are reported in Fig. 1.9. The reported measurements have been carried out immediately after fabrication of the devices and after 40 days of exposure to atmosphere.

A variation in the relative strength of the various bands located around the energy gap has been observed with optical spectroscopy on pentacene thin films as a function of temperature and it has been attributed to molecular reorientations that cause changes in mutual molecular overlap within the unit cell [7]. It has been recently suggested that the influence of air on the charge carrier transport properties of pentacene consists of at least two separate contributions [10] [11] [12]. The first one is due to the adsorbtion and diffusion of oxygen, enhanced by the presence of light, that is reported to produce a reversible effect of the material transport properties. The other is related to the presence of water that may easily diffuse through the gaps between the pentacene grains and be incorporated into the film changing its morphology. This could induce the formation of trapping sites for the injected charges and, due to the polar nature of H_2O, a greater interaction with the charge carriers, resulting in an increase of the energetic disorder through charge-dipole interactions. The morphology of pentacene films has been reported to vary after exposure to atmosphere and the changes have been correlated to adsorbtion on the film of the hydroxyl radical, caused by the presence of H2O, that induces a structural alteration of the pentacene film [12]. Variations observed in the saturation current of a pentacene TFT have been reported as a function of the ambient humidity and have been attributed to induced changes in the hole mobility [12].

Our results suggest that the prolonged exposure to atmosphere during operation of pentacene TFT induces significant alteration in the structure and in the electrical properties of the excited states that permanently alter the macroscopic electronic transport

characteristics of the TFT, differently from what we have observed for TFT only exposed to bias stress during operation. The I_{DS}-V_{DS} characteristics show both a decrease in the current values and an increase in the hysteresis effect, suggesting a larger contribution from charge trapping sites, possibly characterized by a long emission time constant. We believe O and H adsorbed from the atmosphere play a major role in the observed alteration of the semiconductor structure and in the formation of permanent trapping sites.

The correlation of our PC spectra with the I_{DS}-V_{DS} characteristics supports the attribution of the peaks at 1.85 and 2.13 eV to excitons since they decrease with aging, a process that enhances the formation of charge carrier trapping sites. The increase in number and strength of carrier traps indeed could hinder the formation and affect the transport of excitons in the pentacene film. The peak at 1.98 eV, on the other hand, seems to be a good candidate for the energy gap of pentacene since it is not markedly affected by aging and since it has an energy larger than the lowest lying excitation (here the 1.85 eV excitonic transition) [13].

In conclusion, we have analyzed by current-voltage analyses and by photocurrent spectroscopy the effects on pentacene thin films of a prolonged bias stress and of exposure to atmosphere. We have identified the major excitonic and energy gap transition energies. We have observed a quite different electrical behavior and structure and energy distribution of the excited states. By repetitively biasing the device, even for long periods of time, only a local redistribution of charges takes place, possibly due to reversible polarization and short term trapping effects. On the contrary, exposure to atmosphere induces significant alterations on the structure and energy distribution of the excited states, associated with the formation of permanent trapping sites. a function of the ambient humidity and have been attributed to induced changes in the hole mobility [12]. Our results suggest that the prolonged exposure to atmosphere during operation of pentacene TFT induces significant alteration in the structure and in the electrical properties of the excited states that permanently alter the macroscopic electronic transport characteristics of the TFT, differently from what we have observed for TFT only exposed to bias stress during operation. The I_{DS}-V_{DS} characteristics show both a decrease in the current values and an increase in the hysteresis effect, suggesting a larger contribution from charge trapping sites, possibly characterized by a long emission time constant. We believe O and H adsorbed from the atmosphere play a major role in the observed alteration of the semiconductor structure and in the formation of permanent trapping sites.

3.2 Short channel effects

As the transistor channel length is reduced, the characteristics of the devices deviate from equations the classic OTFTs equations presented in Chapter 1 either in the linear and in the saturation regime and exhibit several non-idealities [14]. To account for these short channel effects, like space charge limited currents or the dependence of the mobility on the longitudinal electric field (source-drain), more sophisticated models have been proposed. For instance, it has been recently pointed out by Koehler and Biaggio [15] that, for high applied voltages and short channel lengths, the current conduction can be significantly influenced by space charge limited current (SCLC) phenomena, i.e. the carriers injected from the contacts can constitute a space charge region which affects the behavior of the device. SCLC conduction can explain the non-saturation of the output curves for high drain voltages in OTFTs with short channel lengths. Experimental evidence of SCLC effects has been reported by Chabinyc et al. in [16]. The dependency of the mobility on the longitudinal electric field (source-drain) E_x can be described by the Poole-Frenkel [17] model:

$$\mu(E_x) = \mu_0 \exp\left[\gamma\sqrt{E}_x\right] \tag{1.8}$$

where μ_0 is the zero-field mobility and γ is a prefactor which depends on the material and is generally inverse in proportion to the temperature T , at least for T > 50K [18]. Stallinga et al. [19][20] show that Poole-Frenkel mobility can be responsible of the non-linearities often observed in the output curves for low drain voltages. Hamadani et al. [18] [21] report field dependent mobilities in OTFTs which are consistent with the Poole-Frenkel model for different temperatures. Poole-Frenkel mobility, together with SCLC conduction, can deeply affect the characteristics of short channel OTFTs.

Locci et al. [22] developed a model for the linear, depletion and saturation regimes which accounts for both, determining the characteristic equations for the device at different applied biases.

First we will give a description of the hypotheses on the devices and their geometry. Then the main results of the model will be used to fit some measurements we carried out.

Locci's model considers a device as reported in fig. 3.5. It is a bottom contact OTFT, with insulator thickness, dielectric permittivity and capacitance per unit area equal to d_i, ε_i and C_i, respectively, and with semiconductor thickness, dielectric permittivity and capacitance per unit area equal to d_s, ε_s and C_s, respectively. The contacts are assumed to be ohmic. The channel length is equal to L, whereas its width is Z.

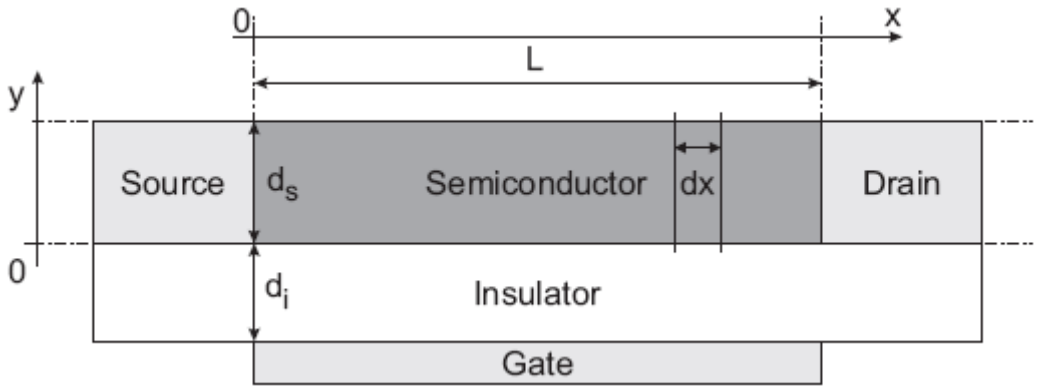

Figure 3.5 Geometry of a bottom contact OTFT considered in the Locci's model

To perform a comparison between the developed model and real data, bottom gate short channel OTFTs with P3HT semiconductor have been realized, with channel length L = 5 μm and L = 2.5 μm. They have been produced by spincasting the pristine polymer solution onto a 230 nm SiO_2 dielectric, thermally grown on a N^+Si wafer, used as gate electrode. Sputtered gold Source and Drain electrodes were used to contact the polymer. Before coating the active layer the SiO_2 surface was treated with a hexamethyldisilazane (HMDS) primer, to improve the film adhesion and formation.

An interdigitated layout, obtained by means of conventional photolithography, was used for the OFET where Z = 10mm is the FET channel width. The dielectric capacitance per unit area is $C_{ins} = 1.5 \cdot 10^{-4}$ F/m^2. The dielectric constant used in the case of the P3HT is $\varepsilon_s = 2$ as determined by quasi static C-V measurements. The nominal value of the semiconductor thickness is 100 nm.

Two sets of measurements were performed: transfer curves are reported in fig. 3.6 and output curves are shown in fig. 3.7 and 3.8.

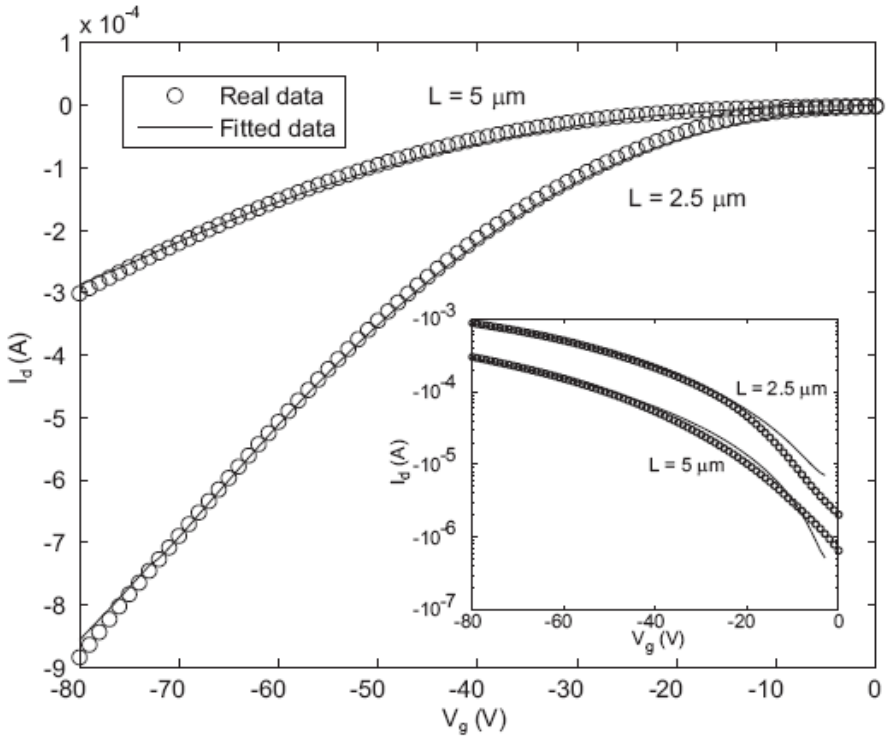

Figure 3.6 Transfer $I_d - V_g$ characteristics for L = 5 μm and L = 2.5 μm devices. $V_d = -75V$

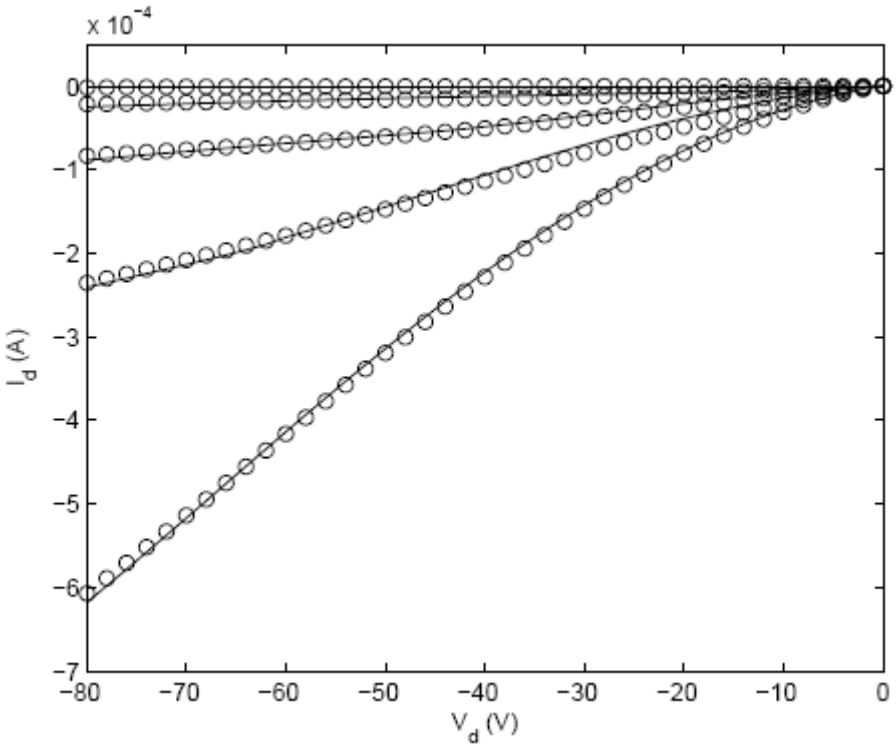

Figure 3.7 Output $I_d - V_d$ characteristics for L = 2.5 μm devices. V_g = 0V, -20V, -40V, -60V, -80V

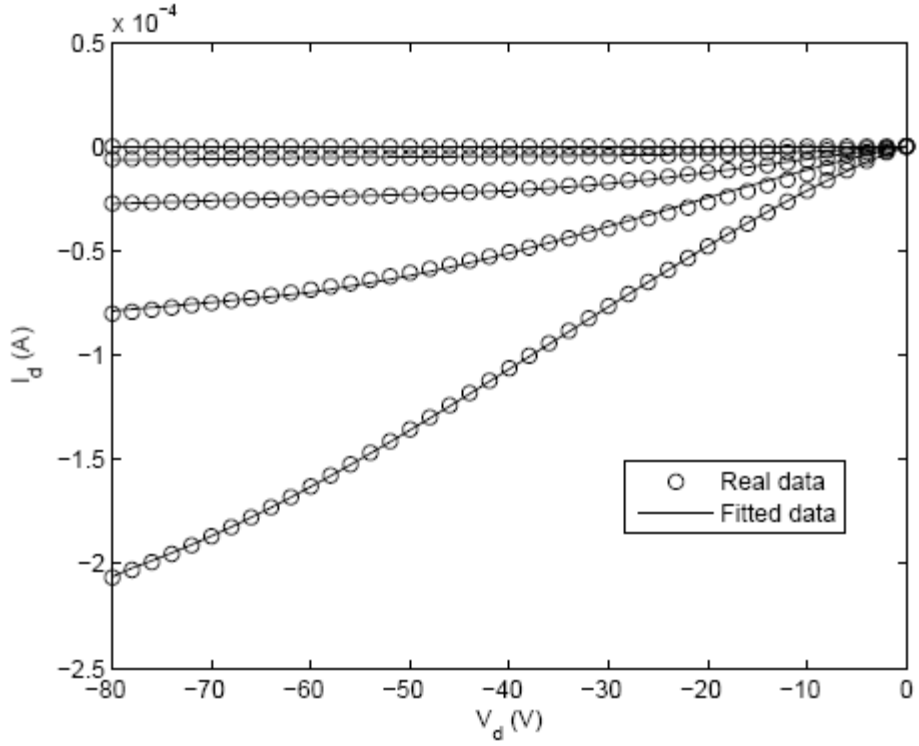

Figure 3.8 Output $I_d - V_d$ characteristics for L = 5 μm devices. V_g = 0V, -20V, -40V, -60V, -80V

To extract the electrical parameters of the devices two contact resistances R_s, at both the source and drain contacts, were added to the model, substituting V_d with $(V_d - 2R_sI_d)$ and V_g with $(V_g - R_sI_d)$ into the equations used. To reduce the number of fitting parameters, a very low density of free carriers was supposed, so that one can assume V_0 practically 0V. Fitting of the transfer curves, which is reported in fig. 3.6, allows the determination of the threshold voltage V_{th}, and the series resistance R_s (besides other model parameters that we do not cite here). Fitting values are reported in table II.

	V_{th}(V)	R_s(kΩ)
Starting point	0	10
L=2.5μm	2.2	5.8
L=5μm	2.5	2.5

Table II: Fitting Parameters

It can be observed that its magnitude is slightly different from that extracted from the transfer curves, and this is consistent with the higher currents in the transfer curves measured for the same applied voltages. Also, μ_0 increases with the gate voltage. The least

squares fitting, which involves a non-linear minimization with respect to (V_{th}, μ_0,E_0,R_s), is obtained by means of the Nedler-Mead simplex direct search algorithm and is initialized with the starting point reported in table II.

Over this thesis work, a model proposed by Locci et al. which describes the electrical characteristics of OTFTs with short channel lengths has been applied. Effects like super-linear output curves for low drain voltage, as well as non-saturating currents can be adequately described. The model is based on the assumption that the field dependent mobility of the organic semiconductor follows the Poole-Frenkel theory; moreover, space charge limited currents beyond the pinch-off point are considered. The length of the channel plays a key role in the determination of the electrical characteristics, since the high longitudinal electric field in short channel devices increases the carriers mobility and SCLC effects. Experimental results for devices with 5 μm and 2.5 μm channel lengths have been analyzed and good agreement with the proposed model is found.

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Chapter4

OTFTs with Cylindrical and Double-gate Geometry

As shown in chapter 1 one of the main advantages of organic electronics over its competitor silicon is that many semiconductors can be chemically tailored so that new applications can be more and more discovered and explored. Among the benefits introduced by the chemistry in electronics is the synthesis of solution-processable organic semiconductors on several substrates through low-cost techniques.

Taking advantage of these novel properties, it is possible to design and easily realize devices with a non planar or more complicated geometries.

In this chapter, we will describe how a semiconductor deposition has been made over cylindrical surfaces leading to cylindrical devices that can be exploited in the smart wearable/sensing field to form a transistor whose geometry and mechanical properties are compatible with a textile process.

In addition, multi-layered structures made of polymers can be obtained giving rise to complex structures realized with very simple techniques. An example of these structures is given by a polymeric double-gate structure that is used to achieve a better charge modulation in the semiconductor layer.

In the following both these structures will be described and analyzed.

4.1 Cylindrical geometry

Up to date, only a few steps have been done towards the realization of organic-based e-textile devices.

In 2003 Lee and Subramanian [1] proposed a cylindrical transistor device assembled starting from a 500□m diameter aluminum wire. Then either a thin (150nm-200nm thick) SiO_2 dielectric layer or a cross-linked PVP were deposited by respectively low-temperature chemical vapor deposition (LTO) and dip-casting and successively covered by a thermally evaporated pentacene layer. They managed to carry out output characteristics on SiO_2/Aluminum-based yarn transistors, but chemical vapor deposition is definitely not suitable to textile processes and in addition, the poor quality of the performances was not promising for any future development. However, the achieved performances with PVP/pentacene yarn transistors were fairly good: measured charge carriers mobility sometimes exceeded 0.5cm^2/V*s. However the thick yarn diameter (more than 500μm) is not completely suitable for textile processes even though it was intended for arrays of e-textile embedded sensors.

In 2006 we presented [2] an example of organic field-effect transistor (OFET) characterized by textile process fully compatible size and geometry. The device has been

obtained starting from a cylindrical metal fiber with a diameter of 45 μm, covered by a uniform layer of polyimide of about 1 μm (Elektrisola). As a result, this yarn is very flexible and can be employed, alone or twisted to a cotton fiber, in textile processes.

We have obtained a cylindrical top-contact OFET (general structure shown in Fig. 4.1) by evaporating pentacene (Sigma Aldrich) on the structure.

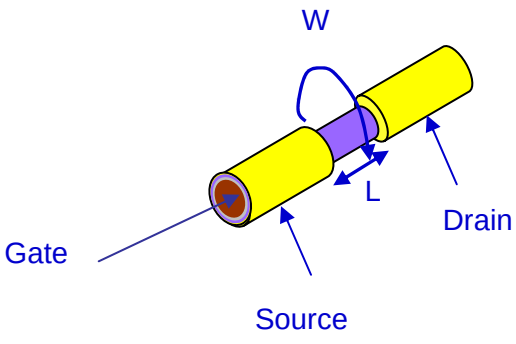

Figure 4.1 Structure of the cylindrical OFET

This was done without rotating the wire with respect to the crucible; therefore a non-uniform coverage of the wire has been obtained (basically, about half of the lateral surface is covered; the nominal thickness on a flat surface aside the wire is 50 nm). A uniform coating of the yarn with the semiconductor could be achieved by rotating the wire during the semiconductor evaporation. After this step, source and drain contacts have been realized in two different ways: either by evaporating gold electrodes directly on pentacene by interposing a thin crossing wire as a shadow mask during the evaporation procedure (Fig. 4.2, an optical microscope image of the channel; in this way, a channel length with almost the same size as the wire diameter is obtained, but a good control on dimensions is not possible) or by employing a soft lithographic process for transferring a thin layer of the conductive polymer poly(ethylene-dioxythiophene)/polyStyrene sulfonate (PEDT:PSS) on the pentacene surface.

Figure 4.2 Optical microscope image of the channel area

This method has several advantages: it allows to exploit the favorable mechanical properties of conductive polymers as contacts; it allows to have an optimal control of geometries because the relieves of the stamp used for soft lithography are obtained with a high resolution technique as already demonstrated for planar devices [3]; it allows (by rotating the yarn on the stamp surface) to deposit contacts on the whole surface of the yarn (while with evaporation only the side exposed toward the crucible is uniformly covered); it allows to easily make a whole set of contacts along the wire length at the same time.

In devices with gold contacts, the gold tips have been simply pressed against the source and drain of the transistor wire. In devices with PEDOT:PSS contacts (Fig. 4.3), the measurements have been made by sandwiching the wire between a cover slide where two gold electrodes had been previously deposited and a poly(dimethyl-siloxane) stamp reproducing source and drain covered with a thin layer of PEDOT:PSS (Baytron P CPP 105D).

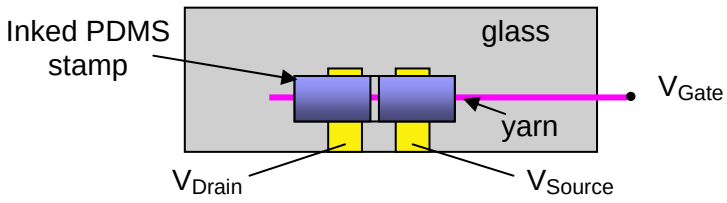

Figure 4.3 Measurement set-up for the device with PEDT:PSS contacts: source and drain are created by lamination using an "inked" PDMS stamp put in contact with gold pattern deposited on a glass substrate

In Fig. 4.4 the I_D-V_D curves of a device with gold (Fig 4.4, left) and PEDOT:PSS (Fig. 4.4, right) source and drain contacts are shown.

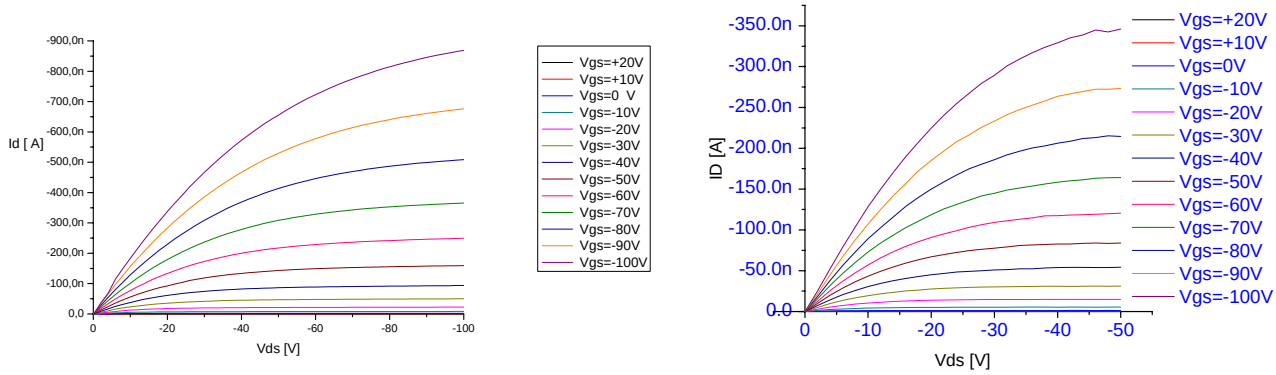

Figure 4.4 Output characteristics carried out on cylindrical OFET devices with (left) Gold and (right) PEDT:PSS source and drain electrodes

It is worth to note that establishing a reliable electrical contact with source and drain was particularly difficult due to the very low dimensions and also to the non-planar surface of the wire. Interestingly enough, despite the above mentioned problems and the very low value of the *W*/*L* ratio (estimated as 1.2), the on current and, above all, the I_{on}/I_{off} ratio are reasonably high (around 10^4), fully comparable with those of planar devices. In order to derive a reliable estimation of the electronic parameters, we fitted the *I*-*V* curves with an

electronic model that takes into account the cylindrical geometry [4]. In addition, we estimated the series resistance effect according to the concept proposed by Horowitz [5] but fitting the whole I-V curves in order to have a reliable value of all free parameters of the model (threshold voltage, mobility, series resistance). We found a difference in devices made with gold contacts with respect to those obtained by soft lithography assembling of PEDOT:PSS contacts. In Table 4.1, the main parameters are shown for a couple of representative devices.

Device	***Ion/Ioff***	***Vt (V)***	***μ (cm^2/V*s)***	***Rs (MΩ)***
Gold contacts device	$7*10^3$	-17.3	0.04	32
PEDT:PSS contacts device	$3*10^3$	-9.6	0.06	14

Table 4.1 Comparison between average main parameters extracted from both gold and PEDT:PSS source and drain electrodes

As it can be observed, the device with gold contacts shows a lower value of mobility, together with a higher value of series resistance. In addition, also the threshold voltage is more negative. Therefore, it seems that, despite the better value of the I_{on}/I_{off} ratio (estimated on curves with the same V_G-V_T value), the trend for the main electronic parameters is more favorable in devices with PEDOT:PSS contacts. Obviously this issue is of great importance, especially in view of future applications in "textile circuits". It is worth noting that the derived mobility values in cylindrical devices are comparable if not better than those recorded for polycrystalline pentacene on planar devices.

In order to better understand the reason for this behavior, an AFM investigation on the channel area of the wire was needed. A larger average size of pentacene grains grown on the polymide dielectric was found with respect to the one usually found (in the same evaporation conditions) on Mylar films that we typically use as insulating films for planar OFETs [6]. This means that considering a model where the mobility is limited by traps localized at grain boundaries, this should coherently result in a higher value of mobility. This is confirmed by the electrical measurements, where a typical value in the range of 10^{-2} cm^2/V*s has been recorded for the cylindrical transistor (while in planar devices the typical value is lower than 10^{-2}) showing that polyimide, as previously reported in literature for planar devices [7], forms a good insulator/organic semiconductor interface.

In conclusion, we have obtained a cylindrical organic thin film transistor that, due to its form factor and the employed materials, is fully compatible with a textile process (weaving and knitting equipment). This transistor has shown very interesting performances, with typical values of the electronic parameters very similar to those of planar devices. This result is very promising in view of innovative applications in the field of smart textiles. In particular, the realization of distributed transistors and sensors in a textile network is the natural, most promising perspective for a variety of applications.

4.2 Double-gate geometry

A double-gate transistor is basically a transistor that follows the traditional transistor layout but in addition it is provided with a further gate that usually tops the whole structure.
The first silicon-based double-gate FET (DG FET) was proposed in the early 1980s [8] and was somehow intended to obviate to the short-channel effects by adding a further electrode that could control the field through the channel and consequently better modulate the transport.
Very recently the double-gate geometry has entered the organic semiconductor world as well. In fact, despite most of the applications for OFETs are switches (which require high values of I_{ON}/I_{OFF} ratio ($>10^6$) and reduced power dissipation in the off-state) the leakage currents through solution-processed polymeric insulators and processing issues often limit the minimum insulator thickness and consequently the dielectric capacitance C_i. High values of V_G, V_D are then required to achieve modest levels of drain current, already limited by the low carrier mobility of conjugated polymers or small molecules. A double-gate FET structure (Fig. 4.5) can help improve the organic transistor performances by enhancing the on-state current and eventually modulating the threshold voltage and the off-current as shown later .

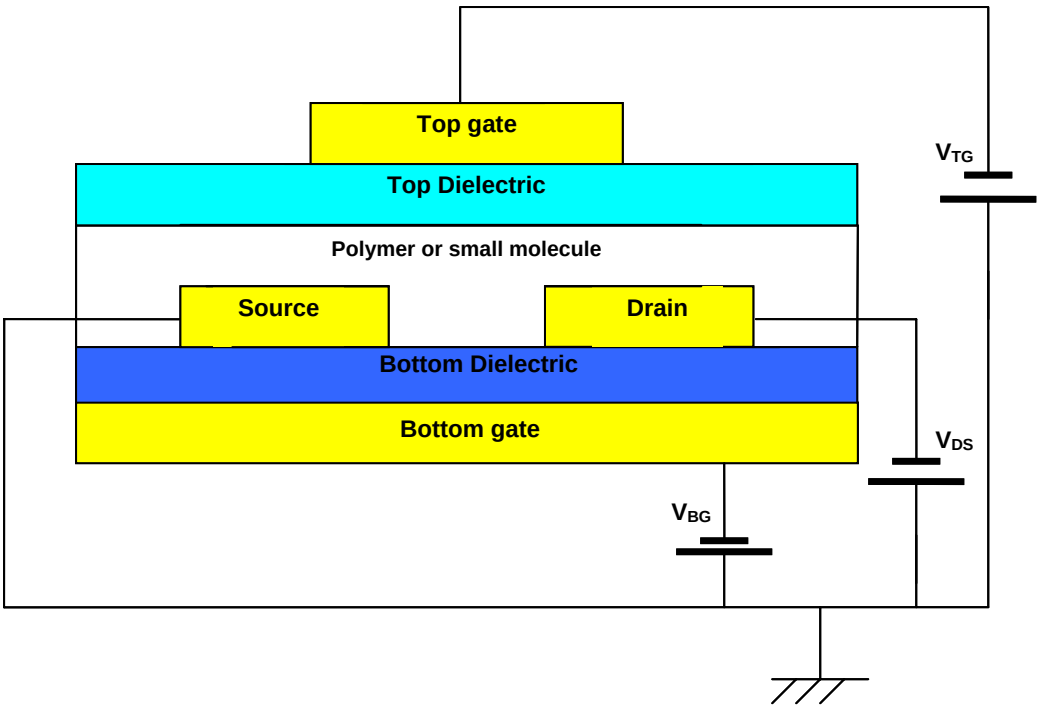

Figure 4.5 Schematic of a double-gate organic field-effect transistor (DG-OFET) structure

The DG-OFET can be seen as a combination of a top-gate (top-contact) stacked on a bottom-gate (bottom-contact) OFET: the two devices share the source and drain electrodes and the semiconductor layer, while the two gates can be designed to be independent or alternatively electrically connected.

The higher capacitance (C_i) gate, controlling the metal-insulator-semiconductor (MIS) structure, which will be responsible for the higher contribute to the drain current is called *primary* and consequently the other is called *secondary*; The different operation modes can be distinguished in *single-gate* modes or *double-gate* modes (DG). For the *single-gate* operation mode alternatively a top gate (TG) or bottom gate (BG) is obtained when the correspondent gate is biased and the other one is connected to ground. The double gate bias modes for the p-type DG-OFET are described in Fig. 4.6 Applying simultaneously different, independent bias levels to the TG and BG (V_{TG}, V_{BG}) drives the device in the *asymmetric* bias mode (AB). If both gates are connected to the same voltage source the DG-OFET is operated in the *symmetric* bias mode (SB, dashed line). In both cases the *double accumulation* regime ($V_{TG}<0$, $V_{BG}<0$) or the *double depletion* regime ($V_{TG}>0$, $V_{BG}>0$) are obtained respectively with concordant negative or positive polarities; the application of

discordant biases to the gates allows to operate a depletion OFET, where the device (*On*) is switched *Off by* biasing one of the gates positively, we call this *Mixed mode*.

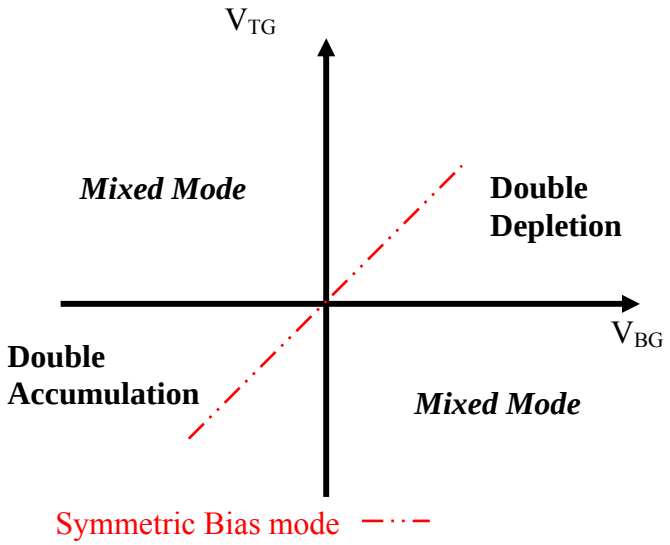

Figure 4.6 Operation modes of a double-gate organic field-effect transistor (DG-OFET) structure

Up to date only a few papers have been published on the DG-OFET topic. The first ones were in 2005.

Morana et al. [9] carried out measurements on F8T2-based polymeric FET with polymeric top and bottom gate dielectric layers. Using the top gate as the primary gate the drain current on the I_D-V_D curves has been modulated through the application of a bottom-gate voltage: the drain current lowers (respect to the floating V_{BG} case) when a positive V_{BG} is applied while it increases (with respect to the floating V_{BG} case) when a negative V_{BG} is applied to the bottom-gate. This behavior can be attributed to the formation of a second conductive channel that increases the number of charge carriers collected at the drain electrode when the bottom-gate is driven to negative voltages; when the bottom-gate is driven towards positive voltages an earlier and flatter saturation together with a drain current lowering can be observed on the curves due to an enhanced depletion of holes in the depletion region close to the drain electrode.

In the same study the effect of a secondary gate is evident also from the Sqrt|Id| vs. V_{TG} where a decrease towards smaller values of the threshold voltage together with a higher I_{OFF} current is measured while V_{BG} (the bottom gate being used as the secondary gate in their study) increases negatively. In fact, as stated by them, a higher density of holes (due to V_{BG}

that increases from 0 to more negative values) results in the filling of traps at low V_{TG} values and this is confirmed by the higher values of I_{OFF}.

Iba et al. [10] mainly used the double-gate structure in order to modulate pentacene-based devices threshold voltage without underlining any other specific benefits of employing a further gate.

In order to have a deeper insight, Chua et al. [11] solved Poisson-continuity equations for a unipolar four-terminal device using reasonable values for the physical parameters of the organic semiconductor with only the mobile charge term incorporated to represent carrier accumulation in an intrinsic semiconductor material. By doing this they demonstrated clearly that when both gates are on, two parallel conduction channels are formed in the device. The accumulation width was found to be only a few angstroms wide with the bulk of the semiconductor body screened by these two channels.

Experimental results confirmed some of their theoretical assumptions. When both the gates are biased in a symmetric mode the drain current is higher than the single-gate case. Moreover, when either of the gates is biased away from the conduction the overall drain current can be attenuated by several orders of magnitude. What they observed in addition to that was that the top and bottom channel potentials are coupled and the electrical characteristic of one channel is markedly modulated by the bias applied to the opposite gate as predicted. Another important point they stressed was that if the gate capacitance values are not matched then the gate with a lower dielectric capacitance exerts a stronger effect on the overall channel conductance. In conclusion, they came up with a further comment: the well-controlled modulation of the drain current by using double-gate structures compared to the single-gate structures can be ascribed to screening of the longitudinal source-drain electric field at the drain end by the equipotential volume setup by the two identical gate voltages, which suppresses the carrier velocity through the “pinch-off” region in the saturation regime.

Some experimental results were carried out by us by testing the following double-gate FET structure:

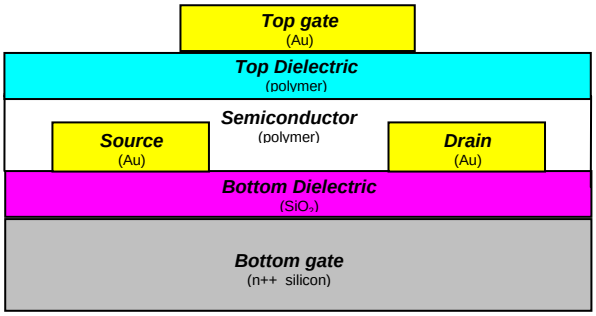

Figure 4.7 Description of the tested DG-OFET structure

These structures have been produced by spincasting the pristine polymer (P3HT) solution onto a 230 nm SiO_2 dielectric, thermally grown on a n^{++}-Si wafer, used as gate electrode. Gold source and drain electrodes (with a 10nm thick ITO adhesion layer) were used to contact the polymer. Before coating the active layer the SiO_2 surface was treated with a hexamethyldisilazane (HMDS) primer, to improve the film adhesion and formation. An interdigitated layout, obtained by means of conventional photolithography, was used for the OFET where Z = 10mm is the FET channel width. The dielectric capacitance per unit area is C_{bottom} = 15 nF/cm^2. The nominal value of the semiconductor thickness is 100 nm. Successively a polymeric dielectric layer (PMMA) was spun onto the semiconductor layer resulting in an almost 1 μm thick top dielectric layer (C_{top} = 2.8 nF/cm^2). Then a gold top electrode (top-gate electrode) was sputtered in argon environment.

The output characteristics measured only by using the bottom-gate electrode are depicted in (Fig. 4.8):

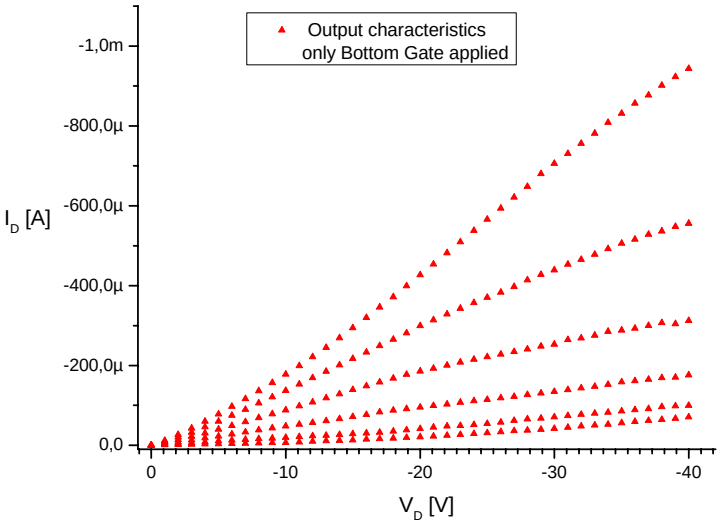

Figure 4.8 output characteristics of tested DG-OFET structures while biasing only the bottom-gate electrode. V_{BG} varies from 0 to -100V in -20V step. The top-gate electrode was floating. Channel length L = 10μm

Then the output characteristics measured only by using the top-gate electrode are depicted in (Fig. 4.9):

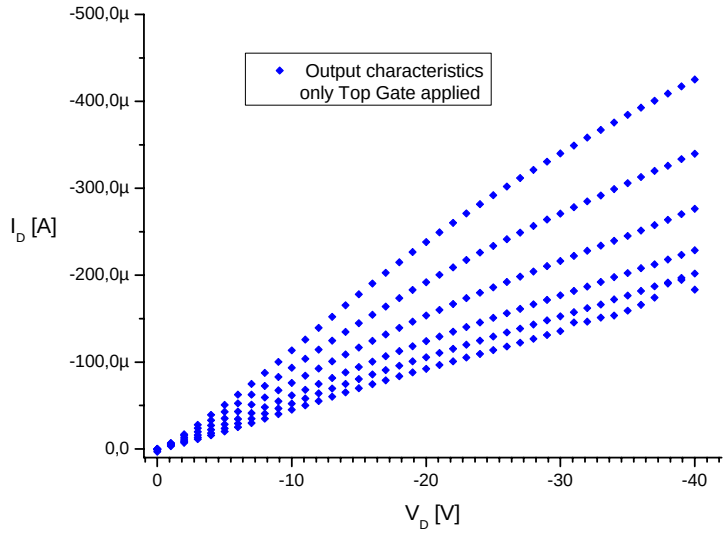

Figure 4.9 output characteristics of tested DG-OFET structures while biasing only the top-gate electrode. V_{TG} varies from 0 to -100V in -20V step. The bottom-gate electrode was floating. Channel length L = 10µm

Two preliminary considerations come out from this measurements: a. the bottom gate will act as the primary gate for the structure because of its ability to better control the charge modulation through the channel and consequently b. the top-electrode could be used in an asymmetric bias configuration to help the bottom-gate better modulate the drain current. Furthermore the formation of two independent channels through two different interfaces (top dielectric/semiconductor and bottom dielectric/semiconductor) is evident because two output characteristics could be measured. In this case the top dielectric/semiconductor interface should be the same of the bottom dielectric/semiconductor since spincoated polymers have the same smooth interface both on the bottom and on the top of the film. In this case the poorest performance that usually was carried out on the "top" transistor (Fig. 4.9) depends on the use of thicker dielectric layers compared to the SiO_2 thickness which is able to better couple the signal and to the higher leakage current through the PMMA film that results into higher off-current values.

When the DG-OFET is employed in an asymmetric bias configuration:

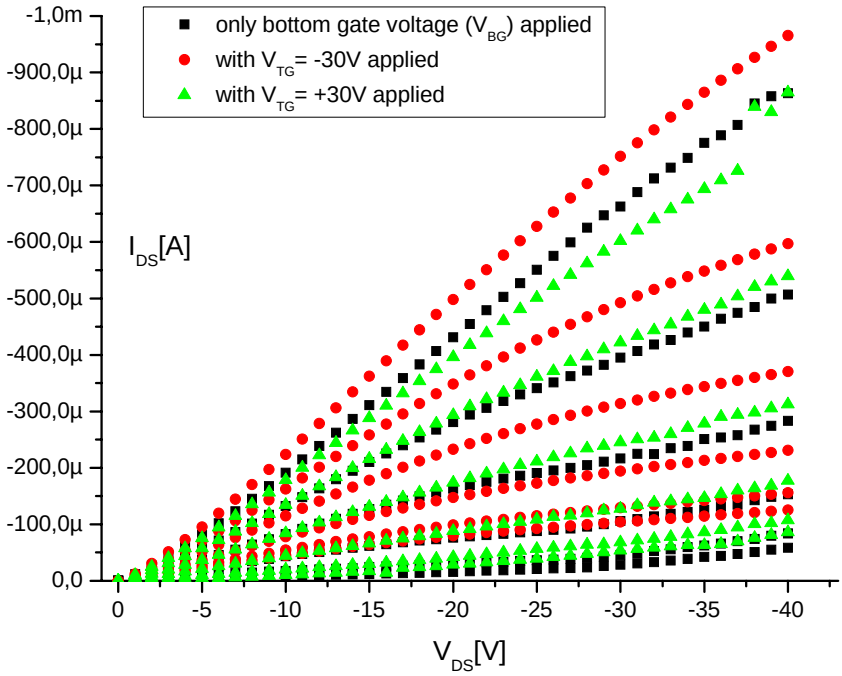

Figure 4.10 Output characteristics of tested DG-OFET structures while biasing the device in an asymmetric mode with the bottom-gate as the primary gate electrode. V_{BG} varies from 0 to -100V in -20V step. The top-gate electrode was floating, then biased in order at -30V and +30V. Channel length L = 10µm

By examining the curves a few considerations can be made. When the top gate is negatively (positively) biased higher (lower) drain currents are achieved compared to the only bottom gate case. As an example let us consider the last three curves set in the graph, taken at V_{BG} = -100V.

However the off current increases as well for both V_{TG} = -30V and +30V. In the last case (V_{TG} = +30V) a lower off current should be expected according to Chua et al. This higher off current could be ascribed to a better charge confinement due to the positive bottom gate voltage that pushes charges away towards the other channel to which they get coupled.

The same phenomenon can be observed on different groups of curves like the ones taken at V_{BG} = -80V (let us compare the three curves without top gate voltage applied, V_{TG} = -30V and +30V whose drain current values range from 400µA to roughly 600µA). The curve taken at V_{TG} = +30V is slightly higher (for high V_{DS} values) than the one taken without the application of a top gate. In conclusion we generally found that biasing positively (when dealing with p-type semiconductors) the secondary gate is a powerful instrument to better confine charge carriers to the major conduction channel (enhancing in this way the overall drain current collected) rather than shut it off. On the other hand, Chua et al. [11] remarked

the importance of having the same gate dielectric capacitance for both bottom and top gate in order to have reliable coupling between the two gates and their model, by the way, relies on this assumption; in addition to that, they highlight the role of the semiconductor thickness: this one should have the optimal thickness in order to be fully depleted by both the gates when needed. In our studies the gate dielectric capacitances were not matched each other but as stated above, a primary and a secondary gate was employed and after several experiments the semiconductor optimal thickness that allows a coupling between the two channels and at the same time the formation of two separate channels was found to be around 100nm.

In conclusion the double-gate OFET was found to be a very powerful tool to modulate the charges into the channel. This suggests the exploitation of these structures in the sensor field. In fact, when certain chemical or biological species can be grabbed on one of the two metallic (or polymeric like, for instance, PEDT:PSS) gates a modulation of the drain current depending on both the sign and the quantity of the immobilized charge on that gate can be obtained while biasing the other one with a known voltage. Again, the better confinement of charge carriers due to the presence of two gates could also be employed with Organic Light Emitting Transistors (OLETs) where a light coming through two transparent polymeric dielectrics from both upper and bottom side can better stimulate photoemission process.

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Chapter 5

Dielectric/Semiconductor Interfaces in OTFT

The interface between an organic semiconductor/dielectric pair plays a decisive role in the functional performance of the Organic Thin-Film Transistors (OTFTs). Since it is well-known that the charge carriers flow through the channel in the first few nanometers of the channel, namely at the interface between the semiconducting and the insulating layer, a better understanding of which phenomena are involved in the conduction mechanism is due. In fact designed interface that promotes synergistic interactions between the semiconductor and dielectric is essential in achieving optimum FET performance.

First in this chapter an overview of the main organic dielectrics employed as the gate insulator in OTFTs fabrication will be presented; then the dielectrics we have been testing throughout this thesis work as well as the role of the interfaces will be discussed together with the trapping mechanisms occurring when dealing with organic materials, and finally how semiconductor morphology and chemical-physical nature of the interface can influence the OTFTs electrical performances.

5.1 Organic Dielectrics

Polymeric Dielectrics, referred in literature as to Organic Dielectrics, have been more and more employed in organic electronics [1] [2] [3] progressively substituting the silicon-dioxide that has been used over the past years mainly as a standard substrate for testing materials.

Organic dielectrics are making their own way in future electronics for several reasons:
- they are solution-processable and can be chemically tailored for specific applications. Moreover, being soluble into different solvents the dielectric properties of the film can be tuned by varying the solvent as well as the dielectric percentage into the solution.
- the deposition of inorganic dielectrics is difficult on top of the organic semiconductors. The surface treatments usually employed on inorganics (such as HDMS or OTS treatment) is practically impossible to be used in top-gate devices. Organic dielectrics, however, offer the freedom to build both top and bottom gate devices more easily by the use of solution coating techniques and printing.
- being transparent these dielectrics can be used in optoelectronic applications. Furthermore, the optical inspection of the semiconductor layer from the gate side is possible with them, not with silicon dioxide which is not transparent. In fact, it is widely accepted that the formation of the organic-based devices conductive channel is supposed to occur at the interface between semiconductor layer and insulator that therefore strongly affects the electrical performances. By optically investigating this area a wide set of major information useful for a deeper transport properties understanding could be thus gathered.

In general, high gate capacitance (C_{ins}) is a desirable parameter for FETs, because it allows a higher charge density to be induced at lower voltages and it increases drive capability. The capacitance can be increased by using a thinner dielectric or by using a high permittivity insulator material.

Unfortunately, there is a limit to how thin the dielectric can be due to breakdown and reliability issues such as defects and yield. In fact, with lowering the dielectric thickness the leakage currents through the dielectric bulk increase resulting in major consequences for OTFTs function [4] such as irreversible degradation of the organic semiconducting layer.

According to de Boer et al. this degradation occurs even when the leakage current is several orders of magnitude smaller than the source-drain current so this parameter must be considered when properly designing the gate insulator for OFETs.

The major organic insulator materials reported in literature are shown in Figure 5.1:

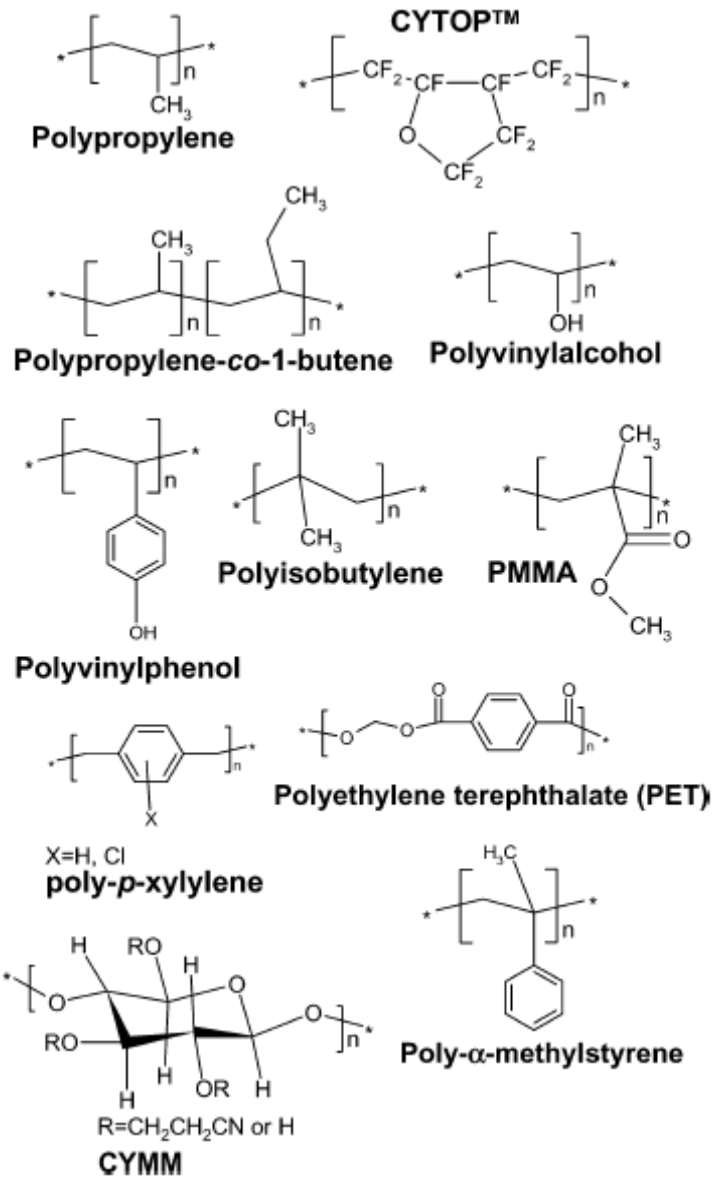


Figure 5.1 Major organic polymers used as gate insulator in organic electronics [5]

In 2004 J. Veres et al [5] conducted a systematic study on several polymeric dielectrics as the gate insulator for FET devices and their influence on amorphous polytriarylamines.

One of the main findings of this work was that low polarity (low-k) resins resulted in far superior devices than PMMA or PVP. The latter polymers having permittivities around 3.5-4.5 resulted in approximately 10 times mobility reduction compared to those with a

permittivity of 2.1-2.3. In fact temperature activation of the field-effect mobility increased when high permittivity insulators were used. This led to the hypothesis that localization is enhanced in the channel region if the interface is more polar and that randomly oriented interface dipoles modify site energies on the microscopic level. A common feature of organic semiconductors is that almost all sites can be considered localized and thus local variations in dipole orientation/chemistry have an influence on these sites, potentially scattering them in energy. Precisely the bulk density of states is broadened according to this mechanism by dipolar disorder at the interface with the dielectric.

It must be noted, however, that permittivity is not the only parameter for the optimal material choice, as the dielectric is also required to have high dielectric breakdown, yield a uniform and defect- and pinhole-free film, and be deposited from an orthogonal solvent to the semiconductor.

Analysis of the morphology of the composite of layers is therefore important for overall device performance, and this can be achieved using several methods such as either TEM and AFM.

Another parameter to be taken into account when designing a proper semiconductor/dielectric interface is the surface energy. Veres et al. [5] used bottom gate OFET devices for investigating dielectrics with varying surface energies. On one hand, SiO_2 was used with different surface treatments, resulting in a range of water contact angles on the surface of the gate dielectric. On the other hand, polymeric photoresists were also tested, each having slightly different surface properties. It was found that the mobility monotonically increased as the dielectric surface became more hydrophobic (Fig. 5.2).

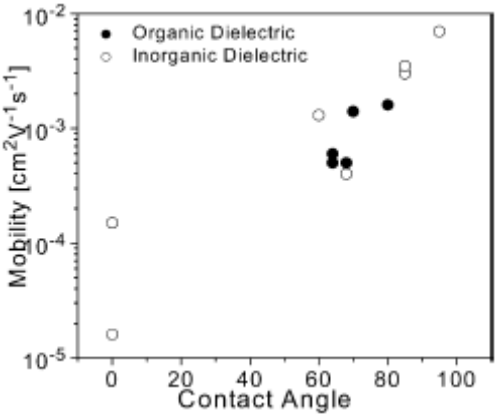


Figure 5.2 Field effect mobility measured on bottom-contact FET devices (with PTAA as a semiconductor) with varying the contact angle on the gate insulator. The gate insulator was either SiO_2 with different surface treatments or organic dielectrics employed by Philips

Anyway, it is not known yet whether the polarity of the OSC dielectric interface is a critical parameter for highly ordered materials beyond affecting their morphologies. Indeed, there are some examples of devices exhibiting high mobilities on both high- and low-k dielectrics.

In addition to what stated above, a further and major effect has been attributed to the gate dielectric choice. The presence of electron trapping sites on the surface of the insulating layer can even strongly influence the charge transport in the semiconductor [1] while inhibiting the electrons collection at the drain electrode. By controlling the chemical-physical interface between this two players, dielectric and semiconductor, is possible to obtain ambipolar conduction (meaning both n-type and p-type) even on widely p-type believed organic semiconductors. Paragraph 5.5 is dedicated to this issue.

Moreover, very recently Kim et al. [6] tested OFET devices having pentacene as semiconductor and several organic polymers (such as PMMA, PVP and different PS batches) as gate insulator. They stressed the point that the polymer surface thermal and viscoelasticity phenomena are of general importance and demonstrated their crucial consequences for pentacene TFT response when polymers are used as gate dielectrics. First, there is an unprecedented and general effect of the dielectric glass transition temperature (T_g) on the charge transport properties of overlying thin-film organic semiconductors. General and abrupt mobility transitions occur at well-defined pentacene film growth temperatures characteristic of each underlying polymer dielectric. This temperature,

associated with a surface T_g, is substantially lower than the bulk T_g and is independent of film thickness. Second, the transition from high to low pentacene TFT field-effect mobility is closely correlated with large microstructural and morphological alterations of pentacene film growth occurring at the same surface T_g. Third, pentacene grain size–TFT carrier mobility analysis reveals two mobility states for pentacene TFTs, well separated by a critical grain size (~0.8 μm). Fourth, observing and quantifying surface T_g via field effect mobility measurements suggest a useful new probe of polymer interfacial viscoelastic properties versus those in thin films and the bulk.

Despite strong effort has been so far put on understanding the role of the polymeric gate dielectrics still a complete and general picture of the interactions among surface properties, dielectric thickness, permittivity constant and physical-chemical interaction of the interface with the semiconductor is needed.

The following paragraphs of this chapter represent an attempt of having a deeper insight into this lively debate on the role of the interface organic semiconductor/organic dielectric on the OFET performances.

5.2 Gate Dielectrics tested

Throughout this paragraph are presented the dielectrics we tested over this work.

In particular, some of them such as Poly(4-vinyl phenol) (PVP), Poly(4-vinyl alcohol) (PVA), Poly(dimethyl-siloxane) (PDMS) and Poly(methylsilsesquioxane) (pMSSQ) are spin-coatable where as the others, namely poly(ethylene-terephtalate) (Mylar®) and a biocompatible plastic (Mater-Bi), were provided in thin films adapted on a plastic frame.

5.2.1 Poly(4-vinyl phenol) (PVP)

Poly(4-vinyl phenol) (PVP) (Fig. 5.3) with average weight of 50000 (Sigma-Aldrich) was used as received. Cross-linkable PVP was spin coated onto at 600 rpm and then prebaked at 80 °C for 10 min in a oven. The cross-linkable PVP solution was composed of PVP polymer, poly melamine-co formaldehyde methylated (Aldrich, M_n 511) as a cross-linking agent, and propylene glycol monomethyl ether acetate (PGMEA) as a solvent. Spin-coated

PVP films were cross-linked at 200 °C for 60 min in a oven. Cured PVP films were vacuum dried at 100 °C for 24h.

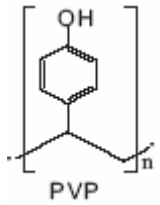


Figure 5.3 Chemical structure of PVP

Here are reported the main electrical parameters measured on organic thin-film transistor in top-contact bottom-gate configuration having pentacene as the semiconductor layer, PVP as the gate dielectric and gold source, drain and gate electrodes deposited via thermal evaporation as well as the RMS roughness measured on the bare dielectric:

	PVP
RMS roughness *bare dielectric*	0,20nm
μ ($cm^2/V*s$)	$3.4*10^{-1}$
$\mathbf{V_{TH}}$ (Volt)	-5

5.2.2 Poly(vinyl alcohol) (PVA)

Polyvinyl alcohol (PVA) (Fig. 5.4) is a synthetic resin that is prepared by polymerization of Poly(vinyl acetate), followed by hydrolysis of the resulting ester in the presence of an alkaline catalyst. As to the hydrolysis degree PVA can be classified in partially hydrolyzed (87-89% degree of hydrolysis) and fully hydrolyzed (98-99% degree of hydrolysis).

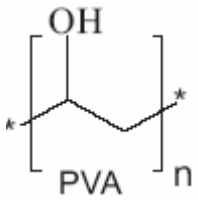
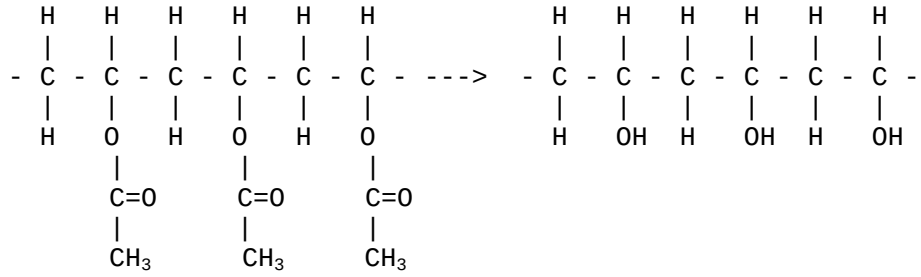
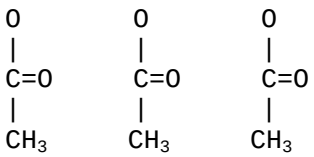


Figure 5.4 Chemical structure of PVA

According to the following reaction:



As stated above poly(vinyl acetate) is turned into poly (vinyl alcohol) through hydrolysis. When the hydrolysis is partial not all of the



will be substituted by the – OH group, forming an alcohol (C-OH). This means that when PVA is not fully hydrolyzed carbonyl groups (C=O) will be still present.

A comparison between the FTIR spectra of fully and partially hydrolized PVA can be seen in Fig. 5.5:

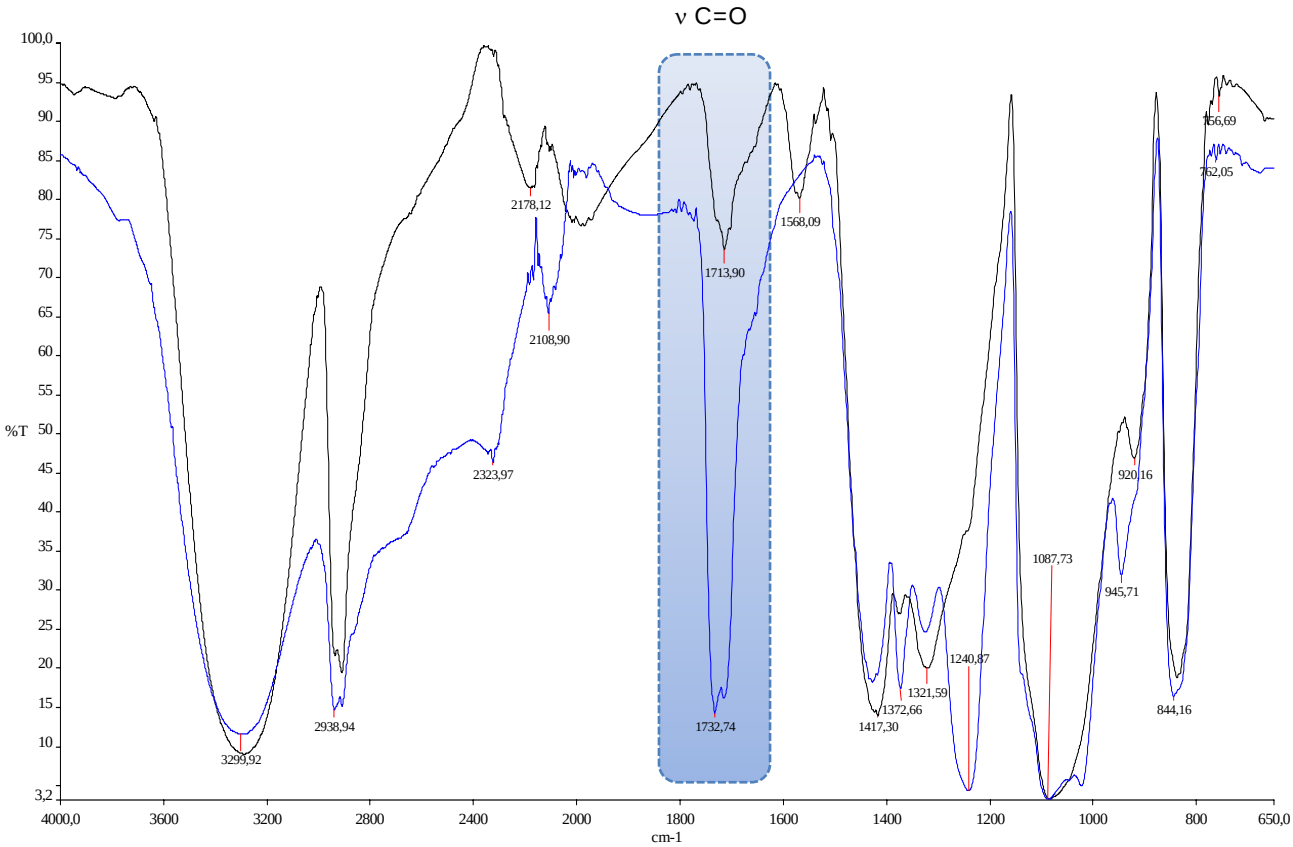


Figure 5.5 Differences on the FTIR spectra between fully (98-99%) hydrolyzed PVA (black curve) and partially (86.7 – 88.6%) hydrolyzed PVA (blue curve), 10% (weight) in water: the 98-99% hydrolyzed PVA is far less C=O-rich than the 86.7 – 88.6% hydrolyzed PVA as highlighted by the blue bar. In fact the transmittance of the C=O in 98-99% hydrolyzed PVA is very high because no carbonyl groups should be ideally (100% hydrolysis degree) present.

We made dielectric films starting from PVA (10% weight) dissolved in bidistilled water but also films made by solutions containing a different percentage of Ammonium Dichromate in addition were tested. The ammonium dichromate acts as a cross-linking agent for PVA. Cross-linking PVA chains should result into a higher resistance gate dielectric that therefore should exhibit lower leakage currents.

This reaction (water + PVA + ammonium dichromate) is rather complex and was studied by L. Grimm et al. [7]. In fact eight steps are needed in order to have the reaction product which basically can be written in this final form:

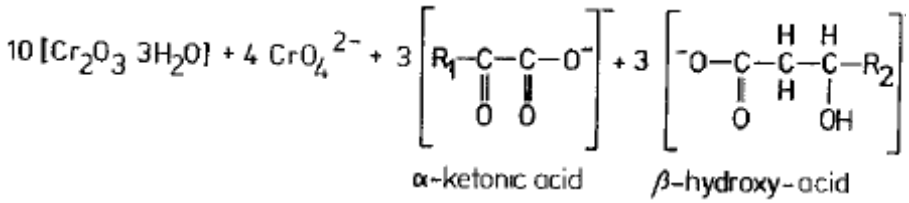


Figure 5.6 Final product of the reaction among water, PVA and Ammonium Dichromate: the chain ends having the structure of α-ketonic and β-hydroxy acid (eighth reaction) [7]

The final product of this cross-linking reaction is C=O-rich and the percentage of carbonyl groups is governed by the percentage of Ammonium Dichromate present in the solution. This fact is confirmed also by FTIR spectra in Fig.5.7:

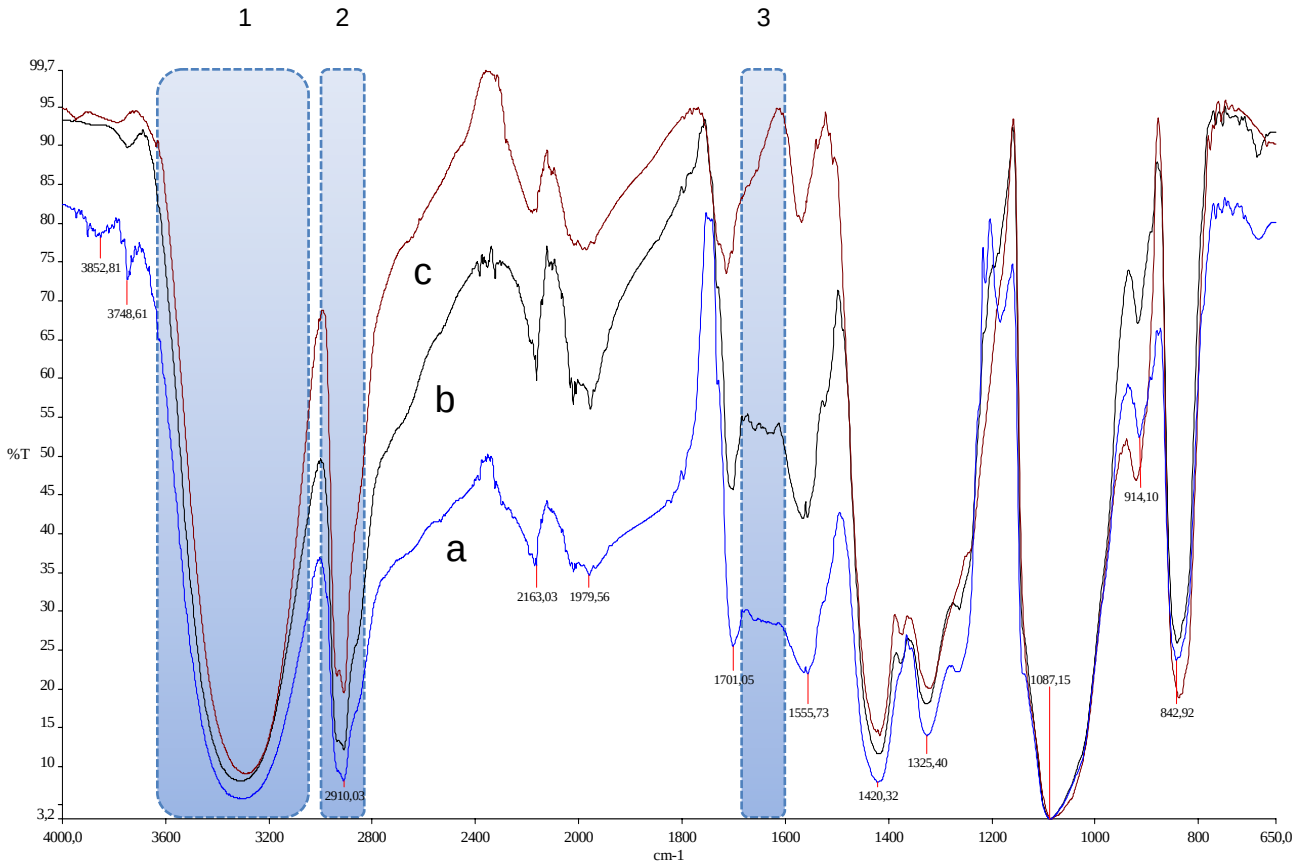


Figure 5.7 Differences on the FTIR spectra carried out on different films made from aqueous solutions containing (a) fully (98-99%) hydrolyzed PVA 10% (weight) plus Ammonium Dichromate 1.4% (weight), (b) fully (98-99%) hydrolyzed PVA 10% (weight) plus Ammonium Dichromate 0.5% (weight) and (c) fully (98-99%) hydrolyzed PVA 10% (weight).

The blue bars 1, 2 and 3 indicate the presence of respectively –OH groups, -CH groups (from aldehyde) and C=O groups. In particular, strong differences in the percentage of

carbonyl groups is highlighted. According to what stated above very low presence of C=O groups is evident in solutions containing PVA without ammonium Dichromate whereas the percentage of carbonyl groups increases gradually with the ammonium dichromate percentage. The role of carbonyl groups in the gate dielectric will be better highlighted in paragraph 5.5.

For preparing PVA dielectric films, Poly(vinyl alcohol) (Mowiol® 40-88, Sigma Aldrich) with an average molecular weight of 205000 was used as received. PVA films were prepared by depositing 10% (weight) in water solution via spin-coating at 600rpm and then baked at 100 °C for 24h. The cross-linked PVA solution is composed of PVA (10% in water), Ammonium Dichromate (Sigma-Aldrich) as a cross-linking agent (in different percentage) and bi-distilled water as a solvent. Spin-coated PVA films were cross-linked by UV irradiation (5') and then baked at 100 °C for 24h.

Here are reported the main electrical parameters measured on organic thin-film transistor in top-contact bottom-gate configuration having pentacene as the semiconductor layer, PVA (partially hydrolyzed) as the gate dielectric and gold source, drain and gate electrodes deposited via thermal evaporation as well as the RMS roughness measured on the bare dielectric:

	PVA
RMS roughness *bare dielectric*	0,45nm
μ_p ($cm^2/V*s$)	$1.5*10^{-2}$
μ_n ($cm^2/V*s$)	$2*10^{-3}$
$V_{TH,p}$ (Volt)	-25
$V_{TH,n}$ (Volt)	-80

As it can be easily deduced by the table, evidence for electron transport was found on FET having PVA partially hydrolyzed as the gate insulator. This ambipolar behavior will be better discussed as well as explained in paragraph 5.5.

Here are reported the main electrical parameters measured on organic thin-film transistor in top-contact bottom-gate configuration having pentacene as the semiconductor layer, PVA

(partially hydrolyzed) with 1.4% Ammonium Dichromate (PVA/AD) as the gate dielectric and gold source, drain and gate electrodes deposited via thermal evaporation as well as the RMS roughness measured on the bare dielectric:

	PVA/AD
RMS roughness *bare dielectric*	0,25nm
μ_p ($cm^2/V*s$)	$3.5*10^{-2}$
$V_{TH,p}$ (Volt)	-12

5.2.3 Poly(dimethyl siloxane) (PDMS)

Poly(dimethylsiloxane) (PDMS) (Sylgard 184, Dow Corning) was used as received.

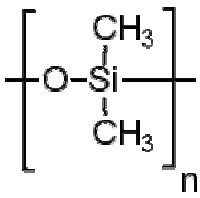


Figure 5.8 Chemical structure of PDMS

After mixing its pre-polymer with the curing agent (ratio 10:1) the solution was spun at 10000 rpm and then oven baked for 1h.

No FET characteristics were measured when PDMS as the gate dielectric due to either poor degree of cristallinity of gold grown on top of it and pinholes through the dielectric bulk resulting in very high leakage currents. However we found evidence for ambipolar conduction as shown in [8].

5.2.4 Poly(methylsilsesquioxane) (pMSSQ)

Poly(methylsilsesquioxane) (pMSSQ) with its solvent was provided by Ciba Specialty Chemicals Inc.

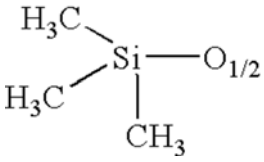


Figure 5.9 Chemical structure of pMSSQ

After spinning at 2000 rpm it was baked at 160 °C for 1h. We tested pMSSQ as a dual-layer gate dielectric [9] [10] in combination with PVP. The expected thickness of the pMSSQ layer is around 45nm, as reported in [9].

Here are reported the main electrical parameters measured on organic thin-film transistor in top-contact bottom-gate configuration having pentacene as the semiconductor layer, pMSSQ on top of PVP as the gate dielectric and gold source, drain and gate electrodes deposited via thermal evaporation:

	pMSSQ on PVP
RMS roughness *bare dielectric*	1.4-1.5nm
μ_p ($cm^2/V*s$)	$2.17*10^{-1}$
$V_{TH,p}$ (Volt)	+5

5.2.5 Mater-Bi®

Biocompatible film with different thicknesses were provided by Novamont S.p.A. (http://www.materbi.com/) and tested in our laboratories.

In particular we focused on the thinnest film we were provided, namely NF01U and CF03A both 15μm thick.

The dielectric permittivity of both of them was unknown and measured through capacitance-frequency measurements on Metal-Insulator-Metal structures. The metal used for preparing MIM structures was gold.

The C-f characterization carried out on NF01U and CF03A MIM structures is shown respectively in Fig. 5.10 and Fig. 5.11:

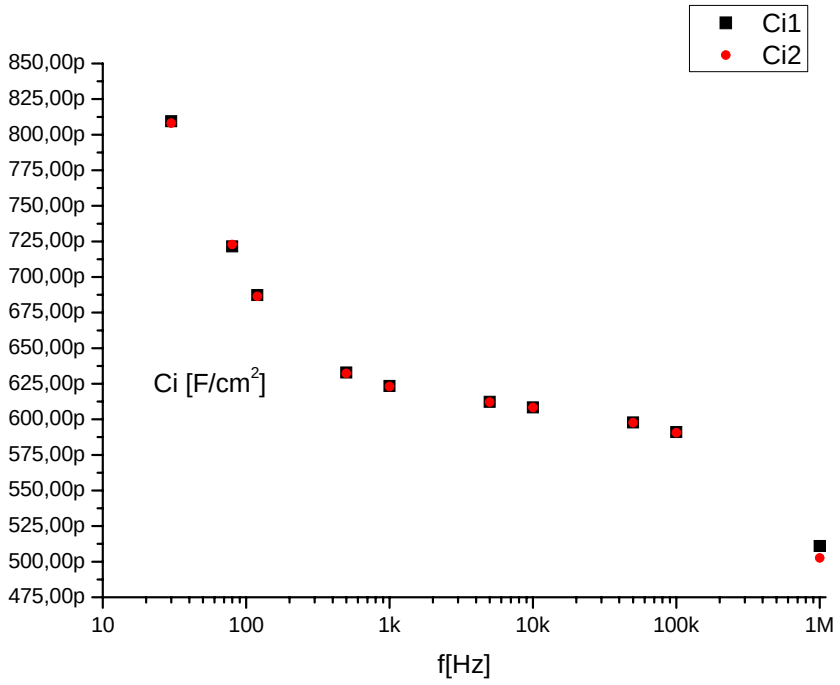


Figure 5.10 C-f measurements carried out on NF01U Biocompatible plastic

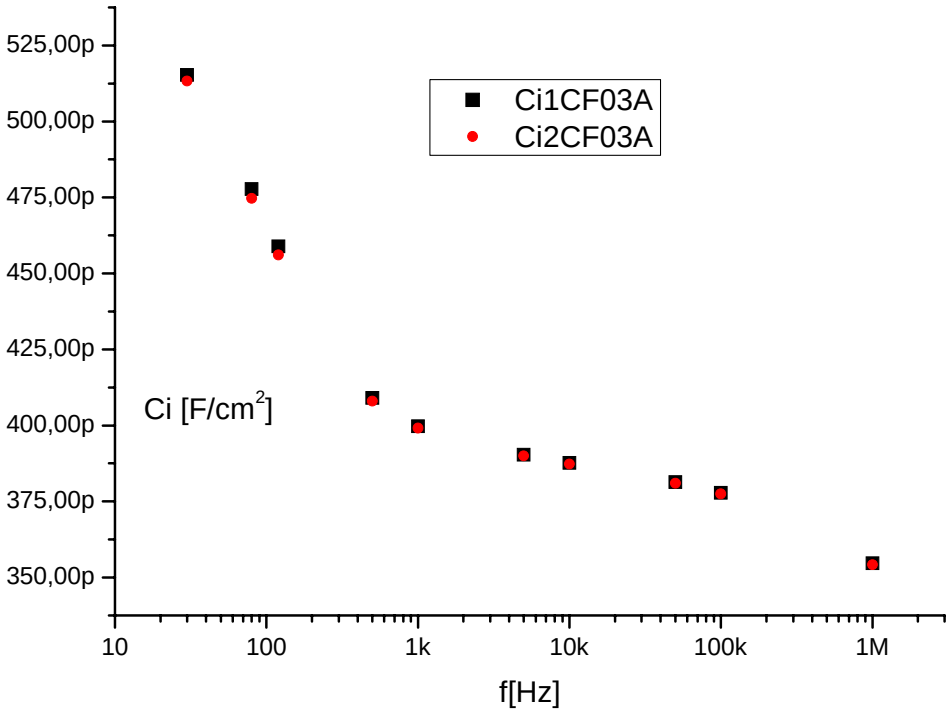


Figure 5.11 C-f measurements carried out on CF03A Biocompatible plastic

It is evident from the previous figures that despite the fact that the dielectric films have the same thickness the former has higher dielectric permittivity than the latter.

In particular: $\varepsilon_{ins[\,f=30Hz]} = \frac{C_i d_{ins}}{\varepsilon_0} = \frac{810*10^{-12}*15*10^{-4}}{8.85*10^{-14}} \cong 13{,}72$ for NF01U

and $\varepsilon_{ins[\,f=30Hz]} = \frac{C_i d_{ins}}{\varepsilon_0} = \frac{515*10^{-12}*15*10^{-4}}{8.85*10^{-14}} \cong 8{,}7$ for CF03U.

No AFM characterization on these bare dielectric films has been carried out so far.

Here are reported the main electrical parameters measured on organic thin-film transistor in top-contact configuration having pentacene as the semiconductor layer, Mater-Bi® films 15μm thick as the gate dielectric and gold source, drain and gate electrodes deposited via thermal evaporation.

	NF01U	**CF03U**
μ_p ($cm^2/V*s$)	$2*10^{-3}$	10^{-3}
$V_{TH,p}$ (Volt)	-40	-45

5.2.6 Mylar®

Mylar® (provided by DuPont) is a poly(ethyleneterephtalate) foil with thickness ranging from 0.9 to 1.6 μm, which can act at the same time as the gate dielectric and as the mechanical support for the final device when mechanically adapted to a plastic frame, as we did for preparing our samples. This material is characterized by a dielectric constant similar to that of SiO_2 (ε_{diel} = 3.3), high resistivity (surface resistivity 10^{16} Ohm/sq) and low permeability to oxygen, hydrogen, water and CO_2 [11]. Moreover, due to its mechanical properties, it can be used as a flexible mechanical support for the realization of completely flexible electronic devices. After the assembly, such patterned film can be applied to any kind of substrate allowing, on one hand, to access to unusual applications (substrates as soft as paper or fabric or 3D surfaces can be used) and, on the other hand, to protect the organic semiconductor from the contact with atmosphere, without the constraints of top gate structures. The first step for the realization of an OFET on Mylar® is the assembly of the plastic foil on a circular frame in order to obtain a flat surface. Gold source and drain electrodes can be either patterned on Mylar by means of standard photolithographic procedure (bottom-contact configuration) or deposited on the top of the semiconductor through a shadow mask (top-contact configuration). The Mylar® films were cleaned with acetone, deionized water and then dried with a nitrogen flux so they do not require any special kind of cleaning treatment.

Here are reported the main electrical parameters measured on organic thin-film transistor in top-contact configuration having pentacene as the semiconductor layer, a 1.4 μm thick Mylar® film as the gate dielectric and gold source, drain and gate electrodes deposited via thermal evaporation.

	Mylar®
RMS roughness *bare dielectric*	2nm
μ_p ($cm^2/V*s$)	$5*10^{-2}$
$V_{TH,p}$ (Volt)	-30

5.3 Trapping mechanisms in OTFTs

The knowledge about properties of electronics traps in organic semiconductors [12] [13] [14] [15] [16] is one of the major keys for the understanding and optimization of charge transport in organic devices.

There are different sources for trap states in the organic layers:

- *Impurities*, due to the weak interaction between molecules in an organic solid, a specific molecule can keep its HOMO/LUMO position independent of the surrounding matrix. If the HOMO or LUMO of an incorporated molecule is positioned in the gap of the host molecules, it will form a trap state.
- *Structural defects*: even if there are only molecules of the same species, the HOMO/LUMO levels may vary from molecule to molecule. The exact energy position of the HOMO/LUMO level is not only determined by the chemical structure of the molecule itself but also by the electronic polarization of its surrounding. Structural imperfections will lead to a fluctuating surrounding. If a specific kind of structural defect occurs on grain boundaries in polycrystalline layers, for instance with pentacene films, structural defects may result in more or less discrete trap states deep in the gap [16]. Structural defects in polycrystalline films are strongly correlated on the properties of the substrate where the film is grown; in fact the substrate properties as well as the deposition parameters will dictate the morphology of the films or, in other words, the domains density, the number and size of grains and consequently the inter grain transport properties; these correlations will be further discussed here in this chapter.

In addition to that, the area of the junction between different materials has normally a higher density of structural defects. This is the case, for instance, of the organic semiconductor/dielectric interface in an organic field effect transistor. The interfacial traps generated are thus localized mostly at the semiconductor/dielectric interface.

5.3.1 Bulk traps

Space charge limited current measurements reveal that the charge transport in highly resistive organic semiconductors is often determined by bulk traps within the material [17]. In order to achieve transistor action on single crystalline materials these trap levels have to

be filled by carriers induced by a gate voltage. Above the threshold voltage V_T all traps are filled and mobile carriers are induced. The field-effect mobility is then formally determined by the ratio of free carriers n_f to the total number of charge carriers n_{tot} (trapped n_t and free carriers n_f) $\Gamma = n_f/(n_t+n_f)$ and the intrinsic mobility μ_0 of the material itself

$$\mu_{FET} = \mu_0 * \Gamma \tag{5.1}$$

Assuming, for simplicity sake, a single discrete trap level at an energy E_t with a concentration N_t , the concentration of trapped carriers n_t as function of the Fermi energy E_F is given

$$n_t = \frac{N_V}{1+\exp\left[\left(E_f - E_t - eV\right)/kT\right]} \tag{5.2}$$

where N_V is the density of states of the valence band. Furthermore, the density of free carriers n_f can be determined from

$$n_f = \frac{N_V}{1+\exp\left[\left(E_V - E_f - eV\right)/kT\right]} \tag{5.3}$$

It has been shown [18], that in this case the threshold voltage is given by

$$V_t = \frac{\sqrt{2kT\varepsilon_r\varepsilon_0 N_t}}{C_i} \tag{5.4}$$

where ε_r and ε_0 are the dielectric constant of the semiconductor and of the vacuum, respectively. It has been shown [17] that the bulk trap density in pentacene and in oligothiophenes can be changed reversibly by annealing in air or hydrogen.

5.3.2 Interface states

It is well-known from Si-technology that the properties of the interface between the insulator and the semiconductor can essentially influence the device performance Here we have studied the influence of interface states using different gate dielectrics while using the same semiconductor (pentacene). It can be clearly seen that devices prepared with different

dielectrics exhibit very different characteristics. We ascribe this difference to traps and defects at the semiconductor/insulator interface. Besides the shift of the threshold voltage from one pentacene/dielectric couple to another, the subthreshold characteristic is often significantly different. The subthreshold swing S, $\left[S = \partial V_G / \partial(\log(I_d))\right]$ can be approximated by [19]:

$$S = \frac{kT}{e}\ln 10\left(1+\frac{C_s}{C_i}\right) \tag{5.5}$$

where C_S is the capacitance of the accumulation layer in the organic semiconductor. If the device exhibits a significant number of interface traps, their capacitance C_{it} is in parallel with C_S [20]. Therefore the subthreshold swing without interface traps, S_0, increases, given by [19]:

$$S = S_0 \frac{1+\dfrac{C_s + C_{it}}{C_i}}{1+\dfrac{C_s}{C_i}} \tag{5.6}$$

Hence, the interface trap density N_{it} can be approximated using $C_{\text{it}}=eN_{\text{it}}$ or in alternative the following expression [21] which is though referred to the maximum density of traps:

$$N_{SS}^{\max} = \left[\frac{S\cdot\log(e)}{kT/q} - 1\right]\frac{C_i}{q} \tag{5.7}$$

5.3.3 Grain boundaries

The influence of the grain boundary traps is not only determined by Γ (see 5.1), more importantly the charge at the grain boundary determines the barrier height E_B at the grain. Therefore, the mobility of the polycrystalline materials significantly depends on the position of the Fermi energy and as a result of this on the gate voltage ($E_B=E_B(V_G)$). The effective mobility μ_{eff} in polycrystalline materials is given by [22]:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_0} + \frac{1}{\mu_{GB}} \tag{5.8}$$

where μ_0 is the bulk mobility (inside the grain) and μ_{GB} the grain boundary mobility, which is generally given by thermionic emission over the barrier

$$\mu_{GB} = \mu_{GB0} \exp\left(-\frac{E_B}{kT}\right) \tag{5.9}$$

where μ_{GB0} usually depends on the grain size L, the carrier concentration, but only slightly on temperature.

5.3.4 Capacitance-Voltage measurement as a tool for understanding the trapping mechanisms

It is well-known from the inorganic semiconductor field that the capacitance-voltage measurements on Metal-Oxide-Semiconductor (MOS) capacitors can provide information on the trapping mechanisms [19] [23] and help quantify this phenomenon. The Metal-Insulator-Semiconductor (MIS) capacitors are also employed as a powerful tool for studying organic materials properties [24] [25] [26] [27] [28]. In the MIS structure, the capacitance is modeled as a serial connection of the dielectric capacitance and the capacitance of the semiconducting layer. The measured capacitance approaches the capacitance of the pure dielectric whenever charges are attracted to the interface between the semiconductor and the dielectric. We can observe hole accumulation when an increase of capacitance at negative bias voltages is measured and vice versa for electron accumulation at positive bias voltages. When an ambipolar small molecule or polymer blend is employed as a semiconductor layer, the combination of these two behaviors will be measured: a charge accumulation will occur for both positive voltages (indicating the presence of electrons) and negative voltages (indicating the presence of holes).

According to the standard Schottky-Mott analysis [19] [23] we can extract the doping density (or more pertinently the concentration of localized charges) from the relationship:

$$\frac{\partial\left(1/C^2\right)}{\partial V_g} = \frac{2}{q\varepsilon_0\varepsilon_s N_A A^2} \tag{5.10}$$

where C is the capacitance in the depletion region, Vg is the gate bias, ε_0 is the vacuum permittivity, ε_s is the relative semiconductor permittivity, A is the area of the device, N_A is the concentration of localized charges. Here, the localized charge refers to the charge that cannot respond at the speed of the test signal used for the measurement of the capacitance. The localized charge cannot be emitted within the time of testing, i.e., within the period of the high-frequency testing voltage. Therefore, the value of N_A is representative for the concentration of the localized charges, which react too slowly to respond at the testing frequency.

When interfacial trapping mechanism occurs the ideal model of the semiconductor and dielectric capacitors in series does not hold anymore [27] [28] and a further capacitor in parallel with the gate insulator capacitor must be taken into account. This capacitor explains why values higher than the ones measured on the only insulator capacitance were carried out on MIS structures at low frequencies.

Last but not least, the presence of interfacial trap states is able to modify the shape of the ideal C-V curve and create pronounced hysteresis effects between the back and the forth branch of the measured capacitance values. In particular, the amount of trapped charge at the interface can be estimated by

$$N_{it} = C_{ins}\Delta V_{FB}/qA \qquad (5.11)$$

where C_{ins} is the insulator capacitance, q is the electronic charge, A the device area and ΔV_{FB} is the variation on the flatband voltage between the back and the forth curve branch.

In addition to that, it should be pointed out that a clockwise hysteresis (starting from negative bias voltages) indicates an interfacial electron trapping, whereas an anticlockwise hysteresis indicates an interfacial hole trapping.

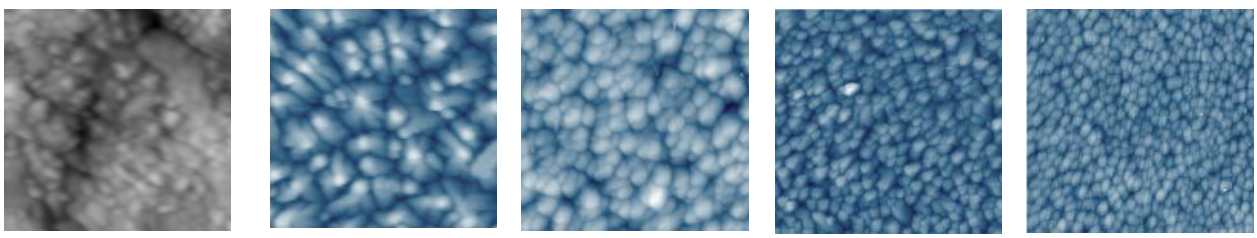
Moreover, dynamic C-V measurements (C-V measurements done with varying the frequency) can help estimate the so-called characteristic frequency f_c that is the frequency after which the curve abruptly decreases indicating the relaxation time [$\tau_R=1/(2\pi f_c)$] of the charge carriers in the device.

5.4 Correlation between semiconductor morphology and gate dielectric

It is generally accepted that the gate dielectric surface roughness is an important parameter affecting OTFT electrical performance [29] [30], and it was shown that rougher gate dielectric surfaces result in smaller pentacene grains and lower OTFT carrier mobilities [31]. Note that several groups have explored correlations between pentacene grain size (tuned by varying film deposition rate, substrate temperature) and charge mobility, with most reporting increased mobility with increased pentacene grain size, although many aspects remain controversial [32] [33] [34]. Surface properties, i.e. surface energy and surface roughness, of a dielectric layer represent distinctive factors which determine potential improvements in electric characteristics of OTFTs because they strongly affect the pentacene growth. In particular, the more hydrophobic is the surface, the bigger will be the grains. Pentacene films grown on hydrophobic surfaces do not give place to good electrical performances [2].

Further research [35] [36] stated that the roughness of the dielectric has a distinct influence on the morphology and structural properties of pentacene films whereas more recent studies [37] indicate that the ordering of pentacene molecules increases significantly on certain surfaces even if these surfaces have higher rms roughness than others.

By comparing Atomic Force Microscopy images of pentacene grown on the gate insulators here studied (Figure 5.12), we observed significant differences in the grain sizes that could affect the bulk transport and the device performances shown in paragraph 5.2 where the average electrical parameters extracted through FET measurements have been reported.



(a) (b) (c) (d) (e)

Figure 5.12 Atomic Force Microscopy images (3,5μm x 3,5μm) of pentacene grown on (a) PDMS (b) PVP (c) cross-linked PVA (d) PVA and (e) pMSSQ from bigger, left, to smaller grain size, right.

Even though the biggest grains have been grown on PDMS surface, no appreciable (low current) field-effect dependent curves were measured due to the high leakage currents caused by pinholes through the dielectric bulk. Moreover, no clear correlation between grain size and electrical performances was found yet when using pMSSQ as a top-layer gate insulator on PVP because it shows quite high mobilities and low threshold voltages despite the smaller pentacene grain size taken on its surface. Transistors employing pMSSQ exhibit better electrical behavior than those with PVA, that shows bigger pentacene grains.

Moreover, a general consideration on surface energy/hydrophobicity (see Table 5.1) and recorded mobility could be attempted because when the surface energy is high, the grains are expected to be larger.

Hydrophobicity ↑ ↓ **Surface Energy**

	Contact Angle
PDMS	105°
pMSSQ	98°
PVP	75°
PVA	45°

Table 5.1 Average contact angle values for each spin-coatable dielectric tested

This correlation is confirmed for each dielectric except for pMSSQ: going from the highest (PDMS) to the lowest (PVA) hydrophobicity value the pentacene grains dimension decreases, giving rise to a consequent lowering of the intergrain trap sites density.

Higher mobility and small V_{th} were measured on PVP FET: this can mean that lower energy surface and bigger grain size enhance transport and transistor performances.

pMSSQ on PVP exhibits small V_{th} even though it has small pentacene grains size and mobility values higher than PVA that has bigger grain size: this can be due to the lowest leakage current that in the former case (double dielectric layer pMSSQ on PVP) was smaller than in the latter.

Small drain current (not shown here) were measured (for the same voltage range employed on the other dielectrics) on PDMS FET due to a huge leakage through the dielectric.

A further point: mobility values are higher in lower rms roughness dielectrics but this trend is not completely confirmed for pMSSQ because $\mu_{\mathbf{pMSSQ}}$ was larger than $\mu_{\mathbf{PVA}}$ and again this fact can be ascribed to a higher leakage.

Anyway, this picture is not enough clear for explaining for instance why we did measure ambipolar behavior on PVA while no evidence for that was found on both cross-linked PVA and PVP. This reflections will be subject of the next paragraph.

5.5 Correlation between chemical-physical nature of the interface and electrical behavior

Although the nature of interface traps is doubtless dependent on intricate microstructural details of the interaction between the semiconducting and dielectric layers, the interface trapping can be better understood also from a chemical perspective.

In particular, since the paper written by Chua et al [1], a lively discussion has arisen about the possibility to obtain ambipolar transport in organic semiconductor layers despite the unfavorable energetics between source and drain contacts and the device channel. As a matter of fact, two mechanisms, namely carrier injection and carrier trapping concur to determine the density of carrier in the channel, and the point is to establish which one prevails. Chua et al. reported measurements which demonstrate that charge trapping plays the main role: transistors with relatively high carrier injection barriers for electrons may show n-type transport, while in devices with low electron injection barriers, no n-type transport may be observed. Therefore, they propose that the key factor is not the injection barrier height but the presence of electron trapping sites on the surface of the insulating layer and, in particular, of hydroxyl groups that are abundant, for instance, on the surface of Silicon Dioxide, that is typically employed as gate insulating layer in OFETs. These groups seem to act as efficient electron traps, so all measurements reported by Chua et al. on devices made on hydroxyl-free dielectrics showed ambipolarity also in the case of unfavorable value of the electron injection barrier (i.e. for high work function metals).

Thus, apparently, the use of trap-free insulating materials for realizing OFET should ensure to obtain ambipolar transport, and, on the opposite, hydroxyl-terminated insulating layers should show efficient electron trapping and therefore, no n-type transport. The last statement has been contested in particular by Singh et al. [3]. Singh et al. demonstrated that the presence of electronegative hydroxyl group on the surface of the insulating layers may be irrelevant for determining the ambipolarity of OFETs: in particular they show that

transistors with PVA dielectric layers (OH-terminated) are ambipolar, while when PVA is replaced by PVP (OH-terminated as well), the n-type transport is completely suppressed.

In order to have a deeper insight on this debate, we studied and compared the electrical properties of two very similar dielectric layers: PVA used as it is and cross-linked PVA, where cross-linking is obtained by means of Ammonium Dichromate (PVA/AD).

Ambipolar behavior in organic semiconductors can be studied both in OFET and in Metal-Insulator-Semiconductor (MIS): in the last case, it can be observed by capacitance - voltage measurements as previously stated above. C-V measurements can give information about the carrier density, while Id-Vd and Id-Vg curves also provide information about carrier mobilities.

As can be seen in Fig.5.13, a device based on a PVA dielectric layer has the typical behavior also observed in inorganic MIS capacitors, symmetric with a minimum around 10-15 V. The main difference lies in the fact that the two branches of the curves (on the left and on the right of the minimum) are due to accumulation of charges, holes in one case (on the left) and electrons in the other case (on the right) No carrier population inversion is possible in organic semiconductors.

Figure 5.13 also shows a typical C-V curve of a MIS structure based on a PVA/AD dielectric. In the case of PVA/AD and PVP, we never observed any n-type branch, indicating that no electron accumulation occurs.

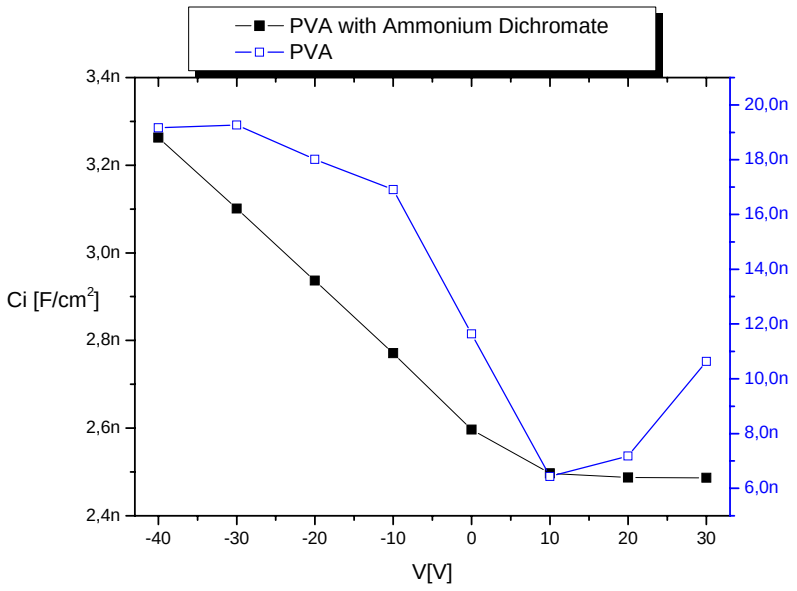


Figure 5.13 Capacitance-Voltage plots recorded on PVA and cross-linked PVA MIS structures

Coherently, we never observed n-type behavior in OFETs based on PVA/AD and PVP while we could detect it in PVA devices, as shown in Figure 5.14.

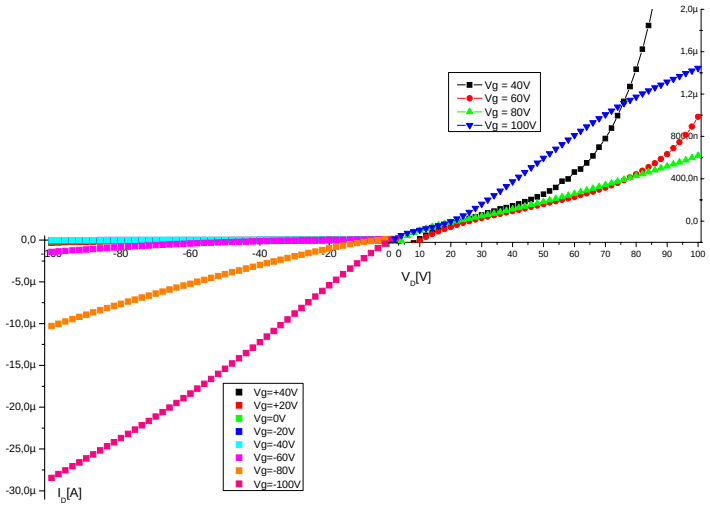


Figure 5.14 Output characteristic measured on FET devices using PVA as the gate dielectric: a marked n-type behavior can be observed for positive drain and gate voltage values

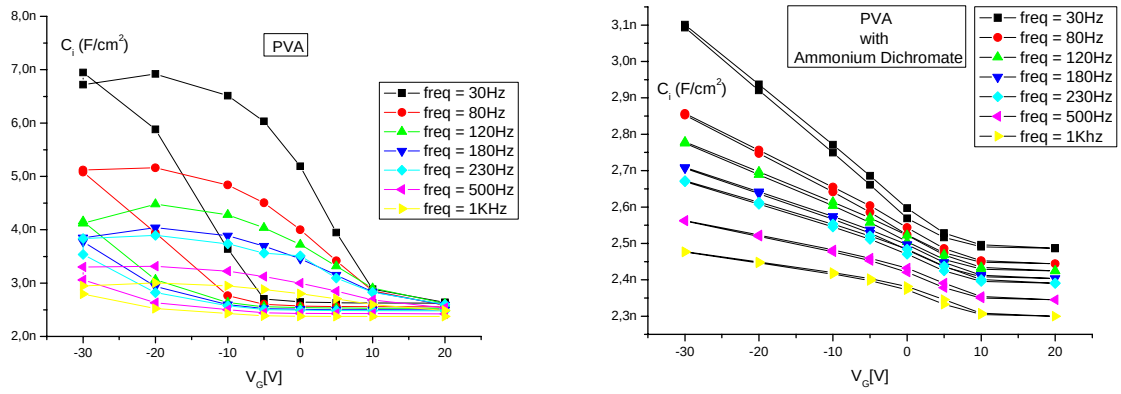
The high Vg needed to activate n-type transport is in good agreement with the high bias values required to observe the n-type branch in C-V curves of MIS based on PVA (figure 5.13).

Table 5.2 reports the values of electrical parameters recorded in PVA, PVA/AD and PVP devices:

	PVP	**PVA/AD**	**PVA**
μ ($cm^2/V*s$)	$3.4*10^{-1}$	$3.5*10^{-2}$	$1.5*10^{-2}$
$\mathbf{V_{TH}}$ (Volt)	-5	-12	-25
$\mathbf{I_{ON}/I_{OFF}}$	10^4-10^5	10^3-10^4	10^2

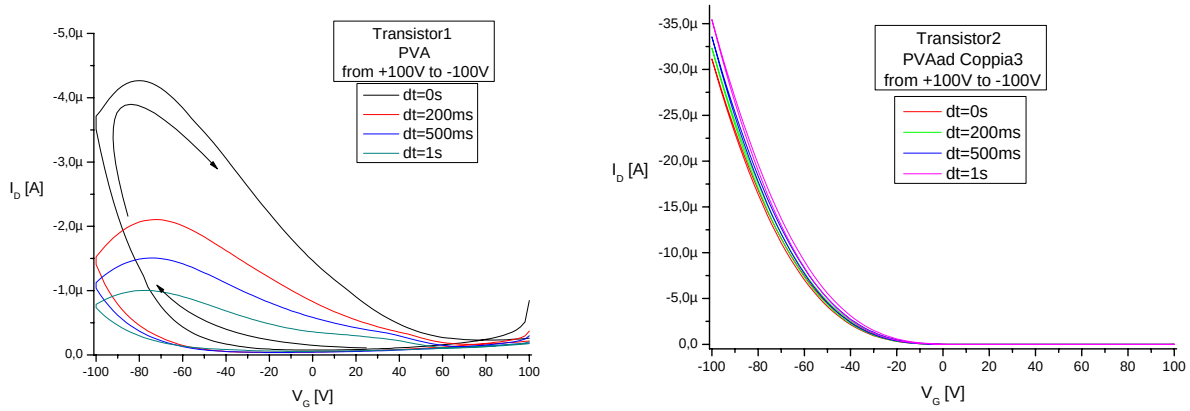
Table 5.2 Electrical parameters recorded on transistors with PVP, PVA/AD and PVA as the gate dielectric

C-V curves as a function of frequency (figure 5.15) and Id-Vg curves (figure 5.16) show an interesting behavior concerning charge trapping and hysteresis. The dependence of C-V curves on the measurement frequency can be observed in fig. 5.15a, where the capacitance decreases with increasing measurement frequency. This behavior is not observed in inorganic MIS but it has been reported for organic MIS structure where mobile charges that can follow the test signal if it varies at low frequencies, may not be able to respond at higher frequencies thus acting as trapped charges.



(a) (b)

Figure 5.15 Capacitance-Voltage measurements with varying frequency on (a) PVA and (b) PVA/AD MIS (gold/dielectric (a) or (b)/pentacene) structure.



(a) (b)

Figure 5.16 Trans-characteristics with varying delay time measured on (a) PVA and (b) PVA/AD FET

Our results show that the capacitance starts to decrease at test frequencies that are very low if compared with standard inorganic MIS structures, thus indicating that the charge carriers in the organic semiconductor have a long relaxation time, possibly caused by a slow response of the trap states, likely to be deep states with long time constants [27] [24].

PVA-based devices show a very evident hysteretic behavior that: (i) decreases with decreasing frequency (with increasing delay times in Id–Vg curves); (ii) has a clockwise loop. On the contrary, PVA/AD based devices show a negligible hysteresis in the range of frequencies/times used for our measurement.

The hysteretic behavior of C-V and Id -Vg curves is normally considered one of the effects of charge traps that, in a certain voltage range (dependent on the type of majority carrier)

subtract carriers to the transport and in another voltage range re-emit carriers thus increasing the current [38].

As already reminded, PVA is an hydroxyl terminated dielectric, while it has been demonstrated that PVA/AD is mainly ketone-terminated [7]. Ketone groups are known to be more effective electron traps than hydroxyls [2]. Therefore, the interface chemistry indicates that in both cases electron traps could play a major role and that, possibly, electron trapping should be even more efficient in PVA/AD based devices. This is confirmed by the C - V and Id - Vg curves (figure 5.15 and 5.16) that can be easily interpreted under this hypothesis.

In fact, in the case of PVA (Figure 5.5 (a)), electron traps act by subtracting electrons in the n-type branch but also, passing from positive to negative voltages, re-emit electrons which recombine with holes, thus decreasing the current. By increasing again the voltage, after all electrons are re-emitted, the hole population is no more influenced by the presence of electrons that are trapped as soon as they enter in the channel and the current is higher. This explains the clockwise hysteresis loop observed in the Id-Vg and C-V curves that indicates negative charge injection into the semiconductor layer followed by trapping [24]. On the other hand, if we assume that in PVA/AD devices electron traps are much more effective than in PVA, as suggested by the chemistry of ketone and hydroxyl groups, we understand why we do not observe an n-type behavior in PVA/AD OFET devices and the n-type branch in C-V curves in completely flat (Figure 5.2): the injected electrons are immediately trapped and no more re-emitted (at least in time frame of our measurements) with a process similar to what has already been observed in P3HT-based TFTs [39]. C-V and Id-Vg curves of MIS structures based on PVA/AD (Figure 5.15b and 5.16b) are also in good agreement with his hypothesis since we cannot detect any relevant hysteresis loop. This observation excludes the occurrence of trapping and emission of carriers within the timeframe of the measurements and indicates that electrons are trapped, cannot be re-emitted and cannot recombine with holes.

As a result, OFET devices based on PVA/AD show no n-type transport but, on the other hand, a more ‘ideal” p-type behavior. We have observed a very similar behavior in the case of PVP based devices [40] that show an “ideal” p-type behavior and no n-type transport (see Table 5.2). In the case of PVP, that is OH-terminated like PVA, this behavior can be explained considering the structure of the whole molecule: the aromatic ring of PVP in fact

tends to better confine electrons inside the ring, thus reinforcing the effect of the hydroxyl group and justifying a significantly longer re-emission time, comparable to the one we observe for PVA/AD.

In conclusion, our measurements support Chua's hypothesis, i.e. that the insulator/semiconductor interface is the main responsible of the ambipolar behavior due to the presence of electron trap sites on the surface (for instance hydroxyl groups), and, in this framework, offer a simple and consistent explanation also for the results obtained by Singh et al, on PVA and PVP that have both hydroxyl terminated surfaces. In addition, we have demonstrated that the presence of very efficient electron traps on the dielectric surface can play a positive role, as the p-type branch of the current curves are positively influenced by the presence of efficient electron traps.

It is obvious that in order to obtain ideal ambipolar device in organic transistors, one should eliminate both electron and hole traps from the dielectric surface, but to optimize the behavior of a p-type transistor, it is advisable to employ a dielectric with very efficient electron traps on the surface. The traps emission time actually determines a lower cut-off frequency of the device, while the upper cut-off frequency is strictly related to the hole mobility.

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Chapter6

Application of OTFTs to chemical detection in liquid solutions

Pros and cons of using organic materials have been already discussed here in this work: they can be easily processed and deposited leading to rapid prototyping processes that are time-saving and low-cost. In addition to that, the infinite possibilities of new applications dictated by the chemical tailoring of such materials would make them really promising. On the other hand, the low mobility values achieved so far together with the strong interaction with the environment that damages them still refrain them from going to the market place.

However, to fully profit of the whole potential of these materials without being limited by these drawbacks, it is necessary to focus on those applications where high performance in terms of switching speed is not required and environmental sensitivity can be an advantage.

In this chapter a brief overview of what is in literature on organic-based chemical sensors will be given. Starting from a deep insight into the Ion-Sensitive FET (ISFET) and its organic version, namely the Ion-Sensitive Organic FET (ISOFET) and some other examples we will then examine the Charge-Modulated FET working principles useful to understand the Charge-Modulated Organic FETs which have been part of this thesis work and whose experimental results will be eventually shown and discussed.

6.1 ISFET and ISOFET devices

The Ion-Sensitive FET (ISFET) is a sensor able to detect the H+ ions concentration and consequently the pH of an aqueous solution through the interaction between the solution and an insulating layer (generally Si_3N_4 or SiO_2) deposited or grown onto a semiconductive substrate.

The ISFET structure is close to that one of a MOSFET where the gate metal is substituted by the electrolyte/reference electrode system. In this way the insulating layer is directly in contact with the electrolytic solution to be analyzed (Figure 6.1) [1]. The reference electrode polarizes the interface and its potential difference with respect to the solution is fixed and does not vary with the pH of the solution.

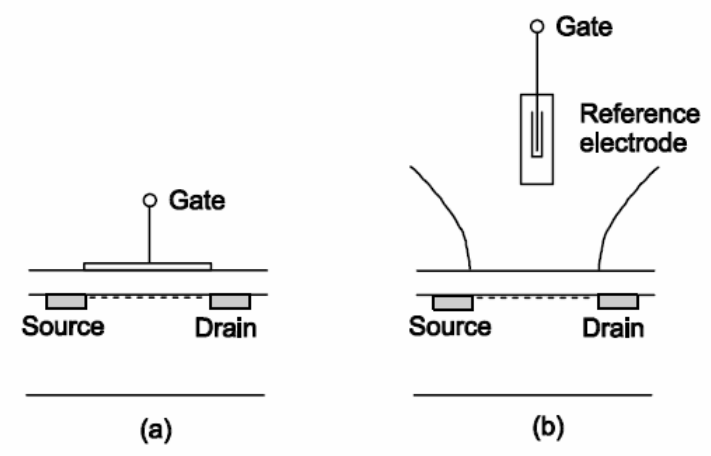

Figure 6.1 Comparison between (a) MOSFET structure and (b) ISFET structure

The ISFET working principle relies on the insulating layer ability to generate an interfacial potential with the solution depending on the ion concentration of the solution itself. The variation is around 25 mV per pH unit for SiO_2 and 59 mV per pH unit for tantalum pentoxide (Ta_2O_5). This variation is responsible for a variation on the drain current of the device.

A more detailed scheme of the ISFET device is shown in Figure 6.2:

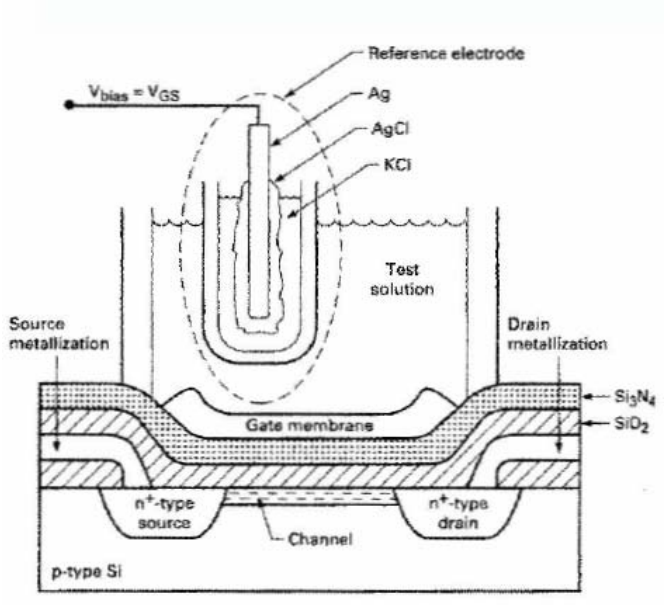

Figure 6.2 More detailed scheme of an ISFET device

The Ag/AgCl reference electrode ensures a constant potential drop with respect to the solution.

In order to explain the potential dependence at the oxide surface on pH, a so-called *site-binding* model (Fig. 6.3) has been developed.

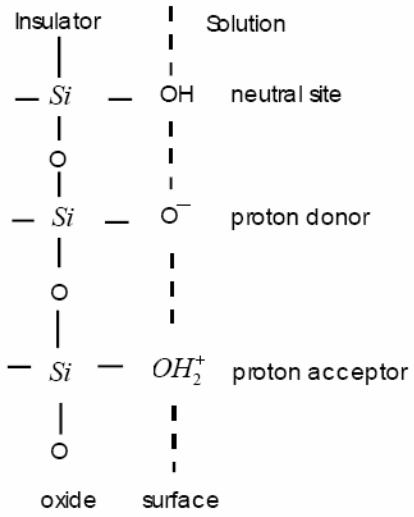

Figure 6.3 Schematic representation of the site-binding model

This model is based on the interaction of the surface groups on the insulator (sites) with the ions contained into the solution (H^+). These sites have a specific density depending on the insulating oxide layer and can have acid, basic or amphoteric (ability to react as either an acid or base) behavior.

In this model, a superficial charge distribution occurs due to the formation of chemical groups. Let us take the silicon dioxide as an example. The following reactions take place:

$$SiOH \overset{k_a}{\Leftrightarrow} SiO^- + H_S^+ \quad ; \quad SiOH + H_S^+ \overset{k_b}{\Leftrightarrow} SiOH_2^+ \tag{6.1}$$

Where the relations on the equilibrium constants are respectively:

$$k_a = \frac{[SiO^-][H^+]_s}{[SiOH]} \quad ; \quad k_b = \frac{[SiOH_2^+]}{[SiOH][H^+]_s} \tag{6.2}$$

From which the superficial proton concentration can be deducted as a:

$$[H^+]_s = \sqrt{\frac{k_a}{k_b}\frac{[SiOH_2^+]}{[SiO^-]}} \tag{6.3}$$

When the surface is neutral, the concentration of negative and positive groups are equal and consequently

$$[H^+]_s = \sqrt{\frac{k_a}{k_b}} \quad \text{that is} \quad pH_s = -\log\sqrt{\frac{k_a}{k_b}} \tag{6.4}$$

that corresponds to the neutrality charge point on the surface.
Let us consider now the total superficial sites concentration that we call N_s:

$$N_s = [SiO^-] + [SiOH_2^+] + [SiOH] \tag{6.5}$$

By correlating the (6.5) with the expressions of k_a e k_b we find:

$$[SiO^-] = N_s \frac{k_a}{k_a + [H^+]_s + k_b[H^+]_s^2} \tag{6.6}$$

$$[SiOH_2^+] = N_s \frac{k_b[H^+]_s^2}{k_a + [H^+]_s + k_b[H^+]_s^2} \tag{6.7}$$

We introduce now the concept of buffer capacity (applied to the surface) as the ratio between the concentration of strong acid or basis to be added to the solution in order to obtain a certain pH variation:

$$\beta_s = \frac{d[B]}{d(pH_s)} = \frac{d[B]}{d[H_s]}\frac{d[H_s]}{d(pH_s)} \qquad (6.8)$$

where

$$[B] = [SiO^-] - [SiOH_2^+] \qquad (6.9)$$

By substituting (6.9) in (6.8) and reminding (6.2), we have:

$$\beta_s = N_s \frac{k_a + 4k_a k_b [H^+]_s + k_b [H^+]_s^2}{\left(k_a + [H^+]_s + k_b [H^+]_s^2\right)^2} 2.3[H^+]_s \qquad (6.10)$$

which means that the buffer capacity increases with both N_S and $k_a k_b$.

At equilibrium conditions, the ionic concentration at the surface is related to the bulk ionic concentration from the Boltzmann law:

$$[H^+]_s = [H^+]_b \exp\left[-\frac{q\varphi_{eo}}{kT}\right] \qquad (6.11)$$

where φ_{eo} is the potential drop between interface and bulk.

By inverting this formula and keeping in mind the pH definition we obtain:

$$\varphi_{eo} = 2.303\frac{kT}{q}(pH_s - pH_b) \qquad (6.12)$$

By recalling the solution of Poisson-Boltzmann equation in the easiest case of just one ionic species, the charge density in the diffused layer according to the following formula and imposing the charge neutrality $\sigma_s + \sigma_d = 0$:

$$\sigma_d = -\sqrt{8kT\varepsilon_0\varepsilon_r c_0}\sinh\left(\frac{zq\varphi_{eo}}{2kT}\right) = -\sigma_s \qquad (6.13)$$

We can define the differential capacity as:

$$C_s = \frac{d\sigma_s}{d\varphi_{eo}} \tag{6.14}$$

From this relationship we can notice that a pH variation in the bulk can induce a pH variation at the surface inducing as a consequence a variation in the φ_{eo} potential:

$$\frac{d\varphi_{eo}}{d(pH_s)} = \frac{d\sigma_s}{d(pH_s)}\frac{d\varphi_{eo}}{d\sigma_s} = -\frac{q\beta}{C_s} \tag{6.15}$$

The relationship (6.15) states that the bigger is β and the smaller is C_s the bigger will be the variation of the potential φ_{eo} with the pH. By using (6.12) we then obtain:

$$\frac{d\varphi_{eo}}{d[pH]_b} = 2.303\frac{kT}{q}\left(\frac{d[pH]_s}{d[pH]_b} - 1\right) = 2.303\frac{kT}{q}\left(\frac{d[pH]_s}{d\varphi_{eo}}\frac{d\varphi_{eo}}{d[pH]_b} - 1\right) \tag{6.16}$$

and,

$$\frac{d\varphi_{eo}}{d[pH]_b} = \frac{2.303\frac{kT}{q}}{2.303\frac{kT}{q}\frac{d[pH]_s}{d\varphi_{eo}} - 1} = -2.303\frac{kT}{q}\frac{1}{2.303\frac{kT}{q^2}\frac{C_s}{\beta_s} + 1} = 2.303\frac{kT}{q}\alpha \tag{6.17}$$

Where the number α ranges from 0 to 1 according with β and C_s values. This relationship states that pH sensitivity for a certain oxide is equal to 2.3 kT/q at the maximum.

The potential φ_{eo}, which is found to be pH dependent, affects the electrical parameters of the FET. It is well known from the MOSFET theory that the threshold voltage V_T is related to the flat band voltage V_{FB}. These last two parameters, related to the drain current variation, are related to pH variations.

With this in mind, let us consider the whole structure including the Ag/AgCl electrode, which will be given by:

Metal / Reference Electrode / Electrolyte / Oxide / Semiconductor / Metal.

The flat band voltage V_{FB} is the voltage to be applied to the metal (in this case to the reference electrode) to make null the potential at the interface with the semiconductor:

$$V_{FB} = (E_{ref} - \varphi_{lj}) - (\varphi_{eo} - \chi_e) - \frac{\Phi_{Si}}{q} - \frac{Q_0}{C_{OX}} \qquad (6.18)$$

where E_{ref} is the reference electrode potential referred to the vacuum level, φ_{lj} is the potential difference (*liquid-junction*) between the reference solution and the electrolyte, φ_{eo} is the potential drop in the electrolyte at the interface with the insulating oxide, χ_e is the dipole surface potential in the solution, Φ_{Si} is the semiconductor work function, C_{ox} and Q_0 are respectively the oxide capacitance and charge per unit area.

The ISFET threshold voltage V_T^*, i.e., the voltage that is to be applied to the gate electrode in order to induce an inversion channel at the semiconductor surface, can be deduced by the the threshold voltage V_T of the corresponding MOSFET by adding the potential drops related to the additional interfaces in the whole structure. In other words, it holds that:

$$V_T^* = V_T + E_{ref} + \varphi_{ij} + \chi_e - \varphi_{eo}(pH) - \frac{\Phi_m}{q} \qquad (6.19)$$

where Φ_m is the work function of the metal in contact with the semiconductor.

In conclusion we can say that the ISFET threshold voltage depends on the pH or, in other words, on the H^+ ions concentration in the solution through the $\varphi_{eo}(pH)$ term.

In analogy with the MOSFET equations, the drain current is function of both V_{GS} e V_{DS} and can be expressed as:

$$I_{DS}(pH) = K\left(V_{GS} - V_T^*(pH)\right)V_{DS} \qquad (6.20) \qquad \text{for the linear regime;}$$

$$I_{DS}(pH) = K\left(V_{GS} - V_T^*(pH)\right)^2 \qquad (6.21) \qquad \text{for the saturation regime.}$$

These equations state once again that the ISFET device can be employed as a pH sensor since by varying the H^+ ion concentration in the solution the threshold voltage V_T^* varies inducing at the same time variations in the measured drain current.

When an organic material is employed as the active layer or the insulating layer for the same structure, we call this *Ion-Sensitive Organic Field Effect Transistor* (ISOFET).
In 2000 Bartic et al. [2] came up with an ISOFET device employed as a pH sensor. In their structure, regio-regular poly(3-hexylthiophene) (rr-P3HT) acts as the active layer. The modulation of the rr-P3HT conductivity occurs through the surface potential fixed by an ionic solution in contact with an oxide H^+-sensitive area. The device structure is shown in Fig. 6.4.

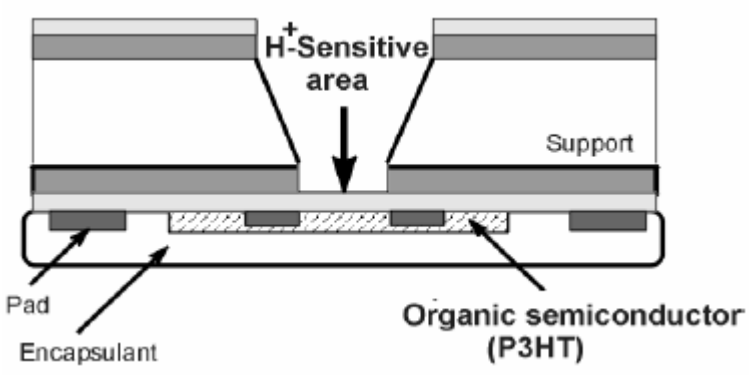

Figure 6.4 Schematic cross-section of the ISOFET device employed by Bartic et al. [3]

The pH variations in the solution in contact with the insulating layer modify the voltage drop at the oxide/semiconductor resulting into a modification of the electrical parameters of the device. The sensitivity to the H^+ ions in such a system is due to the oxide layer exposed to the solution, i.e., silicon nitride (Si_3N_4) that has two specific groups able to protonize: the silanol group (SiOH) and the amino-silane group ($SiNH_2$) both responsible for the surface potential generation. The following reactions take place at the insulator/electrolyte interface:

$$\begin{aligned} SiOH &\Leftrightarrow SiO^- + H^+ \\ SiOH + H^+ &\Leftrightarrow SiOH_2^+ \\ SiNH_2 + H^+ &\Leftrightarrow SiNH_3^+ \end{aligned} \qquad (6.22)$$

which express the amphoteric behavior of the silanol group and the protonation typical in the amine group.
As shown previously when dealing with the ISFET device, the reference electrode here acts as the gate electrode for the MOSFET device.

A silicon wafer with a thickness of 650 µm was used as the mechanical support for the organic transistor. To expose the gate insulator to the solution, a window was anisotropically etched in the silicon. After etching, the resulting device structure is very frail even if the thickness of the sensitive layer has been chosen in order to ensure low mechanical stress. However, the fact that the sensitive area and the electrical contacts are on opposite sides of the insulating layer is very convenient from the packaging point of view. In fact, the device can be encapsulated with a room temperature curable epoxy resin and the semiconductor is therefore protected from the environment and the solution to be monitored.

In order to test the pH response, the transistor was immersed into buffer solutions having different pH values (2, 4, 6, 7, 8, 10). The reference electrode acts as usual as the gate electrode for the transistor. In this case, the gate voltage will be provided by a constant term (V_{ref}) plus a further term associated to the solution/insulator interface potential which depends on the proton concentration, as previously described for the site-binding model.

The sensor was biased as a FET device in common source configuration as shown in the following (Figure 6.5).

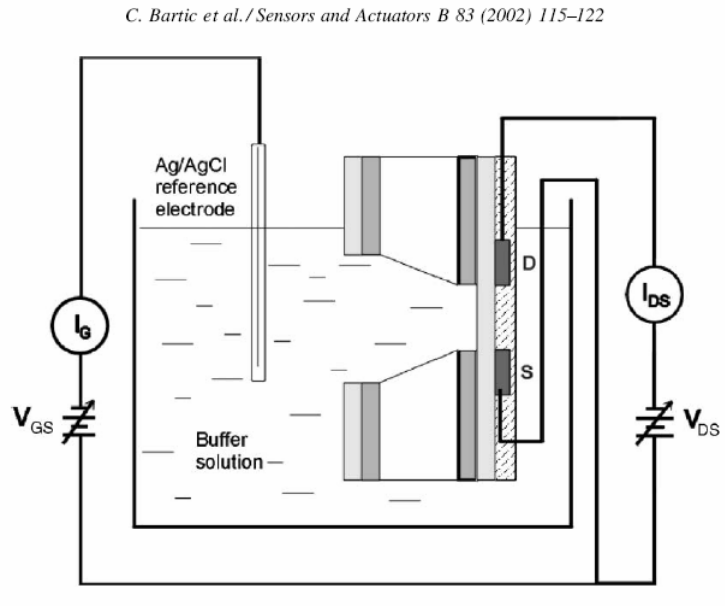

Figure 6.5: Cross-section of the measurement set-up [2]

For the purpose of monitoring both the time response and the stability of the drain current vs. time was measured while keeping V_{DS} e V_{GS} to constant voltage values.

When a potential variation $\delta\psi$ at the interface occurs, a charge variation will be generated according to:

$$\delta Q = C_i \delta\psi \qquad (6.23)$$

where C_i is the oxide capacitance.

Due to the pH variation, the electrical charge into the channel will increase or decrease proportionally to the site activity presented in (6.22).

The drain current variation will be:

$$\delta I_{DS} = \left(\frac{W}{L}\right) \mu C_i V_{DS} \delta\psi \qquad (6.24)$$

where μ is the mobility due to the charge variation.

The description of the threshold variation with the pH is not easy because the band model assumption from where V_T^* came out, that holds for the inorganic semiconductors, here is no longer valid. Although the electrochemical phenomena at the oxide/solution interface are the same considered for the classic ISFET device physics in this case the transport properties of the organic semiconductors are different and thus are able to sense differently pH variations. Bartic et al. experiments showed that for these drain and gate voltages (V_{DS}=-10V, V_{GS}=-2V), the drain current varies linearly with the pH and the measured sensitivity was approximately 25 nA per pH unit.

Another example of ISOFET employing P3HT as the active layer is shown in Fig. 6.6 and presented by Gao et al. [3].

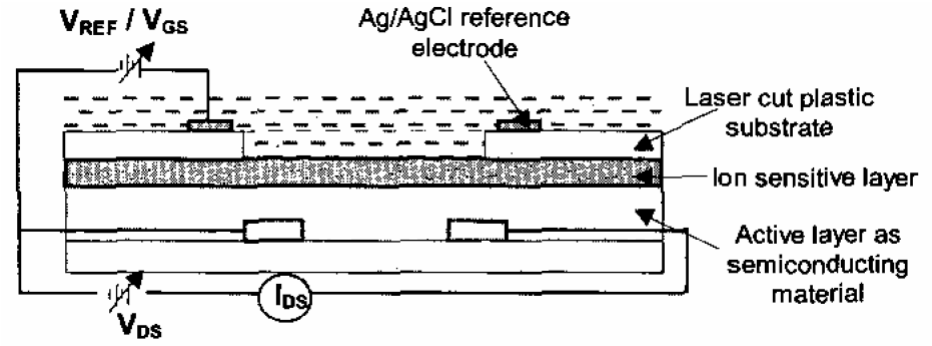

Figure 6.6 Schematic cross-section of the ISOFET used by Gao et al. [3]

Differently from the Bartic's ISOFET device, this one is assembled on a plastic substrate (it is the very bottom layer in the figure) and they call it *polymer*-FET. The sensitive oxide was the tantalum oxide (Ta_2O_5) that showed a more pronounced sensitivity to the pH. The device was provided with a microfluidic system (not shown in this figure) in order to drive the solution right to the sensitive area as well as to the reference electrode. The authors state that this device might be integrated into a more complicated lab-on-chip system.

The sensitivity to the pH (measured as usual as a variation on the drain current) was found to be around 360 nA per pH unit.

Loi et al. [4] proposed a further model of ISOFET (Fig. 6.7) using a lightweight, flexible and substrate-free structure. In fact, a 900nm thick Mylar® foil (adapted to a plastic frame) was used as the dielectric and at the same time as the mechanical substrate for the whole structure.

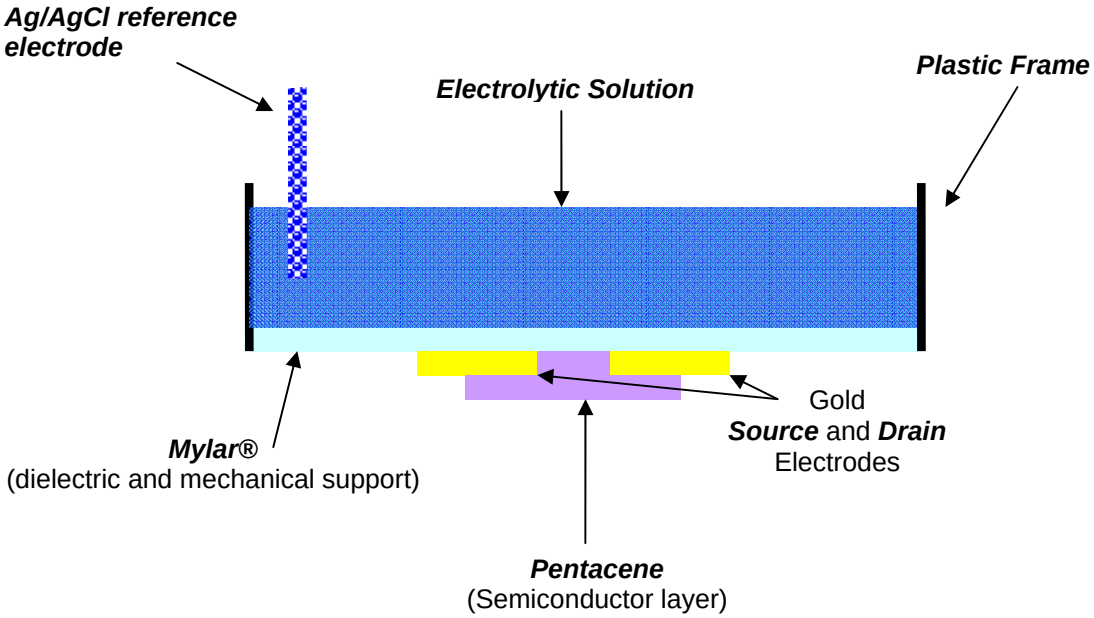

Figure 6.7: Schematic cross-section of the ISOFET used by Loi et al.

The working principle is similar to other ISOFETs described here with the obvious differences due to the employed materials. In particular while the electrochemical phenomena occurring at electrolyte/inorganic dielectric interface are well known, a site-binding model that explains in detail the mechanism at the surface for the Mylar foils has not been developed yet. However, the sensitivity of the device to the pH variation has been demonstrated [4] into a nA range variation.

6.2 CMFET and CMOFET

An ion sensitive FET can be made sensitive to other ionic species, different than H^+, by chemically drafting suitable chemoreceptor on the surface of the insulating layers. This has been done in silicon technology by covalently linking silane-terminated molecules to silicon dioxide. In organic devices, if the insulating layer is not an oxide, this strategy cannot be applied. The chemical functionalization of a metal is a much easier task than grafting molecules on polymeric surfaces. As an example, well known processes such as thiol self-assembly could be very easy to apply to this kind of device structure. Therefore, one of the possible developments of the ion-sensitive strategy for organics concerns the development of floating gate devices similar to those reported previously [5] [6], first realized in our lab using CMOS technology. A Charge Modulated FET (CMFET) can be employed to detect

changes of electric charge without the need for any external components (e.g. an external reference electrode). The schematic of this device is shown in Fig. 6.7. Both the control-capacitor and the charge immobilized on the active area will determine the actual gate voltage drop of the transistor. The final voltage will be due to the combined action of these two parameters and will determine the drain current flowing in the transistor channel. Besides the elimination of the external electrode, another interesting feature of this structure is that the control gate allows one the ability to address a single device in an array rather than switching-on all devices with a common reference electrode. This is very important for practical purposes, for example in the case of sensor arrays for the detection of DNA hybridization or any other biomolecular process involving a change in electric charge (antigen/antibody interaction, proteomics, etc) immobilized on the sensing gate of the device [6] [7].

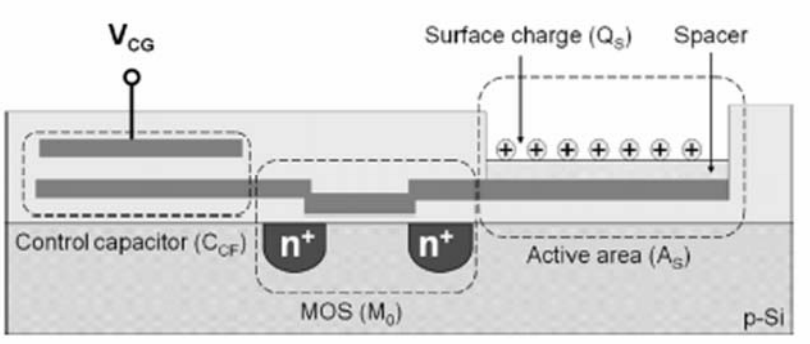

Figure 6.8: Structure of an ion- sensitive organic field effect floating gate device for chemical sensing [5]

The CMFET device consists of a floating-gate transistor (called M_0, in figure), a control-gate that acts as a reference electrode (kept at the potential V_{CG} with respect to the substrate) and an active area where charge induction takes place (A_S).

In this device the drain current will be modulated by the drain voltage, the control-gate and the immobilized charge on the active area.

By considering only the active area, the surface charge immobilized (Q_s) on the metallic pad generates an electric field that allows a charge separation by inducing a charge Q_i on the upper side of the floating-gate and consequently a charge $-Q_i$ on the opposite side (Fig. 6.9).

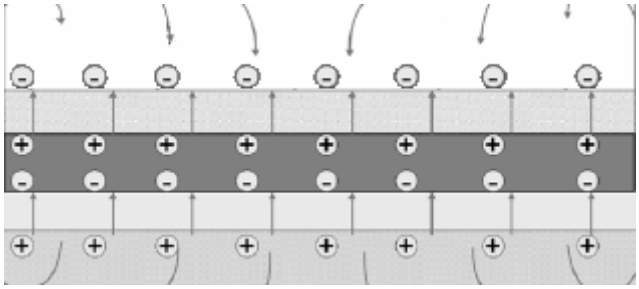

Figure 6.9: Charge separation on the floating-gate due to the presence of charge on the active area

Let V_{FG} be the voltage drop between the floating gate and the silicon substrate and C_{CF} the capacitance value of the parallel-plate capacitor formed by the overlap between control-gate and floating-gate (thus depending on both the oxide thickness and the gates overlap area A_{CG}). The principle of charge conservation states that the total amount of electrical charge on the floating-gate must be constant so we can write:

$$Q_{F0} = Q_i(Q_S) + Q_{CCF} + Q_{CFB} = Q_i(Q_S) + C_{CF}(V_{FG} - V_{CG}) + C_{FB}V_{CG} \qquad (6.25)$$

and consequently V_{FG} is

$$V_{FG} = \frac{C_{CF}}{C_{CF} + C_{FB}} V_{CG} + \frac{Q_{F0} - Q_i(Q_S)}{C_{CF} + C_{FB}} \qquad (6.26)$$

being Q_{F0} the trapped charge into the floating-gate, Q_i the induced charge on the floating – gate by the surface charge Q_S, and Q_{CCF} e Q_{CFB} are the charge contributes due to respectively C_{CF} and C_{FB} capacitors. The (6.27) relates V_{FG}, V_{CG} and Q_S stating that the drain current will be determined by both V_{CG} and Q_S. For floating-gate devices, the sensitivity to external charge contributes is usually modeled as a variation on the actual MOSFET threshold voltage V_{thf}, whose value in this specific case is [5]:

$$V_{thf} \approx V_{th} - \frac{Q_{F0} - Q_i(Q_S)}{C_{CF} + C_{FB}} \qquad (6.27)$$

that, when $Q_i = -Q_s$, can be approximated by (6.28):

$$V_{thf} \approx V_{th} - \frac{Q_{F0} + Q_S}{C_{CF} + C_{FB}} \qquad (6.28)$$

Inspired by the CMFET concept we realized an organic version of such a device (CMOFET) that employs pentacene as the active layer, gold electrodes and moreover is assembled on a free-standing Mylar® film that acts as a dielectric and at the same time as the substrate for the whole structure (Fig. 6.10).

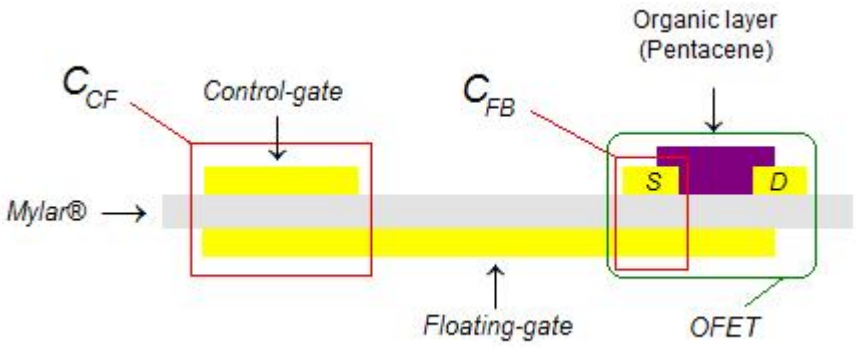

Figure 6.10: Schematic cross-section of an assembled CMOFET

It is evident from Fig. 6.10 that by immobilizing charge on the floating-gate plate a variation on the drain current can be measured. In fact we have been using this device configuration with the purpose of sensing the pH of aqueous solutions put in contact with the floating-gate plate. To do that it is necessary to make somehow sensitive the floating-gate electrode so that the ionic charge can be immobilized on it. In particular, to obtain a pH sensitivity, we functionalized the floating-gate electrode with an aqueous solution of cysteamine (2-Aminoethanethiol) (Fig. 6.11) which is a molecule that thanks to the SH group is able to covalently bond to the gold surface.

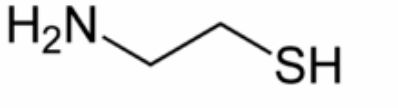

Figure 6.11: Cysteamine or 2-Aminoethanethiol [$NH_2CH_2CH_2SH$]

On the other hand the tail of the molecule, the NH_2 group, is able to protonize when in contact with an ionic solution according to the following chemical reaction,

$$NH_3^+ \underset{k_2}{\overset{k_1}{\Leftrightarrow}} NH_2 + H^+$$

where k_1 and k_2 represent respectively the dissociation and the association constant.
At equilibrium condition, the following relationship holds

$$k_1[NH_3^+] = k_2[NH_2][H^+]$$

From where the ratio between the dissociation and the association constant is:

$$\frac{k_1}{k_2} \equiv K = \frac{[NH_2][H^+]}{[NH_3^+]}$$

where *K* is called equilibrium constant. From the last expression, the H^+ ion concentration can be deduced as:

$$[H^+] = K\frac{[NH_3^+]}{[NH_2]}$$

Or (using co-logarithm of the previous expression):

$$pH = pK - \log\frac{[NH_3^+]}{[NH_2]} = pK + \log\frac{[NH_2]}{[NH_3^+]} \quad (\textit{Henderson-Hasselbach equation}) \ (6.29)$$

By using (6.29) it is possible to calculate analytically the ratio between the amine in its deprotonized and protonized form at a certain pH value:

$$\frac{[NH_2]}{[NH_3^+]} = 10^{(pH-pK_a)}$$

This relationship means that when the pH of the solution where the amine groups are equals their pK, the protonized and deprotonized form have the same concentration This equilibrium point is called isoelectric point (pI). For pH values lower than pI the protonized

form prevails and vice versa when pH is bigger than pI, according to the scheme shown in Fig.6.11.

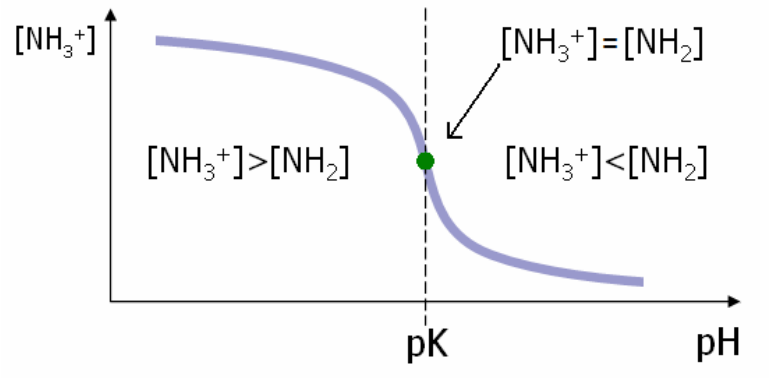

Figure 6.11: A possible graphic interpretation of Henderson-Hasselbach equation in the case of the thio-aminic groups we used over our work

Since we aim at making a pH sensor by using the thio-aminic group we are thus interested in knowing where exactly the isoelectric point is. In fact in the vicinity of the pI the major sensor sensitivity to pH is expected. The determination of the pI can be done through different methods. It can be estimated through contact angle measurements, or better through Electrochemical Impedance Spectroscopy (EIS) measurements whose working principle has been already presented in Chapter 2.

All the measurements carried out on the CMOFET used as a pH sensor will be reported in the following paragraph.

6.3 Measurements results and discussion

In this paragraph are shown and commented the results we obtained from the electrical characterization of the CMOFET device.

In order to characterize the CMOFET device both I_D-V_D and I_D-V_G measurements have been done.

In particular, what we did in order to verify the dependence on the pH was to monitor the variation in the maximum value of the drain current on the I_D-V_D characteristics. In general a certain time was necessary after the deposition of the solution for the stabilization of the measurements. Every time the solution with different pH was changed on the active area, two sets of measurements followed, the former taken 5 minutes after the deposition, the latter taken 20 minutes after the deposition. The time needed to the solution to give a stable output drain current was found to be 20 minutes because by keeping measuring there was no evidence for variations on the output drain current after 20 minutes for each given pH value . In Fig. 6.12 are some I_D-V_D plots measured always in the same polarization conditions but in different moments in time.

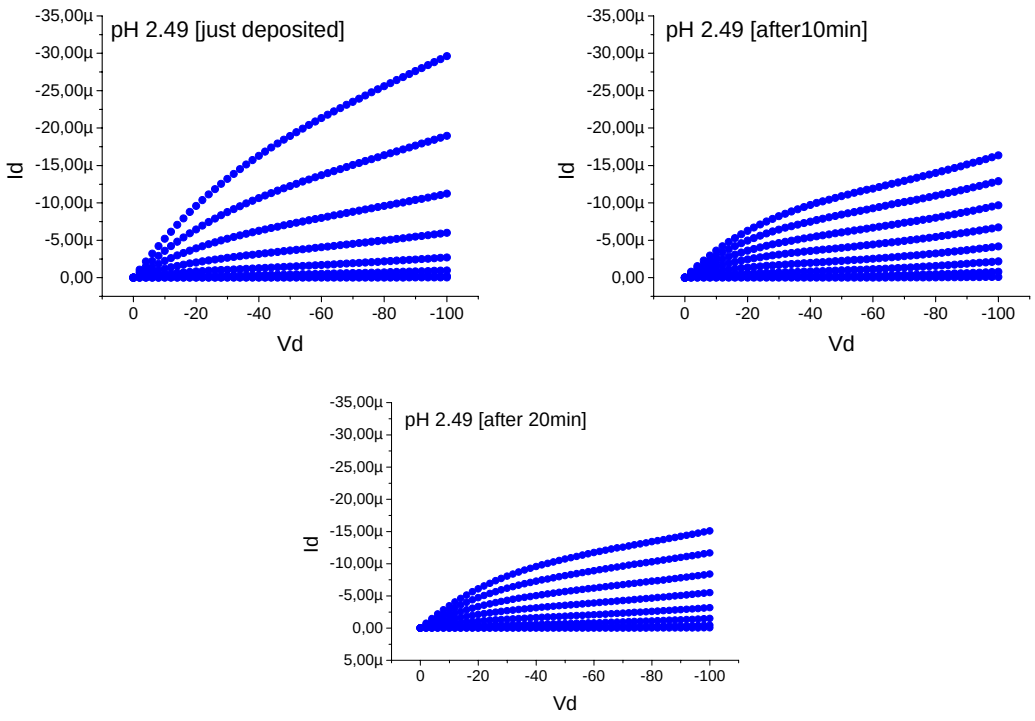

Figure 6.12: Id-Vd characteristics measured at different time instants after the solution deposition at a given pH (in this case 2.49) on the active area. A certain time is needed for the measurement stabilization.

As stated above an issue when dealing with the CMOFET was finding the pH range where the sensor was more sensitive. To do that Electrochemical impedance spectroscopy (EIS) measurements have been performed in collaboration with the Inorganic and Physical Chemistry group of the University of Bologna, Bologna, Italy. The EIS working principle have been previously presented in Chapter 2.

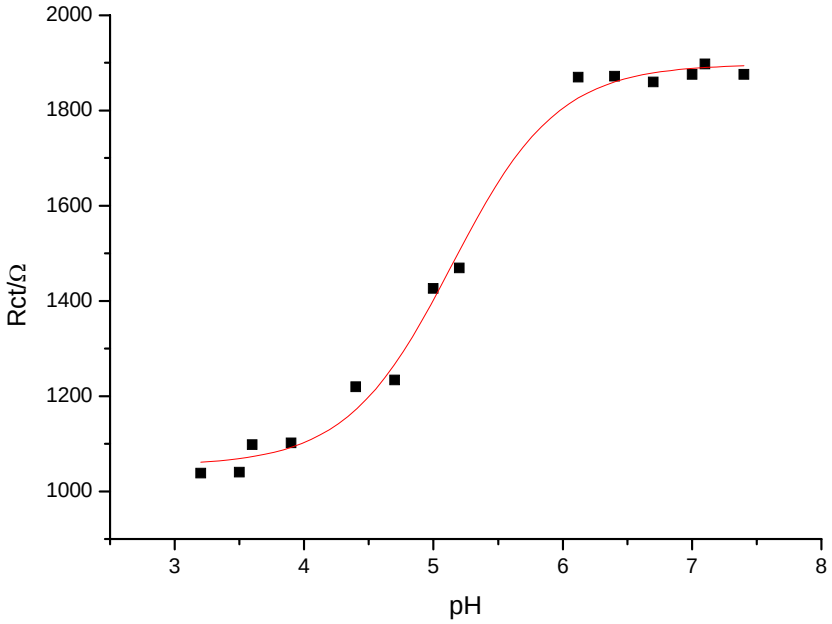

Figure 6.13: Trend of the charge-transfer resistance with varying the pH (EIS measurements) [Measurements carried out by Dr. Erika Scavetta, University of Bologna, Bologna, Italy]

The charge-transfer resistance R_{ct} can be obtained by measuring the diameter of the semicircle in the impedance spectrum via simulation. The charge of the interface of the modified electrode changes by changing the pH value of the solution, due to the presence of amino group. We expect to observe a decrease in R_{ct} value as the we move towards more acid solutions (because we are using a negative redox probe). Comparing this plot with the results of Handerson-Hasselbach equation we found that the major sensitivity range for our pH Sensor, functionalized with thio-aminic groups must be around pH = 4-5 where the curve shows a variation in its concavity.

The expected working principle of the CMOFET is based on an effective device voltage shift towards more negative values with decreasing the pH value. In fact, this behavior is in accordance with the enhanced protonization of the thio-aminic surface groups bonded to the

floating-gate due to higher H^+ ions concentration when going towards more acid pH values. Thus, by protonizing, the thio-aminic groups bond a positive charge on the floating-gate. So the more acid is the solution the more positive charge will be grafted on the floating-gate plate. This results in a more negative gate voltage to be applied in order to overcome this positive voltage offset and turn on the device, that is a more negative actual threshold voltage. This is in accordance with the equation:

$$V_{thf} \approx V_{th} - \frac{Q_S}{C_{CF} + C_{FB}} \qquad (6.30)$$

which is the (6.28) without the term Q_{f0} that does not make sense for the CMOFET. As a consequence, for the same V_G value, if the threshold voltage decreases also the drain current is expected to decrease according to the general OFET equation in saturation regime:

$$i_{Dsat} = \frac{1}{2}\frac{W}{L}\mu C_i (V_{GS} - V_{th})^2$$

The measurements we carried out confirm this expected behavior on the threshold voltage with varying the pH:

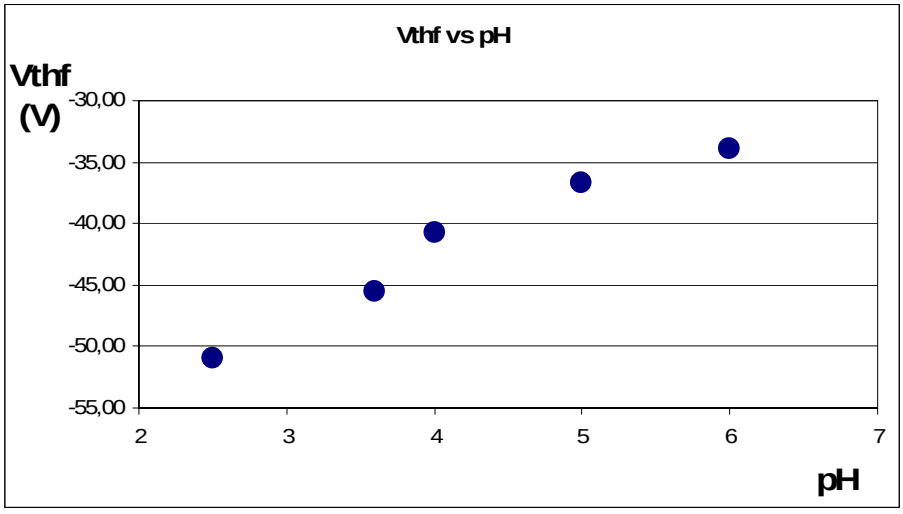

Figure 6.14: Variation of the V_{thf} with varying the pH in the solution: a clear trend in accordance with what the model foresees. Threshold voltage values were extracted from sqrt|I_D| vs. Vg in saturation regime.

Consequently the maximum drain current (normalized to a reference transistor that was biased simultaneously and at the same bias conditions of the tested transistor but with the floating-gate in contact with a solution whose pH was kept constant throughout the measurements) measured on the output characteristics varies according with the threshold voltage trend:

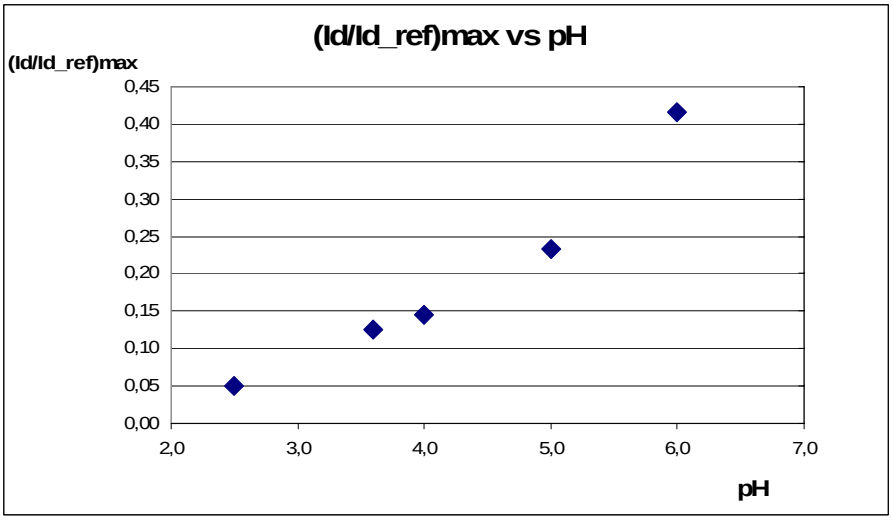

Figure 6.15: Variation of the normalized drain current of the tested CMOFET device with varying pH in the solution.

A further influence of the pH on the electrical parameters involves the charge carrier mobility of the semiconductor layer as shown in (6.16):

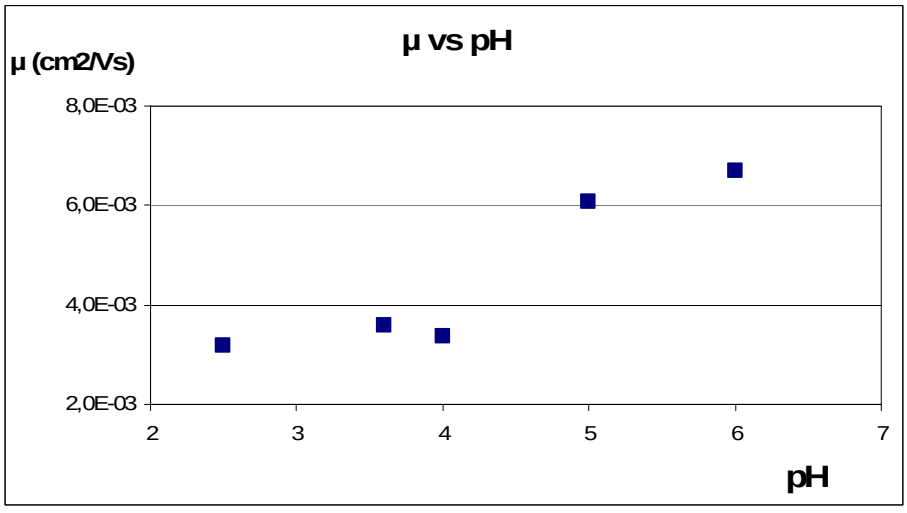

Figure 6.16: Variation of the charge carrier mobility with varying pH in the solution. The mobility values were extracted from sqrt$|I_D|$ vs. Vg in saturation regime.

The mobility dependence on the pH is not expected in the classic inorganic CMFET. But this is not surprising when dealing with organic semiconductors where the mobility dependence on the gate voltage has been subject of intense debate as already discussed in the first chapters of this thesis. In fact, according to a general model as the one that follows

$$\mu = K\left(V_{GS} - V_{th}\right)^{y}$$

the charge carrier mobility increases with increasing the gate voltage. Being that a more acid pH results in a higher positive charge offset bonded on the floating-gate, the mobility variation with the pH presented in 6.15 is coherent with the fact that the negative gate voltage applied to the transistor through the control gate will be eventually lowered by the positive charge amount on the floating-gate that is inversely proportional to the pH.

In order to see whether the sensor response to the pH occurs not only when a from acid to basic transition in the solution pH occurs we tested also from basic to acid pH values variation. In fact, since all of the measurements were carried out at ambient conditions a possible semiconductor doping effect due to the presence of oxygen can be taken into account. The effect of oxygen on the organic materials have been previously discussed in this work: being electronegative, when an oxygen molecule is physisorbed by the semiconductor it generates a undesired p-type doping effect that should (in first approximation) increase the drain current. So when going from acid to more basic pH values a drain current increasing is expected throughout the measurement. But the same trend could be originated by an environmental oxygen doping as well. With the purpose of dispelling this doubt we performed sets of measurements also going from basic to acid pH values. In fig. 6.17 the results of such tests are shown:

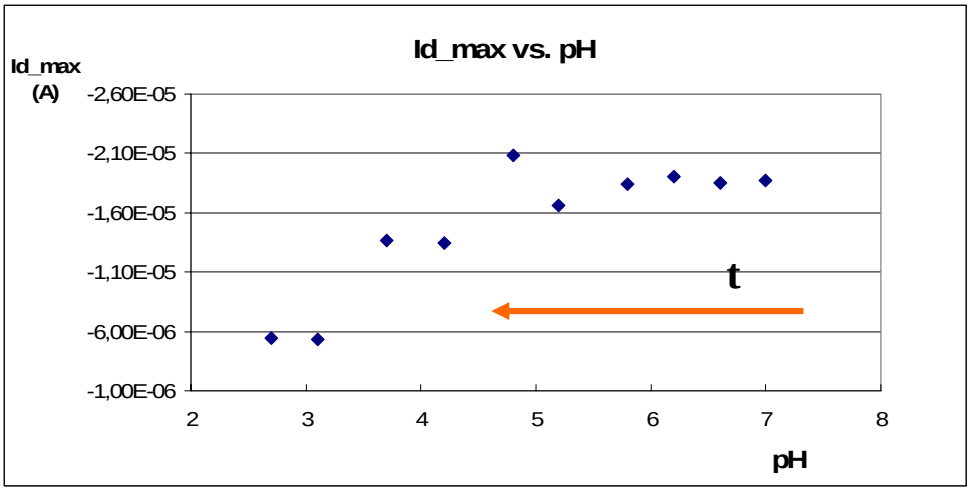

Figure 6.17: Variation of the maximum drain current of the tested CMOFET device with varying the pH in the solution. The drain current is measured on the output curves. Basic to acid transition.

This measurement confirms the expected behavior being in accordance with the model because of the elimination the possible oxygen doping dependence on what is observed. Moreover it confirms once again that the major sensitivity range drops around the pH = 4.

In conclusion, we have realized an organic pH sensor based on the CMOFET concept. In the future a wider pH range variation detection is desirable by using different functional groups such as for instance carboxylic acid group which is sensitive to the OH groups and consequently could be employed for monitoring the pH variation in basic (pH bigger than 7) solutions.

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Chapter7

Market Perspectives of Printable Organic Electronics (POE)

Scientific research and market place sometimes do not cross each other due to either scientists that never would think that what they are working on could be marketable and why or investors that are not into “science stuff” and therefore do not know the huge market potential hidden behind new discoveries and are not able to bring them to the market place.
This chapter represents an attempt to thinking through the relationship between what the organic electronics produces in terms of materials, consequent applications and to what extent these potential technology products are likely to go to market.
In particular paragraph 7.1 will focus on the analysis of possible organic materials that can really go to market. Paragraph 7.2 is about the market trends in organic electronics: what is already on the market? And what are the real perspectives and future market projections for the whole organic electronics world in the years to come?
Finally the last paragraph deals specifically with organic-based sensors and their future success on the market together with an example of possible as well as real application to the market.

7.1 Is Organic Electronics really marketable?

Although the flowering of the Printable Electronics (PE) industry has many roots, it is essentially related to materials. In particular, it is a story of the maturing of certain kinds of inks that can now be used to create complex circuitry of a wide variety of kinds.
Two major trends stand out in this regard. One is the development of stable inks based on organic polymers. Although the fact that polymers can be conductive or semiconductive

when doped has been known for decades, it is really only in the past two or three years that inks that are sufficiently stable over time and resistant to air and water have been produced. With these inks now the Printable Organic Electronics (POE) industry is looking forward to creating highly innovative products in volume, most notably large-area printed OLED displays. The other important trend, that we cite here is for sake of completeness, is the development of inks based on metallic nanoparticles that could make significant improvements in the ability to cure circuitry after printing, most notably in the form of reduced temperature needed for this curing.

As these trends make printable electronics seem more and more like it is a genuine business opportunity, the emerging printable electronics industry has begun to take on a sense of confidence about its future. In particular, it has developed an implicit goal of being able to create “electronics anywhere”, i.e., a new kind of electronics that can be fully integrated in everyday life. This also has important implications for materials, in this case substrates. At the moment most printable organic electronics is created on plastic, but a big open question is whether printable electronic circuitry could be created on paper or card, which is, after all, the “natural” substrate of the printing industry.

The usage of plastic substrates is implicit in the “electronics anywhere,” slogan. Other substrates that have been considered include metals, china, fabrics and even wood. In addition, different shapes of substrate have been considered even if how to print on curved substrates is definitely under consideration but could allow Printable Electronics to fully explore many new and interesting markets.

The main inks used by POE are oligomers, small molecules and obviously polymers as the semiconductor layer, conductive polymers for the realization of electrodes but also dielectric inks.

In particular, among the conductive inks for the realization of electrodes is mainly PEDT:PSS in aqueous solution (Baytron P HCV2 by Bayer or CH8000 by Stark) [internet source: http://www.scied.science.doe.gov/].

As to the semiconductive inks the main are:

- P3HT (provided for instance by Rieke Metals Inc., Plextronic Inc., Solenne BV)
- PCBM (provided for instance by Solenne BV)

Among the tested printable the main organic dielectrics employed is Poly(vinyl alcohol).

However, at the present time many materials are being tested and the information hiding grade is very high so it is not easy to gather sufficient information because of that. Many companies prepare and synthesize new inks but the their formulation is destined to be hidden within the next years.
Anyway, the whole printable electronics is improved by relatively recent developments in the materials sector and this means that these developments should be of interest to everyone in the printable electronics industry.
As to the marketability of the organic materials, this can be understood only under an analysis of the whole chain value in which these materials are just the first link.

According to the **SWOT** (**S**trenghts / **W**eaknesses / **O**pportunities /**T**hreats) analysis, first Strenghts and Threats for the same market opportunity have to be considered.

As to the **Strenghts** related to POE we have:

- *low- cost materials and processes* that lead to *low cost of the final devices*.. In fact, the usage of a few pieces of machinery and the large-area production have a strong impact on the *lowering of fixed costs*.
- *chemically tailored materials* to be adapted to several and different applications
- *printability* of the materials
- *rapid prototyping* of the throughput thanks to the usage of circuit printers that in a few process steps can produce the final item.

As to the **Threats** related to the POE we have:

- *The pressing metal ink-based expertise* could persuade investors or established firms to convert the printing equipment for organic materials into metal-ink printing equipment. In fact, the knowledge acquired in terms of metals is much broader than that related to organic materials.
- *The growing nanotechnologies coming* with all its market potential could persuade investors and established companies to invest on them.
- *Being too far from real marketable products* will discourage investors and companies from keeping on investing on organic electronics.

With this in mind, in the table 7.1 [source: *Nanomarkets.net*], let us set out the primary **Weaknesses** and **Opportunities** that exist for each level of the printable organic electronics value chain.

Stage in the Chain	***Weaknesses and Opportunities***
Materials and specialty chemicals	Stability and performance of inks in different environments and application and cost of processing. Opportunities lie in improved formulations and entirely new inks and substrates
Printing Equipment	• How well existing printing equipment handle currently used and future conductive and semiconductive inks? • What is to be done to make it suitable for use with inks and substrates for PE?
Printers	• Is available clean room-like environment suitable for printing with electronic inks? And last but not least are the Health, Safety and Environmental issues.. • Is staff trained to deal with printable electronics materials?
Device	• What kinds of materials provide significant advantages over existing semiconductor technology in terms of price and novel applications? At some point this may become "price, performance and novel applications". But PE seldom performs more than a conventional application at this point in time. This level in the value chain will be interested in which materials provide the most optimal lifetimes for their products.
Final product	Generally speaking this level of the value chain is less interested in materials matters, assuming that these issues are dealt with lower down in the food chain. However, there is some interest in which materials have the necessary durability to sustain a reasonable lifetime for final products and whether one material or another can better provide novel features for such products.

Table 7.1 The Printable Organic Electronics (POE) Value Chain: Materials Issues and Opportunities

There are still further questions, about involvement and investment to be taken into account: while the interest in printable organic electronics and the materials and production platforms that enable it are broad, it is often not all that deep. Many firms (including many materials firms) are simply at the exploratory level and even in large firms there may be no more than a small group of executives (sometimes no more than one) who is doing this exploration.
The reasons for this are various:

• It is not yet clear whether printable electronics can really live up to its promise.

• There is an unwillingness to invest in high-tech electronics just a few years after the biggest collapse of the high-tech market on record. This factor is enhanced by the fact that many of the firms that are considering entry into the printable electronics industry are rather traditional firms in the printing, materials and specialty chemical industry, and are especially skeptical about a diversification as radical as this one appears to be.
• In almost every case the volumes for any printable electronic application have yet to reach a level where the arguments for early market entry are particularly compelling, especially for the largest suppliers. Even smaller materials suppliers are unlikely to find much to get excited about in new business revenues in the next couple of years.

Another point which is still on debate is whether early entry into this market for materials suppliers make sense even though in this context it can be a potential opportunity of becoming an established supplier in what may eventually be a new electronics era.

But exactly how long will it take for the inevitable trend to make its impact? Once electronics starts to be printed in significant quantities, it seems highly likely that the extremely wide diversity of materials now being considered in terms of inks and substrates will begin to narrow quite quickly.
In conclusion, many questions are still open on the marketability of PE over the long run but all the investors and the companies have to do to discover it is just trying to explore this new and fascinating world of Plastic Electronics.

7.2 Market Trends in Organic Electronics

Organic semiconductors have been known for 40 years, although again it is only very recently that organic electronic inks have exhibited enough environmental stability -- longevity when exposed to air, water and high/low temperatures -- to be a practical way of creating electronics in a general way.
However, let us try to list and analyze emerging opportunities:
The improvements described above go hand in glove with the commercialization of printable electronics applications. Now that the materials look stable and available enough

to actually print organic electronics in commercial quantities, printing and device firms are actually beginning to set up pilot plants to produce real printable electronics products. Antennas for RFIDs are already being printed commercially using organic inks (Fig. 7.1) and the expectation is that the entire RFID could be printed creating very low cost RFIDs that could ultimately make RFIDs as common as barcodes.

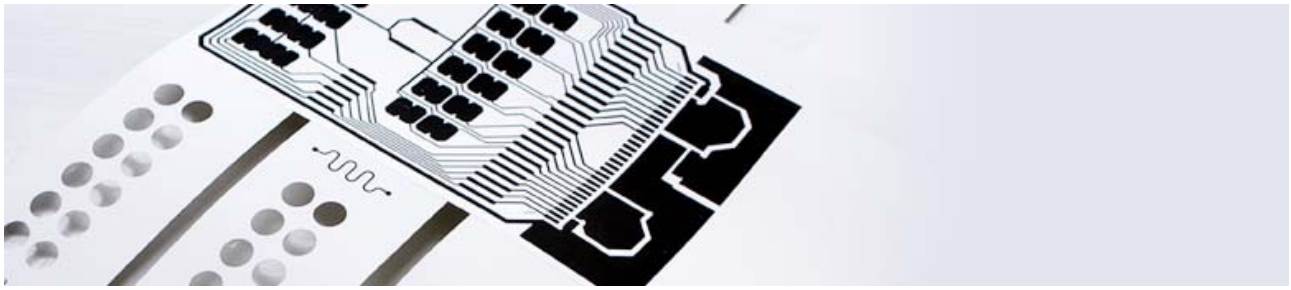

Figure 7.1 Printed antennas by Cypak AB [internet source: http://www.cypak.se]

The other big target area for printable electronics right now is displays which includes both the printing of sizeable OLED displays (Fig. 7.2) that could provide serious competition for LCD screens and the printing of backplanes for flat panel displays of all kinds that could offer a low cost alternative.

Figure 7.2 11-inch OLED-TV 2007 by Sony

Other applications that are being seriously considered, although they do not appear to have quite the same short-term revenue potential as the display and RFID segment, include

printable photovoltaic arrays, sensor arrays, computer memory, wearable electronics, greetings cards and other novelties.

As we noted earlier in this chapter, the maturing of printable electronics will probably be accompanied by a narrowing of the types of inks and substrates to a relatively small number, but this certainly is not happening yet. Indeed, the current flowering of printable electronics is leading to something of a feedback mechanism, encouraging materials and specialty chemical firms to come up with new and better inks and substrates, more suited to the new applications. In particular, we suspect that materials firms are now going to spend more time and money doing R&D with better inks and substrates.

After all, it is only in the past couple of years that doing this kind of work seemed anything more than just a science project and we now have some of the evolving tools and thinking of nanotechnology to help firms in the development task. Among the key development opportunities that NanoMarkets foresees as likely to be given growing attention in the future are inks that use entirely new kinds of materials as their base.

Again, Nanomarkets foresees that the market of OTFTs and organic-based memories in the following will grow very rapidly according to the following exhibit:

Organic Memory and OTFT Markets ($ Millions)					
	2008	***2009***	***2010***	***2011***	***2012***
Products using OTFTs only	2.2	50.8	210.3	699.1	1,424.3
Products using organic memories only	14.2	67.3	331.9	1,265.7	2,588.4
Products using both OTFTs and organic memories	0.0	31.2	175.7	742.3	1,818.7
TOTAL	16.3	149.3	717.9	2,707.1	5,831.4

Exhibit I Organic Memory and OTFT Market forecast [source: Nanomarkets.net]

The very diversity of new materials that is likely to come to market in the next couple of years, virtually guarantees that there are going to be many failed products, and some failed suppliers. It is important, however, for the market planner in this space field to understand that the failure of a particular ink may indicate nothing at all about that kind of product. For example, there is already one instance of a polymer memory product failing to make it to

the market and this has hurt the prospects for polymer memories as a whole. Nonetheless, a closer examination shows that this failure reflected the poor performance of a specific polymer and not those of all polymers. But despite the inevitable failures, with printed organic electronics now promising large markets in a few years, it is believed that their will be growing opportunities for selling new materials products into this sector.

7.3 Are Organic-based sensors going to the market place?

"One of the less talked about markets for printed and organic electronics is sensors. In fact, printed electronics is already used for sensor electrodes and to fabricate DNA arrays. And, while most printed sensors have used screen printing the past, other printing modes are looking promising for fabricating sensors; flexo can do it in greater volumes and inkjet with more accuracy". [source: *Nanomarkets*]

There are many promising markets today for electronic sensors, if mainstream silicon technology could produce sensors at a cost that is low‑enough for most of these markets. Bringing diagnostics closer to the patient and improving the coverage of both environmental and security monitoring in major public buildings are just two that spring to mind. This leaves a wide‑open opportunity for alternative materials and manufacturing technologies. Two of the strategies that suggest themselves in this regards are the use of functional printing and the use of organic electronic materials. And both of these approaches are already in play. NanoMarkets believes that sensors using organic and/or printed electronics will surpass $220 million in revenues in 2008 and will exceed the $1 billion mark in 2013.

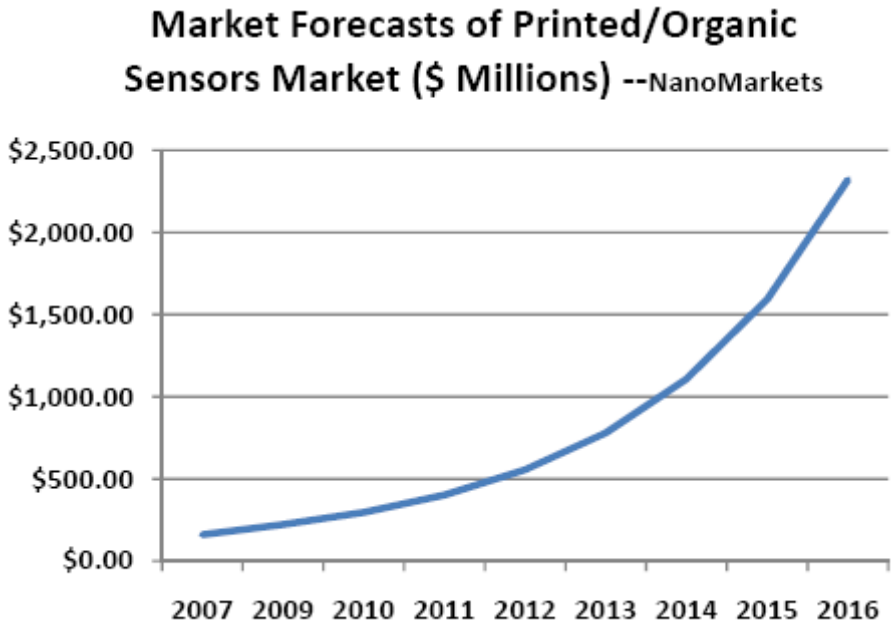

Figure 7.3 Printed Sensors Market Forecast [source: *Nanomarkets.net*]

Perhaps not surprisingly, much of the revenue generation that NanoMarkets expects from printed and organic sensors from now until 2015 will have much to do with biology. DNA microarrays are routinely fabricated using printing and, as a result, genetic applications will provide sensor revenues through 2012, at which point environmental monitoring applications will take over the number one position. Medical diagnostic and therapeutic applications will also play a major role in printed sensor.

Other important applications areas for printed and organic sensors will include smart packaging, robotics and homeland security. One of the most interesting applications for these kind of sensors will be found in smart textiles, which is a business that is just getting started, but it has a very high growth potential; applications for printed and organic textiles will grow consistently over the period, accounting for about a 10% share of a total $2.3 billion market for organic and printed sensors by 2015. The range of applications for printed and organic sensors is quite broad as shown in Table 7.2:

Application area	***Type of sensor***
Architecture and construction	Sensor arrays on flexible substrates that will conform to the contours of walls and ceilings. Such sensor arrays would have immediate application for sensing toxins or atmospheric quality. It might have future uses for imparting ambient intelligence to buildings

Protective clothing and military uniforms	Sensor arrays embedded in clothing would help protect soldiers, police, fire, and power plant workers from exposure to toxins. Clothing of this kind could be targeted towards detecting just one toxin (e.g. radiation) or multiple toxins. The latter kind would be especially appropriate for military uniforms.
Smart labels and smart packaging	Printed sensors on paper or plastic labels that could indicate tampering, freshness, frequency of use (of pills.) Still some way from being cost effective, but fairly close to commercialization
Robotics	Artificial skin would consist largely of tactile and (perhaps) heat sensors on a plastic substrate
Automotive and aerospace	Extension of the current wide use of sensors to arrays that cover entire surfaces, both inside and outside the vehicle. Applications could range from security, through atmospheric controls, to passenger comfort.

Table 7.2 Opportunities for flexible sensors

In the gradually emerging view of the future, printed and organic electronics will be used to provide the actual processing power or the sensing fabric of the sensor, not just the electrodes. And as Table 7.3 shows, there are many ways that printed and organic electronics can be used in the sensor business.

Feature of organic/printable electronics	Description	Impact on Sensors	Other comments
The ability to create circuitry with modest upfront investments	A full-scale plant capable of turning out perhaps millions of sensors per year might entail a capital investment of $100 million or much less. Industrial printing equipment is much less costly than the semiconductor industry standard photolithography equipment	Complex sensors can be built and sold at lower prices. This can turn expensive medical diagnostic equipment into lower cost point-of-care or even home diagnostic equipment, with the obvious benefits. Or it can enable the wider deployment of important homeland security or environmental	At present, this is the aspect of organic/ printable electronics that sees the broadest application. Sensors are often layered devices and it is now not uncommon for sensor firms to consider using printing as a way of depositing such layers

		testing gear.	
The suitability of organic/printable electronics to create wide area electronics	Transistors, memory, Photo-sensitivity can be deployed over a large surface to create unique products	It is possible to create large arrays of sensors using printable electronics relatively easily. These could have applications in many fields	Sensor arrays have been a mainstay of the sensor business for many years. Printable electronics offers a new and easy way to make them
The ability to create flexible products	Organic, metallic and other inks can be printed on flexible substrates including plastic, metal foil and even paper	Sensor arrays can be made to conform to the shapes of products and buildings more easily. Low cost substrates can be used to create disposable sensor products that would be useful in medical and other fields	The ability to print functional devices onto flexible substrates is just beginning to see full commercialization in the display area, but it clearly has some potential in the sensor area too
The ability to manufacture in very large or very small quantities	Maskless printing techniques, such as inkjet, can create functional devices economically in very small quantities; or even in "one offs." Highthroughput printing techniques, such as flexo, can be treated as low-cost manufacturing approaches for high volumes of devices	These new manufacturing techniques may be used to create cost effective sensors for specialist scientific, medical or military applications. Or they may be used to create millions of sophisticated sensors for mass deployment.	The low-volume capabilities of printing fits well with the perceived general marketing trend towards the customization of products. The highvolume capabilities of printing adds a new kind of tool to tool kit commonly used to create mass market functional devices.

Table 7.3 Printed Electronics (PE) opportunities in the sensor business

In conclusion, market reports and projections estimate that the sensor market represents an attractive opportunity for printed and organic electronics manufacturers in part because unlike radiofrequency identification (RFID), this segment of electronic devices is underserved by existing manufacturers. There are many indications that the market for sensors will grow rapidly, especially in the security and medical arenas.

7.4 An example of an all-organic plastic device for chemical detection for anti-doping testing and its relative market perspective forecast

Even when dealing with a rough forecast on the real market perspectives that a product could have, knowing the so-called "tipping points" is needed. Tipping points are some special events that could happen and that could make easy the market entry for a certain product. For instance after "September 11" the security market has grown incredibly fast.

In the case of an organic-based printable sensor for chemical detection of doping in athletes we consider a major tipping point:

In 1999, World Anti-doping Agency (WADA) was founded and funded equally by the sports movement and governments of the world to harmonize anti-doping policies in all sports and all countries. This event would have pushed all the sport world to progressively be tested before competition in order to verify that nobody takes performance-enhancing drugs.

Other information gathered have however to be taken into account:

1. **number athletes tested/year** is at least doubling every year
2. **186 nations** have made the political commitment to the global fight against doping by signing the Copenhagen Declaration, and
3. **44 countries** have already followed through on that commitment.

What listed above together with the tipping points represents the *Opportunity for the anti-doping market*.

But let us come to consider the current costs for a complete anti-doping test for an athlete [source: Italian anti-doping official site]:

Cost/analysis in itself €235

Cost/reiterated analysis €441,57

Cost/sampling €48

Cost/doctor €190

Other expenses €150

total costs/test €1064,57 = $1.432,91

the cost of a single test multiplied by number of tests/year gives the ***Annual Cost of Antidoping:***

Total cost/test x Number of tests/year = $286,5M/year

But, in contrast to this foreseen cost, there are several other numbers to be taken into account related to the anti-doping prevention investments:

1. The budget of the USA anti-doping agency in 2003 was 10 million dollars.
2. The WADA (World Anti-Doping Agency) budget amounted to 21 million dollars in 2004.
3. The budget of the Swiss Anti-Doping Commission for 2004 was about SFr. 1.5 million whereof SFr. 800,000 came from the government.

These data tell us that despite the growing need of testing athletes the amount of investments is still lower than needed. Thus, this consideration has also to be taken into account to estimate the potential market picture.

As to the tests there are further considerations:

- **Every athlete** can be tested on **different doping agents**
- The accuracy of the test and the number of species to be detected increase with the importance of the competition
- Detection of different kinds of dopant requires **different kind of analysis** as well as **different kind of machinery** employed

This means that every complete test/athlete results in many single tests with different reagents and machinery employed to detect different doping agents.

All of these factors suggest that for cutting costs we should have:

- devices that can make the whole analysis avoiding the employment of expansive and bulky machinery in the lab
- devices that can detect more doping agents all in once

A solution to this problem is the employment of printable organic-based devices on plastic substrates due to all the advantages over silicon electronics previously discussed here in this chapter.

Clearly the more intellectual property there is, the better. The know-how and the amount and the control of intellectual property is crucial for starting every kind of investments, because acquiring know-how or buying intellectual property are expenses that have to be taken into account among the so-called “seed money”, which is the money needed for starting every kind of business activity. Established companies can sometimes face such costs but for small or medium enterprises this problem could be impossible to be solved unless big private or public investors are involved into that promising business.
That being said a financial plan that could cover at least four years of activity (to get a prototype) has to be done, including different kind of expenses such as:

- Research personnel
- Machinery costs
- Material costs
- Consulting costs
- Patent costs
- Legal costs

Then after a consideration on how many years are needed to produce a prototype, further considerations are needed. The calculation of the so-called breakeven point, i.e., the amount of time necessary for the generated revenues to equal all the expenses is often an important parameter that all the investors consider when dealing with a new business.

This point can be roughly calculated by gathering information such as, in our case:

Cost per Roll-to-roll equipment	$1M
Cost per materials	$150,000
Other expenses (e.g maintenance)	$50,000
Cost per personnel (over three years)	$500,000
Total	$1,7M

Then, once a first price estimation was done (in our case the calculated price/device was approximately $12) by comparing this with the present price/analysis ($400) required by the

traditional procedures we obtained a cost approach that was roughly 30 times cheaper, so very appealing for potential investors.

By making some calculations, the expected revenues targeting 40% of the market (80,000 items/year) can be done later in time after considering that the breakeven point will happen after at least 5,5 years. So the revenues in this case would come after 5,5 years.