Ph.D. in Electronic and Computer Engineering
Dept. of Electrical and Electronic Engineering
University of Cagliari

Modeling of Physical and Electrical Characteristics of Organic Thin Film Transistors

Simone Locci

Advisor: Prof. Dr. Annalisa Bonfiglio
Curriculum: ING-INF/01 Electronics

XXI Cycle
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Contents

*

List of Figures

*

List of Tables

*

Abstract (Italian)

Il materiale maggiormente studiato ed impiegato nell'elettronica è indubbiamente il silicio. Le sue proprietà e i costi ad esso associati lo rendono un candidato ideale per la maggior parte delle necessità dell'elettronica odierna. Tuttavia, diversi altri materiali sono stati studiati negli anni passati. Nel 1977, Alan J. Heeger, Alan G. MacDiarmid e Hideki Shirakawa scoprirono un nuovo polimero su base carbonio altamente conduttivo: l'oxidized iodine-doped polyacetylene. Per la loro scoperta, che è stata una delle pietre miliari più importanti per l'elettronica organica, sono stati insigniti del Premio Nobel per la chimica nel 2000.

I semiconduttori organici hanno consentito a scienziati ed ingegneri di sviluppare dispositivi con caratteristiche innovative e costi ridotti, rendendo questa tecnologia particolarmente interessante per diversi settori dell'elettronica. I semiconduttori organici possono essere realizzati e processati a temperatura ambiente, rendendo la loro produzione più facile e conveniente rispetto al silicio e agli altri semiconduttori inorganici; possono essere trasparenti, flessibili e sviluppati su grandi aree o su geometrie non planari; possono essere realizzati anche dispositivi completamente plastici.

Le loro prestazioni, comparate con quelle del silicio, sono tuttavia inferiori: la mobilità dei portatori è ordini di grandezza inferiore, anche se questa è notevolmente cresciuta negli ultimi anni; sono particolarmente sensibili alle condizioni ambientali, specialmente all'atmosfera (ossigeno e umidità); le loro prestazioni decadono col tempo.

Nonostante questi inconvenienti, il grande potenziale dell'elettronica organica ha portato ad un'intensa attività di ricerca, sia teorica che sperimentale, le cui origini risalgono alla fine degli anni Settanta, periodo in cui avvennero le prime scoperte. In questa tesi di dottorato viene sviluppato un quadro teorico che descriva l'elettronica dei transistor organici.

Nel capitolo 2 viene presentata una panoramica dell'argomento: a partire dalle proprietà fondamentali dei semiconduttori organici, il capitolo si sviluppa per fornire una approfondita analisi della fisica e dei modelli elettrici che descrivono il comportamento dei transistor organici a film sottile.

Nel capitolo 3 vengono modellati i transistor organici a film sottile con geometria

cilindrica. Questa particolare geometria ben si adatta a nuove applicazioni, come sistemi tessili intelligenti per funzioni di monitoraggio biomedicale, interfacce uomo macchina e, più in generale, applicazioni e-textile. Viene presentato anche un confronto con risultati sperimentali.

Il capitolo 4 presenta un modello per transistor organici a film sottile a canale corto. Il riscalamento delle dimensioni nei dispositivi organici conduce a differenze significative, rispetto alle teorie introdotte nel capitolo 2, nelle caratteristiche del dispositivo, con effetti che possono già essere rilevanti per dispositivi con lunghezze di canale di dieci micron. Vengono considerati la mobilità dipendente dal campo ed effetti di carica spaziale, che limita la corrente; viene inoltre fornito un confronto con i risultati sperimentali.

Il capitolo 5 analizza il comportamento dei transistor organici come funzione del tempo. Vengono esposti i modelli teorici che consentono di descrivere fenomeni di carica e scarica di stati trappola, e vengono successivamente simulati per differenti parametri. Al variare di tali parametri, vengono studiate le curve di trasferimento, per i transistor organici a film sottile, e le curve capacità-tensione per le strutture metallo-isolante-semiconduttore.

Il capitolo 6 conclude questa tesi di dottorato. Vengono qui riassunti i risultati e le considerazioni più importanti, così come vengono esposti possibili future linee di ricerca sull'argomento.

Chapter 1

Introduction

The most studied and widely employed material for electronics is undoubtedly silicon. Its semiconductor properties and its associated costs make it an ideal candidate for most of the needs of today electronics. However, several different materials have been studied in the last years. In 1977, Alan J. Heeger, Alan G. MacDiarmid, and Hideki Shirakawa discovered a new, carbon based, highly-conductive polymer: the oxidized, iodine-doped polyacetylene. For their discovery, which was one of the most important milestones for organic electronics, they were jointly awarded the chemistry Nobel Prize in 2000.

Carbon based semiconductors allowed scientists and engineers to develop devices with novel features and reduced costs, making this technology become a premier candidate for several sectors of electronics. Organic semiconductors can be manufactured and processed at room temperature, making their production easier and cheaper than for conventional silicon and inorganic semiconductors; they can be transparent, flexible and developed over large areas or non-planar geometries; completely plastic devices can be realized.

Their performances, compared to silicon, are however inferior: carrier mobility is orders of magnitude lower, even if this largely increased in the last years; they are highly sensitive to environmental conditions, especially to the atmosphere (oxygen and humidity); their performances decrease over time.

Despite these drawbacks, the great potential of organic electronics has led to extensive theoretical and experimental research since the first discoveries during the late seventies. In this doctoral thesis, a theoretical framework for the electronics of organic transistors is developed.

In chapter 2 an overview of the topic is presented: starting from the fundamental properties of the organic semiconductors, the chapter develops to provide a thorough analysis of the underlying physics and the electrical models which describe the behavior of organic thin film transistors.

In chapter 3, organic thin film transistors with a cylindrical geometry are modeled.

This particular geometry is well suited for novel applications, like smart textiles systems for biomedical monitoring functions or man-machine interfaces and, more in general, e-textile applications. A comparison with experimental results are presented.

Chapter 4 features a model for organic thin film transistors with short channel. Scaling of the dimensions in organic devices leads to significant deviations in the electrical characteristics of the devices from the theory exposed in chapter 2, with effects that can already be relevant for devices with channel length of ten microns. Field-dependent mobility and space charge limited current effects are considered, and a comparison with experimental results is also presented.

Chapter 5 analyzes the behavior of organic transistors as a function of time. Theoretical models that describe trap recharging are exposed and simulated for different parameters sets. For each simulation, transfer curves for organic thin film transistors and capacitance-voltage for metal-insulator-semiconductor structures are analyzed.

Chapter 6 concludes this doctoral thesis. The most important achievements and considerations are here summarized, and possible future activities on the topic are exposed.

Chapter 2

From charge transport to organic transistors

This chapter provides an introduction to the topic, starting from the charge transport in semiconductors up to the models which describe the behavior of planar organic thin film transistors. Section 2.1 describes how conjugated polymers can conduct a current and the most important theories regarding charge transport; section 2.2 gives an overview of the most important organic semiconductors whereas, from section 2.3 on, a detailed description of the transistor models is provided. The chapter ends with a short general description of the drift diffusion model.

2.1 Charge transport in conjugated polymers

Materials employed as organic semiconductors are conjugated polymers, i.e. sp^2-hybridized linear carbon chains. This kind of hybridization is the one responsible for giving (semi)-conducting properties to organic materials.

Starting from the electron configuration of a single carbon atom, which is $1s^2\,2s^2\,2p^2$, when multiple carbons bond together different molecular orbital can be originated, as the electron wavefunctions mix together [Vol90] [Bru05].

While $1s$ orbitals of the carbons do not change when the atoms are bonded, $2s$ orbitals mix their wavefunctions with two of the three $2p$ orbitals, leading to the electron configuration that is reported in Figure 2.1. Three sp^2 orbitals are formed and lie on the molecular plane, at a 120° angle to each other, leaving one p orbital which is orthogonal to the molecular plane. Hybrid sp^2 orbitals can then give origin to different bonds. sp^2 orbitals from different carbon atoms which lie on the molecular plane form strong covalent bonds, which are called σ bond, whereas p orbitals which are orthogonal to the molecular plane can mix to give less strong covalent bonds, which are called π bonds. The π bonds

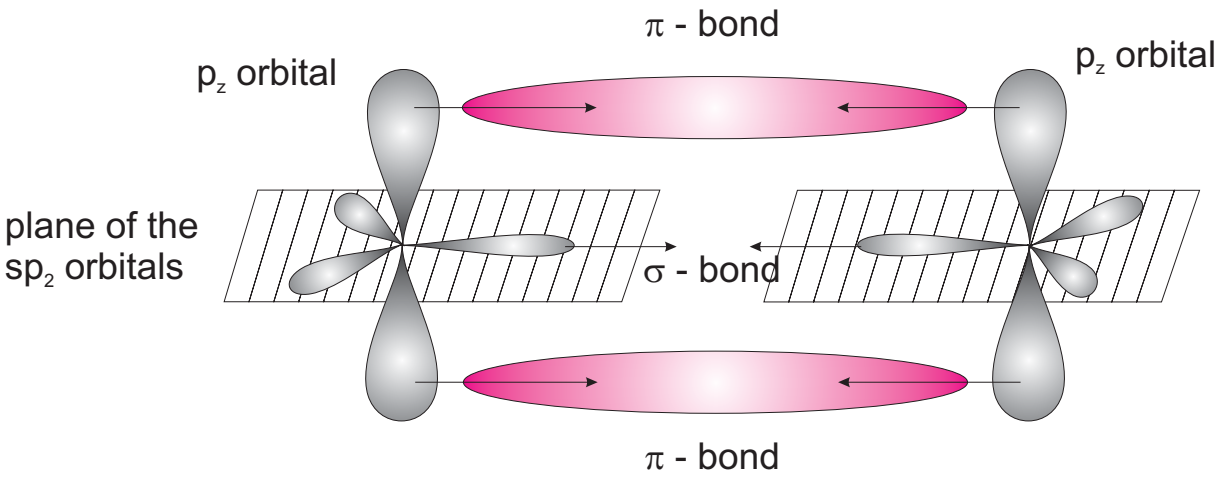

Figure 2.1: sp^2 hybridization of two carbon atoms. sp^2 orbitals lie on the same plane and bond into a σ-bond, p_z orbitals are orthogonal to the plane and bond into a π-bond.

constitute a delocalized electron density above and below the molecular plane and are responsible for the conductivity of the molecule, as the charge carriers move through these bonds.

Depending on the sign of the wavefunction of the orbitals, these can be π (bonding) or π^* (anti-bonding) orbitals, the latter having a higher energy level, as shown in fig. 2.2. When multiple molecules are considered, the energy levels of the orbitals give origin to energy bands, in analogy to what happens in inorganic semiconductors: the edge of the valence band corresponds then to the Highest Occupied Molecular Orbital (HOMO), whereas the edge of the conduction band corresponds to the Lowest Unoccupied Molecular Orbital (LUMO). The difference between the energy of the HOMO and the energy of the LUMO is the energy gap E_g of the organic material and usually $1.5 < E_\mathrm{g} < 4\,\mathrm{eV}$ [ZS01].

Charge transport in organic semiconductor is, however, quite different with respect to silicon and other mono-crystalline inorganic semiconductors. The periodic lattice of these materials and their very low density of defects allows one to accurately describe the charge transport by means of delocalized energy bands separated by an energy gap. Most of the organic semiconductors, on the other hand, are amorphous and rich in structural and chemical defects, therefore requiring conventional models for charge transport to be adapted and extended; moreover, charges can move, with different mobilities, within the molecular chain (intra-chain), between adjacent molecules (inter-chain), or between different domains, generally referred as grains (inter grain).

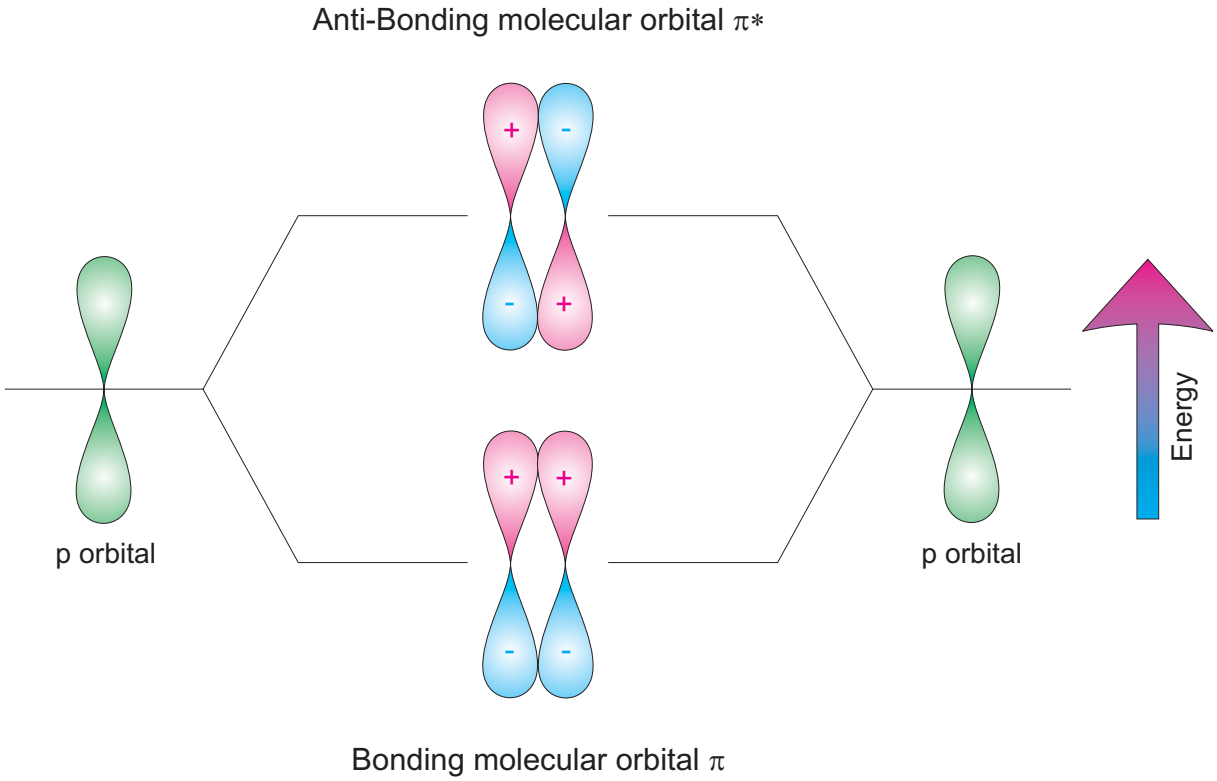

Figure 2.2: Bonding of p_z orbitals: depending on the sign of the wavefunctions, π orbitals with lower energy or π^* orbitals with higher energy can be originated.

2.1.1 Hopping between localized states

The presence of defects and the non-crystalline structure of the organic polymers leads to the formation of localized states. In order to move, charges must hop between these localized states and overcome the energy difference between them, emitting or adsorbing phonons during intra-chain or inter-chain transitions. Attempts to model hopping in inorganic semiconductors are reported in [Mot56] [Con56], later followed by Miller and Abrahams [MA60], who described the rate of single phonon jumps.

In 1998 Vissenberg and Matters [VM98] developed a theory for determining the mobility of the carriers in transistors with amorphous organic semiconductors. They pointed out that the transport of carriers is strongly dependent on the hopping distances as well as the energy distribution of the states. At low bias, the system is described as a resistor network, assigning a conductance $G_{ij} = G_0 \exp(-s_{ij})$ between the the hopping site i and the site j, where G_0 is a prefactor for the conductivity and

$$s_{ij} = 2\alpha R_{ij} + \frac{|E_i - E_\mathrm{F}| + |E_j - E_\mathrm{F}| + |E_i - E_j|}{2kT}. \tag{2.1}$$

The first term on the right-hand side describes the tunneling process, which depends on the overlap of the electronic wave functions of the sites i and j, E_F is the Fermi energy

and E_i and E_j the energies of the sites i and j. a In a lowest-order approximation, this tunneling process may be characterized by the distance R_{ij} between the sites and an effective overlap parameter α. The second term takes into account the activation energy for a hop upwards in energy and the occupational probabilities of the sites i and j. Starting from this expression, with the percolation theory, they can relate the microscopic properties of the organic semiconductors to the effective mobility of the carriers in a transistor. More details are provided in section 2.4.3, where mobility models for the organic transistors are discussed.

2.1.2 Multiple trapping and release model

The Multiple Trapping and Release (MTR) model has been developed by Shur and Hack [SH84] to describe the mobility in hydrogenated amorphous silicon. Later, Horowitz *et al.* extended it to organic semiconductors [HHD95] [HHH00].

The model assumes that charge transport occurs in extended states, but that most of the carriers injected in the semiconductor are trapped in states localized in the forbidden gap. These traps can be *deep*, if their energy level is near the middle of the band gap, or *shallow*, if they are located near the conduction or valence band. This is exemplified in fig. 2.3.

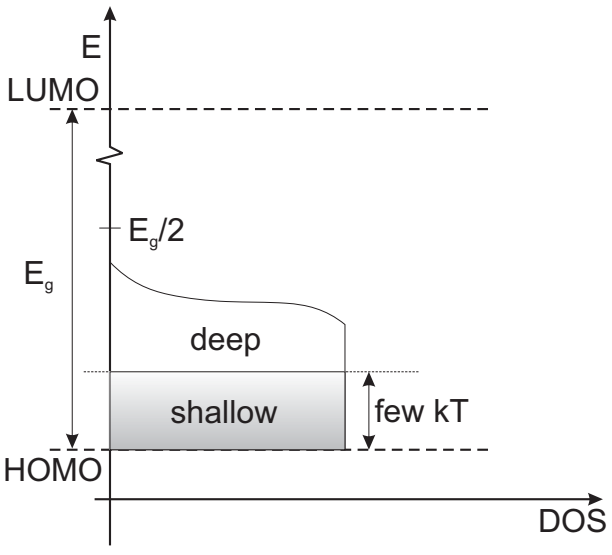

Figure 2.3: Distribution of trap states in the band gap. Shallow traps energy is just few kT over the valence band, for a p-type semiconductor (conduction band for n-type).

The model shows a dependence of the mobility of the carriers on temperature, the energetic level of the traps, as well as on the carrier density (and therefore on the applied

voltage to a device). For a single trap level with energy E_{tr} the drift mobility is

$$\mu_{\mathrm{D}} = \mu_0 \alpha \exp\left(-\frac{E_{\mathrm{tr}}}{kT}\right). \tag{2.2}$$

The temperature dependance decreases with temperature itself and, for low values, the size of the grains of the semiconductor must be accounted. The polycrystalline semiconductor is described as trap-free grains separated by boundaries with high trap density. If their size is lower than the Debye length, the distribution of the traps can be considered uniform. However, if the grains are much larger than the Debye length, charges move through the grain boundaries. At high temperature, this occurs via thermionic emission and a dependence on the temperature is found; at low temperatures, the charges can tunnel through the grain boundaries, so the mobility becomes temperature independent. At intermediate temperatures, charge transport is determined by thermally activated tunneling.

2.1.3 The polaron model

The polaron model was introduced by Yamashita *et al.* [YK58] in 1958 for inorganic semiconductors. Later, it was extended by Holstein [Hol59] and by Fesser *et al.* [FBC83] to molecular crystals and conjugated polymers.

Charge transport in organic semiconductors can be described by means of polarons: a polaron is a quasiparticle composed of an electron plus its accompanying polarization field. In organic polymers, they result from the deformation of the conjugated chain under the action of the charge. Holstein [Hol59] proposed a model to determine the mobility μ of polarons in the semiconductor, as a function of the lattice constant a, the electron transfer energy J, the reduced mass of the molecular site M, the frequency of the harmonic oscillators associated to the molecules ω_0, the polaron binding energy $E_{\mathrm{b}} = A^2/(2M\omega_0^2)$ and the temperature T:

$$\mu = \sqrt{\frac{\pi}{2}} \frac{qa^2}{\hbar} \frac{J^2}{\sqrt{E_{\mathrm{b}}}} (kT)^{-3/2} \exp\left(-\frac{E_{\mathrm{b}}}{2kT}\right). \tag{2.3}$$

Equation (2.3) holds for temperatures $T > \Theta$, where Θ is the Debye temperature defined as $k\Theta = \hbar\omega_0$.

2.2 Materials

Semiconductors are generally referred as n-type or p-type if their carriers are electrons or holes, respectively. For organic semiconductors, the same definitions hold, although the

most widely used and studied semiconductors are p-type. This is mainly because of their higher stability in air and higher mobility (with respect to n-type semiconductors) when they are employed for organic transistors. On the contrary, n-type semiconductors are highly sensitive to oxigen and water, for the presence of carbanions in their structure.

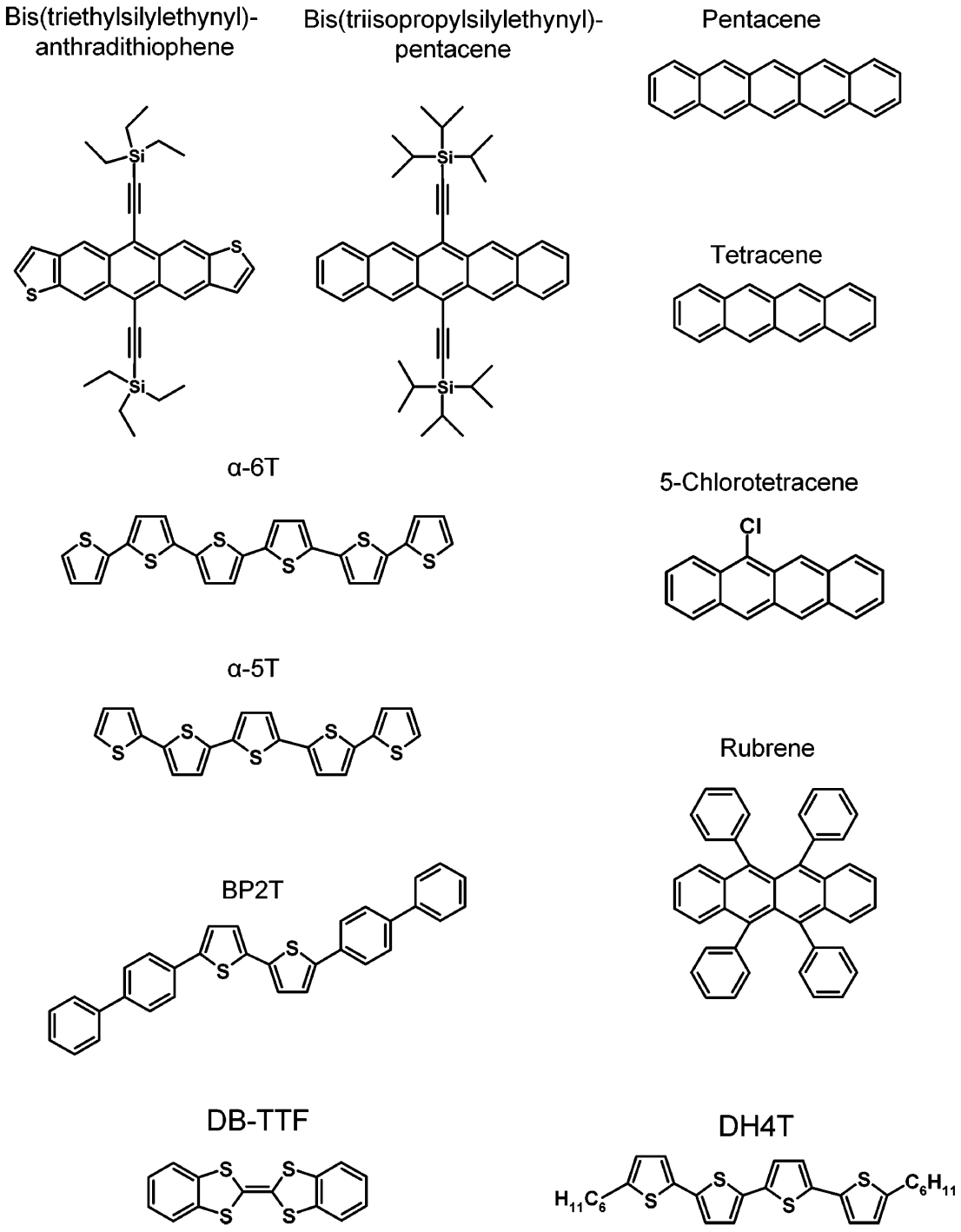

Figure 2.4: p-type organic semiconductors.

Figures, 2.4, 2.5 and 2.6 [ZS07] show the most common organic semiconductors. Figure 2.4 shows p-type semiconductors. Pentacene is probably the most used, as it offers the best mobility among all organic semiconductors (hole mobility in OFETs of up to $5.5\,\mathrm{cm}^2/\mathrm{Vs}$ have been reported). It is a polycyclic aromatic hydrocarbon consisting of 5 linearly-fused benzene rings. Also shown in fig. 2.4 is P3HT, which results from the polymerization of thiophenes, a sulfur heterocycle. Just like pentacene, also P3HT has been of interest because of its high carrier mobility, mechanical strength, thermal stability and compatibility with fabrication process. Figure 2.5 shows semiconductors with predominantly n-channel behavior, in transistors with SiO_2 as a gate dielectric and gold source-drain electrodes. Figure 2.6 shows semiconductors with ambipolar behavior (they can have both p- and n-type conduction).

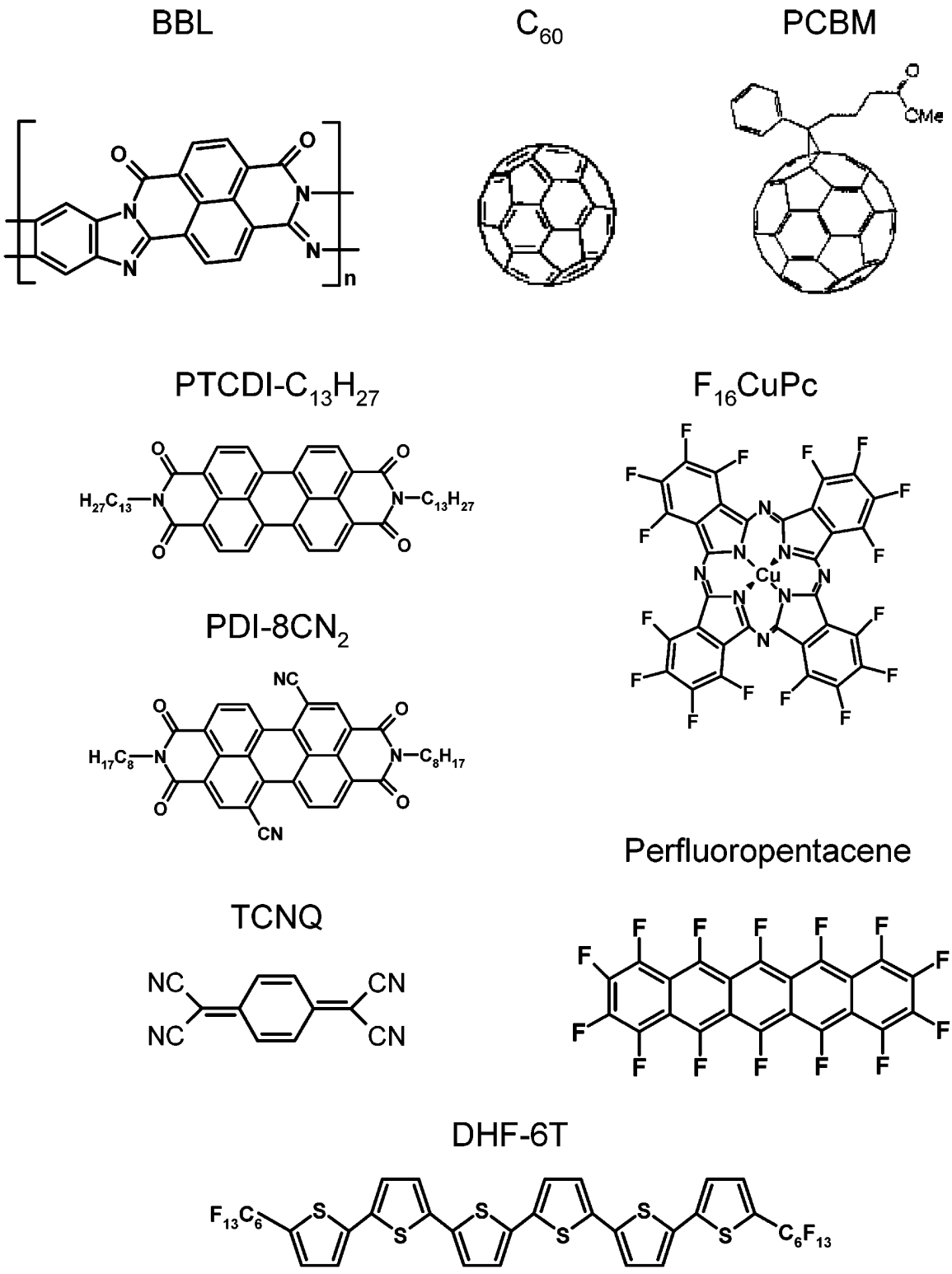

Figure 2.5: *n*-type organic semiconductors.

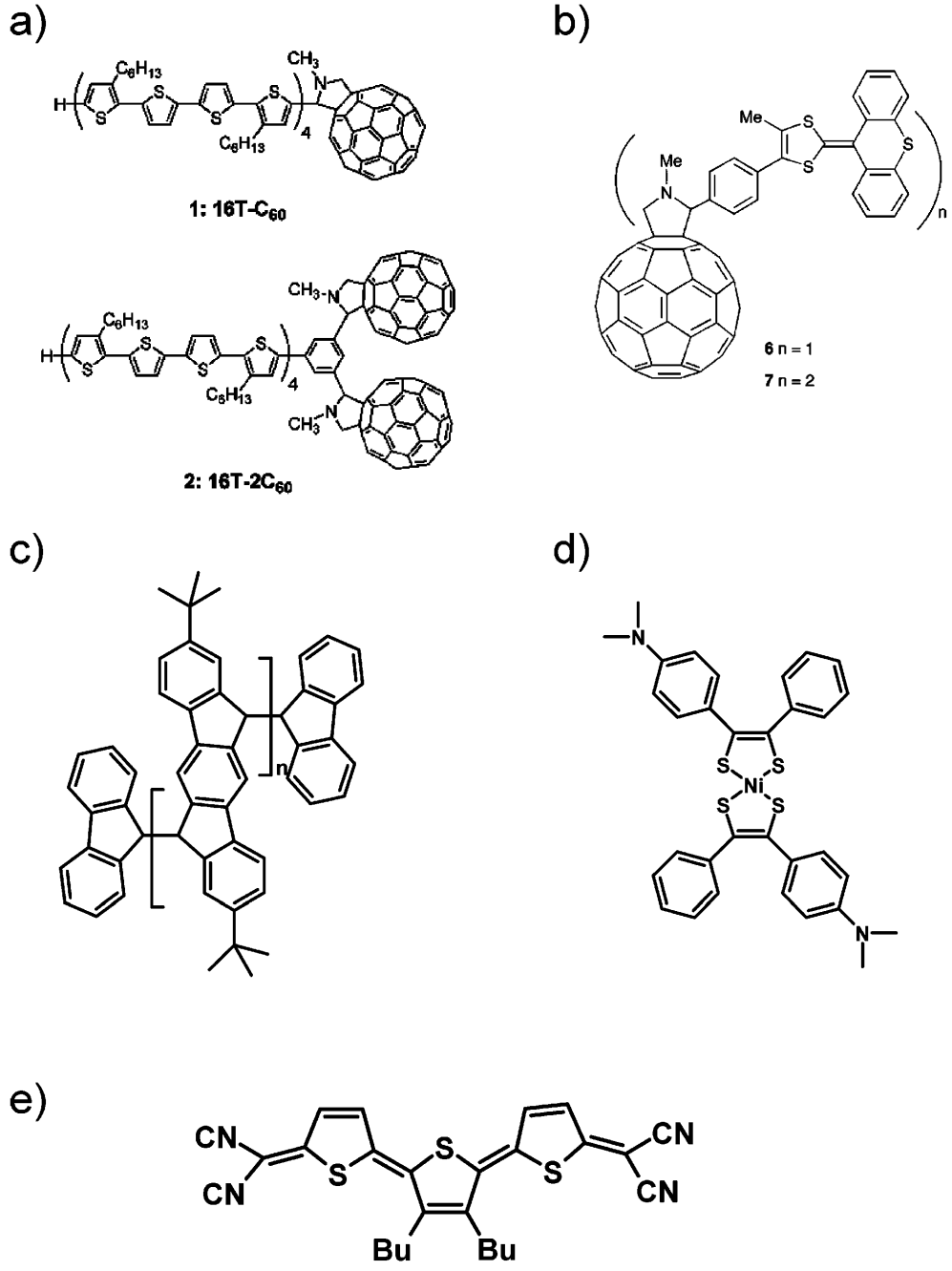

Figure 2.6: Ambipolar organic semiconductors: (a) oligothiophene/ fullerene dyad and oligothiophene/fullerene triad; (b) 9-(1,3- dithiol-2-ylidene)thioxanthene-C_{60} system (n = 6); (c) poly(3,9-di-*tert*-butylindeno[1,2-*b*]fluorene) (PIF); (d) the near-infrared absorbing dye bis[4-dimethylaminodithiobenzyl]nickel (nickel di- thiolene); (e) quinoidal terthiophene (DCMT).

2.3 Organic field effect transistors

Organic transistors are three terminal devices in which the current flow going between source and drain is modulated by a gate potential. A major difference with commonly used inorganic transistors is that no inversion layer is formed, but the conduction occurs by means of the majority carriers, which accumulate at the semiconductor/insulator interface.

Possible transistor structures are shown in fig 2.7 and 2.8. Both have a substrate which acts as mechanical support for the structure. Over it, there is an insulating dielectric film, under the which a gate contact is realized. Top contact structures have the semiconducting layer all over the insulator, with the source and drain contacts lying on top of the semiconductor; on the contrary, bottom contact devices have their contacts under the semiconductor layer. Moreover, both structures can also be realized without the substrate, if the mechanical support to the structure is provided by the insulating film itself (*free standing* devices).

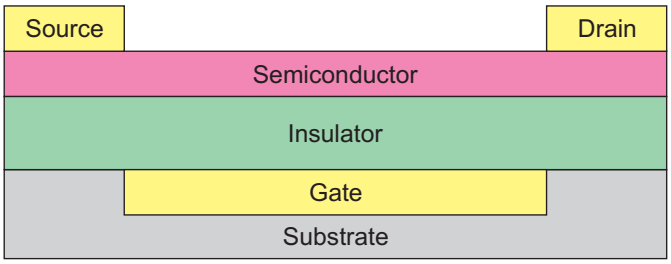

Figure 2.7: Top contact transistor structure.

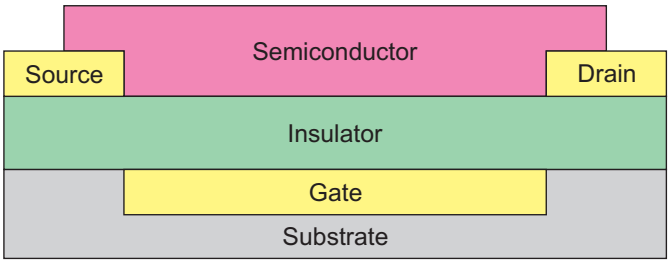

Figure 2.8: Bottom contact transistor structure.

2.3.1 Analytical derivation of the current

The determination, by analytical means, of the drain current for any applied voltages, has been object of extensive research over the years. For example, Horowitz *et al.* [HHB+98], assuming a constant mobility, developed a model which can describe the behavior of the

transistor in the linear and saturation region. Colalongo *et al.* [CRV04] and Li *et al.* [LK05] included also the effect of the variable range hopping mobility. The same effect has been taken into account by Calvetti *et al.* [CSKVC05] to model the current in the subthreshold region.

Other contributions to the modeling of the organic transistors, including the effects of traps and ambipolar devices, come also from Stallinga *et al.* in [SG06a, SG06b].

In this section, we will describe a model based on constant mobility and doping, in linear and saturation region. It is mostly based on [HHB+98]. Extensions to the model will be provided in the other sections of this thesis.

Device characteristics

Figure 2.9 shows the basilar structure for the transistor to be modeled. It is a free-standing bottom contact structure.

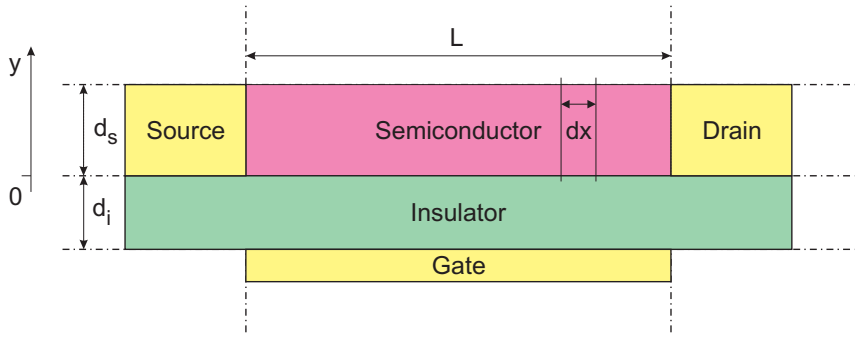

Figure 2.9: Geometry of the bottom contact transistor.

The length of the channel is L, its width is Z. The dielectric layer has thickness d_i and dielectric permittivity ε_i, with an associated capacity $C_\mathrm{i} = \varepsilon_\mathrm{i}/d_\mathrm{i}$ whereas the semiconductor film has thickness d_s and dielectric permittivity ε_s, with an associated capacity $C_\mathrm{s} = \varepsilon_\mathrm{s}/d_\mathrm{s}$. We will assume an n-type semiconductor with doping N and a density of free carriers $n_0 \simeq N$; an analogous model can be derived for p-type semiconductors changing the sign of the current and the applied voltages.

The threshold voltage of the device, which accounts for different workfunctions between the semiconductor and the gate and for possible charges located in the insulator or in the insulator/semiconductor interface, is set to be zero, to simplify notation. Since it just determines a shift of the gate voltages, non-zero threshold voltages can be included in the model substituting V_g with $V_\mathrm{g} - V_\mathrm{th}$.

Linear region

The total drain current I_d in the linear region ($V_\mathrm{d} < V_\mathrm{g}$) can be expressed as the sum of the bulk current originating from the free carriers in the semiconductor and the current determined by the carriers in the accumulation layer. Therefore

$$\frac{I_\mathrm{d}}{Z\mu} = -\left[Q_\mathrm{g}(x) + Q_0\right]\frac{\mathrm{d}V}{\mathrm{d}x}, \tag{2.4}$$

where Q_0 is the surface density of the free carriers given by

$$Q_0 = \pm q n_0 d_\mathrm{s}, \tag{2.5}$$

wherein the sign of the right hand side of (4.3) is that of charge of the carriers (plus for holes, minus for electrons). The surface density of the carriers in the accumulation layer $Q_\mathrm{g}(x)$ which forms as a capacitive effect, is

$$Q_\mathrm{g}(x) = -C_\mathrm{i}\left[V_\mathrm{g} - V_\mathrm{s}(x) - V(x)\right], \tag{2.6}$$

wherein $V_\mathrm{s}(x)$ is the ohmic drop in the bulk of the semiconductor, which can be generally neglected [HHK98], and $V(x)$ is the potential with respect to the source at the coordinate x. Then we can state that

$$\frac{I_\mathrm{d}}{Z\mu} = C_\mathrm{i}\left[V_\mathrm{g} + V_0 - V(x)\right]\frac{\mathrm{d}V}{\mathrm{d}x}, \tag{2.7}$$

where $V_0 = -Q_0/C_\mathrm{i}$. Equation (4.5) can be integrated from $V(x = 0) = 0\,\mathrm{V}$ to $V(x = L) = V_\mathrm{d}$ to obtain

$$I_\mathrm{d}\int_0^L \mathrm{d}x = I_\mathrm{d}L = Z\int_0^{V_\mathrm{d}} \mu C_\mathrm{i}\left(V_\mathrm{g} - V + V_0\right)\mathrm{d}V, \tag{2.8}$$

which leads, for a constant mobility, to

$$I_\mathrm{d} = \frac{Z}{L}\mu C_\mathrm{i}\left[\left(V_\mathrm{g} + V_0\right)V_\mathrm{d} - \frac{V_\mathrm{d}^2}{2}\right]. \tag{2.9}$$

The transconductance in the linear zone, from which the field effect mobility can be extracted, can then be defined as

$$g_\mathrm{m} = \left(\frac{\partial I_\mathrm{d}}{\partial V_\mathrm{g}}\right)_{V_\mathrm{d}=\mathrm{const}} = \frac{Z}{L}\mu C_\mathrm{i} V_\mathrm{d}. \tag{2.10}$$

Saturation region

When the drain voltage exceeds the effective gate voltage $V_\mathrm{d} > V_\mathrm{g}$ the accumulation layer near the drain changes to a depletion layer. The depletion layer will extend from a coordinate x_0 such that $V(x_0) = V_\mathrm{g}$ to the drain contact ($x = L$). At those coordinates where there is the depletion layer, the only contribution to the current is given by the free carriers, which are only in the volume of the semiconductor which has not been depleted. Then

$$I_\mathrm{d}\mathrm{d}x = Zq\mu n_0 \left[d_\mathrm{s} - W(x)\right] \mathrm{d}V, \tag{2.11}$$

wherein $W(x)$ is the width of the depletion region, which can be determined solving the Poisson equation [HHK98]

$$\frac{\mathrm{d}^2V}{\mathrm{d}y^2} = -\frac{qN}{\varepsilon_\mathrm{s}}, \tag{2.12}$$

subject to the boundary conditions

$$V(W) = 0, \tag{2.13}$$

$$\left.\frac{\mathrm{d}V}{\mathrm{d}y}\right|_{y=W} = 0. \tag{2.14}$$

The solution is

$$V(x) = \frac{qN}{2\varepsilon_\mathrm{s}} \left(x - W\right)^2. \tag{2.15}$$

Therefore, at the semiconductor/insulator interface the potential is

$$V_\mathrm{s} = \frac{qN}{2\varepsilon_\mathrm{s}} W^2. \tag{2.16}$$

The voltage drop at the insulator is

$$V_\mathrm{i} = \frac{qNW}{C_\mathrm{i}}, \tag{2.17}$$

so the following Kirchhoff equation holds:

$$V_\mathrm{g} + V(x) = V_\mathrm{i} + V_\mathrm{s}. \tag{2.18}$$

The width of the depletion region can then be determined as

$$W(x) = \frac{\varepsilon_\mathrm{s}}{C_\mathrm{i}} \left\{ \sqrt{1 + \frac{2C_\mathrm{i}^2 \left[V(x) - V_\mathrm{g}\right]}{qN\varepsilon_\mathrm{s}}} - 1 \right\}. \tag{2.19}$$

Since we have assumed that the accumulation layer extends up to a point where $V(x_0) = V_\mathrm{g}$ and since beyond x_0 only the non-depleted free carriers add to the current, we can write the latter as the sum of these two contributions

$$I_\mathrm{d} = \frac{Z}{L}\mu C_\mathrm{i} \int_0^{V_\mathrm{g}} \left(V_\mathrm{g} + V_0 - V\right) \mathrm{d}V + \frac{Z}{L}\mu q n_0 \int_{V_\mathrm{g}}^{V_\mathrm{dsat}} \left(d_\mathrm{s} - W\right) \mathrm{d}V. \tag{2.20}$$

The second integral on the right end side means that we account for all the free carriers which are in the semiconductor out of the depletion region, whose extension is $W(V_\mathrm{g}) = 0$ at the end of the accumulation layer and is $W(V_\mathrm{dsat}) = d_\mathrm{s}$ when the device reaches the saturation voltage. Changing the integration variable in (2.20) from V to W leads to

$$\begin{aligned} I_\mathrm{d} &= \frac{Z}{L}\mu C_\mathrm{i}\int_0^{V_\mathrm{g}}(V_\mathrm{g}+V_0-V)\,\mathrm{d}V + \frac{Z}{L}\mu\frac{q^2 n_0 N}{\varepsilon_\mathrm{s}}\int_0^{d_\mathrm{s}}(d_\mathrm{s}-W)\left(W+\frac{\varepsilon_\mathrm{s}}{C_\mathrm{i}}\right)\mathrm{d}W = \\ &= \frac{Z}{L}\mu\left[C_\mathrm{i}\left(\frac{V_\mathrm{g}^2}{2}+V_0 V_\mathrm{g}\right)+\frac{q^2 n_0 N}{\varepsilon_\mathrm{s}}\frac{d_\mathrm{s}^3}{6}\left(1+\frac{3C_\mathrm{s}}{C_\mathrm{i}}\right)\right], \end{aligned} \tag{2.21}$$

The pinch-off voltage V_p, i.e. the gate voltage for which the depletion region extension is equal to d_s, can be obtained by substituting $V_\mathrm{p} = V_\mathrm{g} - V(x)$ in (2.19). This leads to

$$V_\mathrm{p} = \pm\frac{qNd_\mathrm{s}^2}{2\varepsilon_\mathrm{s}}\left(1+2\frac{C_\mathrm{s}}{C_\mathrm{i}}\right) \simeq \frac{qNd_\mathrm{s}}{C_\mathrm{i}}, \tag{2.22}$$

wherein in the approximated expression the flat band voltage has been neglected and $d_\mathrm{s} \ll d_\mathrm{i}$ is reasonably assumed. If also $n_0 = N$ is assumed, then $V_\mathrm{p} = V_0$ and

$$I_\mathrm{dsat} = \frac{Z}{2L}\mu C_\mathrm{i}\left(V_\mathrm{g}-V_0\right)^2. \tag{2.23}$$

2.4 Mobility models

As different theories for charge transport in organic semiconductors have been developed, several models for the mobility in organic field effect transistors exist. Most of them determine a mobility which depends on the temperature and the electric field in the semiconductor. The most common are hereafter reported.

2.4.1 Multiple trap and release mobility

To determine the MTR mobility, the width of the accumulation layer is first estimated solving the Poisson equation

$$\frac{\mathrm{d}^2 V}{\mathrm{d}x^2} = \frac{qn_0}{\varepsilon_\mathrm{s}}\exp\frac{qV(x)}{kT}, \tag{2.24}$$

where n_0 is the density of carrier at the equilibrium. For a semi-infinite semiconductor, the carrier density $n(x)$ is found to be

$$n(x) \simeq \frac{2\varepsilon_\mathrm{s} kT}{q^2\left(x+L_\mathrm{a}\right)^2}, \tag{2.25}$$

where L_a is the effective length of the accumulation layer. Since the total induced charged is almost equal to the accumulation charge, then

$$\int_0^\infty qn(x)\,\mathrm{d}x \simeq C_\mathrm{i}V_\mathrm{g} \tag{2.26}$$

, and the effective length is

$$L_\mathrm{a} = \frac{2\varepsilon_\mathrm{s}kT}{qC_\mathrm{i}V_\mathrm{g}}. \tag{2.27}$$

This length is usually around a nanometer, so the accumulation layer lies within the first atomic monolayer.

The MTR model assumes that the charge σ, induced by the gate voltage V_g, splits in a free charge σ_f and a trapped charge σ_t, the latter being much greater than the former $\sigma_\mathrm{t} \gg \sigma_\mathrm{f}$. Therefore

$$\sigma_\mathrm{t} \simeq \sigma \simeq C_\mathrm{i}V_\mathrm{g}. \tag{2.28}$$

Boltzmann statistics says that the free charge is given by

$$\sigma_\mathrm{f} = \sigma_\mathrm{f0} \exp \frac{qV_\mathrm{s}}{kT}, \tag{2.29}$$

wherein $\sigma_\mathrm{f0} = qN_\mathrm{C} \exp\left[-\left(E_\mathrm{C} - E_\mathrm{F}\right)/kT\right]$ is the free charge at the equilibrium. N_C is the surface density of charge at the conduction band (for n-type semiconductor, valence band for p-type), whereas E_F is the Fermi level at the equilibrium. the measured mobility in the device is

$$\mu = \mu_0 \frac{\sigma_f}{\sigma}. \tag{2.30}$$

Therefore

$$E_\mathrm{C} - E_\mathrm{qF} = E_\mathrm{C} - E_\mathrm{F} - qV_\mathrm{s} = kT \ln \frac{q\mu_0 N_\mathrm{C}}{\mu C_\mathrm{i}V_\mathrm{g}}, \tag{2.31}$$

where E_qF is the quasi-Fermi level. The trapped charge σ_t depends on the density of states so that

$$\sigma_\mathrm{t} = \int_{-\infty}^{+\infty} N_\mathrm{tr}(E) f(E)\,\mathrm{d}E \tag{2.32}$$

and if the Fermi distribution function $f(E)$ is varying slow, it can be approximated with a step function so that

$$N_\mathrm{tr}(E) = \frac{\mathrm{d}\sigma_\mathrm{t}}{\mathrm{d}E}. \tag{2.33}$$

Assuming an exponential distribution of states, like

$$N_\mathrm{tr}(E) = \frac{N_\mathrm{t0}}{kT_\mathrm{c}} \exp\left(-\frac{E_\mathrm{C} - E}{kT_\mathrm{c}}\right), \tag{2.34}$$

wherein N_{t0} is the density of traps at the equilibrium and T_c is a characteristic temperature to account for the steepness of the exponential distribution. It follows that the trapped charge is

$$\sigma_t = \sigma_{t0} \exp \frac{qV_s}{kT_c} = \sigma_{t0} X, \tag{2.35}$$

wherein $\sigma_{t0} = N_{t0} \exp\left[-\left(-E_C - E_F\right)/kT_c\right]$ is the trapped charge at the equilibrium ($V_g = 0$) and $X = \exp\left(qV_s/kT_c\right)$. The free charge can be now written as

$$\sigma_f = \sigma_{f0} X^{\ell}, \tag{2.36}$$

where $\ell = T_c/T$. Combining the previous equations leads to

$$\mu_{FET} = \mu_0 \frac{N_C}{N_{t0}} \left(\frac{C_i V_g}{qN_{t0}}\right)^{\ell-1}. \tag{2.37}$$

When a threshold voltage V_{th} is included, the mobility can be written as

$$\mu_{FET} = \mu_0 \left(V_g - V_{th}\right)^{\alpha}, \tag{2.38}$$

where μ_0 and α are parameters usually extracted by means of fitting of the experimental data.

The MTR model does not always return correct results, as it does not include the effects of the grain nature of many organic materials, and it fails when the devices operate at low temperatures.

2.4.2 Grain Boundaries

Horowitz accounted for the grain nature of the semiconductor in the second part of his paper [HHH00]. His analysis assumes that the mobility is limited by the grain boundaries, in which the conductivity is much lower than in the crystal grain. This phenomenon has been already studied in the past for inorganic polycrystalline materials [OP80], whose mobility is found to increase with the size of the grains.

Being the grains and the boundaries connected in series, the mobility can be expressed as

$$\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{1}{\mu_g}, \tag{2.39}$$

where μ_b is the mobility of the boundary and μ_g is the mobility of the grain, whose size is supposed to be much larger than the boundary region. Between the grains, a back-to-back Schottky barrier is formed. Depending on the temperature, the current will be modeled differently, as thermionic emission dominates at high temperatures, whereas tunnel transport can dominate at lower ones.

At high temperatures, the current density through a boundary is given by [Hee68]

$$j_{\mathrm{b}} = \frac{1}{4} q n_{\mathrm{g}} \overline{v} \exp\left(\frac{-E_{\mathrm{b}}}{kT}\right) \left[\exp\left(\frac{qV_{\mathrm{b}}}{kT}\right) - 1\right], \tag{2.40}$$

where n_{g} is the carrier concentration in the grains, $\overline{v} = \sqrt{8kT/\pi m^*}$ is the electron thermal velocity, E_{b} is the barrier height and V_{b} is the voltage drop across a grain boundary. For grain boundaries of the same size, the source-drain voltage V_{d} is equally divided between the barriers and $V_{\mathrm{b}} = V_{\mathrm{d}}(l/L)$, where l is the length of the grain and L is the distance between source and drain. Equation (2.40) can be expanded to the first order for high T so that

$$j_{\mathrm{b}} \simeq q n_{\mathrm{g}} \mu_{\mathrm{b}} \frac{V_{\mathrm{d}}}{L}, \tag{2.41}$$

wherein the mobility in grain boundary is

$$\mu_{\mathrm{b}} = \mu_0 \exp\left(-\frac{E_{\mathrm{b}}}{kT}\right) \tag{2.42}$$

and

$$\mu_0 = \frac{q\overline{v}l}{8kT}, \tag{2.43}$$

where the factor 1/2 that appears between (2.40) and (2.43) is related to the two Schottky barriers at the sides of the grain boundary. It should be noted that the model can only qualitatively fit the experimental data [HHH00].

At low temperatures, the mobility can be modeled starting from tunnel transport in a metal-semiconductor junction [PS66]:

$$j_{\mathrm{b}} = j_0 \exp\left(\frac{qV_{\mathrm{b}}}{E_{00}}\right), \tag{2.44}$$

where

$$j_0 = j_{00}(T) \exp\left(-\frac{E_{\mathrm{b}}}{E_{00}}\right) \tag{2.45}$$

and

$$E_{00} = \frac{\hbar q}{2} \sqrt{\frac{N}{m^* \varepsilon_{\mathrm{s}}}}. \tag{2.46}$$

Equation (2.44) holds for $kT < E_{00}$ and can be expanded to the first order so that the mobility at low temperature becomes

$$\mu = \mu_{00}(T) \exp\left(-\frac{E_{\mathrm{b}}}{E_{00}}\right), \tag{2.47}$$

where $\mu_{00}(T)$ varies slowly with the temperature. For low temperatures, the mobility μ is no longer thermally-activated.

2.4.3 Variable range hopping

VRH mobility has already been introduced in section 2.1.2 and refers to [VM98]. Here further details are reported to obtain a power law for the mobility in organic transistors.

The model can be developed starting from the conductivity given by the percolation theory [AHL71] for a semiconductor with an exponential distribution of states. The conductivity is

$$\sigma(\delta, T) = \sigma_0 \left[\frac{\pi N_\mathrm{t} \delta (T_0/T)^3}{(2\alpha)^3 B_\mathrm{c} \Gamma(1 - T/T_0)\Gamma(1 + T/T_0)} \right]^{T_0/T} \tag{2.48}$$

where N_t is the number of states per unit volume, T_0 is a parameter that accounts for the width of the exponential distribution of states, δ is the carrier occupation at the temperature T, α is the effective overlap parameter, B_c is a parameter given by the percolation theory and Γ is the Γ-function. The carrier occupation δ is given by the Boltzmann distribution and is related to the gate-induced applied voltage by

$$\delta(x) = \delta_0 \exp\left[\frac{qV(x)}{kT} \right] \tag{2.49}$$

where δ_0 is the value of the distribution far from the semiconductor/insulator interface, where $V(x) = 0$. The relation between the potential and the $\delta(x)$ is determined by the Poisson equation. For an accumulation layer $\delta(x) \gg \delta_0$, the electric field is [HHD95]

$$\mathcal{E}^2(x) = 2kT_0 N_\mathrm{t} \delta(x)/\varepsilon_\mathrm{s}. \tag{2.50}$$

Gauss law gives the electric field at the interface as

$$\mathcal{E}(0) \simeq C_\mathrm{i} V_\mathrm{g}/\varepsilon_\mathrm{s}. \tag{2.51}$$

The current in the linear region for a transistor with source-drain potential V_d, semiconductor thickness t, width Z and length L is

$$I = \frac{WV_\mathrm{d}}{L} \int_0^t \sigma\left[\delta(x), T\right] \mathrm{d}x. \tag{2.52}$$

The field-effect mobility can be determined from the conductance as

$$\begin{aligned} \mu_\mathrm{FET} &= \frac{L}{C_\mathrm{i} W V_\mathrm{d}} \frac{\partial I}{\partial V_\mathrm{g}} = \\ &= \frac{\sigma_0}{q} \left[\frac{\pi (T_0/T)^3}{(2\alpha)^3 B_c \Gamma(1 - T/T_0)\Gamma(1 + T/T_0)} \right]^{T_0/T} \left[\frac{(C_\mathrm{i} V_\mathrm{g})^2}{2kT\varepsilon_\mathrm{s}} \right]^{T_0/T-1}, \end{aligned} \tag{2.53}$$

where it has been assumed that the semiconductor layer in large enough so that $V(t) = 0$. Again, including also the threshold voltage V_th, the effective mobility can be expressed as

$$\mu_\mathrm{FET} = \mu_0 \left(V_\mathrm{g} - V_\mathrm{th}\right)^\alpha. \tag{2.54}$$

A similar approach [LK05] allows the determination of the current in the triode an saturation region. Given the following coefficients,

$$\beta = \sigma_0 \sqrt{\frac{2\varepsilon_\mathrm{s} kT}{\delta_0 N_\mathrm{t}}} \frac{kT}{q\left(T - 2T_0\right)}, \tag{2.55}$$

$$\gamma = \frac{\left(2\alpha\right)^3 B_\mathrm{c} 2kT\varepsilon_\mathrm{s}}{C_\mathrm{i}^2 \left(T_0/T\right)^3 \sin\left(\pi T/T_0\right)}, \tag{2.56}$$

the current in the triode region is

$$I_\mathrm{d} = \beta \frac{W}{L} \left[\left(\frac{V_\mathrm{g} - V_\mathrm{fb}}{\gamma} \right)^{2T_0/T} - \left(\frac{V_\mathrm{g} - V_\mathrm{fb} - V_\mathrm{d}}{\gamma} \right)^{2T_0/T} \right] \tag{2.57}$$

and in the saturation region is

$$I_\mathrm{d} = \beta \frac{W}{L} \left(\frac{V_\mathrm{g} - V_\mathrm{fb}}{\gamma} \right)^{2T_0/T}. \tag{2.58}$$

2.4.4 Poole-Frenkel mobility

Poole-Frenkel mobility was first theorized in 1938 by Frenkel [Fre38] to explain the increase of conductivity in insulators and semiconductor when high fields are applied. Its form is

$$\mu = \mu_0 \exp\left(\gamma\sqrt{\mathcal{E}}\right), \tag{2.59}$$

where μ_0 and γ are parameters which depend on the physics of the considered system and $\mathcal{E}$ is the electric field. Poole-Frenkel mobility has been extensively studied for modeling charge transport in organic LEDs with disordered semiconductors [DPK96] [SPG89] [NDK+98], but it can also describe several experimental results for organic field effect transistors which show a variation of the mobility with the source-drain electric field [WFBD07] [HRG+07] [HN07].

In disordered organic semiconductors charge transport occurs mainly by hopping between nearby localized states which are induced by disorder. In a transistor, the physical effect of the source-drain electrical field is then to effectively reduce the hopping barrier. Assuming also a Coulomb potential type for hopping barrier, the hopping probability and the mobility, will have a dependence on electrical field which follows a Poole-Frenkel law like (2.59) with zero-field mobility μ_0 given by

$$\mu_0 = \mu_\mathrm{i} \exp\left(-\frac{\Delta}{kT}\right), \tag{2.60}$$

where μ_i is the intrinsic mobility at zero hopping barrier and Δ is the zero-field hopping barrier, also known as low field activation energy. Equation (2.59) can be rewritten as

$$\mu = \mu_\mathrm{i} \exp\left(\frac{\beta\sqrt{\mathcal{E}} - \Delta}{kT}\right). \tag{2.61}$$

Equation (2.61) has been modified by Gill [Gil72] to increase agreement with experimental data substituting T with an effective temperature T_{eff} so that

$$\frac{1}{T_{\text{eff}}} = \frac{1}{T} - \frac{1}{T_0}, \tag{2.62}$$

where T_0 is a fitting parameter.

2.5 Drift diffusion model

All the models proposed in this chapter are based on the drift-diffusion model. Even if it was originally developed for inorganic semiconductors, it has been extended to account for the organic semiconductors characteristics. In this section we report a more general description of the drift-diffusion model, providing the differential equations for the potential and the current, as well as the boundary conditions which are generally applied by conventional drift-diffusion solvers available, like Sentaurus by Synopsys [sen] or Atlas by Silvaco [atl] . The drift diffusion model is based on the Poisson equation:

$$\nabla \cdot (\varepsilon \nabla V) = q\left(n - p + N_{\text{A}} - N_{\text{D}} + n_{\text{tr}}\right), \tag{2.63}$$

where V is the potential in the structure, ε is the electric permittivity of the material, q is the elemental charge, n and p are the density of holes and electrons, respectively, N_{A} and N_{D} are the concentrations of ionized acceptors and donors, respectively, and n_{tr} is the density of occupied traps.

The continuity equations are

$$\nabla \cdot \mathbf{J}_n = +qR_n + q\frac{\partial n}{\partial t}, \tag{2.64}$$

$$\nabla \cdot \mathbf{J}_p = -qR_p - q\frac{\partial p}{\partial t}, \tag{2.65}$$

where $\mathbf{J}_n$ and $\mathbf{J}_p$ are the current densities and R_n and R_p are the net generation-recombination rate.

In the DD model the currents of electrons and holes are described as the sum of two contributions, namely a drift component, proportional to the electrostatic field $\boldsymbol{\mathcal{E}} = -\nabla V$ and a diffusion component, proportional to the gradient of the carrier density:

$$\mathbf{J}_n = -qn\mu_n \nabla V + qD_n \nabla n, \tag{2.66}$$

$$\mathbf{J}_p = -qp\mu_p \nabla V - qD_p \nabla p. \tag{2.67}$$

The density of carriers is described by means of Boltzmann statistics:

$$n = N_{\mathrm{C}} \exp\left(\frac{E_{\mathrm{qF},n} - E_{\mathrm{C}}}{kT}\right), \tag{2.68}$$

$$p = N_{\mathrm{V}} \exp\left(\frac{E_{\mathrm{V}} - E_{\mathrm{qF},p}}{kT}\right), \tag{2.69}$$

where N_{C} and N_{V} are the effective density of states, $E_{\mathrm{qF},n} = -q\Phi_n$ and $E_{\mathrm{qF},p} = -q\Phi_p$ are the quasi-Fermi energies for electrons and holes, Φ_n and Φ_p are the quasi-Fermi potentials, respectively. E_{C} and E_{V} are the conduction and valence band edges, defined as:

$$E_{\mathrm{C}} = -\chi - q\left(V - \phi_{\mathrm{ref}}\right), \tag{2.70}$$

$$E_{\mathrm{V}} = -\chi - E_{\mathrm{g}} - q\left(V - \phi_{\mathrm{ref}}\right), \tag{2.71}$$

where χ is the electron affinity and E_{g} the band gap. The reference potential ϕ_{ref} can be set equal to the Fermi potential of an intrinsic semiconductor. Then (2.68) and (2.69) become

$$n = n_{\mathrm{i}} \exp \frac{q\left(V - \phi_n\right)}{kT}, \tag{2.72}$$

$$p = n_{\mathrm{i}} \exp \frac{q\left(\phi_p - V\right)}{kT}, \tag{2.73}$$

where $n_{\mathrm{i}} = \sqrt{N_{\mathrm{C}} N_{\mathrm{V}}} \exp\left(-E_{\mathrm{g}}/2kT\right)$ is the intrinsic density.

2.5.1 Boundary conditions

Ohmic contacts

For ohmic contacts charge neutrality and equilibrium are assumed:

$$n_0 - p_0 = N_{\mathrm{D}} - N_{\mathrm{A}}, \tag{2.74}$$

$$n_0 p_0 = n_{\mathrm{i}}^2. \tag{2.75}$$

Applying Boltzmann statistics we obtain

$$V = \phi_{\mathrm{F}} + \frac{kT}{q} \operatorname{asinh}\left(\frac{N_{\mathrm{D}} - N_{\mathrm{A}}}{2n_{\mathrm{i}}}\right), \tag{2.76}$$

$$n_0 = \sqrt{\frac{\left(N_{\mathrm{D}} - N_{\mathrm{A}}\right)^2}{4} + n_{\mathrm{i}}^2} + \frac{N_{\mathrm{D}} - N_{\mathrm{A}}}{2}, \tag{2.77}$$

$$p_0 = \sqrt{\frac{\left(N_{\mathrm{D}} - N_{\mathrm{A}}\right)^2}{4} + n_{\mathrm{i}}^2} - \frac{N_{\mathrm{D}} - N_{\mathrm{A}}}{2}, \tag{2.78}$$

where n_0 and p_0 are the electron and hole equilibrium densities and ϕ_{F} is the Fermi potential at the contact, that is equal to the applied potential.

Schottky contacts

For Shottky contacts, the following boundary conditions hold:

$$V = \phi_{\mathrm{F}} + \frac{kT}{q} \ln\left(\frac{N_{\mathrm{C}}}{n_{\mathrm{i}}}\right), \tag{2.79}$$

$$\mathbf{J}_n \cdot \widehat{\mathbf{n}} = v_n \left(n - n_0^{\mathrm{B}}\right), \tag{2.80}$$

$$\mathbf{J}_p \cdot \widehat{\mathbf{n}} = v_p \left(p - p_0^{\mathrm{B}}\right), \tag{2.81}$$

$$n_0^{\mathrm{B}} = N_{\mathrm{C}} \exp\left(\frac{-q\Phi_{\mathrm{B}}}{kT}\right), \tag{2.82}$$

$$p_0^{\mathrm{B}} = N_{\mathrm{V}} \exp\left(\frac{-E_{\mathrm{g}} + q\Phi_{\mathrm{B}}}{kT}\right), \tag{2.83}$$

where ϕ_{F} is the Fermi potential at the contact, that is equal to the applied potential, $\Phi_{\mathrm{B}} = \phi_{\mathrm{m}} - \chi$ is the barrier height (the difference between the metal work-function ϕ_{m} and the electron affinity χ), v_n and v_p are the thermionic emission velocities and n_0^{B} and p_0^{B} are the equilibrium carrier densities. Fig. 2.10 shows a band diagram for a Schottky contact between an n-type semiconductor and metal, including also the difference between the metal and the semiconductor workfunction ϕ_{ms}.

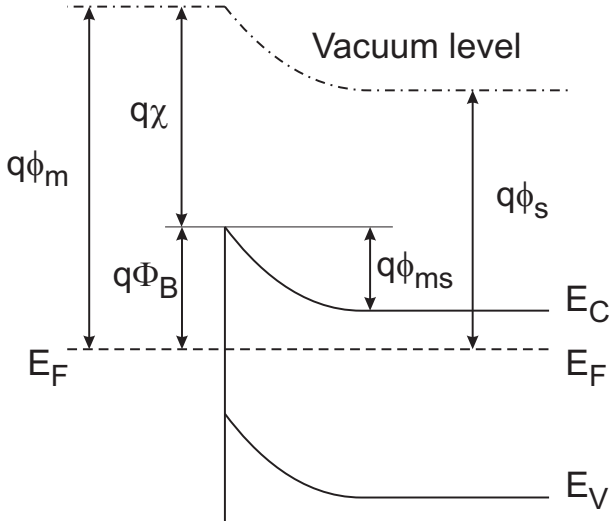

Figure 2.10: Band diagram for a Schottky contact between an n-type semiconductor and metal at the thermal equilibrium.

Gate contacts

For gate contacts, the boundary condition for the potential is

$$V = \phi_{\mathrm{F}} - \phi_{\mathrm{ms}}, \tag{2.84}$$

where ϕ_{F} is the Fermi potential at the contact and $\phi_{\mathrm{ms}} = \phi_{\mathrm{m}} - \phi_{\mathrm{s}}$ is the difference between the metal and the semiconductor work-functions.

Chapter 3

Cylindrical thin film transistors

The evolution of modern device electronics has led to the realization of devices with several geometries, in order to fulfill different requirements. For instance, cylindrical geometries are often used to obtain device size reduction without the occurrence of short channel effects like in surrounding gate devices [AP97] [KHG01]; recently, cylindrical geometries have been used for producing thin film transistors by means of organic semiconductors [LS] [MOC$^+$06] with the aim of obtaining distributed transistors on a long yarn-like structure suitable to be employed for e-textile applications. This field has recently attracted a strong interest for several novel applications that are potentially feasible thanks to this new technology: smart textiles systems for biomedical monitoring functions, man-machine interfaces and more could be, in the near future, realized using innovative electron devices and materials in a textile form.

Different approaches have led to textile transistors [MOC$^+$06] [BRK$^+$05], whose functionality is given by the particular topology and materials of the yarns used, or to weave patterned transistors [LS]. In [MOC$^+$06], an organic field effect transistor with a cylindrical geometry was developed with mechanical features and size fully compatible with the usual textile processes.

Each of the above mentioned devices was developed using organic materials but, in principle, these devices could also be produced with other semiconductors as, for instance, amorphous silicon.

To describe the electronic behavior of cylindrical thin film transistors, we have developed a model that can be applied to whatever kind of semiconductor, focusing in particular on the geometrical constraints that define the cylindrical geometry.

As any other organic thin film transistor (OTFT), the proposed devices operate in accumulation mode. In the following the usual models known for planar OTFTs [HHB$^+$98] [HHK98] will be adapted to the new cylindrical geometry. Section 3.1 describes the structure of the device; section 3.2 and 3.3 are dedicated, respectively, to the description of the

model in the linear and in the saturation regions. Finally, in section 3.4, experimental results for an organic semiconductor based device are shown and compared to the developed model.

3.1 Device structure

A schematic view of the device is shown in fig. 4.1. A metal cylinder, with radius r_g, acts as the gate electrode, and is surrounded by an insulating layer, with thickness d_i and outer radius r_i. The semiconductor surrounds the insulator with thickness d_s and outer radius r_s. The source and drain electrodes are the two external rings and their distance, i.e. the length of the conducting channel, is L.

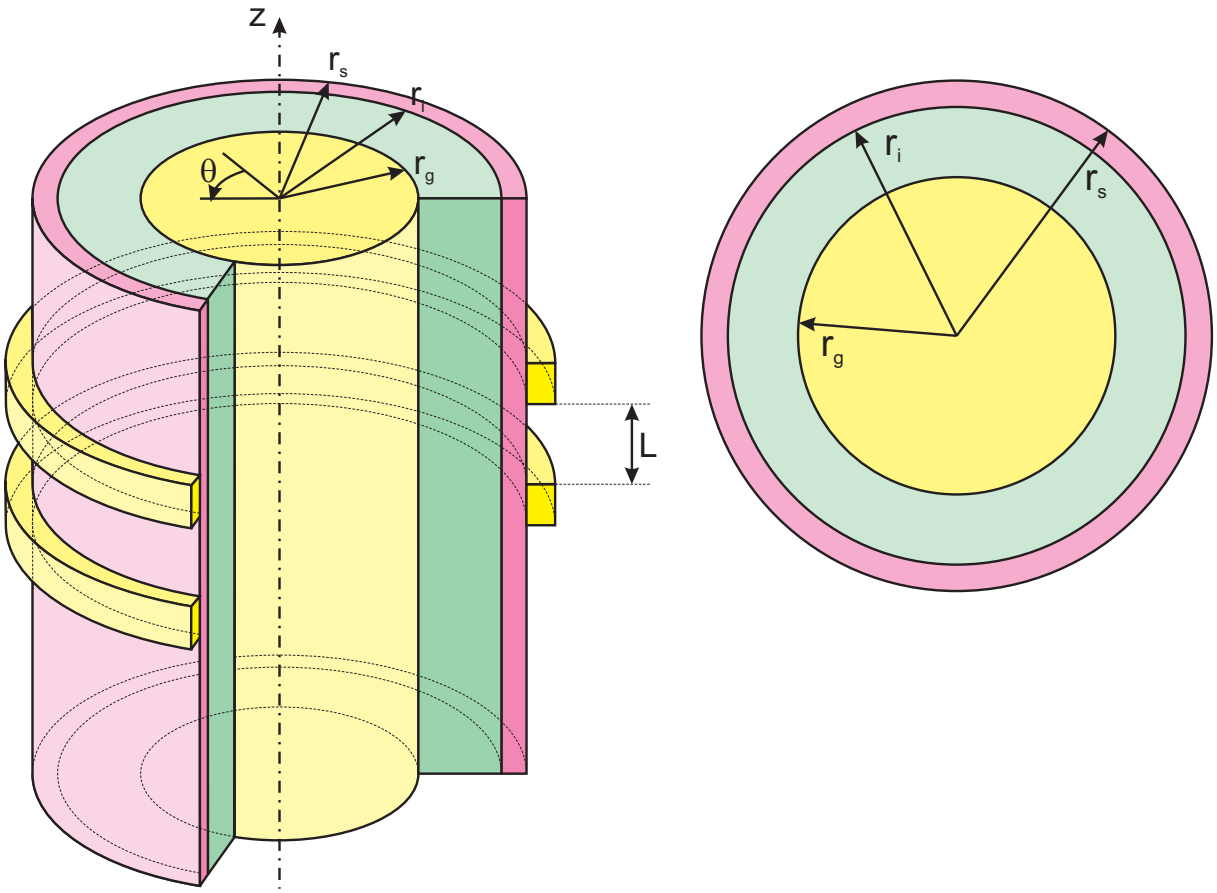

Figure 3.1: Geometry of the cylindrical TFT.

In the following we aim at showing the effects of the geometry on the device characteristics. All non geometrical parameters, used in the proposed simulations, are fixed to the values reported in table 3.1. These values are plausible for OTFTs. However, the model is general and is valid for different values of these parameters.

Parameter	*Symbol*	*Value*
Dielectric permittivity	ε_s	$3\varepsilon_0$
Insulator permittivity	ε_i	$3\varepsilon_0$
Density of free carriers	n_0	$10^{17}\,\mathrm{cm}^{-3}$
Semiconductor doping	N	$10^{17}\,\mathrm{cm}^{-3}$

Table 3.1: Simulation parameters.

3.2 Linear region

In this section the current-voltage equations of the devices, for the linear operation regime, will be determined. The main difference with a planar TFT is in the threshold voltage, which depends on the gate radius r_g as it is related to the number of free carriers available.

Let $\mathcal{D}$ be the domain determined by the annulus of inner radius r_i and outer radius r_s at any cross-section of the cylinder. Its area A is equal to

$$A = \pi \left(r_\mathrm{s}^2 - r_\mathrm{i}^2\right).$$

The conductivity $\overline{\sigma}$, averaged over the annulus surface, is given by (3.1)

$$\overline{\sigma} = \frac{q\mu}{A} \iint_{\mathcal{D}} n(r) r \,\mathrm{d}r \,\mathrm{d}\theta, \tag{3.1}$$

where q is the elemental charge, μ is the carrier mobility and $n(r)$ is the carrier density at radius r. The elemental resistance $\mathrm{d}R$ of an elemental segment $\mathrm{d}z$ is given by

$$\mathrm{d}R = \frac{1}{\overline{\sigma}} \frac{\mathrm{d}z}{A}. \tag{3.2}$$

For a TFT operating in the accumulation regime, in addition to the free carriers of the semiconductor, the density of which is uniform and equal to n_0, there are the carriers determined by the accumulation layer, localized at the interface between the insulator and the semiconductor, at radius r_i, with density $n_\mathrm{a}(r)$. Therefore, the total density of carriers is given by

$$n(r) = n_0 + n_\mathrm{a}(r). \tag{3.3}$$

The density $n_\mathrm{a}(r)$ can be determined considering the capacitor with inner radius r_g and outer radius r_i, which has a capacitance per area unit

$$C_\mathrm{i} = \frac{\varepsilon_\mathrm{i}}{r_\mathrm{i} \ln\left(\frac{r_\mathrm{i}}{r_\mathrm{g}}\right)}, \tag{3.4}$$

where ε_i is the dielectric permittivity of the insulator. The voltage V_c applied to the capacitor is given by

$$V_\mathrm{c} = V_\mathrm{g} - V_\mathrm{fb} - V(z), \tag{3.5}$$

where V_{g} is the gate voltage, V_{fb} is the flat band potential and $V(z)$ is the potential at the point z. Under the gradual channel approximation (i.e. the electric field along z is negligible with respect to that along r), $V(z)$ increases from 0 at the source to V_{d} at the drain.

The density n_{a} is then given by

$$n_{\mathrm{a}}(r) = \frac{C_{\mathrm{i}} V_{\mathrm{c}}}{q} \delta\left(r - r_{\mathrm{i}}\right), \tag{3.6}$$

where a Dirac distribution is used in order to account for the superficial distribution of the carriers accumulated at the interface between the insulator and the semiconductor.

The substitution of (3.6) in (3.3) and in (3.1) leads to

$$\overline{\sigma} = \frac{q\mu}{A} \iint_{\mathcal{D}} \left[n_0 + \frac{C_{\mathrm{i}} V_{\mathrm{c}}}{q} \delta\left(r - r_{\mathrm{i}}\right) \right] r \, \mathrm{d}r \, \mathrm{d}\theta = \frac{q\mu}{A} \left(A n_0 + \frac{Z C_{\mathrm{i}} V_{\mathrm{c}}}{q} \right), \tag{3.7}$$

where Z is the width of the channel and is equal to

$$Z = 2\pi r_{\mathrm{i}}. \tag{3.8}$$

Thus, the elemental resistance $\mathrm{d}R$ is given by

$$\mathrm{d}R = \frac{\mathrm{d}z}{q\mu \left(A n_0 + \frac{Z C_{\mathrm{i}} V_{\mathrm{c}}}{q} \right)}. \tag{3.9}$$

The drain current can I_{d} can be determined starting from

$$\mathrm{d}V = I_{\mathrm{d}} \mathrm{d}R = \frac{I_{\mathrm{d}} \mathrm{d}z}{q\mu \left(A n_0 + \frac{Z C_{\mathrm{i}} V_{\mathrm{c}}}{q} \right)}. \tag{3.10}$$

Integrating (3.10) between 0 and V_{d} with respect to V and between 0 and L with respect to z to obtain

$$I_{\mathrm{d}} = \frac{Z}{L} \mu C_{\mathrm{i}} \left[\frac{q n_0 A}{Z C_{\mathrm{i}}} V_{\mathrm{d}} + \left(V_{\mathrm{g}} - V_{\mathrm{fb}} \right) V_{\mathrm{d}} - \frac{V_{\mathrm{d}}^2}{2} \right]. \tag{3.11}$$

Since a non-zero drain current flows in the device even if no bias is applied to the gate, a threshold voltage V_{th} can be introduced:

$$V_{\mathrm{th}} = \pm \frac{q n_0 A}{Z C_{\mathrm{i}}} + V_{\mathrm{fb}} = \pm \frac{q n_0 \left(r_{\mathrm{s}}^2 - r_{\mathrm{i}}^2 \right) \ln\left(\frac{r_{\mathrm{i}}}{r_{\mathrm{g}}} \right)}{2\varepsilon_{\mathrm{i}}} + V_{\mathrm{fb}}. \tag{3.12}$$

The sign of the right hand side accounts for the type of majority carriers involved (holes or electrons). The drain current becomes

$$I_{\mathrm{d}} = \frac{Z}{L} \mu C_{\mathrm{i}} \left[\left(V_{\mathrm{g}} - V_{\mathrm{th}} \right) V_{\mathrm{d}} - \frac{V_{\mathrm{d}}^2}{2} \right] = \frac{2\pi}{L} \frac{\varepsilon_{\mathrm{i}}}{\ln\left(\frac{r_{\mathrm{i}}}{r_{\mathrm{g}}} \right)} \mu \left[\left(V_{\mathrm{g}} - V_{\mathrm{th}} \right) V_{\mathrm{d}} - \frac{V_{\mathrm{d}}^2}{2} \right]. \tag{3.13}$$

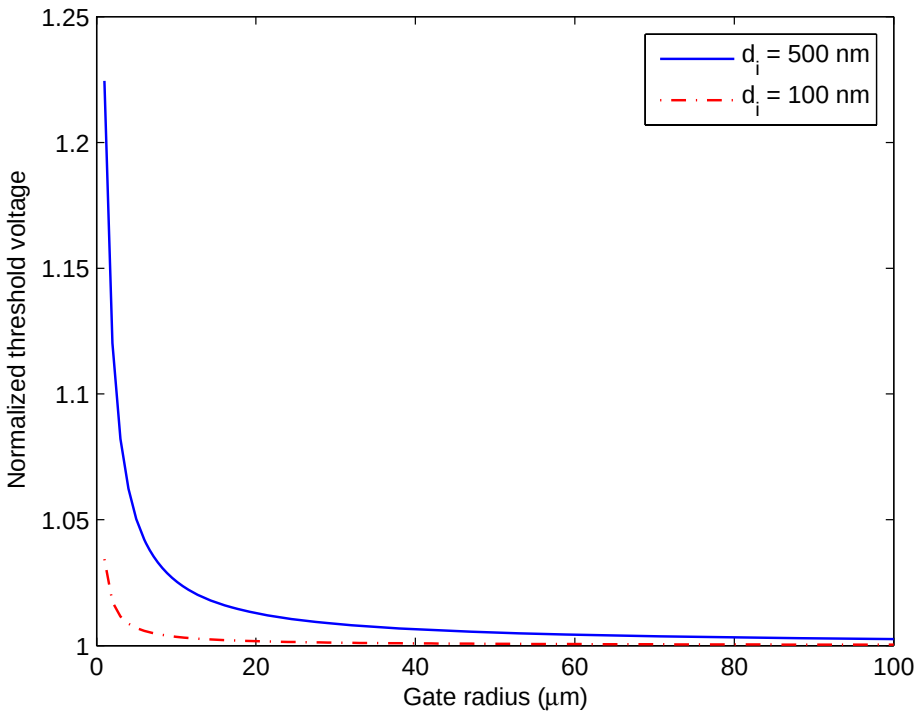

Figure 3.2: Normalized threshold voltage vs. gate radius for $V_{\mathrm{fb}} = 0\,\mathrm{V}$, and $d_{\mathrm{s}} = 50\,\mathrm{nm}$ and different insulator thicknesses. The curves are normalized with respect to the threshold voltages of planar devices with the same thicknesses.

Under the hypotheses that $r_{\mathrm{g}} \gg d_{\mathrm{s}}$ and $r_{\mathrm{g}} \gg d_{\mathrm{i}}$, which usually hold for any organic electron device, (3.12) can be simplified to obtain

$$V_{\mathrm{thp}} = \frac{q n_0 d_{\mathrm{s}} d_{\mathrm{i}}}{\varepsilon_{\mathrm{i}}} + V_{\mathrm{fb}}, \tag{3.14}$$

wherein V_{thp} is also the expression for the threshold voltage for a planar TFT as described by Horowitz in [HHB+98]. Fig. 3.2 shows the threshold voltages, for a cylindrical TFT as a function of the gate radius for different insulator thicknesses. The curves are normalized with respect to the threshold voltages of planar devices with the same thicknesses. It can be seen that the voltages of the cylindrical devices asymptotically tend to the ones of the planar TFTs (provided that the thickness of the insulator and the semiconductor are the same in both cases). Moreover, it can be noticed that increasing the insulator thickness also increases the difference of the threshold voltage shift between a cylindrical and a planar device.

One last remark is about contact resistance, which can reach values of MΩ [KSR+03], especially with organic polycristalline semiconductors. In a cylindrical TFT it is proportional to the length of the circumference with radius r_{s}, and can be included in the model

of (3.13) by substituting V_d with $V_\mathrm{d} - 2R_\mathrm{s}I_\mathrm{d}$ and V_g with $V_\mathrm{g} - R_\mathrm{s}I_\mathrm{d}$, where $R_\mathrm{s}I_\mathrm{d}$ is the ohmic drop due to one contact resistance R_s:

$$I_\mathrm{d} = \frac{2\pi\varepsilon_\mathrm{i}\mu}{L\ln\left(\frac{r_\mathrm{i}}{r_\mathrm{g}}\right)}\left\{\left[(V_\mathrm{g} - R_\mathrm{s}I_\mathrm{d}) - V_\mathrm{th}\right](V_\mathrm{d} - 2R_\mathrm{s}I_\mathrm{d}) - \frac{(V_\mathrm{d} - 2R_\mathrm{s}I_\mathrm{d})^2}{2}\right\}. \tag{3.15}$$

A planar device can have any contact width, so its contact resistance can be small; in a cylindrical device this could be achieved only increasing r_s, which cannot be performed without affecting also the other parameters of the device.

3.3 Saturation region

When the TFT enters the saturation region, the channel gradually depletes, so that no free carriers are available in the depletion region and the accumulation layer is limited to the part of the interface between insulator and semiconductor which has not been depleted. Let r_d be the radius of the extremity of depletion region and W be its width, so that

$$r_\mathrm{d} = r_\mathrm{i} + W. \tag{3.16}$$

To determine the extension of the depletion region, so that one can find the voltage drop φ_s across the semiconductor, the Poisson equation in (3.17) must be solved. Equations (3.18) and (3.19) show the boundary conditions, i.e. both the electric field and the potential must be null at the extremity of the depletion region, located at $r = r_\mathrm{d}$.

$$\frac{1}{r}\frac{\partial}{\partial r}r\frac{\partial}{\partial r}V(r) = \frac{qN}{\varepsilon_\mathrm{s}}, \tag{3.17}$$

$$\left.\frac{\partial V(r)}{\partial r}\right|_{r=r_\mathrm{d}} = 0, \tag{3.18}$$

$$V\left(r_\mathrm{d}\right) = 0. \tag{3.19}$$

The density of carriers N is equal to the doping of the semiconductor and can be greater than n_0, ε_s is the dielectric permittivity of the semiconductor. The solution for the Poisson equation is shown in (3.20).

$$V(r) = \frac{qN}{4\varepsilon_\mathrm{s}}\left(r^2 - r_\mathrm{d}^2\right) - \frac{qNr_\mathrm{d}^2}{2\varepsilon_\mathrm{s}}\left(\ln r - \ln r_\mathrm{d}.\right) \tag{3.20}$$

The expression for the electrostatic potential $V(r)$ is different from its planar analogous, here named $V_\mathrm{p}(x)$, which only depends on the distance x from the interface between the insulator and the semiconductor and, as reported by [Sze81], is given by

$$V_\mathrm{p}(x) = \frac{qN}{2\varepsilon_\mathrm{s}}(x - W)^2. \tag{3.21}$$

The potential V_s at the interface between the insulator and the semiconductor is

$$V_\mathrm{s} = V\left(r_\mathrm{i}\right) = \frac{qN}{4\varepsilon_\mathrm{s}}\left(r_\mathrm{i}^2 - r_\mathrm{d}^2\right) - \frac{qNr_\mathrm{d}^2}{2\varepsilon_\mathrm{s}}\left(\ln r_\mathrm{i} - \ln r_\mathrm{d}\right) \tag{3.22}$$

and (3.20) can be written again as

$$V(r) = V_\mathrm{s}\left[1 - \frac{qN}{4\varepsilon_\mathrm{s}}\left(r_\mathrm{i}^2 - r^2\right) + \frac{qNr_\mathrm{d}^2}{2\varepsilon_\mathrm{s}}\left(\ln r_\mathrm{i} - \ln r\right)\right]. \tag{3.23}$$

Since (3.16) holds, the potential V_s becomes

$$V_\mathrm{s} = \frac{qN}{4\varepsilon_\mathrm{s}}\left(-2Wr_\mathrm{i} - W^2\right) + \frac{qN\left(r_\mathrm{i}^2 + 2Wr_\mathrm{i} + W^2\right)}{2\varepsilon_\mathrm{s}}\ln\left(1 + \frac{W}{r_\mathrm{i}}\right). \tag{3.24}$$

To go further in the development of the model one must proceed with some approximations: if one supposes $W \ll r_\mathrm{i}$, which is reasonable for the devices developed so far, (3.24) can be expanded in a Taylor series up to the second order to obtain

$$V_\mathrm{s} = \frac{qN}{2\varepsilon_\mathrm{s}}W^2, \tag{3.25}$$

which is also the expression for the potential at the interface semiconductor/insulator for a planar FET.

The voltage drop on the insulator V_i is given by

$$V_\mathrm{i} = \frac{Q_\mathrm{s}}{C_\mathrm{i}} = \frac{qN}{2r_\mathrm{i}C_\mathrm{i}}\left(r_\mathrm{d}^2 - r_\mathrm{i}^2\right) = \frac{qN}{2r_\mathrm{i}C_\mathrm{i}}\left(W^2 + 2r_\mathrm{i}W\right), \tag{3.26}$$

where Q_s is the charge per area unit in the depletion region.

In order to find the width of the depletion region W, we need to solve

$$-V_\mathrm{g} - V_\mathrm{fb} + V(z) = V_\mathrm{i} + V_\mathrm{s}. \tag{3.27}$$

An analytical solution can be found under the same hypotheses of (3.25), to obtain

$$W = \frac{-\frac{1}{C_\mathrm{i}} + \sqrt{\frac{1}{C_\mathrm{i}^2} + \left(\frac{1}{\varepsilon_\mathrm{s}} + \frac{1}{r_\mathrm{i}C_\mathrm{i}}\right)\frac{2[-V_\mathrm{g} - V_\mathrm{fb} + V(z)]}{qN}}}{\frac{1}{\varepsilon_\mathrm{s}} + \frac{1}{r_\mathrm{i}C_\mathrm{i}}}. \tag{3.28}$$

The differences with the planar analogous are in the term $1/r_\mathrm{i}C_\mathrm{i}$, which is not present, and in the expression for the capacitance for area unit, which is a function of the gate radius and the insulator thickness. Fig. 3.3 shows the width W of the depletion region versus the insulator thickness d_i. For a cylindrical device, W is always smaller than the width of a planar device with the same thickness. Both widths become null as the thickness tends to infinity.

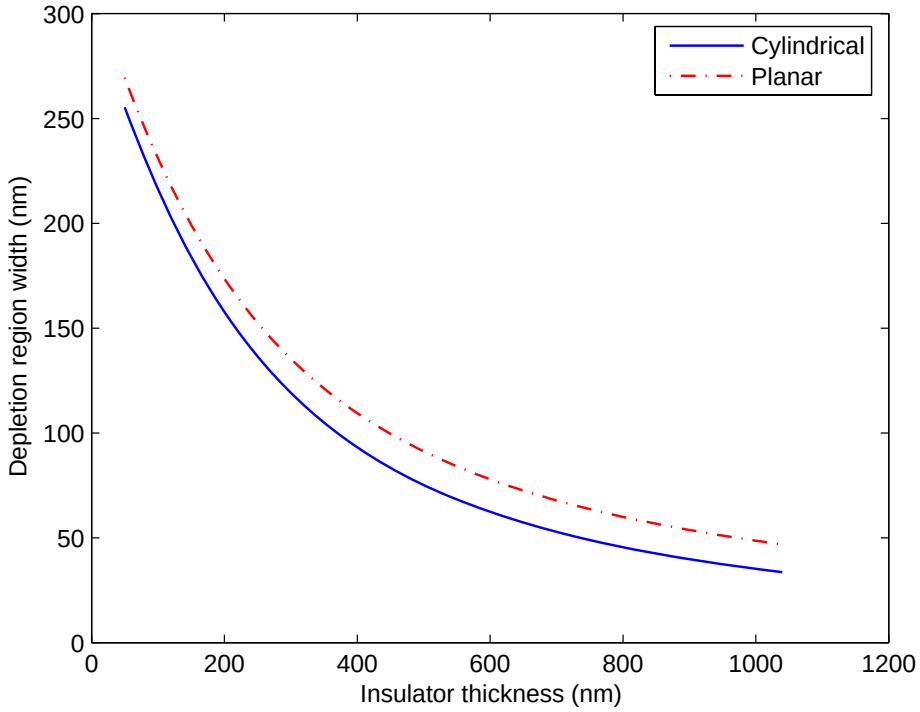

Figure 3.3: Depletion region vs. insulator thickness. A planar device and a cylindrical device, but with $r_{\mathrm{g}} = 1\,\mu\mathrm{m}$, are shown. $-V_{\mathrm{g}} + V(z) = 10\,\mathrm{V}$, $V_{\mathrm{fb}} = 0$.

Figure 3.4 shows the width of the depletion region as a function of the gate radius. As for the threshold voltage, it tends asymptotically to the width of a planar TFT. Figure 3.5 shows the behavior of the TFT. For those values of z where there is no depletion region, the value of $\mathrm{d}R$ is still given by (3.9) and the accumulation layer extends from the source up to where $V(z_{\mathrm{a}}) = V_{\mathrm{g}}$; instead, for those values of z where the depletion region is present, only the free carriers within the volume which has not been depleted (i.e. between radius r_{d} and r_{s}) contribute to the current. In this case, the resulting elemental resistance is given by

$$\mathrm{d}R = \frac{\mathrm{d}z}{q\mu n_0 \pi \left(r_{\mathrm{s}}^2 - r_{\mathrm{d}}^2\right)}. \tag{3.29}$$

Thus,

$$\mathrm{d}V = I_{\mathrm{d}}\mathrm{d}R = \frac{I_{\mathrm{d}}\mathrm{d}z}{q\mu n_0 \pi \left(r_{\mathrm{s}}^2 - r_{\mathrm{d}}^2\right)}. \tag{3.30}$$

Differentiating W with respect to V gives

$$\mathrm{d}W = \frac{\mathrm{d}V}{qN\left[\left(\frac{1}{\varepsilon_{\mathrm{s}}} + \frac{1}{r_{\mathrm{i}}C_{\mathrm{i}}}\right)W + \frac{1}{C_{\mathrm{i}}}\right]}. \tag{3.31}$$

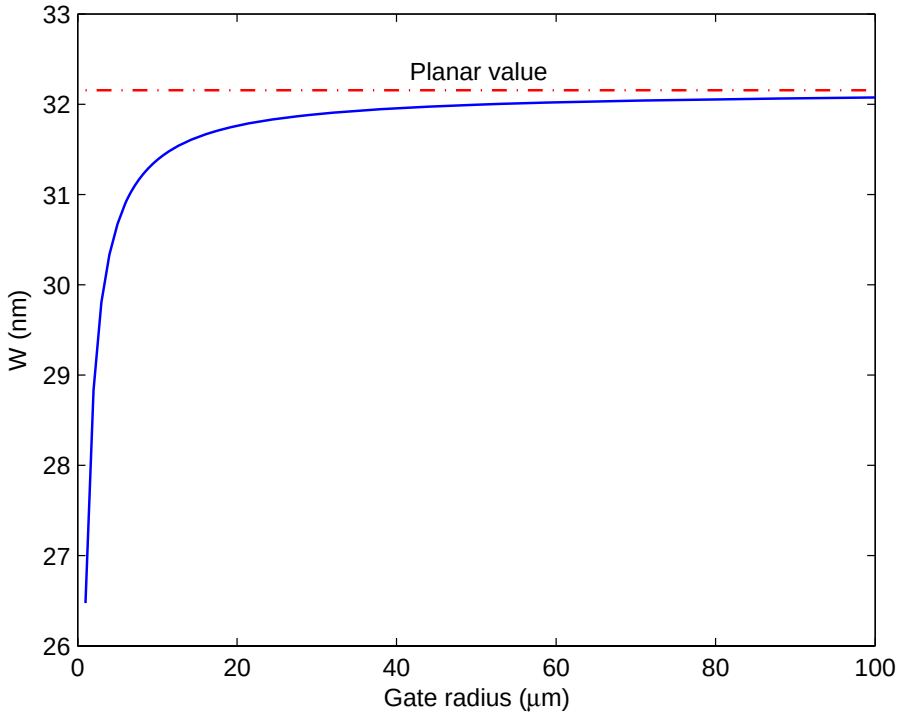

Figure 3.4: Width of the depletion region vs. gate radius for $-V_{\mathrm{g}}+V(z) = 10\,\mathrm{V}$, $V_{\mathrm{fb}} = 0\,\mathrm{V}$, $d_{\mathrm{i}} = 500\,\mathrm{nm}$. The depletion region for a planar TFT with the same insulator characteristics is equal to $W = 32.15\,\mathrm{nm}$.

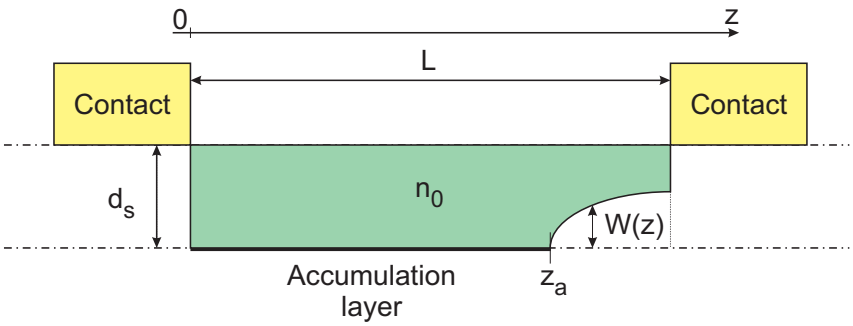

Figure 3.5: Section of the TFT transistor. The depletion region at the lower right corner has a width $W(z)$. The accumulation layer extends up to z_{a}.

Substituting (3.31) and (3.16) into (3.30) leads to

$$\mathrm{d}W = \frac{I_{\mathrm{d}}\mathrm{d}z}{q^2 N \mu n_0 \pi \left[\left(\frac{1}{\varepsilon_{\mathrm{s}}} + \frac{1}{r_{\mathrm{i}} C_{\mathrm{i}}}\right) W + \frac{1}{C_{\mathrm{i}}}\right] \left[r_{\mathrm{s}}^2 - (r_{\mathrm{i}} + W)^2\right]}. \tag{3.32}$$

As in [HHB+98] [BJDM97], to obtain the saturation current I_{dsat}, one must sum the contribution given by the integration of (3.10) up to $V(z_{\mathrm{a}}) = V_{\mathrm{g}}$, with that given by the

integration of (3.30), between z_a and the drain contact, so

$$I_{dsat} = \frac{Z}{L}\mu C_i \int_0^{V_g} (V_g - V_{th} - V)\, dV + \frac{1}{L}\int_{V_g}^{V_d} q\mu n_0 \pi \left(r_s^2 - r_d^2\right) dV. \tag{3.33}$$

Changing the integration variable in the second addend in (3.33) from V to W, with $W(V_g) = 0$ and $W(V_d) = r_s - r_i = d_s$, leads to

$$\begin{aligned} I_{dsat} = {} & \frac{Z}{L}\mu C_i \int_0^{V_g} (V_g - V_{th} - V)\, dV + \\ & + \frac{1}{L}\left\{ \int_0^{d_s} q\mu n_0 \pi \left[r_s^2 - (r_i + W)^2\right] qN \left[\left(\frac{1}{\varepsilon_s} + \frac{1}{r_i C_i} \right) W + \frac{1}{C_i} \right] dW \right\}. \end{aligned} \tag{3.34}$$

Integrating:

$$\begin{aligned} I_{dsat} = {} & \frac{Z}{L}\mu C_i \left(\frac{V_g^2}{2} - V_{th} V_g \right) + \\ & + \frac{q^2 \mu n_0 N \pi}{L} \left\{ \frac{d_s}{C_i} \left[\left(r_s^2 - r_i^2\right) - d_s r_i - \frac{d_s^2}{3} \right] + \right. \\ & \left. + \frac{d_s^2}{2} \left(\frac{1}{\varepsilon_s} + \frac{1}{r_i C_i} \right) \left[\left(r_s^2 - r_i^2\right) - \frac{4 d_s r_i}{3} - \frac{d_s^2}{2} \right] \right\}. \end{aligned} \tag{3.35}$$

The pinch-off voltage V_p, i.e. the voltage for which the depletion region extension is equal to d_s, can be obtained substituting $V_p = V_g - V(z)$ in (3.28). This leads to

$$V_p = \pm qN \left[\frac{d_s^2}{2} \left(\frac{1}{\varepsilon_s} + \frac{1}{r_i C_i} \right) + \frac{d_s}{C_i} \right]. \tag{3.36}$$

The saturation current becomes:

$$\begin{aligned} I_{dsat} = {} & \frac{Z}{L}\mu C_i \left(\frac{V_g^2}{2} - V_{th} V_g \right) + \frac{Z}{L}\mu C_i \frac{V_p V_{th}}{2} + \\ & + \frac{q\mu n_0 \pi}{L} \left[-V_p d_s r_i - V_p \frac{d_s^2}{2} - \frac{qN d_s^3 r_i}{6\varepsilon_s} \right]. \end{aligned} \tag{3.37}$$

Under the hypotheses that $n_0 = N$ and $r_i \gg d_s$, the threshold voltage is equal to the pinch-off voltage, $V_p = V_{th}$ and all the terms in the second row of (3.37) can be neglected, to obtain the equation:

$$I_{dsat} = \frac{Z}{2L}\mu C_i \left(V_g - V_{th}\right)^2. \tag{3.38}$$

Figure 3.6 shows a simulation of the $I_d - V_d$ characteristics of a cylindrical device and a planar device, with same insulator and semiconductor thicknesses. The different behavior is primarily due to the different threshold voltages of the devices. Increasing the gate radius as well as reducing the insulator thickness would cause the curves to be more similar.

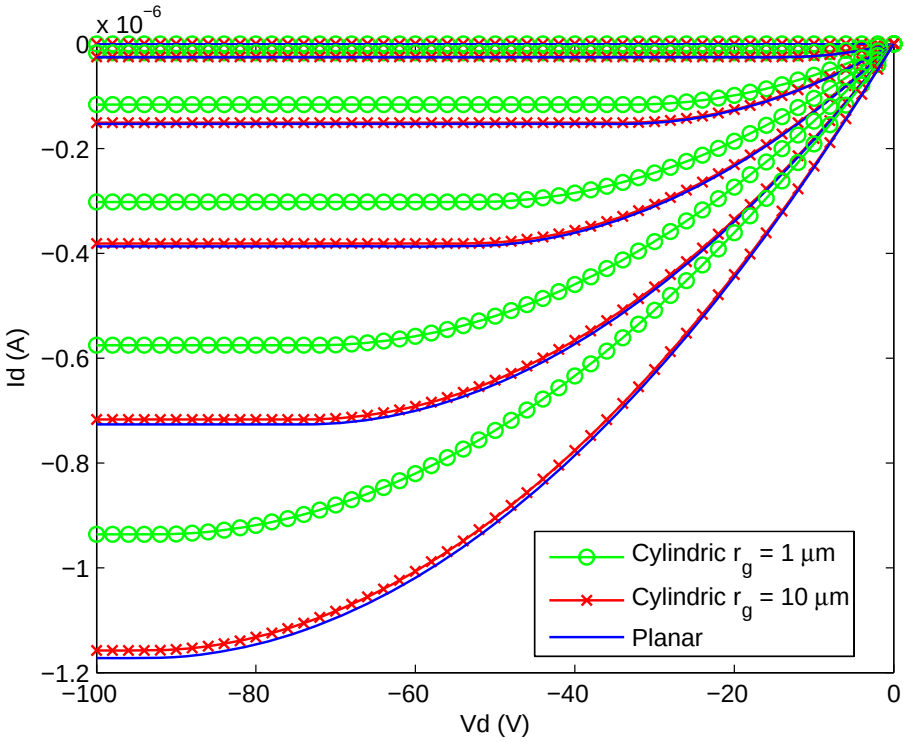

Figure 3.6: $I_d - V_d$ characteristics simulated for cylindrical devices with $r_g = 1\,\mu$m and $r_g = 10\,\mu$m and a planar device. Both have $V_{fb} = 0\,$V, $d_i = 500\,$nm, $d_s = 20\,$nm. It is supposed that the devices have $Z/L = 1$. Characteristics are simulated for a variation of the gate voltage from $0\,$V to $-100\,$V in steps of $-20\,$V.

3.4 Experimental results

Cylindrical transistors have been realized by means of high vacuum evaporation of pentacene on fibers with an inner core of copper, covered by an insulating layer of polyimide. In particular, the gate of the developed structure is a copper cylinder with radius $r_g = 22.5\,\mu$m and is uniformly surrounded by a polyimide insulating layer with a thickness $d_i = 500\,$nm. The organic semiconductor, pentacene, was evaporated over the polyimide, with an estimated thickness $d_s = 50\,$nm. Since, during the evaporation process, the wire was not rotated with respect to the crucible, only about half of the device was uniformly covered with the semiconductor, therefore the width of the conducting channel Z is also half of the one reported in (3.8).

Source and drain contacts have been realized with gold as well as a conductive polymer, Poly(ethylene-dioxythiophene)/PolyStyrene Sulfonate (PEDOT:PSS), by means of high vacuum evaporation and soft lithography, respectively. Figure 4.11 shows the $I_d - V_g$ curves of the experimental data, measured by a HP4155 semiconductor parameter ana-

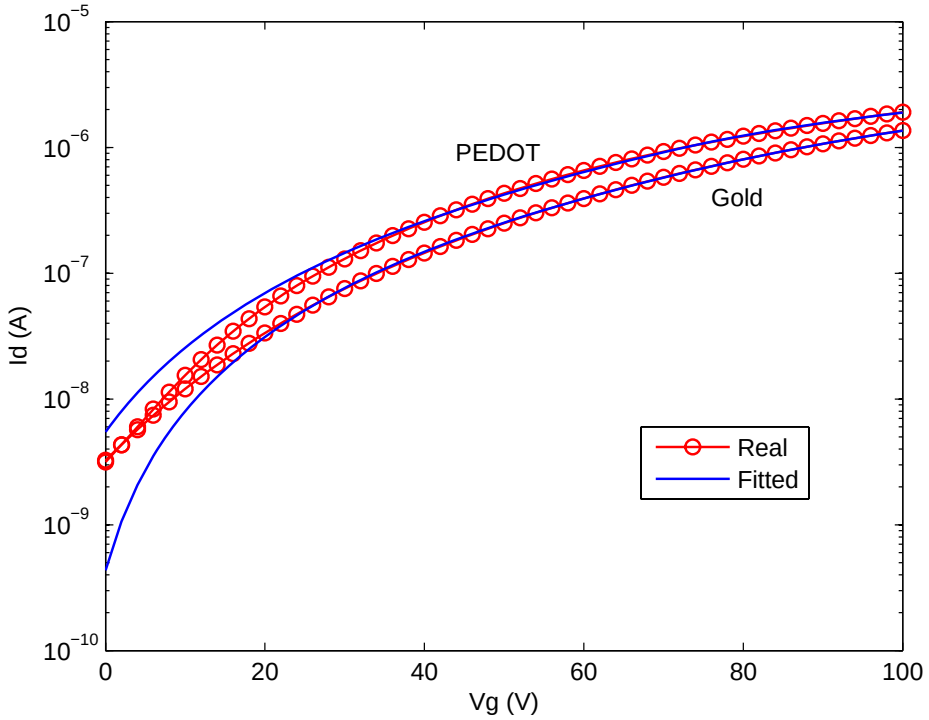

Figure 3.7: $I_\mathrm{d} - V_\mathrm{g}$ characteristics for devices with gold and PEDOT contacts. The drain voltage is kept at $V_\mathrm{d} = -100\,\mathrm{V}$.

lyzer, together with the ones of the fitted data, whereas fig. 3.9 and 3.10 show the $I_\mathrm{d} - V_\mathrm{d}$ curves.

To give an estimate of the electrical parameters of the devices, a least squares fitting of the experimental data with equations (3.15) and (3.37) was performed. In sections 2.4.1 and 2.4.3 it has already been pointed out that in organic devices the mobility can depend on the electric field determined by the gate bias. A semi-empirical power law was found for both the variable range hopping and the multiple trap and release model:

$$\mu = \kappa \left(V_\mathrm{g} - V_\mathrm{th}\right)^\alpha . \tag{3.39}$$

For the MTR model, for example, a p-type transistor would have the following field dependent mobility:

$$\mu = \mu_0 \frac{N_\mathrm{V}}{N_\mathrm{t0}} \left(\frac{C_\mathrm{i} \left(V_\mathrm{g} - V_\mathrm{th}\right)}{q N_\mathrm{t0}} \right)^{\frac{T_\mathrm{c}}{T} - 1} , \tag{3.40}$$

where N_t0 is the total surface density of traps, T_c is a characteristic temperature and N_V is the effective density of states at the band edge. Equation (3.40) shows the same gate-voltage dependency of (3.39) and can be heuristically extended to cylindrical TFTs, provided that (3.4) and (3.12) are used as capacitance per area unit and threshold voltage,

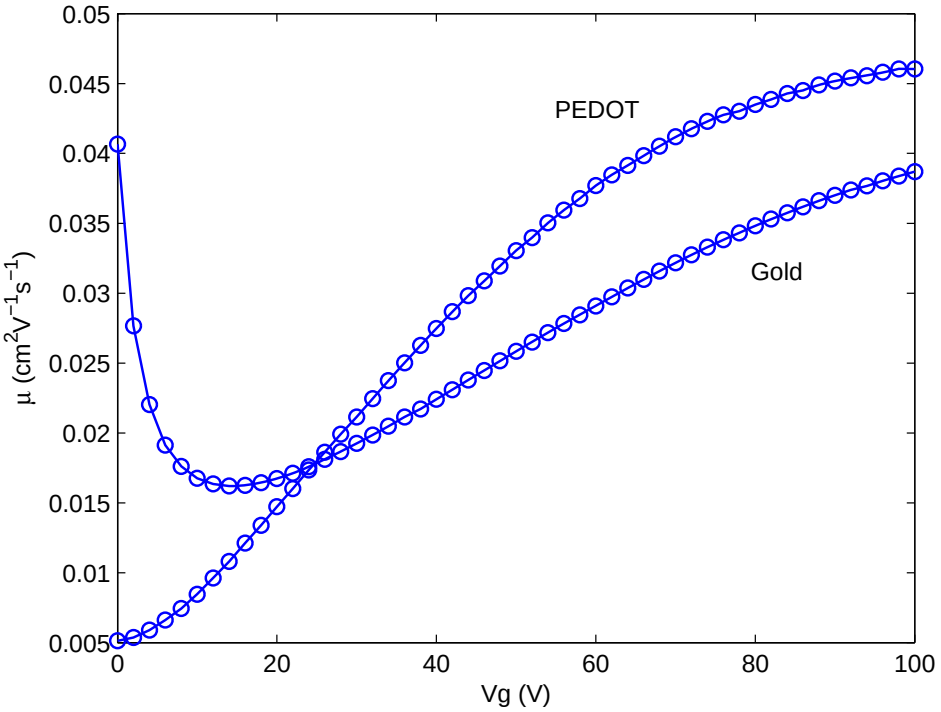

Figure 3.8: Mobility vs. gate voltage. The drain voltage is kept at $V_{\mathrm{d}} = -100\,\mathrm{V}$.

respectively. It is worth noting that, since the mobility only depends on the gate voltage, the model developed in section 3.2 and 3.3, where the integrations are performed with respect only to drain voltage, still holds. A more rigorous derivation of the field dependent mobility for cylindrical transistors would require the resolution of the Poisson equation and the current equation for the device in the accumulation region considering a field-dependent conductance.

To give an estimate of the threshold voltage, $I_{\mathrm{d}} - V_{\mathrm{g}}$ data have been fitted with equations (3.37), together with (3.39) which accounts for the field dependent mobility. Moreover, to determine possible deviances from (3.39), the mobility has been directly extracted from the transfer characteristic considering the previously estimated threshold voltage and is shown in figure 4.14. Finally the contact resistance, which could also be field dependent [NSGJ03], has been extracted from the output curves. However, it was supposed to be constant not to introduce too many independent parameters in the fitting procedure. The extracted parameters are reported in table 3.4.

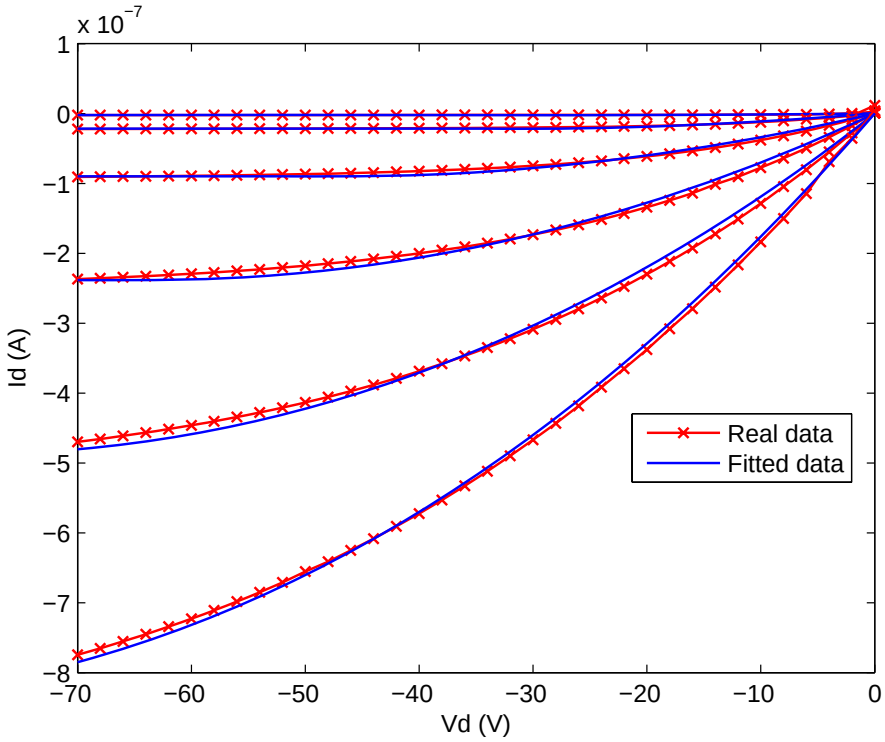

Figure 3.9: $I_\mathrm{d} - V_\mathrm{d}$ characteristic for device with gold contacts. The gate voltage is kept at $V_\mathrm{g} = -100\,\mathrm{V}$.

Device	V_th (V)	κ	α	R_s (MΩ)	$I_\mathrm{on}/I_\mathrm{off}$
Au	5.1	$1.9 \cdot 10^{-3}$	0.66	7.4	$7 \cdot 10^3$
PEDOT	13.8	$0.96 \cdot 10^{-3}$	0.85	2.3	$3 \cdot 10^3$

Table 3.2: Electrical parameters of the devices.

3.5 Summary

In this chapter we have developed a model which describes the electrical characteristics of TFTs with cylindrical geometry. Under reasonable approximations (i.e insulator and semiconductor thicknesses are much smaller than the gate radius), the model becomes very similar to its known planar analogous, provided that parameters like channel width and capacitance per area unit are changed consistently. Differences between the two geometries become more important as the gate radius is reduced. The insulator thickness too can have an important role in the determination of the threshold voltage and the width of the depletion region, leading to significative differences in the output curves. Experimental results have been fitted with the proposed model, showing that it can adequately describe the physical behavior and the electrical characteristics of the cylindrical devices. Future

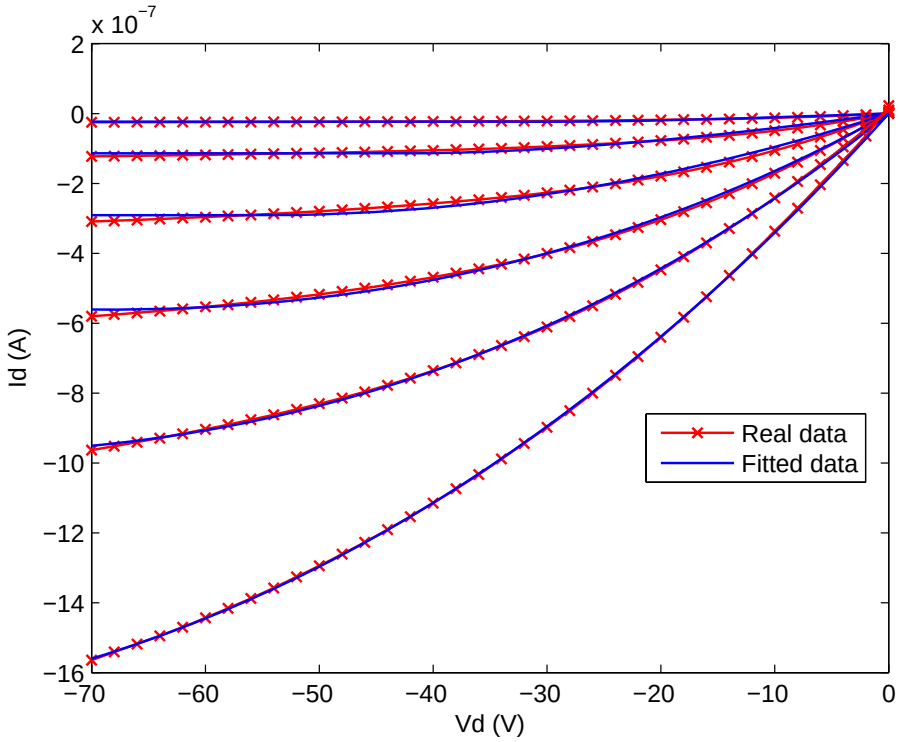

Figure 3.10: $I_\mathrm{d} - V_\mathrm{d}$ characteristic for device with PEDOT contacts. The gate voltage is kept at $V_\mathrm{g} = -100\,\mathrm{V}$.

work in this topic includes, in the theoretical analysis, a rigorous determination of the current equations when a field dependent mobility given by MTR or VRH is considered; on the experimental side, the development of simple circuits with interconnected transistors is the future step for the development of the e-textile.

Chapter 4

Short channel effects

In the previous chapter theoretical models for organic transistors have been extended to cylindrical geometries, but no hypotheses on the length of the channel L were made. However, channel length in organic thin film transistors is an important parameter, because it can lead to substantial deviations when the physical dimensions of the device scale down. Considerations on this point are reported, for example, by Torsi *et al.* [TDK95], while experimental evidence by Chabinyc *et al.* [CLS$^+$04] shows that, already for devices with channel length $L < 10\,\mu$m, short channel effects arise.

The equations (2.9) and (2.23),introduced in section 2.3.1, cannot describe completely the device characteristics, as they exhibit several non-idealities, as reported by Haddock *et al.* [HZZ$^+$06]. To account for these short channel effects, like space charge limited currents or the mobility dependence on the longitudinal electric field (source-drain), more sophisticated models have been proposed. For instance, it has been recently pointed out by Koehler and Biaggio [KB04] that, for high applied voltages and short channel lengths, the current conduction can be significantly influenced by space charge limited current (SCLC) phenomena, i.e. the carriers injected from the contacts can constitute a space charge region which affects the behavior of the device. SCLC conduction can explain the non-saturation of the output curves for high drain voltages in OTFTs with short channel lengths. Experimental evidence of SCLC effects has been reported in [CLS$^+$04].

The mobility dependence on the longitudinal electric field (source-drain) E_x can be described by the Poole-Frenkel model described in section 2.4.4:

$$\mu(\mathcal{E}_x) = \mu_0 \exp\left(\gamma\sqrt{\mathcal{E}_x}\right) \tag{4.1}$$

where μ_0 is the zero-field mobility and γ is a prefactor which depends on the material and is generally inverse in proportion to the temperature T, at least for $T > 50\,\mathrm{K}$ [HN07]. Stallinga *et al.* [SGB$^+$04] [SG06b] show that Poole-Frenkel mobility can be responsible of the non-linearities often observed in the output curves for low drain voltages. Hamadani

et al. [HN07] [HRG+07] report field dependent mobilities in OTFTs which are consistent with the Poole-Frenkel model for different temperatures. Numerical simulations have been carried on by Bolognesi *et al.* [BCLC03] [BBM+04] including Poole Frenkel mobility in the drift-diffusion model, showing good agreement with experimental results.

In this chapter we will develop a model which accounts for SCLC conduction together with a field dependent mobility which is described by the Poole-Frenkel model, determining the device characteristic equations at different applied biases.

In section 4.1 a description of the hypotheses on the devices and their geometry are shown. In section 4.2 the model is obtained for the linear, depletion and saturation regimes. In section 4.3, the model is validated with experimental results obtained from short channel OTFTs.

4.1 The device

We consider a device as reported in fig. 4.1, which is also the device already described in section 2.3.1. It is a bottom contact OTFT, with insulator thickness, dielectric permittivity and capacitance per unit area equal to d_i, ε_i and C_i, respectively, and with semiconductor thickness, dielectric permittivity and capacitance per unit area equal to d_s, ε_s and C_s, respectively. The channel length is equal to L, whereas its width is Z. It is assumed that the semiconductor has a free density of carriers n_0 which is equal to the doping of the semiconductor N. The contacts are assumed to be ohmic. Nevertheless, it should be noted that real OTFTs behavior can be deeply affected by source-drain contact resistances, especially in short channel devices. In section 4.3 experimental data will be analyzed extending the model to include also contact resistances. A complete list of the

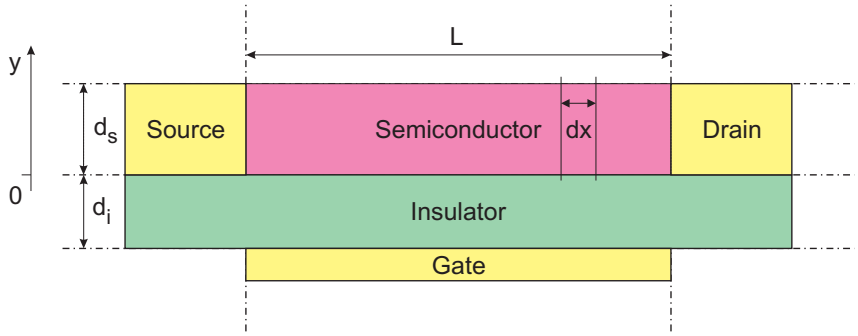

Figure 4.1: Geometry of a bottom contact OTFT.

parameters used in this chapter, together with the values used for simulations, is reported in table 4.1.

Parameter	*Symbol*	*Value*
Device width	Z	5 mm
Device length	L	15 μm
Insulator thickness	d_i	200 nm
Insulator dielectric permittivity	ε_i	$3.9 \cdot \varepsilon_0$
Semiconductor thickness	d_s	100 nm
Semiconductor dielectric permittivity	ε_s	$3.9 \cdot \varepsilon_0$
Semiconductor doping	N	$10^{14}\,\mathrm{cm}^{-3}$
Free carrier density	n_0	$10^{14}\,\mathrm{cm}^{-3}$
Free carrier mobility	μ_0	$10^{-4}\,\mathrm{cm}^2/\mathrm{Vs}$

Table 4.1: Simulation parameters.

4.2 Model derivation

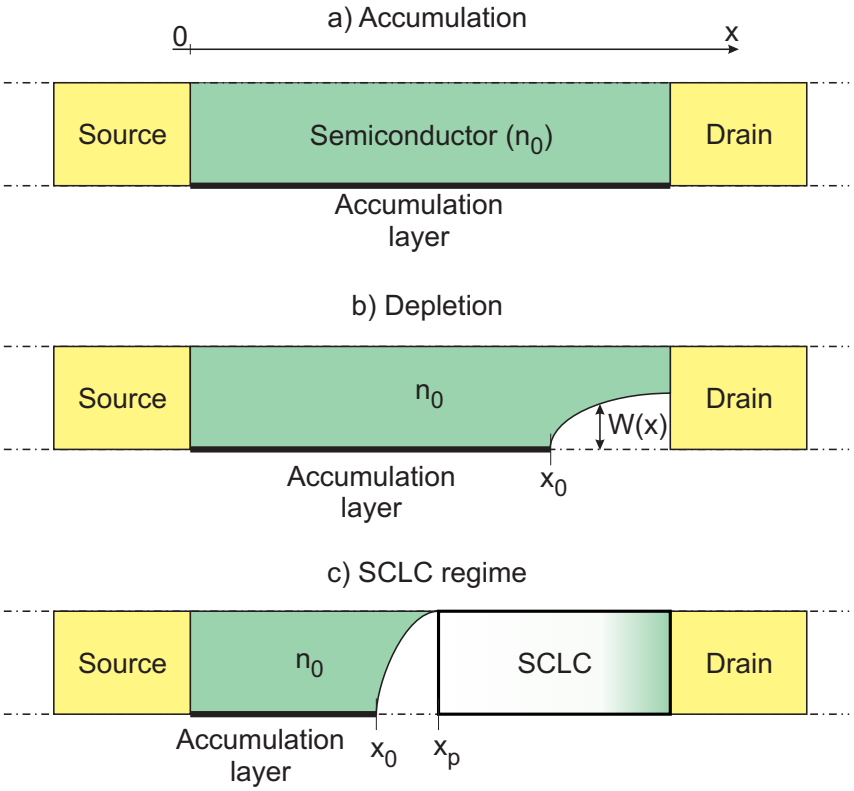

Figure 4.2: Modes of operation of the OTFT. The origin of the x-axis is at the source contact.

The first issue when describing the behavior of an organic thin-film transistor is in the definition of the threshold voltage, which can be expressed as the voltage to apply

to the gate electrode, referenced to the source, in order to create the accumulation layer. This definition implies that an ideal accumulation device, where there are no localized states originating from acceptors or donors, has a null threshold voltage [SG06a]. Without speculating on the possible origins of non-ideal values of the threshold voltage, we will assume in the following that it has a generic value of V_{th}. In the following paragraphs, we will assume to have an n-type transistor; for a p-type transistor the sign of the currents and applied voltages have to be changed accordingly.

4.2.1 Linear region

The characteristic equation of the device in the linear regime (fig. 4.2-a), i.e. for $V_{\mathrm{d}} < V_{\mathrm{g}} - V_{\mathrm{th}}$, can be obtained considering that the total drain current I_{d} can be expressed as the sum of the bulk current originating from the free carriers in the semiconductor and the current determined by the carriers in the accumulation layer. Therefore

$$\frac{I_{\mathrm{d}}}{Z\mu(\mathcal{E}_x)} = -\left[Q_{\mathrm{g}}(x) + Q_0\right]\frac{\mathrm{d}V}{\mathrm{d}x}, \tag{4.2}$$

where Q_0 is the surface density of the free carriers given by

$$Q_0 = \pm q n_0 d_{\mathrm{s}}, \tag{4.3}$$

wherein the sign of the right hand side of (4.3) is that of charge of the carriers (plus for holes, minus for electrons). The surface density of the carriers in the accumulation layer $Q_{\mathrm{g}}(x)$ which forms as a capacitive effect, is

$$Q_{\mathrm{g}}(x) = -C_{\mathrm{i}}\left[V_{\mathrm{g}} - V_{\mathrm{th}} - V_{\mathrm{s}}(x) - V(x)\right], \tag{4.4}$$

wherein $V_{\mathrm{s}}(x)$ is the ohmic drop in the bulk of the semiconductor, which can be generally neglected [HHK98], and $V(x)$ is the potential with respect to the source at the coordinate x. Then we can state that

$$\frac{I_{\mathrm{d}}}{Z\mu(E_x)} = C_{\mathrm{i}}\left[V_{\mathrm{g}} - V_{\mathrm{th}} + V_0 - V(x)\right]\frac{\mathrm{d}V}{\mathrm{d}x}, \tag{4.5}$$

where $V_0 = -Q_0/C_{\mathrm{i}}$. Under the gradual channel approximation (i.e. the electric field along x is negligible with respect to that along y), $V(x)$ increases from 0 at the source to V_{d} at the drain and also

$$\left|\frac{\mathrm{d}\mathcal{E}_y}{\mathrm{d}y}\right| \gg \left|\frac{\mathrm{d}\mathcal{E}_x}{\mathrm{d}x}\right|. \tag{4.6}$$

Moreover, the electric field along x can be expressed as

$$\mathcal{E}_x \simeq \frac{V_{\mathrm{d}}}{L}, \tag{4.7}$$

so the mobility is constant along the channel and

$$\mu(\mathcal{E}_x) \simeq \mu_0 \exp\left(\gamma\sqrt{\frac{V_\mathrm{d}}{L}}\right). \tag{4.8}$$

Integration of (4.5) between $V(0) = 0$ and $V(L) = V_\mathrm{d}$ gives

$$I_\mathrm{d} = \frac{Z}{L}\mu_0 \exp\left(\gamma\sqrt{\frac{V_\mathrm{d}}{L}}\right) C_\mathrm{i}\left[(V_\mathrm{g} - V_\mathrm{th} + V_0)\, V_\mathrm{d} - \frac{V_\mathrm{d}^2}{2}\right]. \tag{4.9}$$

4.2.2 Depletion region

For $V_\mathrm{d} > V_\mathrm{g} - V_\mathrm{th}$, a depletion region forms, starting from a point x_0 where $V(x_0) = V_\mathrm{g} - V_\mathrm{th}$ and ending at the drain contact (fig. 4.2-b). Solving the Poisson equation along the y direction [HHK98] allows to determine its extension, which is

$$W(x) = \frac{\varepsilon_\mathrm{s}}{C_\mathrm{i}}\left\{\sqrt{1 + \frac{2C_\mathrm{i}^2\left[V(x) - (V_\mathrm{g} - V_\mathrm{th})\right]}{qN\varepsilon_\mathrm{s}}} - 1\right\}. \tag{4.10}$$

The condition $W = d_\mathrm{s}$ is verified at the pinch-off abscissa x_p and the pinch-off voltage can be obtained from $W(V_\mathrm{p}) = d_\mathrm{s}$, so that

$$V_\mathrm{p} = (V_\mathrm{g} - V_\mathrm{th}) + V_0\left(1 + \frac{C_\mathrm{i}}{2C_\mathrm{s}}\right). \tag{4.11}$$

For every $x_0 \leq x \leq x_p$ contributions to the current are only given by the free carriers in the volume which has not been depleted, so

$$\frac{I_\mathrm{d}}{Z\mu(\mathcal{E}_x)} = qn_0\left[d_\mathrm{s} - W(x)\right]\frac{\mathrm{d}V}{\mathrm{d}x}. \tag{4.12}$$

We consider the electric field along x constant in this region, up to the pinch-off abscissa x_p, so again the mobility can be expressed as in (4.8). It should be noted that this approximation is used only in a limited range of x since, for thin film transistors, the pinch-off voltage V_p is near to $(V_\mathrm{g} - V_\mathrm{th})$ and, in the limit of $d_\mathrm{s} \to 0$, $V_\mathrm{p} = (V_\mathrm{g} - V_\mathrm{th})$ and $x_0 \equiv x_\mathrm{p}$. Integrating (4.12) between $V(x_0) = (V_\mathrm{g} - V_\mathrm{th})$ and $V(L) = V_\mathrm{d}$ and applying the continuity of the current with (4.9) at $V_\mathrm{d} = (V_\mathrm{g} - V_\mathrm{th})$ we find

$$\begin{aligned} I_\mathrm{d} = \frac{Z}{L}\mu_0 \exp\left(\gamma\sqrt{\frac{V_\mathrm{d}}{L}}\right) \{ & C_\mathrm{i}\left[(V_\mathrm{g} - V_\mathrm{th})\, V_0 + \right. \\ & \left. + \frac{(V_\mathrm{g} - V_\mathrm{th})^2}{2}\right] + (C_\mathrm{i} + C_\mathrm{s})\, V_0\left[V_\mathrm{d} - (V_\mathrm{g} - V_\mathrm{th})\right] + \\ & + \frac{(C_\mathrm{s}V_0)^2}{3C_\mathrm{i}}\left[1 - \left(1 + \frac{2C_\mathrm{i}}{V_0 C_\mathrm{s}}\left[V_\mathrm{d} - (V_\mathrm{g} - V_\mathrm{th})\right]\right)^{3/2}\right]\Bigg\}. \end{aligned} \tag{4.13}$$

4.2.3 SCLC region

Beyond the pinch-off abscissa the gradual channel approximation is no longer valid, the electric field varies along the channel and the exact determination of the current in the semiconductor would require the numerical resolution of the two dimensional drift-diffusion model. However, since in the pinch-off region the effects of the drain potential become dominant compared to the effects of the gate potential, we can assume that the behavior of the device beyond the pinch-off resembles that of a thin film SCLC region. Grinberg et al. [GLPS89] determined the expression for the SCLC current in a thin film with ohmic contacts, but now a field-dependent mobility must also be considered. To find a simple yet useful solution, we first reproduce the case study the authors simulated, i.e. a thin film $n^+ - i - n^+$ structure with strip ohmic contacts like the one reported in figure 4.3. The device is surrounded by vacuum, as the electric field related to the charge in the thin

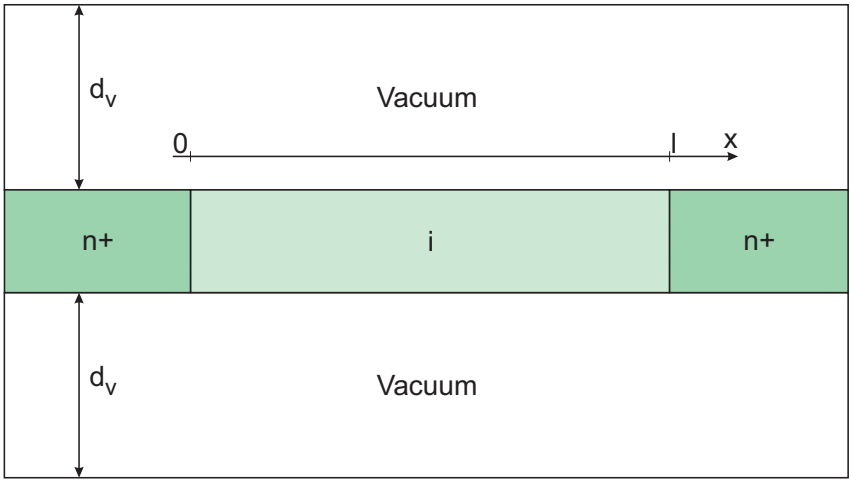

Figure 4.3: Geometry of the thin film $n^+ - i - n^+$ structure: the device has a length of $l = 4.8\,\mu$m and it has a strip contact geometry, with two $25\,\mu$m long ohmic contacts. The structure is surrounded by $d_\mathrm{v} = 10\,\mu$m of vacuum.

film is supposed to exceed the boundaries of the structure. This is an important point, because it also means that a one dimensional model can only approximately describe the behavior of a thin film structure.

A finite element drift-diffusion simulation of the structure is performed using the commercial software Sentaurus by Synopsis [sen]. Poole-Frenkel mobility is implemented and, for various values of γ, $I-V$ curves were determined. The output curves are reported in figure 4.4. The following law is found to provide good approximations to the simulated curves, introducing a fitting parameter β which depends on γ. It is similar to the one found in [GLPS89], but has an additional factor which accounts for the field dependent

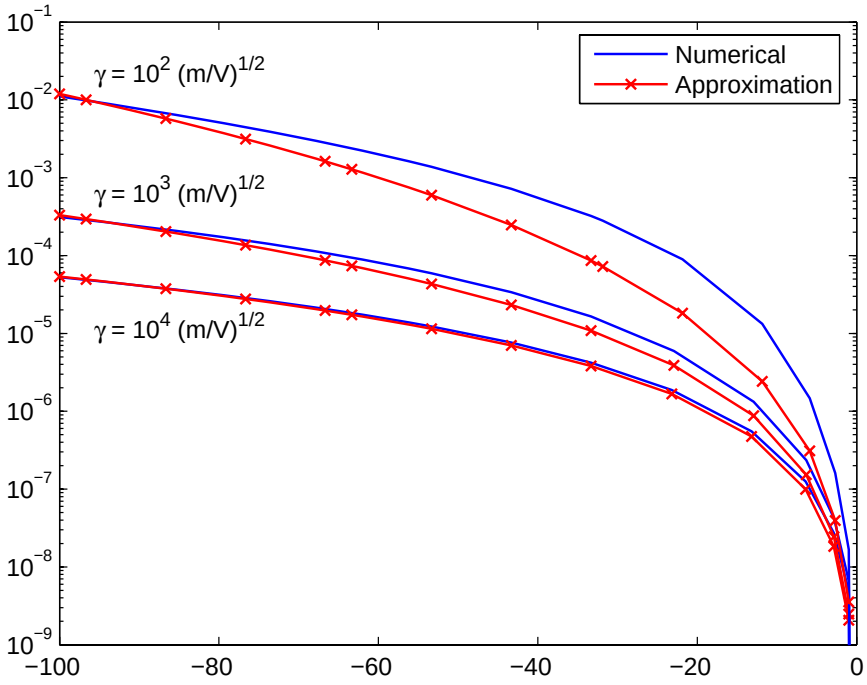

Figure 4.4: $I-V$ curves for n^+-i-n^+ structure for different γ values.

mobility.

$$I = 0.6 Z \varepsilon_s \mu_0 \frac{V^2}{l^2} \exp\left(\beta \cdot \gamma \sqrt{\frac{V}{l}}\right). \tag{4.14}$$

The prefactor in the current is kept equal to the one reported by Grinberg *et. al.* for a structure with strip contacts. Extracted values of β values are reported in table 4.2. Equation (4.14) provides worse approximations of the numerical simulation as the γ parameter increases, because the dependence on the exponential of the square root of the field increases with γ.

γ $(\mathrm{m/V})^{1/2}$	β
10^4	0.72
10^3	0.63
10^2	0.14

Table 4.2: Extracted fitting parameter β.

Figures 4.5 and 4.6 show the absolute value of the electric field, which clearly exceeds the boundaries of the device.

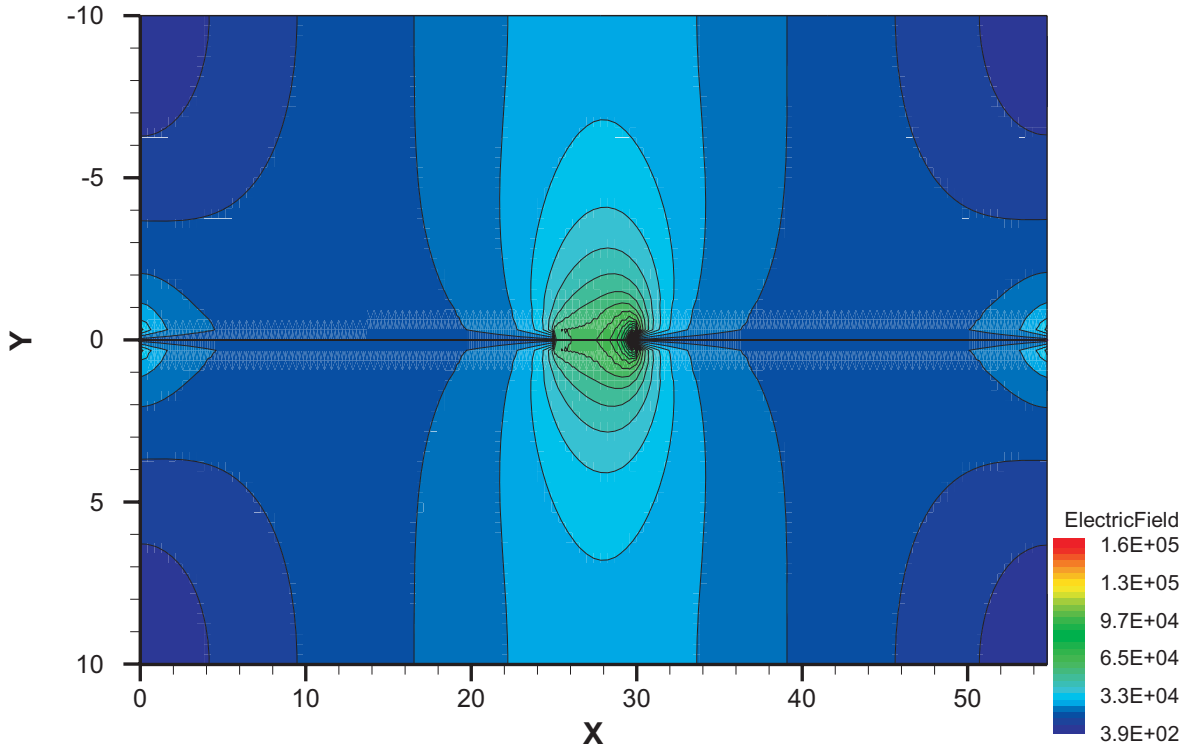

Figure 4.5: Absolute value of the electric field in the structure and in vacuum.

Since $l = (L - x_\mathrm{p})$ and $V_x = (V_\mathrm{d} - V_\mathrm{p})$ we obtain

$$I_\mathrm{d}\,(L - x_\mathrm{p}) = Z 0.6 \mu_0 \varepsilon_\mathrm{s} \frac{(V_\mathrm{d} - V_\mathrm{p})^2}{(L - x_\mathrm{p})} \exp\left(\beta\gamma\sqrt{\frac{(V_\mathrm{d} - V_\mathrm{p})}{(L - x_\mathrm{p})}}\right). \tag{4.15}$$

The $I_\mathrm{d} x_\mathrm{p}$ term in the left hand side can be determined applying the continuity with (4.13) at $L = x_\mathrm{p}$, therefore we find

$$\begin{aligned} I_\mathrm{d} = \frac{Z}{L}\Bigg\{ & \frac{C_\mathrm{i}}{2}\left(((V_\mathrm{g} - V_\mathrm{th}) + V_0)^2 + \frac{V_0^2 C_\mathrm{i}}{3C_\mathrm{s}}\right)\mu\,(V_\mathrm{p}) + \\ & + \; 0.6\mu_0\varepsilon_\mathrm{s}\frac{(V_\mathrm{d} - V_\mathrm{p})^2}{(L - x_\mathrm{p})} \exp\left[\beta\gamma\sqrt{\frac{V_\mathrm{d} - V_\mathrm{p}}{(L - x_\mathrm{p})}}\right]\Bigg\}, \end{aligned} \tag{4.16}$$

wherein $\mu\,(V_\mathrm{p}) = \mu_0 \exp\left(\gamma\sqrt{V_\mathrm{p}/x_\mathrm{p}}\right)$ is the mobility at the pinch-off point and continues to increase as the point becomes closer to the source contact.

The pinch-off abscissa x_p can be determined substituting the term I_d found in (4.24) back in (4.23). This leads to

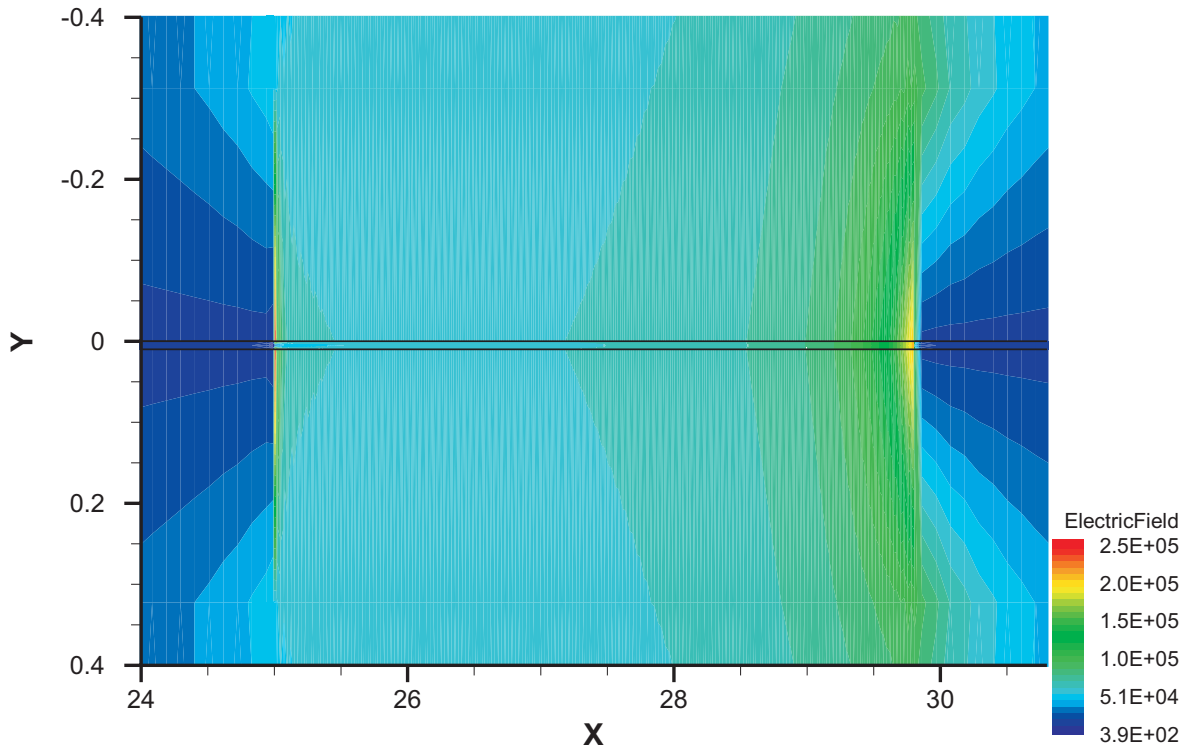

Figure 4.6: Zoom of the absolute value of the electric field in the structure and in vacuum. The structure begins at $x = 25\,\mu$m and ends at $x = 29.8\,\mu$m.

$$C_{\mathrm{i}}\mu\left(V_{\mathrm{p}}\right)\left[\left(V_{\mathrm{g}}-V_{\mathrm{th}}+V_0\right)^2+\frac{V_0^2 C_{\mathrm{i}}}{3C_{\mathrm{s}}}\right]\left(L-x_{\mathrm{p}}\right)^2$$
$$=2\cdot 0.6 x_{\mathrm{p}}\mu_0\varepsilon_{\mathrm{s}}\left(V_{\mathrm{d}}-V_{\mathrm{p}}\right)^2\exp\left[\beta\gamma\sqrt{\frac{V_{\mathrm{d}}-V_{\mathrm{p}}}{\left(L-x_{\mathrm{p}}\right)}}\right]. \tag{4.17}$$

In fig. 4.7 equation (4.25) is solved as a function of the drain voltage V_{d} for several gate voltages V_{g}. For $V_{\mathrm{d}} < V_{\mathrm{p}}$ the depletion region does not extend over the whole semiconductor thickness d_{s}, whereas for $V_{\mathrm{d}} > V_{\mathrm{p}}$ the pinch-off point gradually approaches the source contact.

Output curves simulated for devices with high and low γ are shown in fig. 4.8 and 4.9, respectively. In fig. 4.8, the curves exhibit a super-linear behavior for $V_{\mathrm{d}} < V_{\mathrm{g}} - V_{\mathrm{th}}$, which is due to the Poole-Frenkel mobility, whereas SCLC effects, for $V_{\mathrm{d}} > V_{\mathrm{p}}$, result in the non-saturation of the curves. When the mobility dependence on the electric field E_x is low, that is when γ is low enough to make the argument of the exponential in the mobility tend to zero, as in fig. 4.9, the output curves resemble more those of the conventional

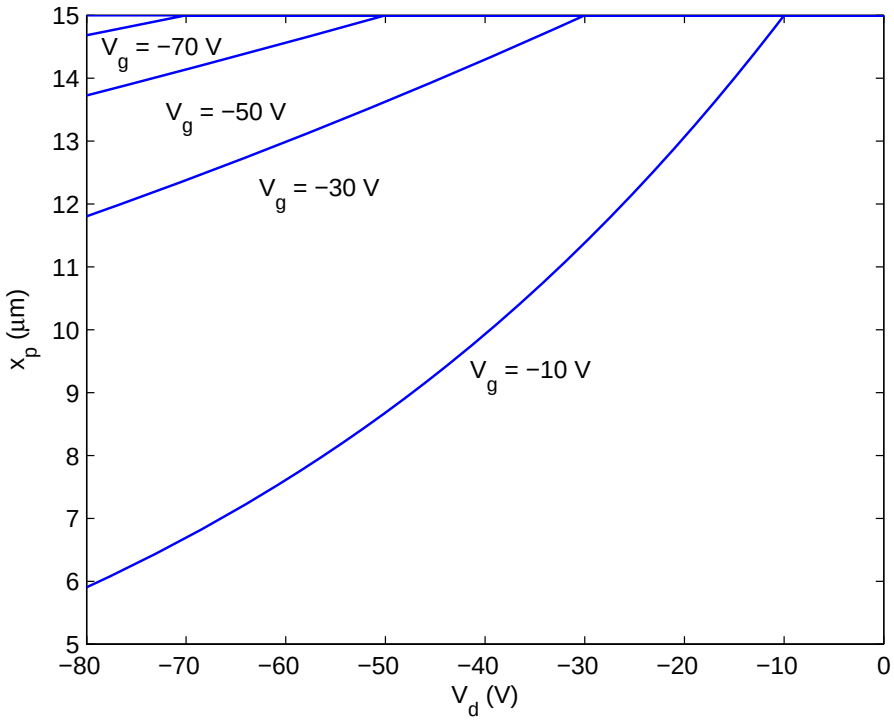

Figure 4.7: Pinch-off abscissa x_p as a function of the drain voltage V_d with $L = 15\,\mu\mathrm{m}$, $\gamma = 1.5 \cdot 10^{-4}\ (\mathrm{m/V})^{1/2}$ and $V_\mathrm{th} = 0$. $V_g = -10, -30, \ldots, -90\,\mathrm{V}$. For $V_g = -90\,\mathrm{V}$ the device remains in accumulation regime, since $V_\mathrm{d} < V_\mathrm{g}$, so $x_\mathrm{p} = L$.

OTFT quadratic model. Even the non-saturation of the curves is less evident, for the SCLC is not enhanced by the Poole-Frenkel mobility.

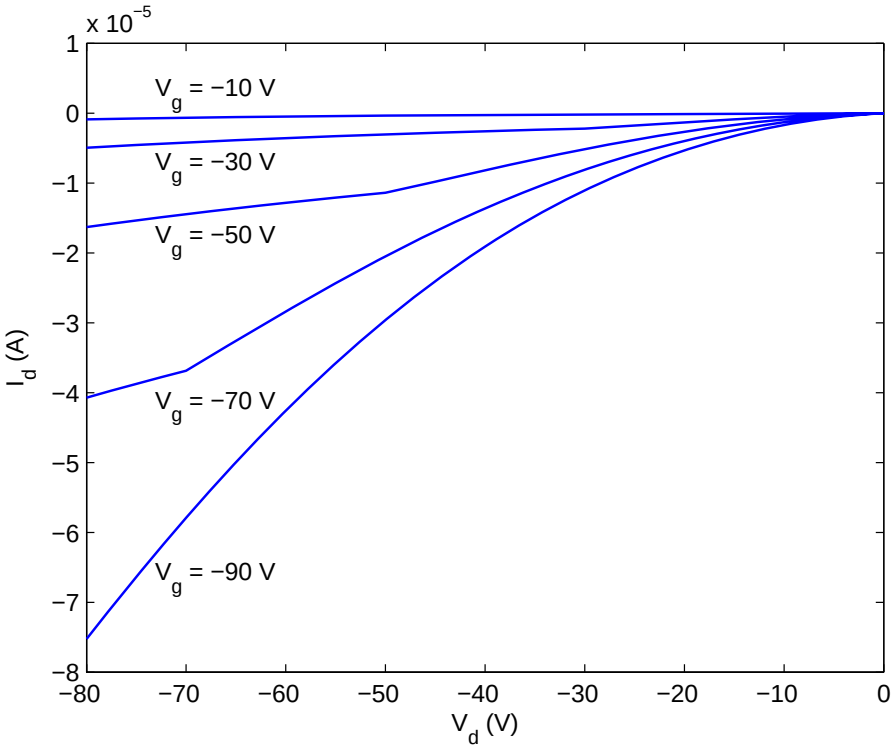

Figure 4.8: Output characteristics for a p-device with $L = 15\,\mu$m, $\gamma = 1.5 \cdot 10^{-3}$ $(\mathrm{m/V})^{1/2}$ and $V_{\mathrm{th}} = 0$. $V_{\mathrm{g}} = -10, -30, \ldots, -90\,\mathrm{V}$.

To better show how the channel length can affect the electrical characteristics of the devices, fig. 4.10 shows the output curves for different channel lengths L and the same applied gate voltage V_{g}. As the channel length decreases both Poole-Frenkel mobility and SCLC effects become more evident, leading to devices which do not saturate at all.

One last remark is about the doping value used in our calculations, which determines the potential V_0. With a doping $N = 10^{14}\,\mathrm{cm}^{-3}$, $V_0 = 9.2\,\mathrm{mV}$. For typical doping values of P3HT [MMH+01], which are equal or less $N = 10^{16}\,\mathrm{cm}^{-3}$, the potential V_0 still remains negligible ($V_0 = 0.92\,\mathrm{V}$) when compared to the voltages applied to the electrodes. This happens because V_0 is directly proportional to the thickness of the thin film d_{s}.

4.2.4 The limit of thick film

When the semiconductor thickness is large enough so that no field exceeds the boundaries of the structures, the proposed model cannot predict correctly the current. In this case, we assume that beyond the pinch-off abscissa the effects of the longitudinal field E_x become

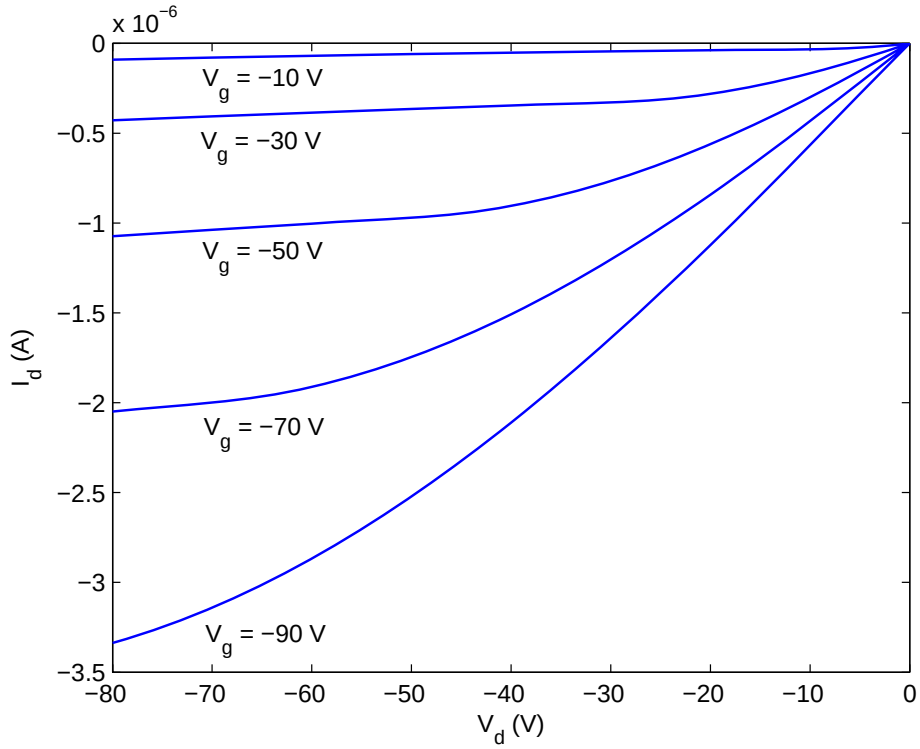

Figure 4.9: Output characteristics for a p-device with $L = 15\,\mu$m, $\gamma = 1.5 \cdot 10^{-4}$ $(\mathrm{m/V})^{1/2}$ and $V_{\mathrm{th}} = 0$. $V_{\mathrm{g}} = -10, -30, \ldots, -90\,\mathrm{V}$.

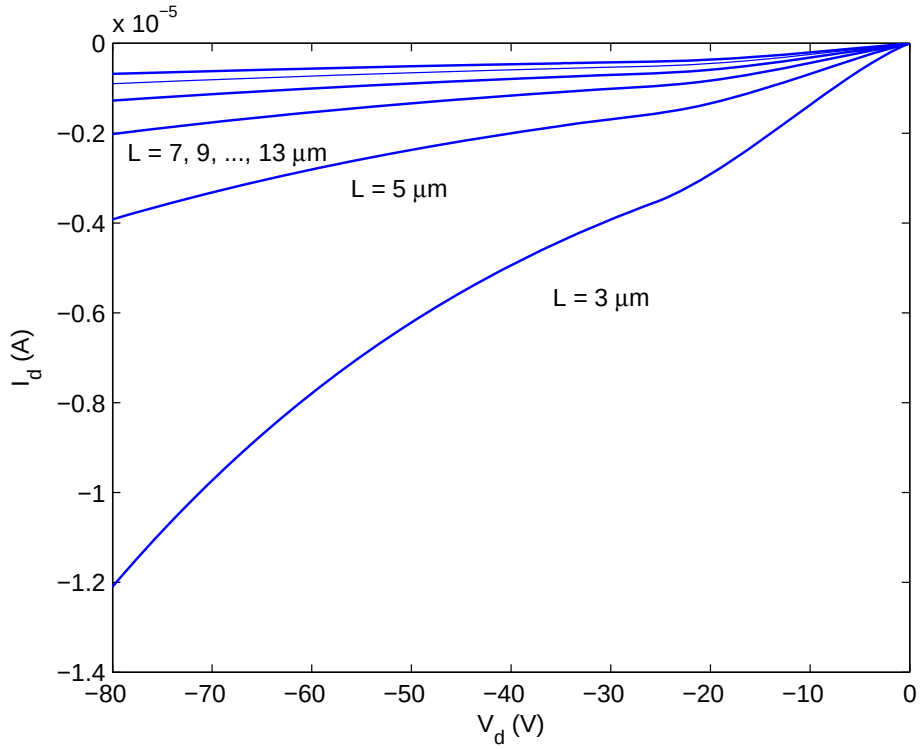

Figure 4.10: Output characteristics for p-devices with $L = 3, 5, \ldots, 13\,\mu$m. $\gamma = 1.5 \cdot 10^{-4}$ $(\mathrm{m/V})^{1/2}$. $V_\mathrm{g} = -25\,\mathrm{V}$.

dominant compared to those of E_y, so that the following approximation can be made:

$$\left|\frac{\mathrm{d}\mathcal{E}_x}{\mathrm{d}x}\right| \gg \left|\frac{\mathrm{d}\mathcal{E}_y}{\mathrm{d}y}\right|. \tag{4.18}$$

The Poisson equation becomes

$$\frac{\mathrm{d}^2 V}{\mathrm{d}x^2} = -\frac{qn}{\varepsilon_\mathrm{s}}, \tag{4.19}$$

where n is the volume charge density of the carriers. The model is one dimensional. The current is

$$\frac{I_\mathrm{d}}{Z} = d_\mathrm{s} q n \mu\left(\mathcal{E}_x\right)\mathcal{E}_x. \tag{4.20}$$

The mobility cannot be approximated with (4.8), since the electric field along the x direction is no more constant due to the space charge present. Combining (4.19) with (4.20) we obtain

$$\frac{I_\mathrm{d}}{Z} = \varepsilon_\mathrm{s} d_\mathrm{s} \mu_0 \exp\left(\gamma\sqrt{\mathcal{E}_x}\right)\mathcal{E}_x \frac{\mathrm{d}\mathcal{E}_x}{\mathrm{d}x}. \tag{4.21}$$

Equation (4.21) cannot be solved analytically, however the Murgatroyd approach [**?**] can be followed to determine the SCLC current in the semiconductor. For a semiconductor of length l and applied voltage V_x, an approximated solution for (4.21) can be found:

$$I_\mathrm{d} = Z\frac{9}{8}\mu_0 \varepsilon_\mathrm{s} d_\mathrm{s} \frac{V_x^2}{l^3} \exp\left(\frac{0.891}{kT}\gamma\sqrt{\frac{V_x}{l}}\right). \tag{4.22}$$

Since $l = (L - x_\mathrm{p})$ and $V_x = (V_\mathrm{d} - V_\mathrm{p})$ we obtain

$$I_\mathrm{d}\left(L - x_\mathrm{p}\right) = Z\frac{9}{8}\mu_0 \varepsilon_\mathrm{s} d_\mathrm{s} \frac{\left(V_\mathrm{d} - V_\mathrm{p}\right)^2}{\left(L - x_\mathrm{p}\right)^2} \exp\left[\frac{0.891}{kT}\gamma\sqrt{\frac{\left(V_\mathrm{d} - V_\mathrm{p}\right)}{\left(L - x_\mathrm{p}\right)}}\right]. \tag{4.23}$$

The $I_\mathrm{d} x_\mathrm{p}$ term in the left hand side can be determined applying the continuity with (4.13) at $L = x_\mathrm{p}$, therefore we find

$$\begin{aligned} I_\mathrm{d} = \frac{Z}{L}\Bigg\{ & \frac{C_\mathrm{i}}{2}\left[\left(V_\mathrm{g} - V_\mathrm{th} + V_0\right)^2 + \frac{V_0^2 C_\mathrm{i}}{3C_\mathrm{s}}\right]\mu\left(V_\mathrm{p}\right) + \\ & + \frac{9}{8}\mu_0 \varepsilon_\mathrm{s} d_\mathrm{s} \frac{\left(V_\mathrm{d} - V_\mathrm{p}\right)^2}{\left(L - x_\mathrm{p}\right)^2} \exp\left[\frac{0.891}{kT}\gamma\sqrt{\frac{V_\mathrm{d} - V_\mathrm{p}}{\left(L - x_\mathrm{p}\right)}}\right]\Bigg\}, \end{aligned} \tag{4.24}$$

wherein $\mu\left(V_\mathrm{p}\right) = \mu_0 \exp\left(\gamma\sqrt{V_\mathrm{p}/x_\mathrm{p}}\right)$ is the mobility at the pinch-off point and continues to increase as the point becomes closer to the source contact.

The pinch-off abscissa x_p can be determined substituting the term I_d found in (4.24) back in (4.23). This leads to

$$4C_{\mathrm{i}}\mu\left(V_{\mathrm{p}}\right)\left[\left(V_{\mathrm{g}}-V_{\mathrm{th}}+V_0\right)^2+\frac{V_0^2C_{\mathrm{i}}}{3C_{\mathrm{s}}}\right]\left(L-x_{\mathrm{p}}\right)^3$$
$$=9x_{\mathrm{p}}\mu_0 d_{\mathrm{s}}\varepsilon_{\mathrm{s}}\left(V_{\mathrm{d}}-V_{\mathrm{p}}\right)^2\exp\left[\frac{0.891}{kT}\gamma\sqrt{\frac{V_{\mathrm{d}}-V_{\mathrm{p}}}{\left(L-x_{\mathrm{p}}\right)}}\right]. \tag{4.25}$$

4.3 Experimental results and parameter extraction

To perform a comparison between the developed model and real data, bottom gate short channel OTFTs with P3HT semiconductor have been realized, with channel length $L = 5\,\mu$m and $L = 2.5\,\mu$m. They have been produced by spin-casting the pristine polymer solution onto a 230 nm SiO_2 dielectric, thermally grown on a N^+Si wafer, used as gate electrode. Sputtered gold Source and Drain electrodes were used to contact the polymer. Before coating the active layer the SiO_2 surface was treated with a hexamethyldisilazane (HMDS) primer, to improve the film adhesion and formation. An interdigitated layout, obtained by means of conventional photolithography, was used for the OFET where $Z = 10\,$mm is the FET channel width. The dielectric capacitance per unit area is $C_{\mathrm{ins}} = 1.5 \cdot 10^{-4}\,\mathrm{F/m^2}$. The dielectric constant used in the case of the P3HT is $\varepsilon_s = 2$ as we determined by means of quasi static C-V measurements. The nominal value of the semiconductor thickness is 100 nm.

Two sets of measurements were performed: transfer curves are reported in fig. 4.11 and output curves are shown in fig. 4.12 and 4.13.

To extract the electrical parameters of the devices two contact resistances R_{s}, at both the source and drain contacts, were added to the model [NFS07], substituting V_{d} with $(V_{\mathrm{d}} - 2R_{\mathrm{s}}I_{\mathrm{d}})$ and V_{g} with $(V_{\mathrm{g}} - R_{\mathrm{s}}I_{\mathrm{d}})$ into the equations used for the fitting, namely equations (4.9), (4.13), (4.24) and (4.25). To reduce the number of fitting parameters, we supposed to have a very low density of free carriers, so that one can assume $V_0 \simeq 0\,$V.

Fitting of the transfer curves, which is reported in fig. 4.11, allows the determination of the threshold voltage V_{th}, the prefactor γ, the zero-field mobility μ_0 and the series resistance R_s. Fitting values are reported in table 4.3.

For low values of V_{g}, the fitting slightly deviates from the experimental data and this could be due to the zero-field mobility which is considered constant, whereas it could depend on V_{g} [TMBdL03]. Therefore, to account for possible dependencies on the gate voltage, the mobility μ_0 has also been extracted from each of the output curves and is shown in fig. 4.14. It can be observed that its magnitude is slightly different from that extracted from the transfer curves, and this is consistent with the higher currents in the

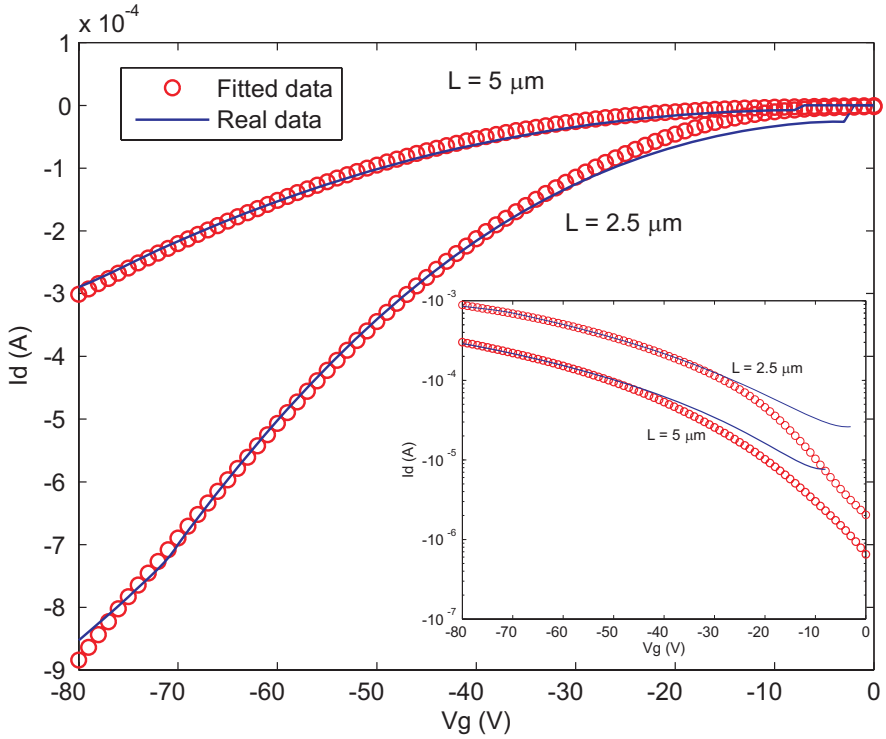

Figure 4.11: $I_d - V_g$ characteristics for $L = 5\,\mu$m and $L = 2.5\,\mu$m devices. Drain voltage is kept at $V_d = -75\,$V.

transfer curves measured for the same applied voltages. Also, μ_0 increases with the gate voltage. It should be noted that the small differences between the fitting parameters of the device with $L = 2.5\,\mu$m and the device with $L = 5\,\mu$m, which represent physical properties of the used materials, can be ascribed to differences in the realization process.

	V_{th} (V)	μ_0 (cm^2/Vs)	γ (m/V)$^{1/2}$	R_s (kΩ)
$L = 2.5\,\mu$m	-2.8	$3.6 \cdot 10^{-4}$	$5.8 \cdot 10^{-4}$	9
$L = 5\,\mu$m	-7.5	$8,4 \cdot 10^{-4}$	$4.5 \cdot 10^{-4}$	17

Table 4.3: Fitting parameters.

4.4 Conclusion

In this chapter a model which describes the electrical characteristics of OTFTs with short channel lengths has been presented. Effects like super-linear output curves for low drain voltage, as well as non-saturating currents can be adequately described. The model is

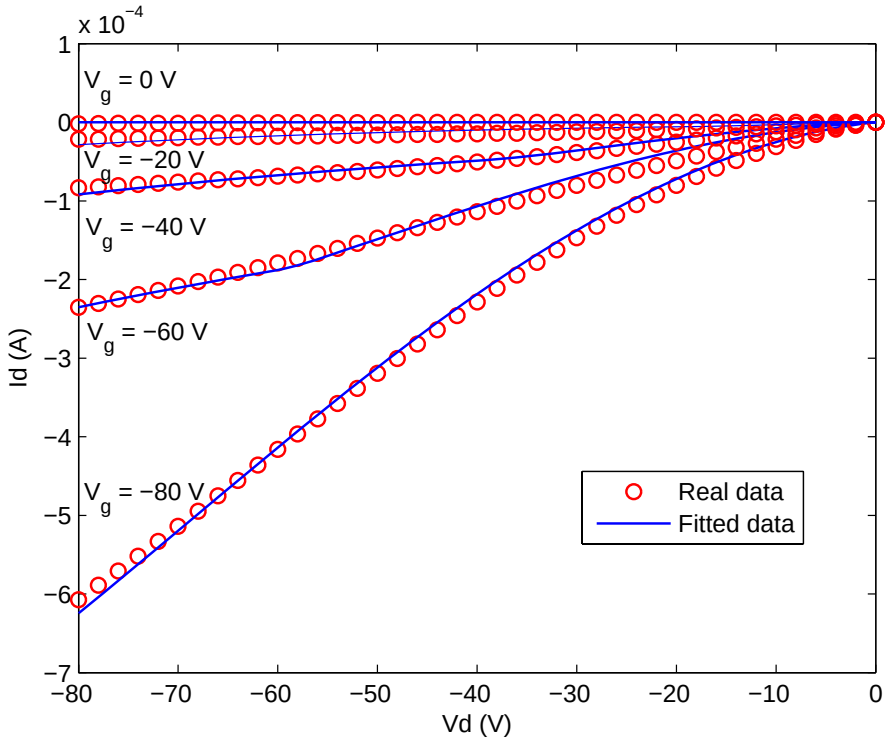

Figure 4.12: $I_\mathrm{d} - V_\mathrm{d}$ characteristics for $L = 2.5\,\mu$m device. $V_\mathrm{g} = 0, -20, \ldots, -80\,\mathrm{V}$.

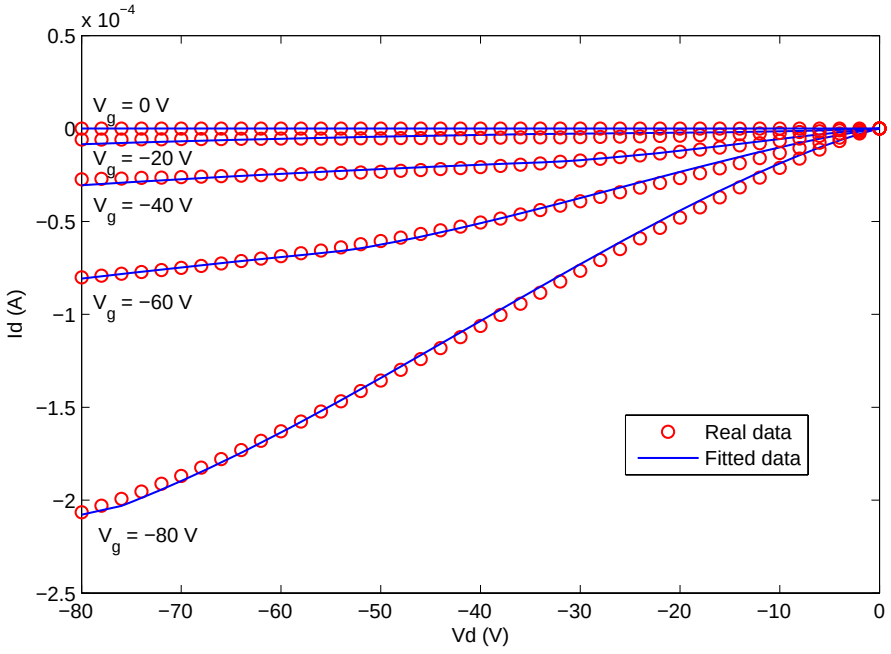

Figure 4.13: $I_\mathrm{d} - V_\mathrm{d}$ characteristics for $L = 5\,\mu$m device. $V_\mathrm{g} = 0, -20, \ldots, -80\,\mathrm{V}$.

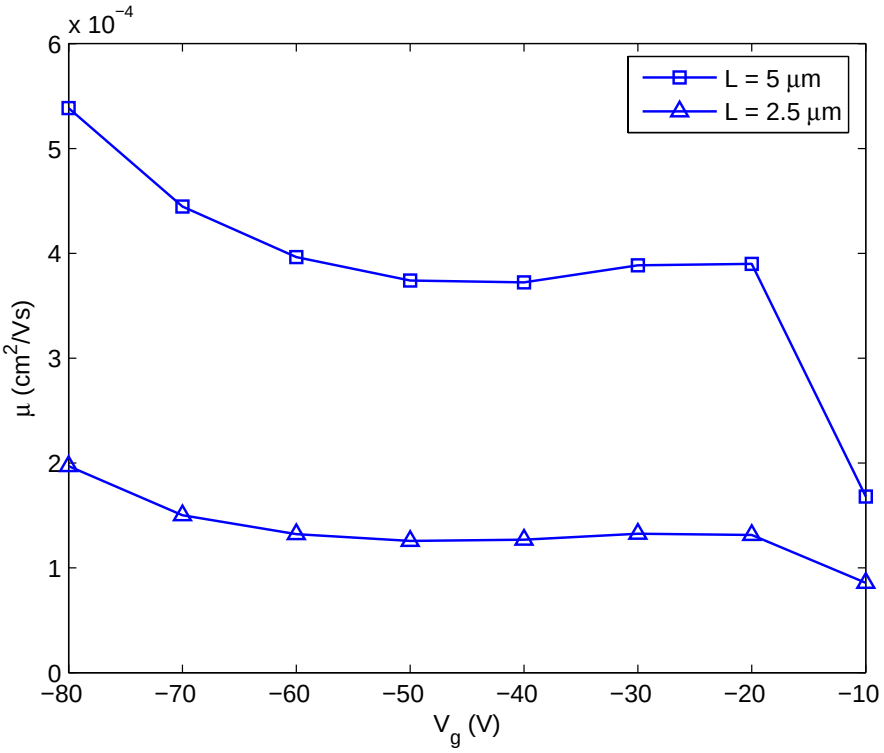

Figure 4.14: Zero-field mobility as a function of the gate voltage.

based on the assumption that the field dependent mobility of the organic semiconductor follows the Poole-Frenkel theory; moreover, space charge limited currents beyond the pinch-off point are considered. The length of the channel plays a key role in the determination of the electrical characteristics, since the high longitudinal electric field in short channel devices increases the carriers mobility and SCLC effects. Experimental results for devices with $5\,\mu$m and $2.5\,\mu$m channel lengths have been analyzed and good agreement with the proposed model is found. Future work in this topic includes an in-depth comparative analysis between the proposed model and numerical drift-diffusion simulations, where the non saturation is studied considering the thickness of the insulator and therefore the complete effects of the gate dependent electric field. Moreover, further analysis is required to precisely describe the effects of the contacts.

Chapter 5

Dynamic models for organic TFTs

In this chapter we would like to explore the characteristics of organic transistors as a function of time. Experimental results in literature, for example the work of Schmechel and von Seggern [SvS04] [SvS02], show that the performances of organic transistors are usually affected by trap states located in the energy gap of the material.

The origin of these localized states is still not completely clear: for example, Kang *et al.* [KdSFBZ05] report, for vapor-deposited pentacene, that shallow traps can arise from the sliding of the molecules along the molecular axis, while two dimensional crystallinity is maintained. Northrup *et. al.* discuss the effects of hydrogen related defects in crystalline pentacene, i.e. when the pentacene molecule $C_{22}H_{14}$ has one more hydrogen atom and becomes $C_{22}H_{15}$, but also analyze the effects of oxygen related defects, i.e. when one oxygen atom replaces one hydrogen atom to give $C_{22}H_{13}O$. Both defects are originated by exposure of the semiconductor to air humidity, but hydrogen defects could also come from bias stress in the device. Goldmann *et al.* [GGB06] also refer to water adsorption on the surface of the insulator, when discussing the generation of discrete traps states in single-crystal pentacene.

The main macroscopic consequence of the presence of traps in a device is hysteresis in its output, transfer or capacitance-voltage curves [SMS$^+$05] [GKDF05], because traps are charged and uncharged with specific dynamics which can lead to different operating conditions, even if the applied bias is the same. Analytical models [LMK07], as well as numerical simulations [LPS05] [PSH$^+$08], have been proposed to study these phenomena, which still constitute a hot topic in the field of organic electronics. In this chapter, we will describe how trap recharging can be modeled, and we will show a gallery of several simulations, which provide an in-depth view of the effects of the parameters involved in trap dynamics.

5.1 Model

The model that describes trap recharging in OFETs is the same that was first introduced by Schockley and Read [SR52] and by Hall [Hal52] and is based on the drift diffusion model reported in section 2.5. There, contributions of the trap states to the charge were included in (3.17) as n_{tr}. We will follow the exposition of Sze [Sze81] for its description.

More in detail, two types of traps can be defined, *donor* traps and *acceptor* traps.

DONOR traps are uncharged when unoccupied and they carry the charge of one hole when fully occupied.

ACCEPTOR traps are uncharged when unoccupied and they carry the charge of one electron when fully occupied.

A trap is a recombination center, determined by impurities or defects in the semiconductor, which can capture or emit one charge carrier. Let us consider the capture of one

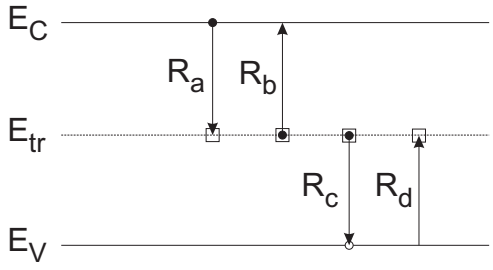

Figure 5.1: Emission and recombination of carriers for a single level of trap.

electron from the conduction band. For a density of traps N_{tr}, the density of occupied centers is $N_{\mathrm{tr}} f_{\mathrm{tr}}$, where f_{tr} is the Fermi distribution function, which gives the probability that a center is occupied by an electron. At the equilibrium it is

$$F = \frac{1}{1 + \exp\left[\left(E_{\mathrm{tr}} - E_{\mathrm{F}}\right)/kT\right]}, \tag{5.1}$$

where E_{tr} is the energy level and E_{F} is the Fermi level. The rate of the capture process is given by

$$R_{\mathrm{a}} = v_{\mathrm{th},n} \sigma_n n N_{\mathrm{tr}} \left(1 - f_{\mathrm{tr}}\right), \tag{5.2}$$

where the constants $v_{\mathrm{th},n}$ and σ_n are the carrier thermal velocity and the capture section, respectively. σ_n gives a measure on how an electron must be near to a center to be captured. For inorganic devices, the capture sections are about $10^{-15}\,\mathrm{cm}^2$ (atomic scale). The emission rate of an electron is given by

$$R_{\mathrm{b}} = e_n N_{\mathrm{tr}} f_{\mathrm{tr}}, \tag{5.3}$$

where e_n is the emission probability of the electron. At the thermal equilibrium the capture and emission rates must be equal: $R_\mathrm{a} = R_\mathrm{b}$. Since at the thermal equilibrium $n = n_\mathrm{i} \exp\left[\left(E_\mathrm{F} - E_\mathrm{i}\right)/kT\right]$ the probability of emission becomes

$$e_n = v_{\mathrm{th},n}\sigma_n n_\mathrm{i} \exp\left[\left(E_\mathrm{tr} - E_\mathrm{i}\right)/kT\right]. \tag{5.4}$$

For a trap located near the conduction band, the emission probability becomes greater, as e_n increases exponentially with $E_\mathrm{tr} - E_\mathrm{i}$.

Similar considerations lead to the following equations for the capture rate for holes

$$R_\mathrm{c} = v_{\mathrm{th},p}\sigma_p p N_\mathrm{tr} f_\mathrm{tr} \tag{5.5}$$

and the emission rate for holes

$$R_\mathrm{d} = e_p N_\mathrm{tr}\left(1 - f_\mathrm{tr}\right). \tag{5.6}$$

Again, at the thermal equilibrium $R_\mathrm{c} = R_\mathrm{d}$, so

$$e_p = v_{\mathrm{th},p}\sigma_p n_\mathrm{i} \exp\left[\left(E_\mathrm{i} - E_\mathrm{tr}\right)/kT\right]. \tag{5.7}$$

As for the emission probability for electrons, the probability of emission for holes increases exponentially as the energy level of the trap becomes nearer to the valence band. The lifetime for holes and electrons, respectively, can be introduced:

$$\tau_n = \frac{1}{v_{\mathrm{th},n}\sigma_n N_\mathrm{tr}}, \tag{5.8}$$

$$\tau_p = \frac{1}{v_{\mathrm{th},p}\sigma_p N_\mathrm{tr}} \tag{5.9}$$

and the balance equation for the net emission-capture rate can be defined:

$$\frac{\mathrm{d}n_\mathrm{tr}}{\mathrm{d}t} = R_\mathrm{b} - R_\mathrm{a} + R_\mathrm{d} - R_\mathrm{c}. \tag{5.10}$$

Substituting the expressions for the rates we finally obtain

$$\frac{\mathrm{d}n_\mathrm{tr}}{\mathrm{d}t} = \frac{1}{\tau_n}\left[\exp\frac{\left(E_\mathrm{tr} - E_\mathrm{i}\right)}{kT} f_\mathrm{tr} - n\left(1 - f_\mathrm{tr}\right)\right] + \frac{1}{\tau_p}\left[\exp\frac{\left(E_\mathrm{i} - E_\mathrm{tr}\right)}{kT}\left(1 - f_\mathrm{tr}\right) - p f_\mathrm{tr}\right]. \tag{5.11}$$

Simulations will be performed solving, together with the drift diffusion model, the equation in (5.11). However, in the following section, we also report the most general model, which holds for an arbitrary distribution of traps in the band gap.

5.1.1 An arbitrary density of trapped states

For completeness, a more general mathematical model [GMS07], which accounts for an arbitrary distribution of states, is also presented. Here it is proposed for acceptor traps, but an analogous model can be developed for donor traps changing the sign of the trapped charges in the Poisson equation (3.17) and substituting p with n and viceversa in all the following equations.

Let's now consider a general semiconductor with a forbidden energy gap E_{g} and conduction band energy E_{C} and valence band energy E_{V}. The constant (in space) density of trap states in the band gap N_{tr} is obtained by means of intergration on all the band gap energies of the energy dependent density of trapped states $M_{\mathrm{tr}}(E)$:

$$N_{\mathrm{tr}} = \int_{E_{\mathrm{V}}}^{E_{\mathrm{C}}} M_{\mathrm{tr}}(E)\,\mathrm{d}E. \tag{5.12}$$

The position density of the trapped states, which is a function of the position $\mathbf{r}$, the energy E and the time t is given by

$$n_{\mathrm{tr}}(\mathbf{r}, E, t) = \int_{E_{\mathrm{V}}}^{E_{\mathrm{C}}} M_{\mathrm{tr}}(E) f_{\mathrm{tr}}(\mathbf{r}, E, t)\,\mathrm{d}E, \tag{5.13}$$

wherein $f_{\mathrm{tr}}(\mathbf{r}, E, t)$ is the fraction of occupied trap states for a given energy E. The recombination rate for electrons and holes can be defined as

$$R_n = \int_{E_{\mathrm{V}}}^{E_{\mathrm{C}}} S_n M_{\mathrm{tr}}\,\mathrm{d}E, \tag{5.14}$$

$$R_p = \int_{E_{\mathrm{V}}}^{E_{\mathrm{C}}} S_p M_{\mathrm{tr}}\,\mathrm{d}E, \tag{5.15}$$

where

$$S_n = \frac{1}{\tau_n N_{\mathrm{tr}}}\left[n_0 f_{\mathrm{tr}} - n\left(1 - f_{\mathrm{tr}}\right)\right], \tag{5.16}$$

$$S_p = \frac{1}{\tau_p N_{\mathrm{tr}}}\left[p_0\left(1 - f_{\mathrm{tr}}\right) - p f_{\mathrm{tr}}\right]. \tag{5.17}$$

Trap dynamics is determined by the balance equation, which gives an additional differential equation

$$\frac{\partial f_{\mathrm{tr}}}{\partial t} = S_p - S_n = \frac{p_0}{\tau_p N_{\mathrm{tr}}} + \frac{n_0}{\tau_n N_{\mathrm{tr}}} - f_{\mathrm{tr}}\left(\frac{p + p_0}{\tau_p N_{\mathrm{tr}}} + \frac{n + n_0}{\tau_n N_{\mathrm{tr}}}\right), \tag{5.18}$$

which is coupled to the continuity equations (2.64) and (2.65), which include the recombination rates defined by (5.14) and (5.15). The rate constants are $\tau_n(E)$, $\tau_p(E)$, $n_0(E)$,

$p_0(E)$ and the law of mass action $n_0(E)p_0(E) = n_\mathrm{i}^2$ holds, where n_i is the independent intrinsic concentration. Integrating (5.18) leads to

$$\frac{\partial n_\mathrm{tr}}{\partial t} = R_p - R_n. \tag{5.19}$$

For a single level of traps located at energy E_tr the energy dependent density of trapped states becomes

$$M_\mathrm{tr} = N_\mathrm{tr}\delta\left(E - E_\mathrm{tr}\right). \tag{5.20}$$

It follows that the recombination rates for electrons and holes become

$$R_n = \frac{1}{\tau_n}\left[n_0\frac{n_\mathrm{tr}}{N_\mathrm{tr}} - n\left(1 - \frac{n_\mathrm{tr}}{N_\mathrm{tr}}\right)\right] \tag{5.21}$$

$$R_p = \frac{1}{\tau_p}\left[p_0\left(1 - \frac{n_\mathrm{tr}}{N_\mathrm{tr}}\right) - p\frac{n_\mathrm{tr}}{N_\mathrm{tr}}\right]. \tag{5.22}$$

For a steady-state solution ($\partial f_\mathrm{tr}/\partial t \to 0$) the fraction of occupied trap states becomes

$$f_\mathrm{tr} = \frac{\tau_n p_0 + \tau_p n}{\tau_n(p + p_0) + \tau_p(n + n_0)}. \tag{5.23}$$

The recombination rate for electrons equals the hole recombination rate and

$$R_n = R_p = R(n,p) = \left(n_\mathrm{i}^2 - np\right)\int_0^1 \frac{M_\mathrm{tr}(E)}{\tau_n(E)\left[p + p_0(E)\right] + \tau_p(E)\left[n + n_0(E)\right]}\,\mathrm{d}E. \tag{5.24}$$

For one trap level the well known Schokley-Read-Hall model is found:

$$R(n,p) = \frac{n_\mathrm{i}^2 - np}{\tau_n(p + p_0) + \tau_p(n + n_0)}. \tag{5.25}$$

5.2 Simulations

In order to understand the effects of the different physical parameters, several simulations have been performed on two typical case studies, i.e. a bottom contact transistor and a metal-insulator -semiconductor (MIS) structure. The structures are reported in figure 5.2 and 5.3, whereas geometrical parameters are reported in table 5.1.

Material parameters are specified in table 5.2. These values are typical for a semiconductor like pentacene [JL04]. The metal workfunction for the gate contact is set to $\phi_\mathrm{m,gate} = 0\,\mathrm{eV}$ whereas source and drain contacts, as well as the bulk contact for the MIS structure, have $\phi_\mathrm{m} = 5\,\mathrm{eV}$. In this way the contacts are ohmic, as $\phi_\mathrm{m} > \phi_\mathrm{s}$. Temperature is $T = 300\,\mathrm{K}$. Densities N_C and N_V are assumed to be twice (spin up and down) the density of molecules of pentacene. Unless specified, the doping profile is assumed to be $N_\mathrm{A} = 10^{16}\,\mathrm{cm}^{-3}$. This implies $n_\mathrm{i} = \sqrt{N_\mathrm{C}N_\mathrm{V}}\exp\left(-E_\mathrm{g}/2kT\right) = 3.695\,\mathrm{cm}^{-3}$.

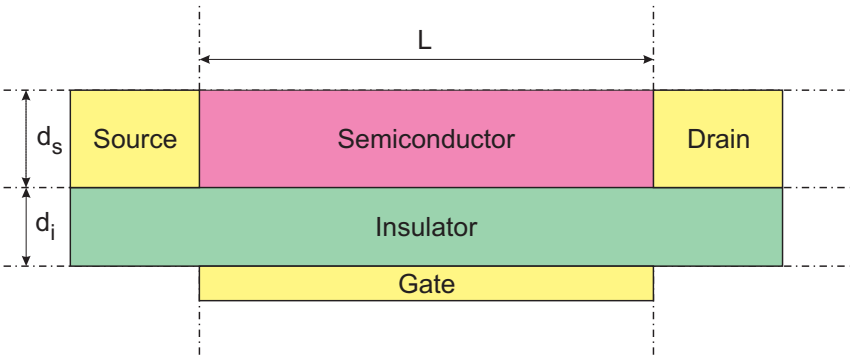

Figure 5.2: Geometry of a bottom contact OTFT.

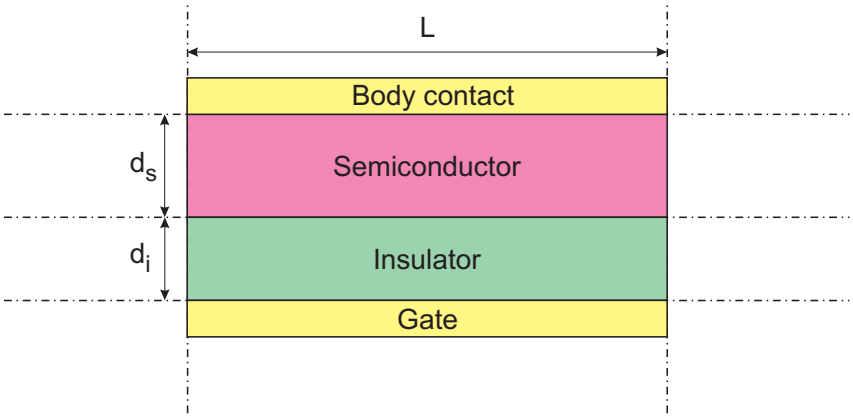

Figure 5.3: Geometry of a MIS.

Parameter	*Symbol*	*Value*
Channel length	L	$75\,\mu$m
Channel width	W	5 mm
Dielectric thickness	d_i	$1.6\,\mu$m
Semiconductor thickness	d_s	50 nm

Table 5.1: Geometry parameters for MIS and bottom contact OTFT.

The parameters for the trap distribution are chosen from table 5.3: the degrees of freedom are the density of trap and the product between the cross section and the thermal velocity. Simulations will be performed for an energy level which usually lies 0.3 eV over the valence band or under the conduction band (deep trap). Traps are physically located at the interface between the insulator and the semiconductor. Here they are most effective, but they can also be spatially distributed in the semiconductor bulk.

Transient simulations are performed for the gate sweep in table 5.4. For trans-characteristic curves, the drain voltage is first set at $V_\mathrm{d} = -25\,\mathrm{V}$ using a stationary

Parameter	*Symbol*	*Value*
Dielectric permittivity	ε_{i}	4
Semiconductor permittivity	ε_{s}	4
Electron affinity	$q\chi$	$2.5\,\mathrm{eV}$
Energy gap	E_{g}	$2.5\,\mathrm{eV}$
Valence band density	N_{C}	$2.8 \cdot 10^{21}\,\mathrm{cm}^{-3}$
Conduction band density	N_{V}	$2.8 \cdot 10^{21}\,\mathrm{cm}^{-3}$
Electrons mobility	μ_{n}	$10^{-20}\,\mathrm{cm}^2/\mathrm{Vs}$
Holes mobility	μ_{p}	$0.0381\,\mathrm{cm}^2/\mathrm{Vs}$
Metal workfunction	ϕ_{m}	$5\,\mathrm{eV}$

Table 5.2: Material parameters.

Parameter	*Symbol*	*Value*
Cross section $\times$ thermal velocity	$\sigma_{n,p}\upsilon_{\mathrm{th},(n,p)}$	$7.8 \cdot 10^{-19}\,\mathrm{cm}^3/\mathrm{s}$
Density of traps	N_{tr}	$10^{12}\,\mathrm{cm}^{-2}$
Trap energy level (acceptor)	E_{tr}	$E_{\mathrm{V}} + 0.3\,\mathrm{eV}$
Trap energy level (donor)	E_{tr}	$E_{\mathrm{C}} - 0.3\,\mathrm{eV}$

Table 5.3: Trap parameters.

drift diffusion solution (all time derivatives are set to zero).

Time (s)	0	1	2	3	4	5
Gate voltage (V)	0	+40	0	-40	0	+40

Table 5.4: Gate sweep.

The purpose of the simulations is to show how the different parameters of a distribution of traps can create macroscopic differences in the shape of the electrical curves. These differences are mostly given by the variation with time of the threshold voltage, which is determined by the different amount of charge which is trapped at different times. A trans-characteristic curve, between different sweeps of voltages, will be translated and modified in its shape. The same will happen for a capacitance-voltage curve.

5.2.1 Capacitance-Voltage curves

Performing $C - V$ simulations for a MIS structure requires the determination of the differential capacitance and must account for the long transient behavior of the traps, which determines the hysteresis. We will use the method explained in [IPR+85], wherein

the differential capacitance is approximated as follows:

$$C = \frac{\partial Q}{\partial V} \simeq \frac{\Delta Q}{\Delta V}, \tag{5.26}$$

where Q is the charge located at the gate electrode plate. In practice the derivative is approximated with a finite difference and the capacitance is extracted as difference between the charges ΔQ in voltage steps of ΔV:

$$C = \frac{Q_{i+1} - Q_i}{V_{i+1} - V_i}. \tag{5.27}$$

The method is effective only when applied to an insulated contact, where there only is displacement current, and is strictly quasi-static [Lau85].

The capacacitance of the MIS structure in fig. 5.3 will be given by the equivalent circuit in fig. 5.4 [Sze81]. The insulator capacitance per unit area will be given by

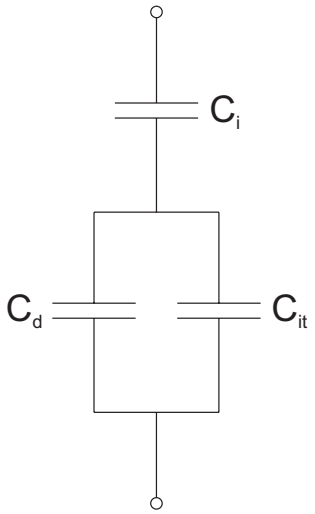

Figure 5.4: Equivalent circuit for the capacitance in a MIS structure.

$$C_{\mathrm{i}} = \frac{\varepsilon_{\mathrm{i}}}{d_{\mathrm{i}}}. \tag{5.28}$$

The interface traps will give a capacitance

$$C_{\mathrm{it}} = -\frac{\partial Q_{\mathrm{tr}}}{\partial V_{\mathrm{s}}}, \tag{5.29}$$

where V_{s} is the surface potential. The depletion region, when present with extension W, will give the depletion capacitance

$$C_{\mathrm{d}} = \frac{\varepsilon_{\mathrm{s}}}{W}. \tag{5.30}$$

5.2.2 Simulation results

In this section we show the results for simulations with different parameter sets. In fig. 5.5 and 5.6 the curves for the MIS and OTFT structures are shown in the absence of any trapped state.

Figure 5.7 and 5.8 report the first set of simulations, performed considering different densities of traps. Two effects are determined by the variation of the trap density: there is an increase of the amplitude of the hysteresis and a translation of the curves towards positive voltages, for increasing trap densities. This becomes clear when one considers that the traps determine a shift ΔV_{th} in the threshold voltage, which is

$$\Delta V_{\text{th}} = -\frac{Q_{\text{tr}}(t)}{C_{\text{i}}}, \tag{5.31}$$

where $Q_{\text{tr}}(t)$ is the average (along the dimensions of the channel) surface trapped charge at the instant t.

A change in the amplitude of the hysteresis can also be obtained with a variation of the product between the cross section and the thermal velocity, as reported in fig. 5.9 and 5.10.

This variation changes the rate at which carriers are emitted and captured: a smaller product means higher rates, so the traps are more responsive to the change of bias and, therefore, less hysteresis appears. A difference with the previous simulation is determined by the absence of threshold shifts, as the total amount of traps that can be filled does not change.

One issue, which is due to numerical problems, can be observed in fig. 5.9, for the curve with $\sigma v_{\text{th}} = 7.8 \cdot 10^{-18}\,\text{cm}^3/\text{s}$ and, in a much lesser way, for the curve with $\sigma v_{\text{th}} = 7.8 \cdot 10^{-19}\,\text{cm}^3/\text{s}$. When reaching the turning point at maximum bias, there is a step, which is due to an erroneous determination of the charge at the electrode, which is amplified by the operation of derivation performed to obtain the capacitance. We were unable to solve this glitch in the simulations, as reduction of the time steps in the solver was useless in increasing the accuracy of the results. But we report the curve with the others as it shows, anyway, the expected behavior given by the increase of the product σv_{th}.

The third set of simulations is reported in fig. 5.12 and 5.13. It shows what happens when the trap level is located differently in the band gap. For an acceptor trap in a p-type semiconductor the effect of the trap is less when the trap level gets farther from the LUMO. Before a bias is applied at the electrodes, the energy levels are those reported in figure 5.11. The Fermi level is located at a greater energy than the trap level, therefore at the thermal equilibrium the traps are almost completely filled, giving an overall negative charge at the interface which shifts the curves on the voltage axis. As soon as a gate voltage is applied, the gate-induced electric field pushes the electrons away and creates an

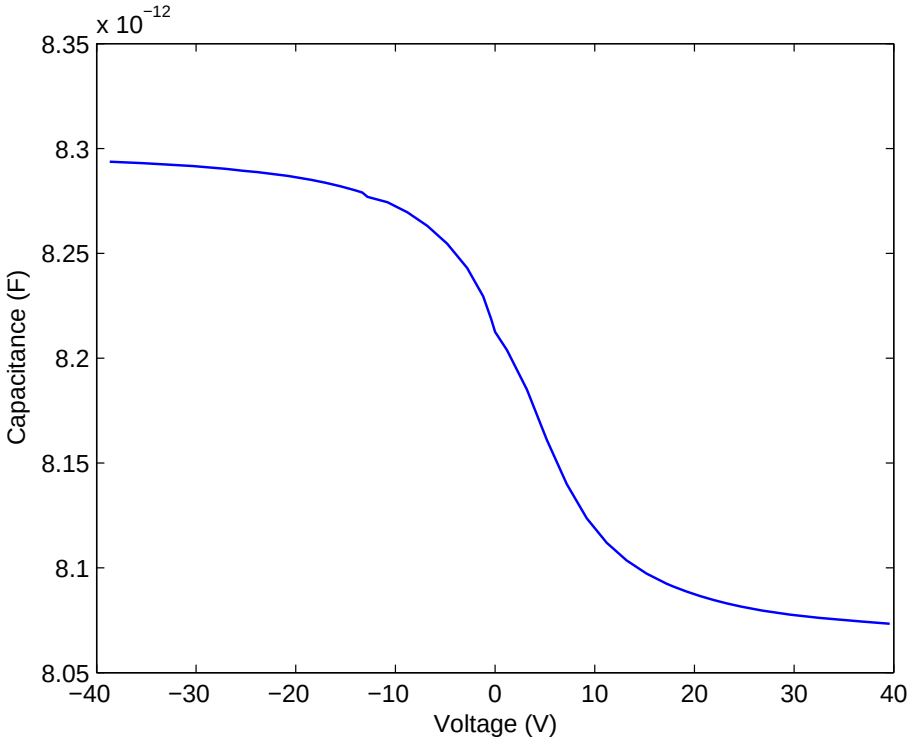

Figure 5.5: $C - V$ simulation for MIS structure with no trap states in the band gap.

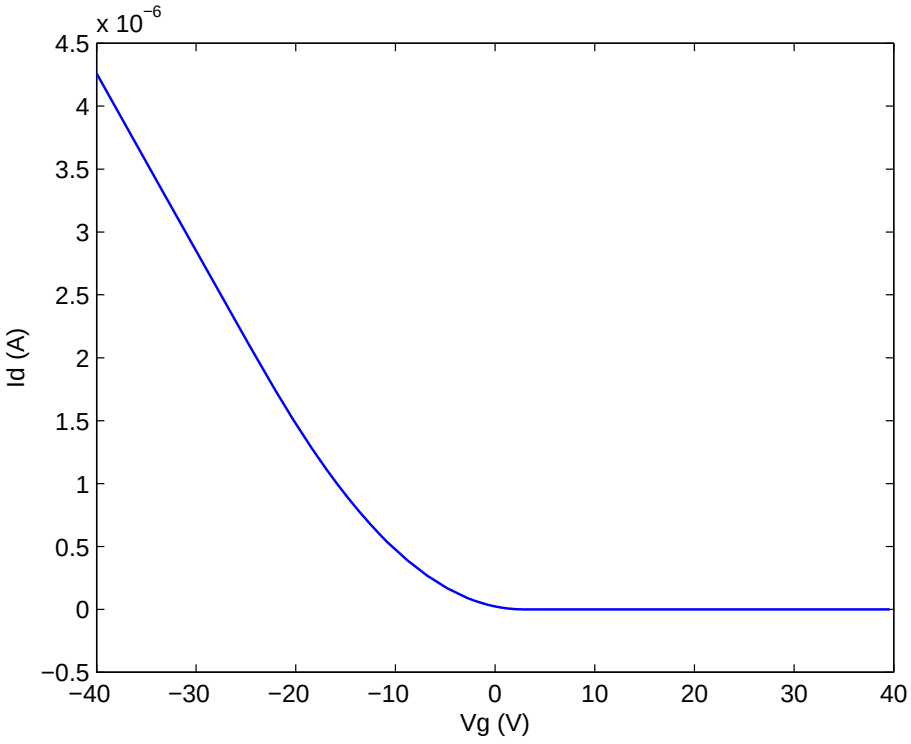

Figure 5.6: $I_{\mathrm{d}} - V_{\mathrm{g}}$ simulation for OTFT structure with no traps states in the band gap.

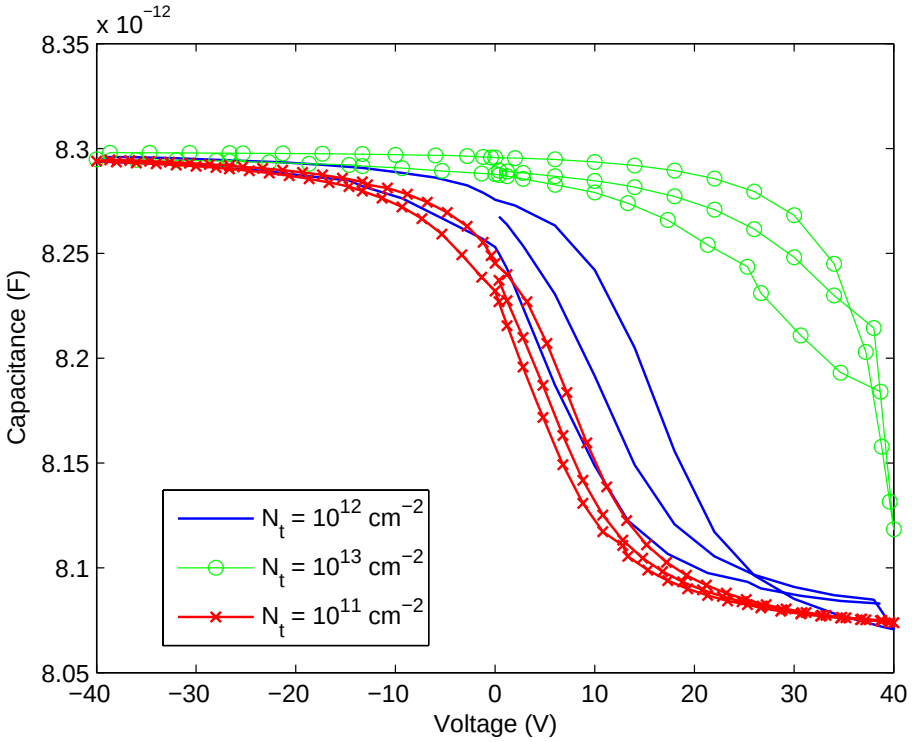

Figure 5.7: $C - V$ simulation for acceptor traps with densities $N_{\rm tr} = 10^{11} \div 10^{13}\,{\rm cm}^{-2}$. Hysteresis is counter-clockwise.

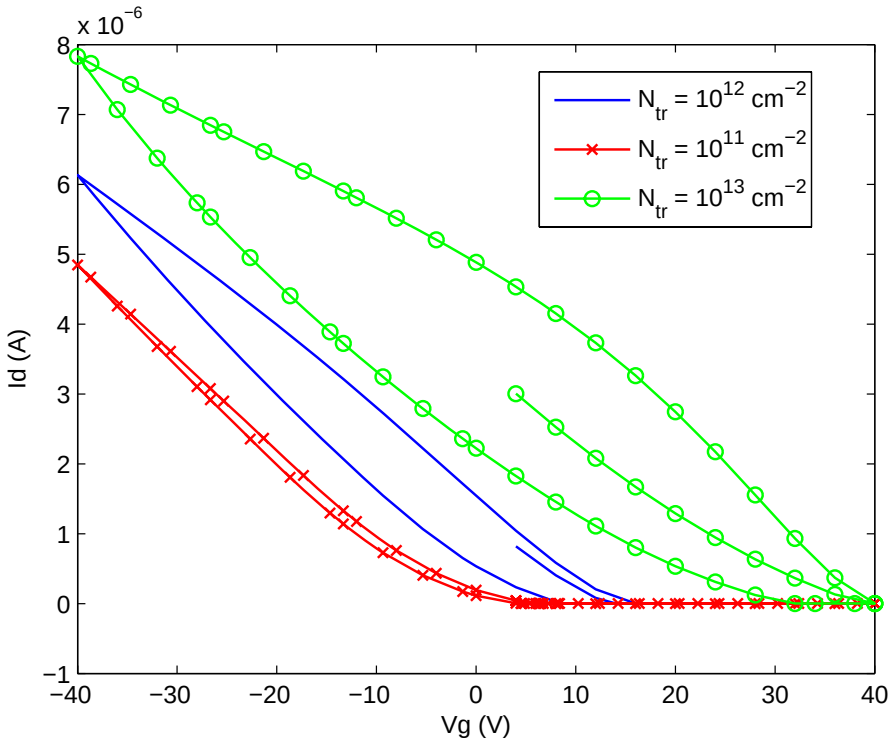

Figure 5.8: $I_{\rm d} - V_{\rm g}$ simulation for acceptor traps with densities $N_{\rm tr} = 10^{11} \div 10^{13}\,{\rm cm}^{-2}$. Hysteresis is counter-clockwise.

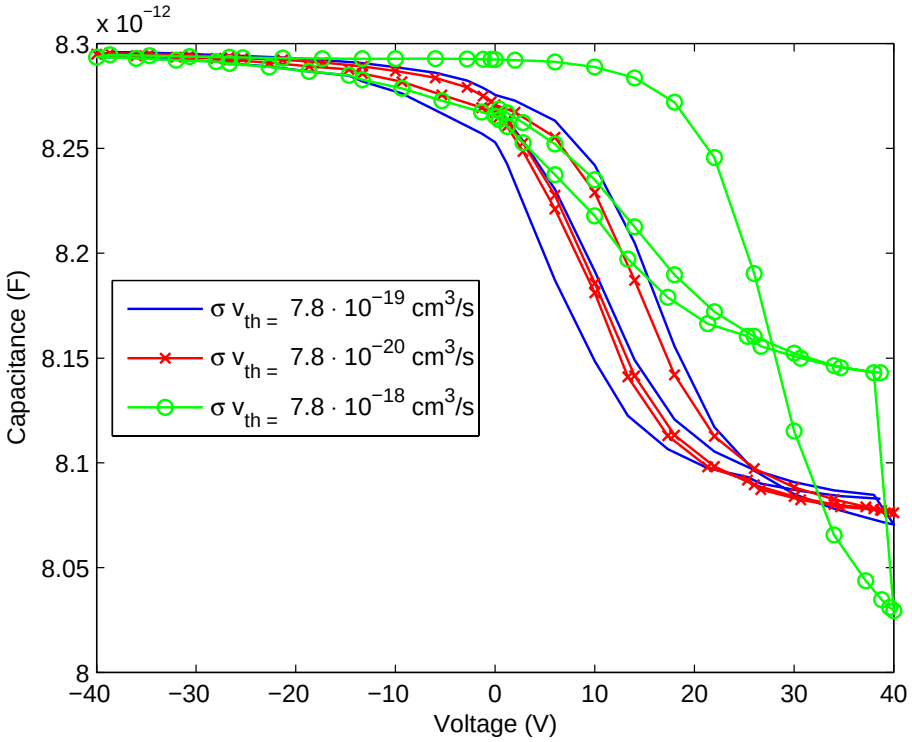

Figure 5.9: $C-V$ simulation for acceptor traps with $\sigma v_{\mathrm{th}} = 7.8\cdot10^{-18} \div 7.8\cdot10^{-20}\,\mathrm{cm}^3/\mathrm{s}$. Hysteresis is counter-clockwise.

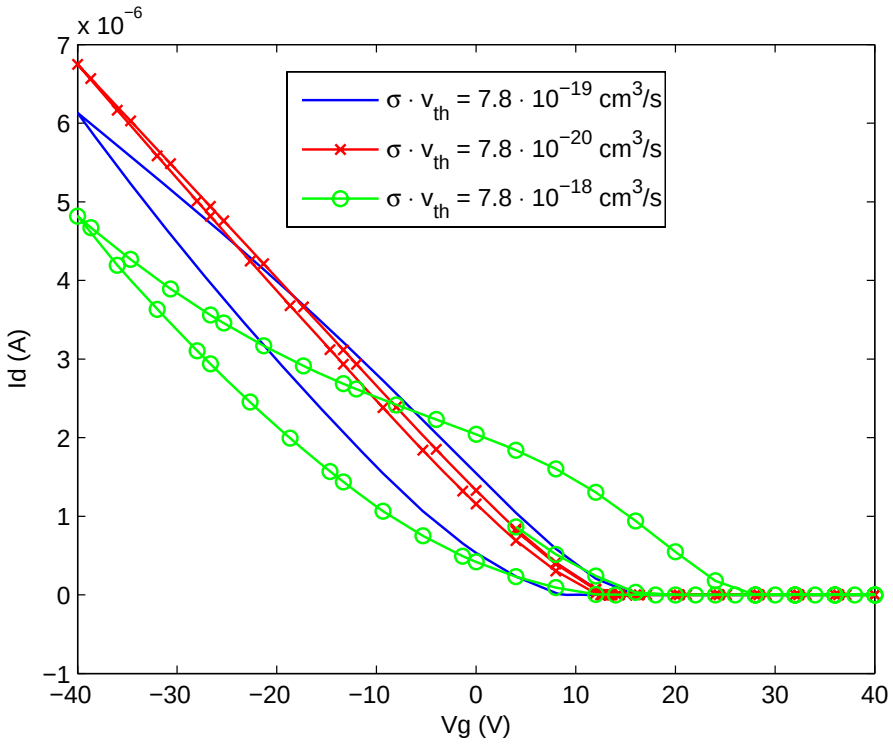

Figure 5.10: $I_{\mathrm{d}}-V_{\mathrm{g}}$ simulation for acceptor traps with $\sigma v_{\mathrm{th}} = 7.8\cdot10^{-18} \div 7.8\cdot10^{-20}\,\mathrm{cm}^3/\mathrm{s}$. Hysteresis is counter-clockwise.

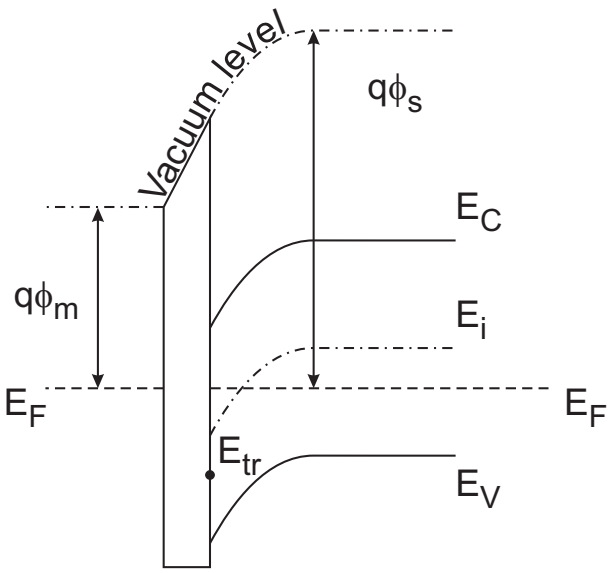

Figure 5.11: Band diagram of a MIS structure with a trap level at energy E_{tr}

accumulation layer of holes, reducing the overall trapped charge at the interface. This can also be understood recalling eq. (5.11) and applying some approximations: exchange of carriers with the LUMO is rather improbable: that is because the density of free electrons n is negligible and the trap level is located at a far lower level than the intrinsic energy level. This means that (5.11) simplifies to

$$\frac{\mathrm{d}n_{\mathrm{tr}}}{\mathrm{d}t} \simeq \frac{1}{\tau_p}\left[\exp\frac{(E_{\mathrm{i}}-E_{\mathrm{tr}})}{kT}\,(1-f_{\mathrm{tr}}) - pf_{\mathrm{tr}}\right]. \tag{5.32}$$

The exponential factor in the right hand side is constant for any applied bias, whereas p increases as a gate bias is applied. As soon as p becomes dominant, the balance equation reads

$$\frac{\mathrm{d}n_{\mathrm{tr}}}{\mathrm{d}t} \simeq -\frac{1}{\tau_p}pf_{\mathrm{tr}}, \tag{5.33}$$

which means that the trapped charge will decrease. This also explains why the hysteresis in the curves is always counter-clockwise, as the traps provide negative charge at the beginning ($t = 0$, positive threshold shift) and are subsequently neutralized as the applied bias increases (less threshold shift at the end of the simulation). When the energy level of the trap is beyond the Fermi level, as in the other simulations of fig. 5.12 and 5.13, the traps are empty, therefore neutral, from the beginning of the simulation, which means that there is no threshold shift from the beginning. The applied bias will not change the trap configuration, and no hysteresis is found.

Simulations in fig. 5.18 and 5.19 show how the hysteresis amplitude can change with the time length of the sweep, because slower sweeps allow more traps to be charged or

uncharged. This means that a slower sweep will lead to greater hysteresis and threshold shift.

The same simulations can be performed for donor traps. Figures 5.16 and 5.17 show a comparison between an acceptor trap and a donor trap located at the same energy level. The same device without traps is also reported.

The devices with traps have curves with a different shape, but both are counter-clockwise. The explanation is the same for the acceptor traps: at the beginning of the voltage sweep the energy level of the traps is located below the Fermi level, therefore the traps are not occupied by a hole and are neutral. When the gate bias is applied, the traps are filled with holes and the threshold voltage becomes more negative; furthermore, the hole concentration near the interface reduces, with a subsequent reduction of the drain current.

5.3 Summary

In this chapter, we have shown how trap recharging can affect the characteristics of organic thin film transistors. We have described the theory behind charge trap dynamics and have simulated it for several parameter sets, showing how different threshold voltage and hysteresis amplitudes can be originated. The present work, however, cannot completely describe all the phenomena that arise in organic transistors. As a a matter of fact, it has been reported by Lindner *et al.* [LPS05], that hysteresis can also be explained by polarons, whose dynamics might better describe the characteristics of organic transistors. Another possible factor is the presence of mobile ions in some dielectrics, like for example Poly-vinyl alcohol (PVA), as described by Egginger *et al.* [EIVS$^+$] or in poly-4-vinyl phenol (PVP) [HOH$^+$08]. Since mobile ions are charge which can move when an electric field is applied, they can change the threshold voltage of the device when they get farther or nearer the semiconductor/insulator interface. Modeling of mobile ions and polarons is the necessary future work to get a better insight of the topic. Despite several experimental studies already available in literature, a theoretical framework is still needed.

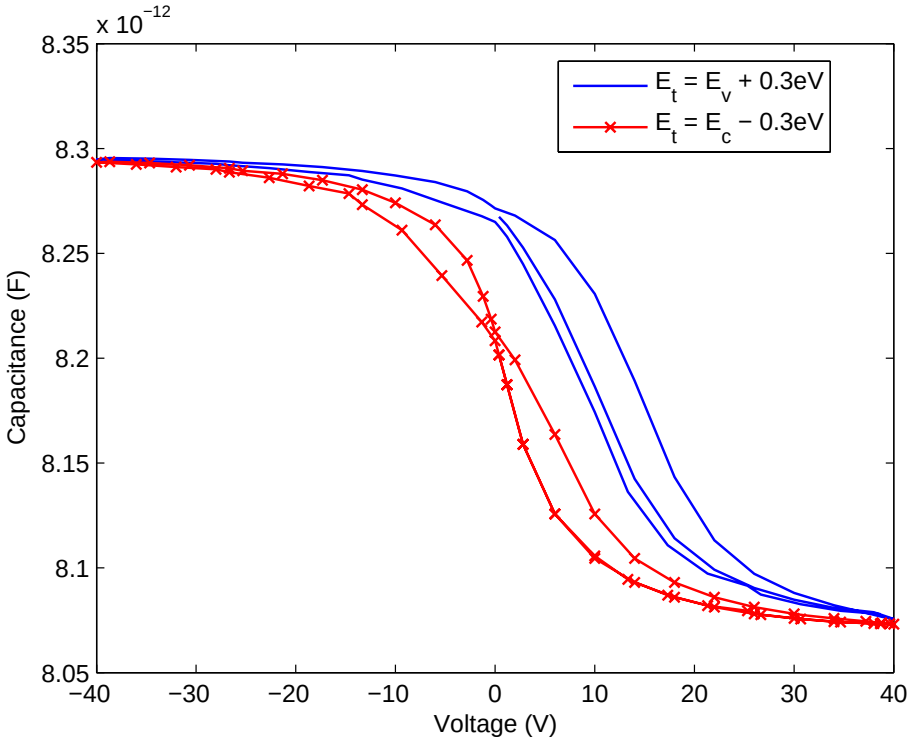

Figure 5.12: $C-V$ simulation for acceptor traps with energy levels at $E_{\mathrm{tr}} = 0.3\,\mathrm{eV} + E_{\mathrm{V}}$ and at $E_{\mathrm{tr}} = E_{\mathrm{C}} - 0.3\,\mathrm{eV}$. The curve with energy level in the middle of the band gap completely overlaps with the curve with $E_{\mathrm{tr}} = E_{\mathrm{C}} - 0.3\,\mathrm{eV}$. Hysteresis is counter-clockwise.

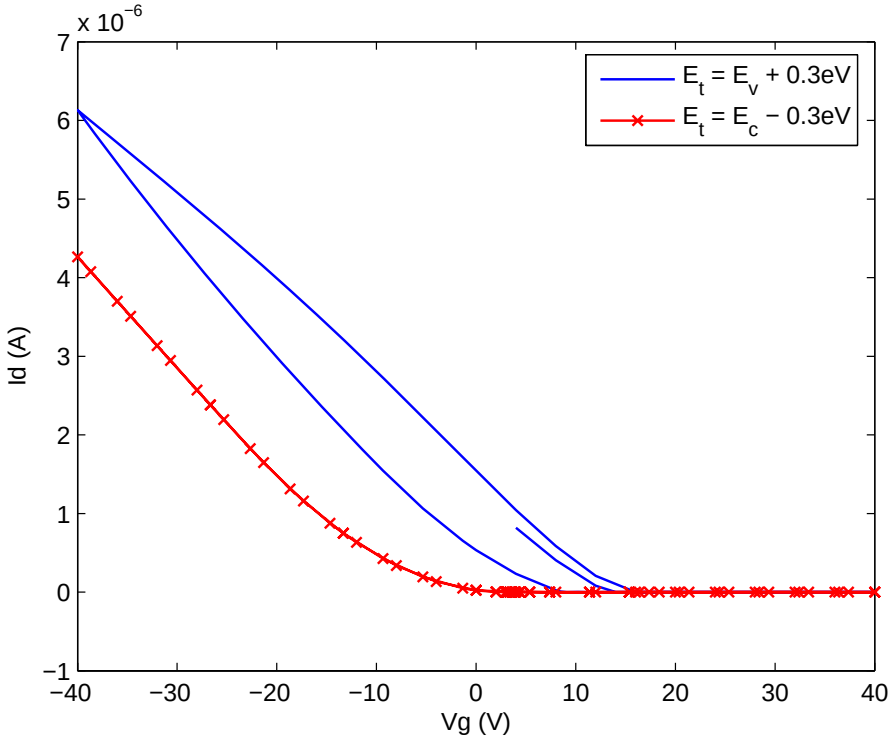

Figure 5.13: $I_{\mathrm{d}} - V_{\mathrm{g}}$ simulation for acceptor traps with energy levels at $E_{\mathrm{tr}} = 0.3\,\mathrm{eV} + E_{\mathrm{V}}$ and at $E_{\mathrm{tr}} = E_{\mathrm{C}} - 0.3\,\mathrm{eV}$. The curve with energy level in the middle of the band gap completely overlaps with the curve with $E_{\mathrm{tr}} = E_{\mathrm{C}} - 0.3\,\mathrm{eV}$ Hysteresis is counter-clockwise.

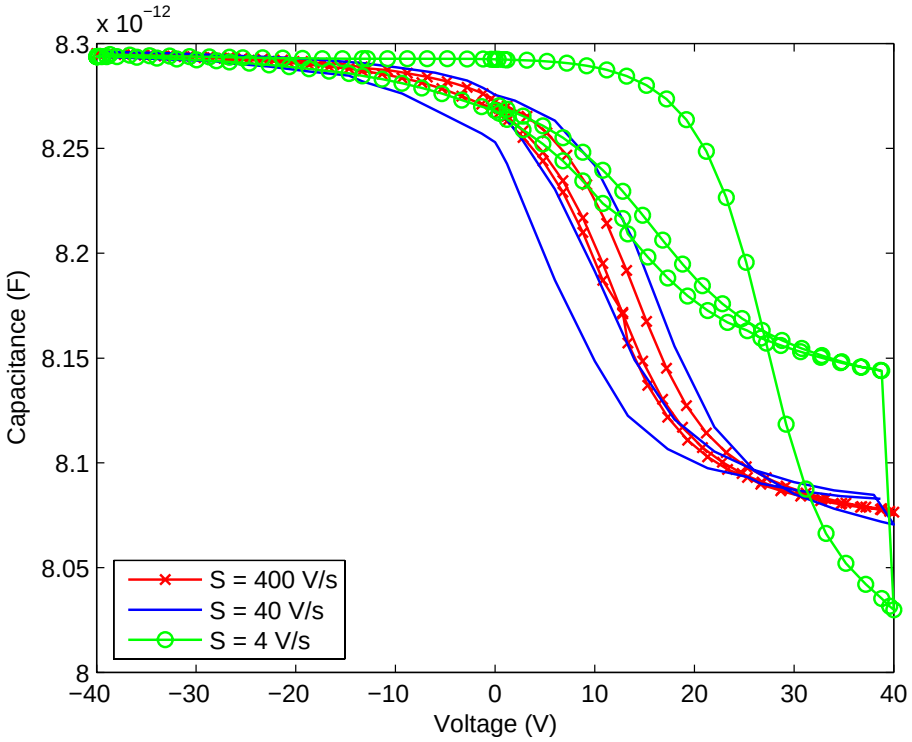

Figure 5.14: $C - V$ simulation for acceptor traps with sweep rates $S = 4 \div 400\,\mathrm{V/s}$. Hysteresis is counter-clockwise.

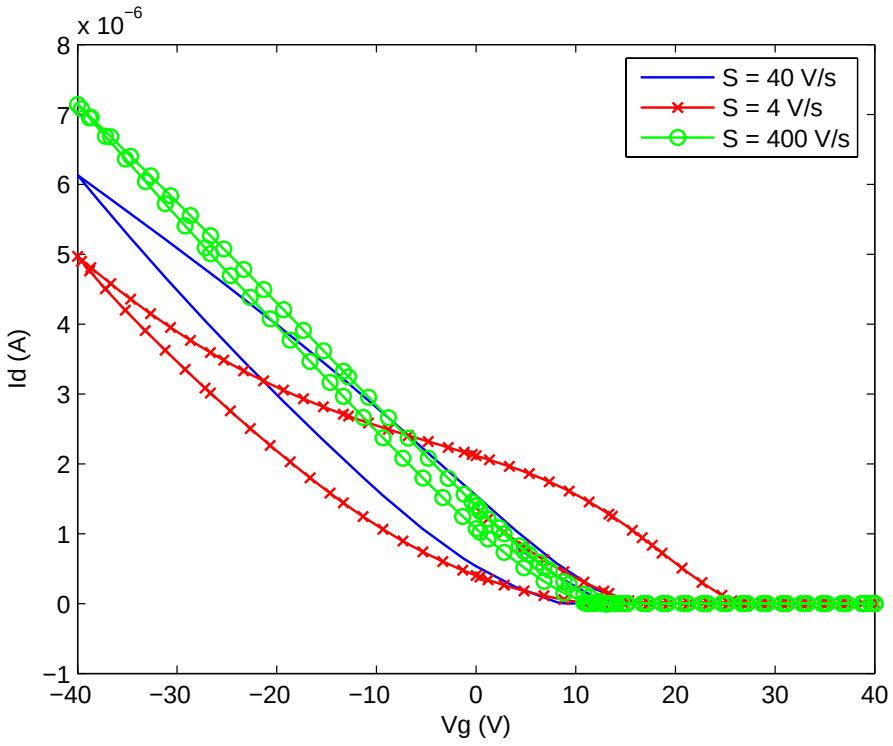

Figure 5.15: $I_\mathrm{d} - V_\mathrm{g}$ simulation for acceptor traps with sweep rates $S = 4 \div 400\,\mathrm{V/s}$. Hysteresis is counter-clockwise.

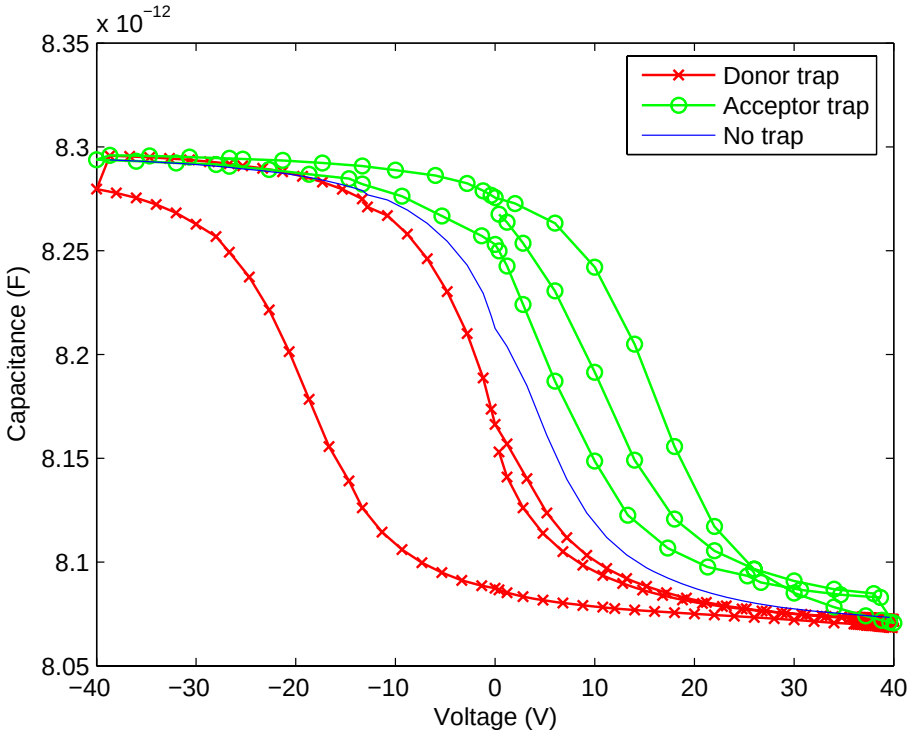

Figure 5.16: $C-V$ simulation for acceptor traps, donor traps and no traps. Hysteresis is counter-clockwise.

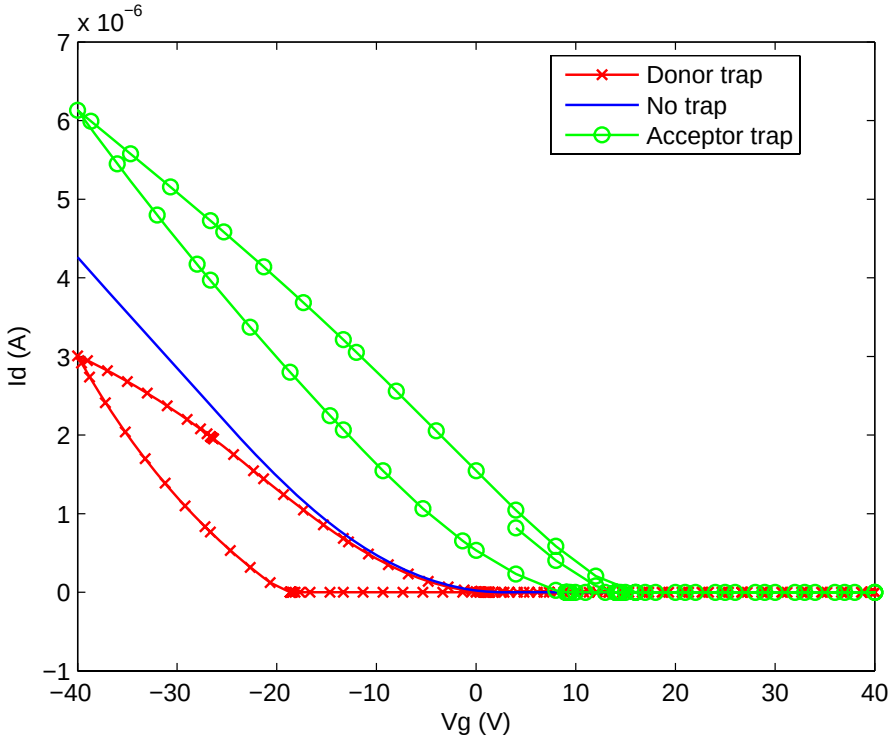

Figure 5.17: $I_{\mathrm{d}}-V_{\mathrm{g}}$ simulation for acceptor traps, donor traps and no traps. Hysteresis is counter-clockwise.

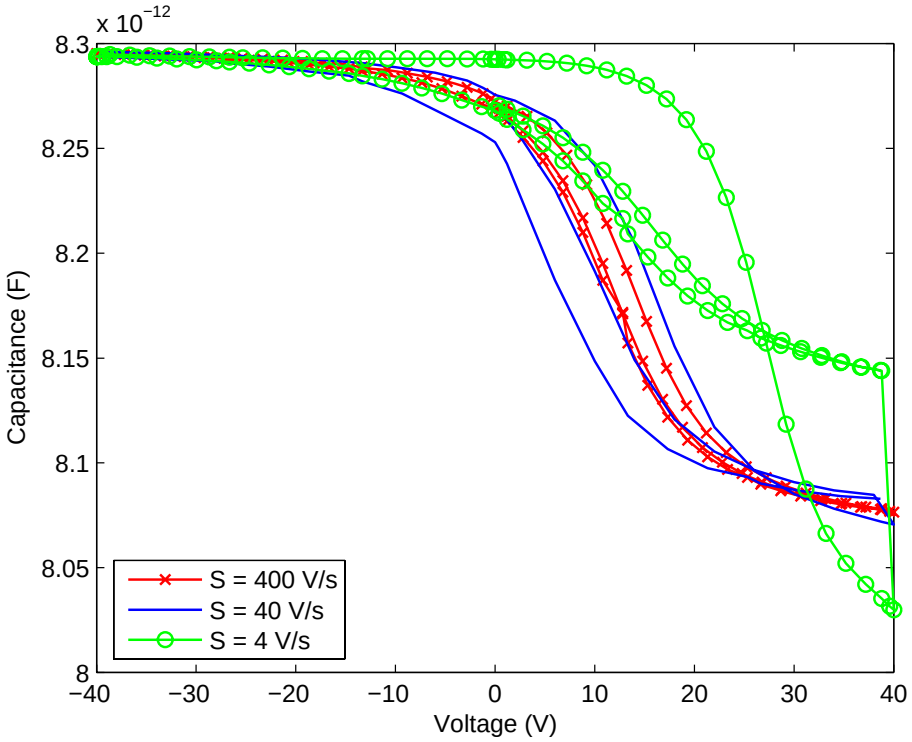

Figure 5.18: $C - V$ simulation for acceptor traps with sweep rates $S = 4 \div 400\,\mathrm{V/s}$. Hysteresis is counter-clockwise.

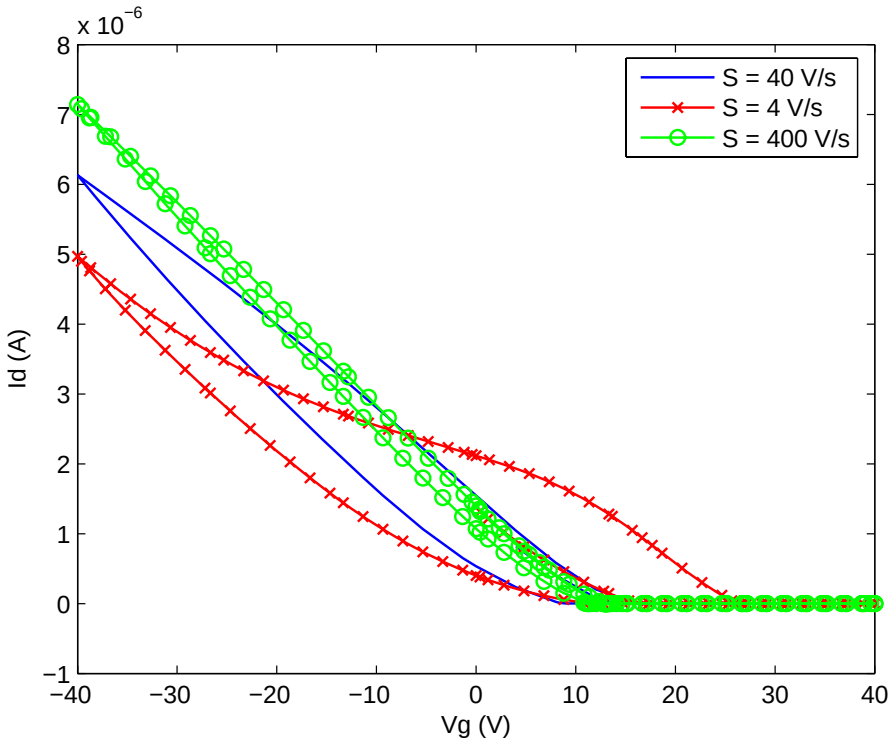

Figure 5.19: $I_\mathrm{d} - V_\mathrm{g}$ simulation for acceptor traps with sweep rates $S = 4 \div 400\,\mathrm{V/s}$. Hysteresis is counter-clockwise.

Chapter 6

Conclusion

In this thesis organic thin film transistors have been theoretically studied and modeled, focusing particularly on the electrical characteristics of the devices. We first introduce the models that describe charge transport in organic semiconductors and current equations in thin film transistors, focusing on their physical and electrical characteristics.

Then, we develop a model for cylindrical transistors, defining their electrical behavior in linear and saturation regime, and showing analogies and differences with the theory for planar transistors. A comparison with experimental results is also shown. Field-effect mobility is extracted and a heuristic equation for it is proposed, but future investigations are needed to derive a rigorous analytical approximation. The ultimate goal is to provide a compact model which can be used on simulations in which several transistors are connected for circuit applications.

We later analyze organic thin film transistors with short channel effects. More in detail, field-dependent mobility and space charge limited current effects are considered. A model is proposed for the thin film device, as well as for devices where no electric field exceeds the boundaries of the semiconductor. Again, a comparison with experimental devices is shown, with good agreement. Future activity on this topic will include a comparative analysis with two dimensional drift diffusion simulations, as well as further investigations on the contact effects in the device.

The last part of this thesis addresses the problem of trap recharging effects, which can affect the characteristics of organic thin film transistors. We have described the theory behind charge trap dynamics and have simulated it for several parameter sets, providing a critical review of the results. It is worth noting that trap recharging alone cannot model all the hysteresis effects experimentally measured, so further investigation is necessary, to incorporate other factors like polarons and mobile ions.

On the whole, this thesis has addressed some of the topics that constitute the theoretical modeling of organic transistors. This research field is rapidly developing as the

properties of the organic semiconductors, which are still partially unknown, are experimentally discovered. New device structures are developed, as well as new analytical and numerical models and theories, so that continuous improvements can enrich both the physical insight and the engineering in the field of organic electronics.

Bibliography

[AHL71] V. Ambegaokar, B. I. Halperin, and J. S. Langer. Hopping conductivity in disordered systems. *Physical Review B*, 4, no. 8:2612–2620, 1971. 20

[AP97] C. P. Auth and J. D. Plummer. Scaling theory for cylindrical, fully-depleted, surrounding-gate mosfets. *IEEE Electron Device Letters*, 18, NO. 2:74–76, 1997. 27

[atl] `www.silvaco.com`. 22

[BBM+04] A. Bolognesi, M. Berliocchi, M. Manenti, A. Di Carlo, P.Lugli, K. Lmimouni, and C. Dufour. Effects of grain boundaries, field-dependent mobility, and interface trap states on the electrical characteristics of pentacene tft. *IEEE Transcations on Electron Devices*, 51 no. 12:1997–2003, 2004. 44

[BCLC03] A. Bolognesi, A. Di Carlo, P. Lugli, and G. Conte. Large drift-diffusion and montecarlo modeling of organic semiconductor devices. *Synthetic Metals*, 138:95–100, 2003. 44

[BJDM97] A. R. Brown, C. P. Jarrett, D. M. Deleeuw, and M. Matters. Field-effect transistor made from solution-processed organic semiconductors. *Synthetic Metals*, 88:37–55, 1997. 35

[BRK+05] A. Bonfiglio, D. De Rossi, T. Kirstein, I. Locher, F. Mameli, R. Paradiso, and G. Vozzi. Organic field effect transistors for textile applications. *IEEE Transactions on Information Technology in Biomedicine*, 9:319–324, 2005. 27

[Bru05] W. Bruetting. *Physics of organic semiconductors*. Wiley-VCH, Weinheim, 2005. 3

[CLS+04] M. L. Chabinyc, J. Lu, R. A. Street, Y. Wu, P. Liu, and B. S. Ong. Short channel effects in regioregular poly(thiophene) thin film transistors. *Journal of Applied Physics*, 96, 4:2063–2070, 2004. 43

[Con56] E. M. Conwell. Impurity band conduction in germanium and silicon. *Physical Review*, 103, no. 1:51–61, 1956. 5

[CRV04] L. Colalongo, F. Romano, and Z.M.K. Vajna. Organic thin film transistors: a dc model for circuit simulation. *Solid-State Device Research conference*, pages 417 – 420, 2004. 13

[CSKVC05] E. Calvetti, A. Savio, Zs. M. Kovács-Vajna, and L. Colalongo. Analytical model for organic thin-film transistors operating in the subthreshold region. *Applied Physics Letters*, 87, no. 223506:1–3, 2005. 13

[DPK96] D.H. Dunlap, P. E. Parris, and V.M. Kenkre. Charge-dipole model for the universal field dependence of mobilities in molecularly doped polymers. *Physical Review Letters*, 77, no. 3:542–545, 1996. 21

[EIVS$^+$] M. Egginger, M. Irimia-Vladu, Reinhard Schwödiauer, Andreas Tanda, I. Frischauf, S. Bauer, and N. S. Sariciftci. Mobile ionic impurities in poly(vinyl alcohol) gate dielectric possible source of the hysteresis in organic field-effect transistors. *Adv. Mater.*, 20:1018–1022. 74

[FBC83] K. Fesser, R. Bishop, and D. K. Campbell. Optical absorption of polarons. *Physical Review B*, 27, no. 8:4804 – 4825, 1983. 7

[Fre38] J. Frenkel. On pre-breakdown phenomena in insulator and electronic semiconductors. *Physical Review*, 54:647–648, 1938. 21

[GGB06] C. Goldmann, D. J. Gundlach, and B. Batlogg. Evidence of water-related discrete trap state formation in pentacene single-crystal field-effect transistors. *Applied Physics Letters*, 88, no. 063501:1–3, 2006. 61

[Gil72] W. D. Gill. Drift mobilities in ampourphous charge-transfer complexes of trinitrofluorenone and poly-*n*-vynilcarbazole. *Journal of Applied Physics*, 43, no. 12:5033–5040, 1972. 22

[GKDF05] G. Gu, M. G. Kane, J. E. Doty, and A. H. Firester. Electron traps and hysteresis in pentacene-based organic thin-film transistors. *Applied Physics Letters*, 87, 243512:1–3, 2005. 61

[GLPS89] A. A. Grinberg, S. Luryi, M. R. Pinto, and N. L. Schryer. Space-charge-limited current in a film. *IEEE Transaction on Electron Devices*, 36, no. 6:1162–1170, 1989. 48

[GMS07] T. Goudon, V. Miljanović, and C. Schmeiser. On the schockley-read-hall model: generation-recombination in semiconductors. *SIAM Journal on Applied Mathematics*, 67, no. 4:1183–1201, 2007. 64

[Hal52] R. N. Hall. Electron-hole recombination in germanium. *Physical Review*, 87:387, 1952. 62

[Hee68] H. F. Van Heek. Hall mobility of electrons in the space-charge layer of cdse transistor. *Solid State Electronics*, 11:459–467, 1968. 19

[HHB+98] G. Horowitz, R. Hajlaoui, H. Bouchriha, R. Bourguiga, and M. Hajlaoui. The concept of threshold voltage in organic field effect transistors. *Advanced Materials*, 10 (12):923–927, 1998. 12, 13, 27, 31, 35

[HHD95] G. Horowitz, R. Hajlaoui, and P. Delannoy. Temperature dependence of the field-effect mobility of sexithiophene. determination of the density of traps. *Jour. Phys. III France*, 5:355–371, 1995. 6, 20

[HHH00] G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui. Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors. *Journal of Applied Physics*, 87 (9):4456–4463, 2000. 6, 18, 19

[HHK98] G. Horowitz, R. Hajlaoui, and F. Kouki. An analytical model for the organic field-effect transistor in the depletion mode. application to sexithiophene films and single crystals. *The European Physical Journal Applied Physics*, 1:361–367, 1998. 14, 15, 27, 46, 47

[HN07] B. H. Hamadani and D. Natelson. Gated nonlinear transport in organic polymer field effect transistors. *Journal of Applied Physics*, 95, 3:1227–1232, 2007. 21, 43, 44

[HOH+08] D. K. Hwang, M. S. Oh, J. M. Hwang, J. H. Kim, and S. Im. Hysteresis mechanisms of pentacene thin-film transistors with polymer/ oxide bilayer gate dielectrics. *Applied Physics Letters*, 92:013304,1–3, 2008. 74

[Hol59] T. Holstein. Studies of polaron motions - part i: the molecular-crystal model. *Annals of Physics*, 8:325–342, 1959. 7

[HRG+07] B. H. Hamadani, C. A. Richter, D. J. Gundlach, R. J. Kline, I. McCulloch, and M. Heeney. Influence of source-drain electric field on mobility and charge transport in organic field-effect transistors. *Journal of Applied Physics*, 102, no. 044503:1–7, 2007. 21, 44

[HZZ+06] J. N. Haddock, X. Zhang, S. Zheng, Q. Zhang, S. R. Marder, and B. Kippelen. A comprehensive study of short channel effects in organic field-effect transistors. *Organic Electronics*, 7:46–54, 2006. 43

[IPR+85] H. Iwai, M. R. Pinto, C. S. Rafferty, J. E. Oristian, and R. W. Dutton. Velocity saturation effect on short-channel mos transistor capacitance. *IEEE Electron Device Letters*, EDL-6, no. 3:120–122, 1985. 67

[JL04] C.H. Park S. S. Kim S. Im J. Lee, D. K. Hwang. Pentacene-based photodiode with schottky junction. *Thin Solid Films*, 451-452:12–15, 2004. 65

[KB04] M. Koehler and I. Biaggio. Space-charge and trap-filling effects in organic thin film field-effect transistors. *Physical Review B*, 70:045314–1,8, 2004. 43

[KdSFBZ05] J. H. Kang, D. da Silva Filho, J. L. Bredas, and X. Y. Zhu. Shallow trap states in pentacene thin films from molecular sliding. *Applied Physics Letters*, 86, no. 152115:1–3, 2005. 61

[KHG01] A. Kranti, S. Haldar, and R.S. Gupta. Analytical model for threshold voltage and i-v characteristics of fully depleted short channel cylindrical surrounding gate mosfet. *Microelectronic Engineering*, 56:241–259, 2001. 27

[KSR+03] H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D.Sheraw, J. A.Nichols, and T. N.Jackson. Contact resistance in organic thin film transistors. *Solid-State Electronics*, 47:297–301, 2003. 31

[Lau85] S. E. Laux. Techniques for small-signal analysis of semiconductor devices. *IEEE Transactions on Electron Devices*, 32:2028–2037, 1985. 68

[LK05] L. Li and H. Kosina. An analytical model for organic thin film transistors. *IEEE Conference on Electron Devices and Solid-State Circuits*, pages 571–574, 2005. 13, 21

[LMK07] L. Li, G. Meller, and H. Kosina. Influence of traps on charge transport in organic semiconductors. *Solid State Electronics*, 51:445–448, 2007. 61

[LPS05] Th. Lindner, G. Paasch, and S. Scheinert. Hysteresis in organic field-effect devices: simulated effects due to trap recharging. *Journal of Applied Physics*, 98, no. 114505:1–9, 2005. 61, 74

[LS] J.B. Lee and V. Subramanian. Weave patterned organic transistors on fiber for e-textiles. *IEEE Transactions on Electron Devices*, 52 (2):269–275. 27

[MA60] A. Miller and E. Abrahams. Impurity conduction at low concentrations. *Physical Review*, 120, no. 3:745–755, 1960. 5

[MMH+01] E. J. Meijer, A. V. G. Mangnus, C. M. Hart, D. M. de Leeuw, and T. M. Klapwijk. Frequency behavior and the mott-schottky analysis in poly(3-hexyl thiophene) metal-insulator-semiconductor diodes. *Applied Physics Letters*, 78, no. 24:3902–3904, 2001. 53

[MOC+06] M. Maccioni, E. Orgiu, P. Cosseddu, S. Locci, and A. Bonfiglio. Towards the textile transistor: assembly and characterization of an organic field effect transistor with a cylindrical geometry. *Applied Physics Letters*, 89, 143515, 1-3, 2006. 27

[Mot56] N. F. Mott. The transition to metallic conduction in semiconductors. *Canadian Journal of Physics*, 34:1356–68, 1956. 5

[NDK+98] S.V. Novikov, D.H. Dunlap, V.M. Kenkre, P. E. Parris, and A.V. Vannikov. Essential role of correlations in governing charge transport in disordered organic materials. *Physical Review Letters*, 81, no. 20:4472–4475, 1998. 21

[NFS07] D. Natali, L. Fumagalli, and M. Sampietro. Modeling of organic thin film transistors: Effect of contact resistances. *Journal of Applied Physics*, 36, no. 6:1162–1170, 2007. 57

[NSGJ03] P. V. Necliudov, M. S. Shur, D. J. Gundlach, and T. N. Jackson. Contact resistance extraction in pentacene thin film transistors. *Solid-State Electronics*, 47:259–262, 2003. 39

[OP80] J. W. Orton and M. J. Powell. The hall effect in polycristalline and powdered semiconductors. *Reports on Progress in Physics*, 43:1263–1307, 1980. 18

[PS66] F. A. Padovani and R. Stratton. Field and thermionic-field emission in schottky barriers. *Solid State Electronics*, 9:695–707, 1966. 19

[PSH+08] G. Paasch, S. Scheinert, A. Herasimovich, I. Hörselmann, , and Th. Lindner. Characteristics and mechanisms of hysteresis in polymer field-effect transistors. *Physica Status Solidi (a)*, 3:534–548, 2008. 61

[sen] `www.synopsys.com`. 22, 48

[SG06a] P. Stallinga and H. L. Gomes. Modeling electrical characteristics of thin-film field-effect transistors i: Trap free materials. *Synthetic Metals*, 156:1305–1315, 2006. 13, 46

[SG06b] P. Stallinga and H. L. Gomes. Modeling electrical characteristics of thin-film field-effect transistors ii: Effects of traps and impurities. *Synthetic Metals*, 156:1316–1326, 2006. 13, 43

[SGB+04] P. Stallinga, H. L. Gomes, F. Biscarini, M. Murgia, and D. M. deLeeuw. Electronic transport in field-effect transistors of sexithiophene. *Journal of applied physics*, 96, 9:5277–5283, 2004. 43

[SH84] M. Shur and M. Hack. Phyisics of amourphous silicon based alloy field-effect transistors. *Journal of Applied Physics*, 55, no. 10:3831–3842, 1984. 6

[SMS+05] Th. B. Singh, N. Marjanovič, P. Stadler, M. Auinger, G. J. Matt, S. Günes, N. S. Sariciftci, R. Schwödiauer, and S. Bauer. Fabrication and characterization of solution-processed methanofullerene-based organic field-effect transistors. *Journal of Applied Physics*, 97, no. 083714:1–5, 2005. 61

[SPG89] L. B. Schein, A. Peled, and D. Glatz. The electric field dependence of the mobility in molecularly doped polymers. *Journal of Applied Physics*, 66, no. 2:686–692, 1989. 21

[SR52] W. Schockley and W. T. Read. Statistics of the recombination of holes and electrons. *Physical Review*, 87, no. 5:835–842, 1952. 62

[SvS02] R. Schmechel and H. von Seggern. Deep-level defect characteristics in pentacene organic thin films. *Applied Physics Letters*, 80, no. 9:1595–1597, 2002. 61

[SvS04] R. Schmechel and H. von Seggern. Electronic traps in organic transport layers. *Physica status solidi (a)*, 201, no. 6:1215–1235, 2004. 61

[Sze81] S. M. Sze. *Physics of semiconductor devices*. Wiley & Sons, 2 edition, 1981. 32, 62, 68

[TDK95] L. Torsi, A. Dodabalapur, and H. E. Katz. An analytical model for short-channel organic thin-film transistors. *J. Appl. Phys.*, 78 (2):1088–1093, 1995. 43

[TMBdL03] C. Tanase, E.J. Meijer, P.W.M. Blom, and D.M. de Leeuw. Local charge carrier mobility in disordered organic field-effect transistors. *Organic Electronics 4*, 4:33–37, 2003. 57

[VM98] M. C. J. M. Vissenberg and M. Matters. Theory of the field-effect mobility in amorphous organic transistors. *Physical Review B*, 57, no. 20:964–967, 1998. 5, 20

[Vol90] K. P. C. Vollhardt. *Organische chemie*. VCH-Verlag, Weinheim, 1990. 3

[WFBD07] L. Wang, D. Fine, D. Basu, and A. Dodabalapur. Electric-field-dependent charge transport in organic thin-film transistors. *Journal of Applied Physics*, 101, no. 054515:1–8, 2007. 21

[YK58] J. Yamashita and T. Kurosawa. On electronic current in NiO. *Journal of Physics and Chemistry of Solids*, 5:34–43, 1958. 7

[ZS01] J. Zaumseil and H. Sirringhaus. Prospects of manufacturing organic semiconductor-based integrated circuits. *IEEE Transactions on Semiconductor Manufacturing*, 14, no. 3:281–296, 2001. 4

[ZS07] J. Zaumseil and H. Sirringhaus. Electron and ambipolar transport in organic field-effect transistors. *Chemical Reviews*, 107:1296–1323, 2007. 9

List of Publications Related to the Thesis

Journal papers

1. *Modeling of short channel effects in organic thin-film transistors*
   S. Locci, M. Morana, E. Orgiu, A. Bonfiglio, P. Lugli - *IEEE Transactions on Electron Devices*, Vol. 55, no. 10, October 2008.

2. *An analytical model for cylindrical thin film transistors*
   S. Locci, M. Maccioni, E. Orgiu, A. Bonfiglio - *IEEE Transactions on Electron Devices*, Vol. 54, no. 9, September 2007.

3. *Towards the textile transistor: assembly and characterization of an organic field effect transistor with a cylindrical geometry*
   M. Maccioni, E. Orgiu, P. Cosseddu, S. Locci, A. Bonfiglio - *Applied Physics Letters* 89, 143515:1-3 (2006) (selected for publication on the Virtual Journal of Nanoscale Science and Technology of the American Institute of Physics and the American Physical Society).

Conference proceedings

1. *Investigation on different organic semiconductor/organic dielectric interfaces in pentacene based thin-film transistors*
   Emanuele Orgiu, Mohammad Taki, Beatrice Fraboni, Simone Locci, Annalisa Bonfiglio, *Mater. Res. Soc. Symp. Proceedings*, Boston, 26-30 November, 2007.

2. *Woven Electronics: a new perspective for wearable technology*
   S. Locci, M. Maccioni, E. Orgiu, A. Bonfiglio, *Proceedings of the 29th Annual International Conference of the IEEE-EMBS*, Cit Internationale, Lyon, France, August 23-26, 2007.

3. *Yarn-like devices for textile electronics*
   A. Bonfiglio, I. Manunza, M. Maccioni, S. Locci, E. Orgiu, P. Cosseddu, G. Le Blevennec, M. Verilhac, *E-MRS 2007 Spring Meeting*, Strasbourg, France - May 28th-June 1st, 2007.

4. *Micro- and nano-technologies for wearable applications in emergencies management*
   A. Bonfiglio, N. Carbonaro, I. Chartier, C. Chuzel, D. Curone, G. Dudnik, F. Germagnoli, D. Hatherall, J. M. Koller, T. Lanier, G. Le Blevennec, S. Locci, G. Loriga, J. Luprano, M. Maccioni, G. Magenes, R. Paradiso, H. Rouault, A. Tognetti, J. M. Verilhac, G. Voirin, R. Waite *Proceedings of PHealth 2007 Conference*, Porto Carras (Greece), 20-23 June 2007.

5. *The textile transistor: a perspective for distributed, wearable networks of sensor devices*
   M. Maccioni, E. Orgiu, P. Cosseddu, S. Locci, A. Bonfiglio, *Proceedings of the 3rd IEEE-EMBS - International Summer School and Symposium on Medical Devices and Biosensors*, MIT, Boston, USA, Sept.4-6, 2006.

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I remember when I first started to talk about my PhD activity with my advisor, prof. Annalisa Bonfiglio, whom I want to thank for giving me the opportunity to work in her team: I was so happy, I was about to do scientific research, and even in a fascinating and attractive topic! I immediately began to study, and soon I made my first scientific hypotheses, I checked their validity, I wrote long, long matlab scripts and equations rich in mysterious symbols. Giving meaning to all those strange physical phenomena, getting nice and useful ideas: yes, that was now my daily challenge. Sometimes hard, but fun, rewarding. I was the only crazy theoretician in my research group in Cagliari, and I want to thank all of them: Piero, Emanuele, Giorgio, Maurizio, Mauro. Our secretary Simona and Ileana, also part of my group, deserve a special big GRAZIE!, because they also became very close and true friends.

The usual PhD routine went on for two years, then the lightning. I got the chance to join a new research group, far away, but I was a bit scared, having to change my life completely from one day to the other. I accepted, and the new home for me became: München! Warm temperatures and crystalline sea, joy and delight of Sardinia? No more! The north icy wind, the soft white snow, suddenly a revolution. I came to München alone, knowing nobody and ignoring completely even the meaning of the simplest words: Grüß Gott, tchüß!, schnitzel :) . The adventure was just starting. I met there my new research group and I could immediately notice a difference with my group in Cagliari: there, I was the only theoretician, being the others all experimental guys; now all of us were, let's say, math lovers.

Now I want to thank them: of course prof. Paolo Lugli, my new boss, our secretaries Bettina and Rita, Giuseppe, Christian. But also the two other Italian Phd students of the group, Mario and Federico, with whom I had so much fun, starting from remembering strange sentences like "Solo Puffin ti darà, forza e grinta a volontà!" (I think in German it's "Nur Puffin schenkt mir die Kraft und Ausdauer die ich brauche", in English I don't know the exact sentence, but ok, somebody knows what we were remembering :)), continuing with repeating countless times and laughing at the famous press conference, in 1998, of the best footlball trainer ever, Giovanni Trapattoni (Ich habe fertig!!!), and ending with

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So, I am at the end of the story. What's next is kindly unknown, and still has to be written.

Simone