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OPTIMIZATION OF THE GATE DRIVER PARAMETERS IN A WIDE BAND GAP MATERIAL BASED DC-DC CONVERTERS FOR HIGH POWER APPLICATIONS

Scientific Disciplinary Sector(s)

ING-IND/32 – Convertitori, Macchine E Azionamenti Elettrici

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ABSTRACT

DC-DC converters are being used for power management and battery charging in electric vehicles (EVs). To further the role of EVs in market, more efficient power electronic converters are needed. In this scenario, wide band gap (WBG) devices, such as silicon carbide (SiC) and gallium nitride (GaN), are inevitably the future of power electronic converters, because they provide higher frequency and lower power loss. However, their high di/dt and dv/dt transients result in higher electromagnetic interference (EMI). On the other hand, some gate driver parameters such as gate resistor (RG) have contradictory effect on efficiency (η) and EMI. So the fast transition switching time makes the gate driver design a challenging task. The idea of the thesis is to investigate the values of these parameters using a multi-objective optimization method to optimize η and EMI at the same time. To this aim, first, the effect of high/low side RG on η and EMI in the half-bridge configuration is studied. Then, the objective functions of the optimization problem are obtained using a numerical regression method on the basis of the experimental tests. Then, the values of the gate resistors are obtained by solving the multi-objective optimization problem. Finally, η and EMI of the converter in the optimum gate resistor design are compared to those in the conventional design to validate the effectiveness of the proposed design approach.

In particular two distinct cases are discussed and presented. The first case, a SiC-based half-bridge converter prototype was tested and the objective functions considered are efficiency and conducted EMI current which passes through the power ground (PG), considering the maximum amplitude of this ground current in μAdB ($\hat{I}_{GR}$) as the EMI level of the converter. In the second case, a GaN-based half-bridge converter prototype was tested and the objective functions considered are efficiency and the near-field EMI of the GaN devices to evaluate the EMI level of the converter.

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1. INTRODUCTION

1.1 Background

Global warming has become a significant concern in recent years. The effects of climate change are visible and result in societies taking action to reduce CO2 emissions. The temperature rise limit to 2°C above pre-industrial levels, to that of 2008, the CO2 emissions must be reduced by half by 2050 [1]. Developed countries are targeting even higher reductions. For example, the United Kingdom targets 80% [2].

Nearly 42% of global CO2 emissions in 2012 were from electricity and heating sources, while transport was responsible for 23% [3]. Reductions in these areas would result in significant decreases since they represent 65% of the total emissions.

The global energy demand is continuously growing; forecasts indicate that electricity generation will grow from 20.2 trillion kWh in 2010 to 39 trillion kWh by 2040, [4], close to a 100% increase. Clean energy sources must meet this additional demand and replace part of the current demand if a reduction of CO2 emissions is to be considered. Solar and wind energies are up-and-coming options to replace fossil fuel generation, but the costs of these technologies need to decrease if they are to be widely used.

Another excellent opportunity area is transport, the second-largest generator of CO2 emissions. Hybrid and fully electric cars have become available in the last few years. However, they are also more expensive than their conventional counterparts limiting their adoption. Meanwhile, the aerospace sector is implementing the concept of more electric aircraft (MEA) where electrical systems replace pneumatic, mechanical, and hydraulic systems to increase efficiency and reduce maintenance costs.

Power Electronics plays a crucial role in the generation, storage, and distribution cycle of electric energy. The central portion of the generated electric energy is consumed after several transformations, with many carried out by power electronic converters. They include different systems (power supplies for computers, motor drives, domestic appliances, industrial converters, industrial and telecom systems, etc.). The most considerable portion of the power

losses in these power electronic converters are dissipated in their power semiconductor devices.

The evolution of power electronics technology has permanently moved toward higher efficiency, higher power density, and more integrated systems [5]-[6]. Power semiconductor devices play a critical role in this ongoing evolution. To date, the advancements have been primarily driven by various silicon (Si) power devices developed and matured over the last 50 years. In applications below 600 V, Si metal-oxide semiconductor field-effect transistors (MOSFETs) dominate the market based on a trench gate structure. At the same time, Si super junction MOSFETs and Si insulated gate bipolar transistors (IGBTs) based on field stop and injection enhancement concepts dominate the market from 600 V to 6.5 kV.

Si MOSFET technology has gradually improved, as reflected in its figures of merit (FOM). FOM commonly used to compare different technologies is the on-state resistance normalized to a unit of area ($R_{DS\text{-}ON}*A$) ($RDS\text{-}ON*A$) and the gate to drain charge normalized to the on-state resistance resistance ($R_{DS\text{-}ON}*Q_{GD}$), [7], charging and discharging processes determine the voltage switching time which is the main factor impacting the switching losses of a unipolar power device, [8]. The first FOM indicates how the conduction losses compare between technologies, while the second shows the potential switching loss difference.

Each technology has a limit in the minimum $R_{DS\text{-}ON} * A$ (called the specific on-resistance) that can be achieved for a specific breakdown voltage, for example, the limit is around $50m\Omega*cm^2$ at 600V for silicon. Current Si devices are very close to the limit, [9-]-[10]-[11].

However, Silicon (Si) power devices have developed a theoretical limit, which makes it almost impossible to further improve the two key drivers by using Silicon-based devices.

Furthermore, Si exhibits some important limitations regarding its voltage blocking capability, operation temperature, and switching frequency. The maximum blocking voltage of the IGBT is lower than 6.5 kV, and the practical operating temperature is lower than 175 C [12]. Because of the bipolar current conduction mechanism in IGBTs, their switching speeds are also relatively slow, limiting them to lower- switching-frequency applications. Future development in Si power device technologies will continue, but it will be incremental.

Therefore, a new generation of power devices is required for power converters in applications where electronic systems based on traditional Si power devices cannot operate.

A revolutionary development in recent entry years has been the introduction of power devices based on wide bandgaps (WBG) materials such as SiC and GaN. As a WBG material, SiC has several superior properties that are attractive for power device design.

Therefore, the new WBG power devices can play the leading role in energy-efficient systems. Among the possible candidates, SiC and GaN present the better trade-off between theoretical characteristics (high voltage blocking capability, high-temperature operation, and high switching frequencies) and actual commercial availability of the starting material (wafers) and maturity of their technological processes. Table 1 and Figure 1 summarize the main material parameters of WBG semiconductors candidates to replace Si.

Material	E_g (eV) @300K	μ_n ($cm^2/V.s$)	μ_p ($cm^2/V.s$)	v_{sat} (cm/s)	E_c (V/cm)	λ (W/cm.K)	ε_r
Si	1.12	1 450	450	10^7	3×10^5	1.3	11.7
GaAs	1.4	8 500	400	2×10^7	4×10^5	0.54	12.9
3C – SiC	2.3	1000	45	2.5×10^7	2×10^6	5	9.6
6H – SiC	2.9	415	90	2×10^7	2.5×10^6	5	9.7
4H - SiC	3.2	950	115	2×10^7	3×10^6	5	10
GaN	3.39	1000	35	2×10^7	5×10^6	1.3	8.9
GaP	2.26	250	150		10^7	1.1	11.1
Diamond	5.6	2200	1800	3×10^7	5.6×10^7	20	5.7

Table 1 - Physical properties of different semiconductors for power devices

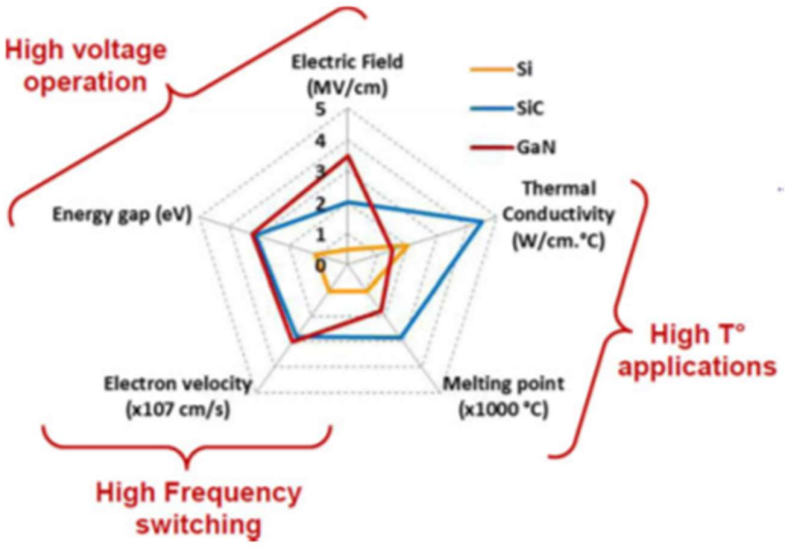

Figure 1 - Summary of Si, SiC and GaN relevant material properties

T These new materials allow significant improvements to the figure of merit of switching devices. Thanks to their wider band-gap energy, it is possible to fabricate smaller appliances for a particular breakdown voltage with similar or smaller on-state resistance than Si devices. The reduction of size is accompanied by reductions in charge, improving the $R_{DS\text{-}ON} * Q_{GD}$ figure of merit and suggesting lower device switching losses for a given on-state resistance. Figure 2 presents the one-dimensional theoretical limit for Si and the new wide band-gap materials [13]

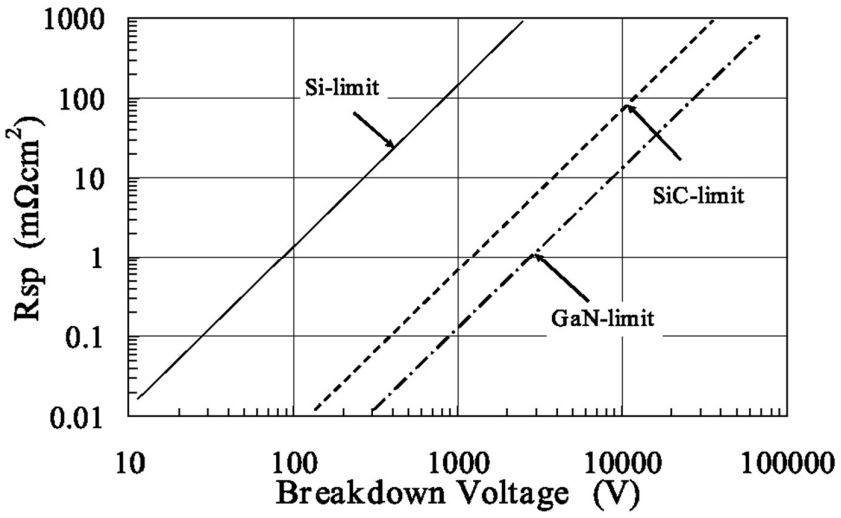

Figure 2 - Specific on-resistance vs breakdown voltage limit for Si, SiC and GaN

The lowest theoretical value of specific on-resistance is presented by GaN and indicates the possibility of reaching the best figure of merit. The reduction of switching losses increases the switching frequency, reducing the size of magnetic devices and output filters and resulting in a smaller and cheaper system.

GaN and especially SiC process technologies are by far more mature and, therefore, more attractive from the device manufacturer's perspective, especially for high power and high-temperature electronics (HTE). GaN can offer better high frequency and high voltage performances, but the lack of quality bulk substrates is a disadvantage for vertical devices. Nevertheless, GaN presents a lower thermal conductivity than SiC. At present, SiC is considered to have the best trade-off between properties and commercial maturity, with considerable potential for both HTE and high power devices. However, the industrial interest in GaN power devices is a fact. For this reason, SiC and GaN are the more attractive candidates. SiC process technologies are more mature and, therefore, more attractive from the device manufacturer's perspective, especially for high power and high-temperature electronics (HTE). GaN can offer better high frequency and high voltage performances, but the lack of quality bulk substrates is a disadvantage for vertical devices. Nevertheless, GaN presents a lower thermal conductivity than SiC. At the present time, SiC is considered to have the best trade-off between properties and commercial maturity with considerable potential for both HTE and high power devices. However, the industrial interest in GaN power devices is a fact. For this reason, SiC and GaN are the more attractive candidates to replace Si in these applications. Some SiC devices, such as Schottky diodes, already compete with Si power diodes. On the other hand, GaN allows forming of hetero-junctions (InAlGaN alloys) that can be grown either on SiC or Si substrates. Currently, there is a sort of competition between SiC and GaN in a battle of performance versus cost. Nevertheless, scientific and industrial actors agree that both will find their respective application fields with a tremendous potential market.

However, many material advantages remain not fully exploited due to specific material quality, technology limitations, non-optimized device designs, and reliability issues. Traps, dislocations, interface states, micro-pipes, micro-cracks, etc., still should be minimized. The role and control of residual strains need new research efforts; the contact resistivity of the metal/WBG-semiconductor has to be significantly reduced; device reliability is in its infancy, etc. Recently SiC power devices reported in the literature include high voltage and high-

temperature diodes, junction controlled devices (like JFETs and MESFETs), MOSFETs, Thyristors, and IGBTs. Those based on GaN include diodes, HEMTs, and MOSFETs, and advanced research on novel devices concerning low-losses digital switches based on SiC and GaN is also of primary concern. These novel devices represent a real breakthrough in power devices.

Furthermore, the progress of modeling and electro-thermal characterization tools for these power devices and the design of their packaging, drivers, and controllers need a significant research effort, and they represent a world-class innovation.

1.2 Wide Band-Gap Power Devices

1.2.1 Silicon Carbide

The progress in SiC wafers quality is contemplated in the achievement of very low micropipe density (0.75 cm-2 for a 75 mm wafer), which provides the basis for a high fabricating process yield of large area SiC power devices. 100 mm SiC wafers are already in the market, and it is expected that 150 mm SiC wafers will be available in the near future [14]. One of the major concerns has been reducing the micropipe density in SiC substrates, which has been driven by the phenomenological understanding of the mechanisms responsible for pipe formation during SiC crystal growth. However, other defects, such as basal plane dislocations, are still under investigation causing poor reliability in bipolar devices. Besides, the minority carrier lifetime in thick epilayers appears to be long enough for conductivity modulation, as inferred from high voltage (20 kV) reported diodes [15]-[16]. High voltage experimental SiC-based two-terminal rectifiers and three-terminal switches have been demonstrated.

Owing to the much wider energy bandgap of a 4H-SiC material compared with Si, its intrinsic carrier density is much smaller, which enables a high-temperature operation capability from a blocking stability point of view. The 10ξ critical electric field in SiC makes ultra–high-voltage (>10 kV) power devices practically achievable. The ideal specific conduction resistance ($R_{on,sp}$) of an SiC unipolar device can be much smaller than that of its Si counterpart. The smaller $R_{on,sp}$ enables SiC chips to be smaller, leading to lower parasitic capacitance and

higher switching speed. Therefore, it is possible to achieve low switching and conduction losses for a wide range of blocking voltages and frequencies. The lower losses enable accessible power converter structures because simple two-level topologies can be used in most applications. So SiC power devices will further rapidly evolve power electronics systems toward even higher efficiency and power density. Although SiC dies can operate at higher temperatures, the peripheral components— such as the package materials, housings, and capacitors—are not mature. Therefore, the exploration of these components lags behind the progress in reaching higher voltages and higher frequencies.

There has been strong momentum in SiC technology development and market growth since the first commercial SiC Schottky diode by Infineon in 2001. Until now, the unipolar SiC diode was the only commercially available diode on the market; its typical voltage ratings are 600 V, 650 V, 1.2 kV, and 1.7 kV. Some 3.3 kV and 8 kV products also are available; however, their current rating is limited by the thick drift layer. These devices are significantly faster than Si PIN diodes because there is no minority carrier storage in the SiC diode.

The active switches available in the market include SiC MOSFETs, junction gate field-effect transistors (JFETs), and bipolar junction transistors (BJTs). Previously, the SiC JFET was more favorable because of its easy implementation and because it does not exhibit the gate-oxide reliability issue observed in the SiC MOSFET. Although its "normally on" characteristic makes it less attractive in some applications, a JFET with a cascode structure could eliminate this issue. The commercial SiC MOSFET was first released in 2011 by Cree. For the SiC MOSFET, the 1.2 kV class became the entry and dominant point in the market, as this is the breaking point between Si MOSFETs (including the super junction MOSFET) and the Si IGBT. The SiC MOSFET provides an excellent balance between conduction losses and switching losses at blocking voltages of less than 2.5 to 3.3 kV. The SiC BJT's switching speed is similar to that of the MOSFET owing to the absence of any sizable minority carrier storage in the drift region. Since the BJT does not have a channel region, its on-resistance is lower than that of the SiC MOSFET. However, the current driving characteristic makes it less attractive for various applications.

In many commercial applications, SiC has found its utility. Such as in power factor correction, lighting, solar, railway traction, and uninterrupted power supply (UPS) will enter into drive, wind, and electrical vehicle (EV). Aside from the technical design challenges,

balancing the higher cost of SiC devices with improved system cost and performance is the most critical issue. The price per watt is one of the most concerning figures of merit from a user perspective. However, depending on the application, a higher device cost does not necessarily lead to a higher system cost, which will be explained later. As can be seen, SiC devices and power conversion systems have entered the commercialization stage. The main focuses of the industry depend on the application demand, cost, and process maturity. From the technology development point of view, the potential of SiC materials is not fully explored, and much more effort is ongoing. The following sections of this paper review the technology advancement of SiC power devices and the critical applications and present the future challenges and development trends.

1.2.2 Gallium Nitride

GaN devices have attracted a great attention in recent years with a remarkable tradeoff between specific on-resistance and breakdown voltage. They are well suited for high-power switching applications, with a projected ×100 performance advantage in the square breakdown voltage per specific on-resistance figure of merit ($V_{BR}^2/R_{DS(on)}$) over silicon power devices [17]. This translates into a GaN high electron mobility transistors (HEMTs) with a smaller die size for a given $R_{DS(on)}$ and breakdown voltage, which directly increases power density.

Furthermore, GaN HEMT has a much smaller gate charge and junction capacitors when compared to the silicon MOSFET. A smaller gate charge achieves a faster turn-on/off speed for the devices, and a smaller junction capacitor stores less energy during the turn-off period. Both of these characteristics can shorten the current and voltage transition interval and thus reduce switching loss. In general, the high performance of GaN HEMT provides the opportunity to achieve a higher frequency compared to the silicon MOSFET with the same efficiency. However, the switching loss of GaN HEMT is not only determined by the GaN to die but is also related to the parasitic inductors of the device package and printed circuit board (PCB) layout. These parasitic inductors will deteriorate the switch transition and increase the switching loss. Furthermore, the device junction capacitor still introduces a significant loss in hard-switching

conditions, especially in a bridge configuration. As a result, the soft-switching technique is still beneficial for GaN HEMT to achieve high efficiency in high-frequency operation [18].

Compared to GaN, the SiC device technology is in an advanced stage, where particularly, SiC-based diodes have proven their maturity and robustness in industry applications. However, due to its higher cost (10-15 times higher than equivalent Si devices), its use has been limited chiefly for critical applications. On the other hand, the predicted GaN device price is soon expected to be in the range of today's equivalent Si device. Due to its attractive pricing, GaN devices are expected to be much more acceptable to the industry shortly than SiC devices. Unlike SiC devices, GaN devices are not widely available in the market. Some GaN manufacturers, like efficient power conversion (EPC), provide GaN devices up to 200-V rating and can be used only in low voltage (LV) applications. A number of applications, however, demand devices with a voltage rating of 600 V and above. As of now, only a few device manufacturers are able to provide 600-V GaN switches and diodes. Many other manufacturers such as IR, GaNSystems, MicroGaN, and Transphorm are developing high-voltage and high-current GaN devices, which are expected to be available as samples from early 2014 [19].

In power electronic converters, an essential component is a switching device. Most power losses are dissipated in the switching devices: switching loss and conduction loss. In addition, the size of the passive component (inductors and capacitors) is directly related to the characteristics of the switching devices, such as switching speed (switching frequency). Operating at a higher switching frequency results in lower current and voltage ripples, which makes the size of the passive components smaller. On the other hand, the lower ripples cause lower heat, which leads to a smaller heat sink. Moreover, the operation temperature of the switching devices also defines the requirement for the thermal design. As a result, the switching device has the key role in determining the efficiency and the volume/weight of the converter, which both factors determine the power density of the power electronic converter.

Silicon (Si) switching devices have been well established in power electronics for the last decades. But, Si shows significant limitations in blocking voltage capability, operation temperature, and switching frequency. In such a situation, wide bandgap (WBG) semiconductors enable high frequency, high-efficiency power electronics. Among the possible semiconductor materials candidates, Silicon Carbide (SiC) and Gallium Nitride (GaN) represent

the best tradeoff between theoretical characteristics (high blocking voltage capability, high-temperature operation, and high switching frequency), actual commercial availability of the initial material (wafers and epitaxial layers), and maturity of their technology.

The higher breakdown field of WBG semiconductors makes the drift regions of the device thinner, which it results in lower specific ON-resistance. The high mobility of GaN further reduces the ON-resistance. This allows a smaller die size to achieve a given current capability, and therefore lower input and output capacitances. Higher saturation velocity and lower capacitances enable faster switching transients and consequently lower switching loss. In short, the material properties of WBG semiconductors result in a device with lower ON-resistance and switching losses than a Si device with comparable voltage and current capabilities

In [20], commercial GaN devices are studied. There are two structures for GaN devices: vertical and lateral. Vertical GaN devices, using structures similar to their Si and SiC counterparts, can take greatest advantage of the superior GaN material properties. However, the lack of availability of high-quality low-cost GaN wafers has limited these prospects. Vertical devices generally require homoepitaxial fabrication, meaning that the substrate and epitaxial layers are fabricated with the same type of semiconductor (i.e., GaN-on-GaN). However, MIT has developed a method of vertical MOSFET and diode fabrication using a heteroepitaxial GaN-on-Si structure. Because vertical GaN devices have not yet been produced on a commercial level, most of the GaN devices available today are lateral heterojunction field-effect transistors (HFETs), also known as high electron mobility transistors (HEMTs). These devices are typically limited at 600–650 V, and consequently have limitation on power rating unlike those with vertical structure. Because of the lateral heterojunction structure, these devices are fundamentally different from MOSFETs and have unique characteristics such as their reverse conduction behavior and their dynamic drain-source ON-resistance.

There is a current path layer between the drain and the source of the GaN HEMT. This layer, shown in the GaN HEMT structure of Figure 3, is called “two-dimensional electron gas” (2DEG). Because of the native 2DEG channel, the HFET is depletion-mode (normally-ON) device. This is not desirable for voltage-source converters, because of the potential for shoot-through during startup or loss of control power.

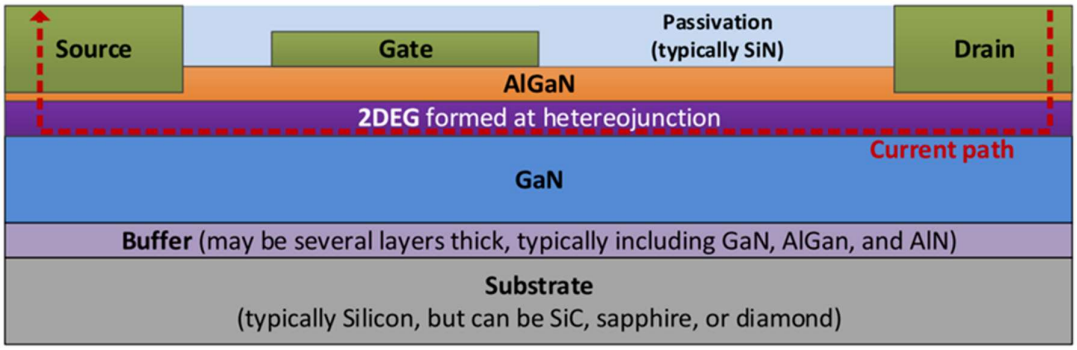

Figure 3 - Basic structure of depletion-mode lateral GaN HEMT

Although the 2DEG makes the lateral GaN HEMT natively depletion-mode, the gate can be modified to shift the threshold voltage positively and thereby make an e-mode device. There are four popular structures that have been used to create enhancement-mode devices: recessed gate, implanted gate, pGaN gate, and cascode hybrid.

The recessed gate structure [22] is created by thinning the AlGaN barrier layer above the 2DEG (Figure 4). By making the AlGaN barrier thinner, the amount of voltage generated by the piezoelectric field is reduced proportionally. When the voltage generated is less than the built-in voltage of the Schottky gate metal, the 2DEG is eliminated with zero bias on the gate. With positive bias, electrons are attracted to the AlGaN interface and complete the circuit between source and drain.

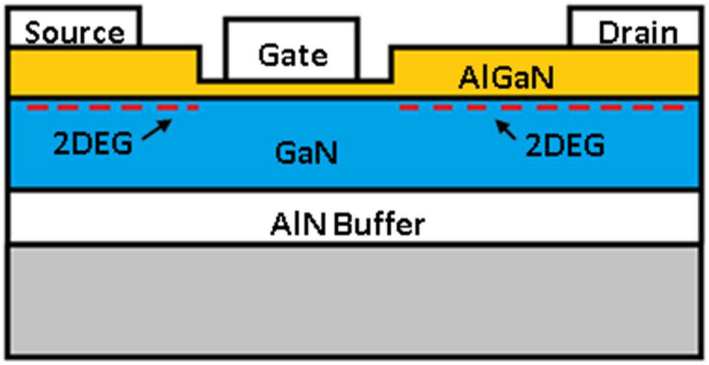

Figure 4 - Basic structure of a HEMT with recessed gate

The aluminium nitride (AlN) buffer layer is used to smooth the transition between GaN and substrate materials because of their lattice mismatch and thermal expansion coefficient difference.

Another method for creating an enhancement-mode device is to implant fluorine ions in the AlGaN barrier layer [23]. These fluorine atoms create a "trapped" negative charge in the AlGaN layer that depletes the 2DEG underneath. By adding a Schottky gate on top, an enhancement-mode HEMT is created.

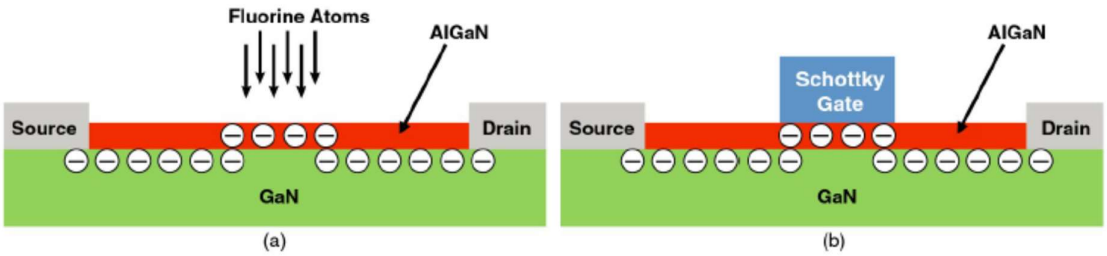

Figure 5 - (a) By implanting fluorine atoms into the AlGaN barrier layer negative charges are trapped in the barrier. (b) A Schottky gate now can be used to reconstruct the 2DEG when a positive voltage is applied [24]

A combination of fluorine doping and a recessed gate was proposed in [25] to improve the behaviour. Adding a cap layer of InGaN beneath the gate has also proved to be effective to generate enhancement mode devices by raising the conduction band, [26].

The first e-mode devices sold commercially had a positively charged (p-type) GaN layer grown on top of the AlGaN barrier (Figure 6) [27]. The positive charges in this pGaN layer have a built-in voltage that is larger than the voltage generated by the piezoelectric effect, thus depleting the electrons in the 2DEG and creating an enhancement-mode structure [28].

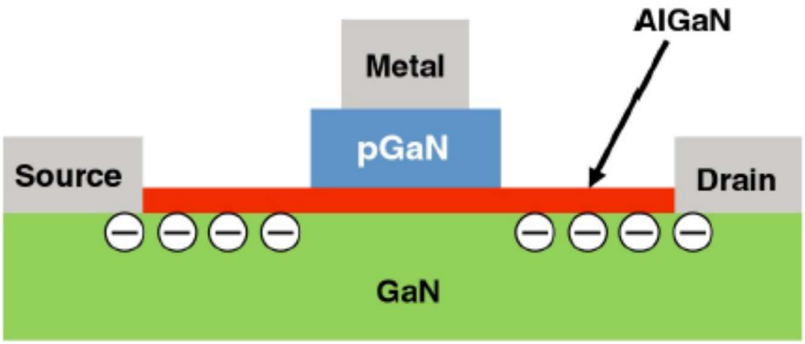

Figure 6 - pGaN HEMT structure [24]

Initially, the most common solution to build a single-chip enhancement-mode GaN transistor was to place an enhancement-mode silicon MOSFET in series with a depletion-mode HEMT device [29]-[30], as shown in Figure 7. The source of the GaN HEMT is connected to the drain of the Si MOSFET and the gate of the GaN HEMT is connected to the source of the Si MOSFET. The gate of the silicon device forms the control input to the cascode circuit, therefore the Si MOSFET controls the turn-off/on of the cascode, while the GaN HEMT blocks virtually all of the voltage.

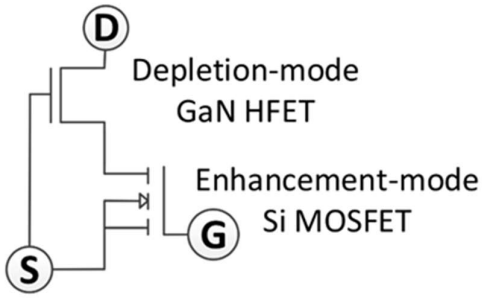

Figure 7 - Schematic cascode GaN HEMT structure

In this circuit, the MOSFET is turned on with a positive voltage on the gate when the depletion-mode GaN transistor's gate voltage goes to near-zero volts and turns on. From this moment the current can flow through the depletion-mode GaN HEMT and the MOSFET, which is connected in series with the GaN HEMT. When the voltage on the MOS gate is removed, a negative voltage is created between the depletion-mode GaN transistor gate and its source electrode, turning the GaN device off.

This type of solution for an enhancement-mode GaN "system" works well when the GaN transistor has a relatively high on-resistance compared with the low voltage (usually 30 V rated) Si MOSFET. Since on-resistance increases with the device breakdown voltage, cascode solutions are most efficient when the GaN HEMT is high voltage and the MOSFET is very low voltage. Inversely, as the required rated voltage goes down, and the on-resistance of the GaN transistor decreases, the weight of the MOSFET contribution becomes more significant., so that cascode solutions are only practical at voltages higher than 200 V.

There are e-mode GaN HEMT devices manufactured by EPC, GaNSystems, or Panasonic. In [21], commercial GaN (Figure 8) and SiC (Figure 9) devices are listed.

Manufacturers	Voltage Ratings	Current Ratings	Conduction Resistance	Configuration
EPC	15 V~450 V	0.5 A~90 A	1.3 mΩ~2800 mΩ	enhancement mode
Transphorm (Fujitsu)	600 V	9 A~17 A	150 mΩ~290 mΩ	cascaded
	600 V (module)	70 A	30 mΩ	cascaded (half bridge)
	650 V	21 A~47 A	35 mΩ~110 mΩ	cascaded
Infineon (IR)	100 V			cascode
	600 V			
Panasonic (Infineon)	600 V	10 A, 15 A	140 mΩ, 54 mΩ, 71 mΩ	enhancement mode
TI	80 V	10 A	18 mΩ	enhancement
	600 V	12 A	70 mΩ	cascode
GaN Systems	100 V	45 A, 80 A, 90 A	7 mΩ, 15 mΩ	enhancement mode
	650 V	7.5 A~60 A	25 mΩ~200 mΩ	

Figure 8 - Commercial GaN devices

Manufacturers	Products	Voltage Ratings	Current Ratings
Cree	SiC Schottky diode	600 V, 650 V, 1200 V, 1700 V	1 A~50 A (100 °C)
	SiC MOSFET	900 V, 1200 V, 1700 V	2.6 A~71 A (100 °C)
	SiC power module	1200 V, 1700 V	20 A~325 A
ROHM	SiC Schottky diode	650 V, 1200 V	5 A~40 A (150 °C)
	SiC MOSFET	400 V, 650 V, 1200 V, 1700 V	2.6 A~49 A (100 °C)
	SiC power module	1200 V	80 A~ 300 A (60 °C)
Infineon	SiC Schottky diode	600 V, 650 V, 1200 V	2 A~40 A
	SiC JFET	1200 V	18 A, 25 A (100 °C)
	SiC module (IGBT or CoolMOS + SiC diode)	650 V, 1200 V, 1700 V	30 A~600 A
	SiC MOSFET	1200 V	
	SiC module (SiC MOSFET)	1200 V	
ST	SiC Schottky diode	600 V, 650 V, 1200 V	4 A~20 A
	SiC MOSFET	1200 V	16 A, 34 A, 85 A (100 °C)
Fairchild	SiC Schottky diode	1200 V	15 A, 20 A, 30 A, 40 A (148 °C)
	SiC module (IGBT + SiC diode)	650 V	40 A, 50 A (80 °C)

Figure 9 - Commercial SiC devices

1.3 Gate driver parameter

As new power transistors, such as SiC Mosfets and GaN HEMTs, are being increasingly used in power electronics systems, it has become necessary to use special drivers. Isolated gate drivers are designed for the highest switching speeds and system size constraints required by technologies such as SiC (silicon carbide) and GaN (gallium nitride), by providing reliable control over IGBT and MOSFET. The evolution of the architectures allows satisfying the new

levels of efficiency and the stability of the timing performances, thus reducing the distortion of the voltage. ROHM Semiconductor is a reference point for power devices based on Silicon Carbide (SiC) technology.

1.4 EMI considerations

In order to increase the scientific content of this thesis and make it more interesting for the readers, a comprehensive literature review on near-field EMI in power electronics is also presented in the introduction. Near-field EMI literature review can be categorized in four main subjects: A) Attenuation, B) Measurement Systems and Probes, C) Modelling, and D) WBG Devices.

A) Attenuation: there are two types of near-field emission coupling: electric and magnetic. The electric emission coupling can be represented by parasitic capacitance [9]. In [10], it is stated that as the power density of the power electronic systems should be increased, and the components of the system should be closer to each other. As a result, the coupling parasitic capacitances between the components will increased so that the near-field electric emission coupling. The emission reduction is achieved by shielding and capacitance cancellation techniques. In [11], grounding and filtering techniques have been applied to attenuate the near-field electric emission. In [12], first a capacitive coupling due to printed circuit board (PCB) traces is investigated. Then, it is reduced using an equivalent parallel capacitance (EPC) cancellation technique.

The causes of magnetic emission coupling are firstly because of differential mode (DM) current between the parallel devices and secondly because of passive magnetic components [9]. In [13], the dynamic current sharing between the parallel devices is improved thanks to a new layout for multichip SiC MOSFET power module. One of the advantages of such a dynamic current sharing is near-field magnetic emission attenuation. In [14], the passive magnetic component planar transformers are introduced as one of the main sources of near-field magnetic emission, while the passive magnetic component common mode (CM) choke is introduced as the main vulnerable component to this emission. In order to mitigate the problem, the position and orientation of planar transformers are optimized.

There are studies that are focused on PCB design itself in order to investigate and reduce near-field emission [15], [16]. For example, in [16], a novel electromagnetic bandgap (EBG) design, using a partial element equivalent circuit (PEEC) algorithm, is proposed for PCB.

B) Measurement Systems and Probes: There are scholars who study state-of-the-art probes and effective measurement system for investigation of near-field emission.

In [17]-[20], J.M. Dienot, et al., have been studied electromagnetic near-field probes for power electronic modules. In [17], first, the power module is analyzed to determine the distribution of the magnetic field close to the switching device. This analysis is helpful to determine the effective placement and dimension of the probe. Further, instead of moving a single probe over the power module surface and measuring the magnetic field step by step, a two-dimensional matrix consisting of 20 single probes, printed on a ceramic substrate is placed and integrated very close to the power module. Thus, allowing to measure the magnetic field in a more precise manner and less time-taking way. This integrated matrix is in fact a real-time near-field emission sensor for the power module. In [20], the previous work on near-field emission embedded sensor is developed for a SiC power module.

In [21], a measurement system is proposed for power electronic converters on the base of multipolar expansion approach. In this case the source of the near-field emission is considered as the center of a sphere, where a single probe measures the near-field emission on the surface of the sphere, step by step, by multiple measurements. The resulted radiating distribution of the near-field emission facilitate calculating a predictive EMI modelling for the system, where the radiating near-field emission can be easily decomposed to a finite set of standard terms (such dipole, quadrupole, octupole, etc.).

C) Modelling: There are studies that intend to model the near-field emission of the switching device [22]-[23] or the power converter [24]-[28]. Using a precise model, the near-field emission can be predicted before prototyping the system. This reduces the cost of manufacturing, by considering electromagnetic compatibility (EMC) issues in advance. To this aim, near-field emission should be first measured experimentally. In most cases, multiple measurements should be performed, by considering a test area above the switching device or the whole power converter to map the near-field emission. This approach is called cartography.

In [22], the switching device is a silicon (Si) MOSFET (IRF640), where the measurements are performed in time-domain in order to achieve a high range of emission frequencies. In [23], an IGBT (STGF3NC120HD) is the subject of magnetic field modelling, where the probe is located 3 mm above the IGBT to cover an area of 2.5x2 cm. The probe is displaced with a measuring step of 1.25 mm on the X axis and 1 mm on the Y axis to create 400 measurement points.

In [24], the magnetic near-field emission of a buck converter is modeled by a circular loop, where the geometric characteristics and the equivalent current of the loop are determined on the base of the measurements of two areas. The first area is considered as the input capacitor of the buck converter while the second one as the switching cell area, including the active devices and the input inductor. In [25], a 3D radiated model for a buck converter is obtained by the use of the near-field emission cartography. A genetic algorithm (GA) optimization method is applied to synthesize all the measured electric and magnetic dipoles and to achieve the best fitted 3D equivalent model. In [26], the radiated far-field EMI of a converter is estimated and validated in semianechoic chamber. The radiation of CM current on the attached cables is introduced as the cause of the radiated far-field EMI, where the CM current is driven by the electric near-field coupling between the PCB and the attached cables of the converter. In short, the radiated far-field EMI of the converter is modelled using electric near-field emission of the converter. In [27], a 3D time-domain near-field emission model is proposed for the ultra-fast transients of PCB with duration of a few nanoseconds. In [28], an effective numerical approach of modelling near-field emission of power electronic equipment is proposed where the computation time of the calculation has been optimized.

D) WBG Devices: With the growingly emergence of WBG devices in power electronic, there are few studies that investigate near-field emission for SiC- and GaN- based converters [9], [11], [13], [20], [29].

The reference [9] is a survey on EMI for WBG-based power electronic systems in general. In particular, it reports that there are limited number of researches for near-field EMI in the case of WBG devices. Moreover, as WBG devices work at higher switching frequency with faster switching transient, their resulted DM and CM currents are greater than those of Si devices, that generate higher flux density and consequently higher near-field emission. The EMI reduction techniques are categorized as firstly reduction from EMI sources and secondly reduction along

with EMI paths. For reduction from EMI sources, some state-of-the-art packaging and PCB design technologies are introduced in order to reduce the parasitic inductances. For reduction along with EMI paths, especially in the case of near-field emission, it is referred to [13], where the innovative dynamic current sharing between the paralleled devices in a SiC power module can effectively reduce the near-field emission.

In [29], near-field EMI is measured and compared between a GaN-based and Si-based hard-switched buck converter. The authors concluded that although the slew rate of the GaN is steeper than that of the Si, over switching frequency range of 150 kHz to 1 GHz, and not much difference in the EMI level (a few dBµV higher in the case of the GaN). This same work also reports that the near-field emission can be sufficiently reduced by adding more layers to the PCB.

Therefore, we can conclude from this comprehensive literature review that so far; very limited works have studied near-field EMI for the case of WBG-base converters. This aspect indeed highlights the importance of this thesis, where the optimization of the gate driver parameters design approach of [8] is addressed with regard to efficiency and EMI level.

2. METHODOLOGY

As mentioned in the previous paragraphs, in recent years, Wide Band Gap devices are finding more and more use in many applications, such as, for example, in the field of Electric Vehicles, where they are used in AC-DC battery chargers, DC-DC bidirectional converters for power management and traction inverters of Electric Vehicles (EVs) [12]-[82]. Still referring to automotive applications, Silicon Carbide (SiC) and Gallium Niitride (GaN) based converters show their superiority compared to Silicon (Si) based devices [83]-[84]-[85]-[86]-[87]. In particular GaN based converters increasingly represent the future of electric vehicles, both and above all thanks to the greater switching frequency capacity, and thanks to the integration and elimination capacity of recirculating diodes [54]-[88]-[89]-[90]-[91]-[92]. At the same time, high-frequency switching applications can cause electromagnetic interference (EMI) problems. This necessitates the design of proper gate driver circuits for WBG devices. Concerning the performance of devices during switching, various considerations on gate driver circuits have been exposed in the scientific literature. In particular, the addition of ferrite spheres, the use of resonant or RC snubber circuits, gate driver resistor and correct design of the gate inductance were suggested. [66]-[93].

In particular, the choice of gate resistor R_G has opposite effects on efficiency and EMI levels: the higher the value of R_G, the greater the switching losses and the lower the ringing; conversely, lower R_G values result in lower switching losses and higher ringing, which increases EMI levels. In addition, if on the one hand lower RG values decrease the switching losses, on the other hand increase the ringing losses due to the oscillating phenomenon that occurs during the switching transition of the semiconductor device [94].

As for the gate inductance (L_G), it should provide stable operation by suppressing parasitic oscillations, which allows switching losses to be minimized. In fact, the oscillation losses are reduced without significantly increasing of the switching losses, since its impedance varies with the frequency. For these reasons, in the design phase it is appropriate to consider all the effects mentioned above in terms of EMI levels and efficiency for the sizing of L_G and R_G.

These kinds of problems can be solved with a multi-objective optimization approach. For parameterization of R_G, multi-objective optimization is proposed, in the studies presented in Chapter 3, to optimize both objectives (η and EMI) at the same time.

In [71], both η (total switching loss) and EMI of a GaN-based inductive battery charging system are considered in an optimization problem and the R_G is parameterized. The methodology is numeric where the amount of both total switching loss and current/voltage overshoot are obtained by experimental tests with five values of R_G (5, 10, 15, 22.5, 27.5 Ω). Then, an objective function, *Total Power Losses* × (%*V_overshoot* + %*I_overshoot*), is defined as a function of the value of R_G. Finally, R_G = 10 Ω is selected for the gate resistor design in order to minimize the defined objective function.

In [31], the idea is the parameterization of the both high side (HS) and low side (LS) gate resistors ($R_{G\text{-}HS}$ and $R_{G\text{-}LS}$) in a GaN-based one leg inverter by solving a multi-objective optimization problem. The objective functions are the efficiency and the EMI level of the circuit. The methodology is numeric where the amount of the objective functions are obtained on the base of the PSpice simulations for 5 × 5 = 25 tests with different values of $R_{G\text{-}HS}$ and $R_{G\text{-}LS}$: five values for each resistor where the objective functions are $\eta = f_1(R_{G\text{-}HS}, R_{G\text{-}LS})$ and EMI = $f_2(R_{G\text{-}HS}, R_{G\text{-}LS})$. Unlike [71], in [31] the mathematical expression of the objective functions is obtained by the use of a regression method. Then, solving a multi-objective optimization problem, the *Pareto Front* of the problem is obtained. Finally, the values of $R_{G\text{-}HS}$ and $R_{G\text{-}LS}$ are selected corresponding to one of the optimum points in the *Pareto Front*.

In the next chapter, the studies carried out on a SiC-based converter and on a GaN-based converter will be reported.

3. RESULTS

3.1 Multi-Objective Optimization of the Gate Driver Parameters in a SiC-Based DC-DC Converter for Electric Vehicles

3.1.1 Introduction

In this work the idea is the same as that of [31], however, there are four gate resistors to be studied instead of two, turn-ON HS gate resistor ($R_{G\text{-}HS\text{-}ON}$), turn-OFF HS gate resistor ($R_{G\text{-}HS\text{-}OFF}$), turn-ON LS gate resistor ($R_{G\text{-}LS\text{-}ON}$), and turn-OFF LS gate resistor ($R_{G\text{-}LS\text{-}OFF}$). Moreover, the power electronic module is a SiC-based half-bridge DC-DC converter for the application of the EVs. Unlike [31], the objective functions are achieved by performing the experimental tests. The detailed methodology is presented below.

Here, it is worthy to review some other state-of-the-art literatures about the gate driver design in general and for SiC-based converters in particular. Then, the relevancy of the following reviewed literatures with the motivations of this work is shown.

In [32], a cost-effective robust active gate driver (AGD) is proposed for IGBTs. The AGDs unlike the conventional gate drivers (CGDs), get feedback from the output voltage/current variables of the switching device in order to control the transient behaviors (dv/dt and di/dt). In this way, both switching loss and EMI can be reduced. To this aim, the desirable transient voltage/current rating should be studied in an analytical way. The gate driver in [32] offers robustness for the junction temperature and the load variations. In [33], a digitally programmable AGD is proposed. While the control parameters of an analog AGD are fixed, the proposed AGD can be programmed digitally to be fitted with the parasitic inductances/capacitances after implementation of the converter.

An important subject of the recent works on SiC devices is to suppress Miller effect crosstalk in half-bridge configuration [34-35] & [36]. Miller effect crosstalk happens in half-bridge configuration when turning-ON and turning-OFF of one switching device generate gate-source voltage spikes on its complementary switching device [34]. In [35], three methods of Miller effect crosstalk suppression for Si devices are stated: 1) add additional capacitance between gate–source terminals to shunt the Miller current, 2) apply a negative-biased turn-OFF

gate voltage, and 3) active Miller clamping. However, due to the intrinsic characteristics of SiC such as low threshold gate voltage, low maximum allowable negative gate voltage, and large internal gate resistance, Miller effect crosstalk is a serious issue and the conventional design approaches are not optimum. So that, additional gate driver circuits are proposed in [35] for an active gate impedance/voltage control. In [36], apart from proposing a new gate driver circuitry to suppress Miller effect crosstalk, the effect of the parasitic inductances is discussed. Therefore, in order to higher suppression of Miller effect crosstalk, beside the active gate control, there are PCB considerations to minimize the parasitic inductances as well.

3.1.2 Multi-Objective Optimization of the Gate Driver Parameters

Now we present the configuration of the SiC-based DC-DC converter and its gate drivers. Then, the method of finding the objective (regression) functions is discussed where the dependency of the efficiency and the conducted EMI to the gate resistors is studied. In this part, it is explained that how the gate resistor pairs can be selected on the base of the Miller effect crosstalk suppression. At the end, the multi-objective optimization problem is solved where a Pareto Front is achieved in order to find the optimal design points.

Figures 10 and Figure 2 present the configuration of the SiC-based DC-DC converter and the gate drivers respectively. In Figure 10, a half-bridge bidirectional boost converter is shown as a typical topology for power management between the battery and the traction inverter in the application of EVs. More about the operation modes and the power stage design of the half-bridge bidirectional boost converter as the power management module in EVs can be found in [37]. Since the converter is bidirectional, there are two SiC MOSFETs as the HS/LS switches. Moreover, because of the characteristic of the body diode of the SiC MOSFETs, that are very similar to those of a typical anti-parallel diode, there is no need to make use of the anti-parallel diodes in the SiC-based converter [38]. In Figure 10, the parasitic elements of the circuit are depicted as well: the loop parasitic inductances L_{dp1}, L_{dp2}, L_{sp1}, and L_{sp2} where d stands for drain, s stands for source, and p stands for parasitic; moreover, the coupled heat-sink parasitic capacitances C_{hp1}, C_{hp2}, and C_{hp3} where h stands for heat-sink. The fast transition voltage ($\frac{dV_{DS}}{dt}$) and current ($\frac{dI_D}{dt}$) of the HS/LS switches, in line with the parasitics of the circuit cause a conducted EMI current which passes through the parasitic capacitances (C_{hp1}, C_{hp2}, and C_{hp3}) to

the heat-sink and then to the power ground (PG). The maximum amplitude of this ground current in μAdB ($\hat{I}_{GR}$) can be considered as the EMI level of the converter [39].

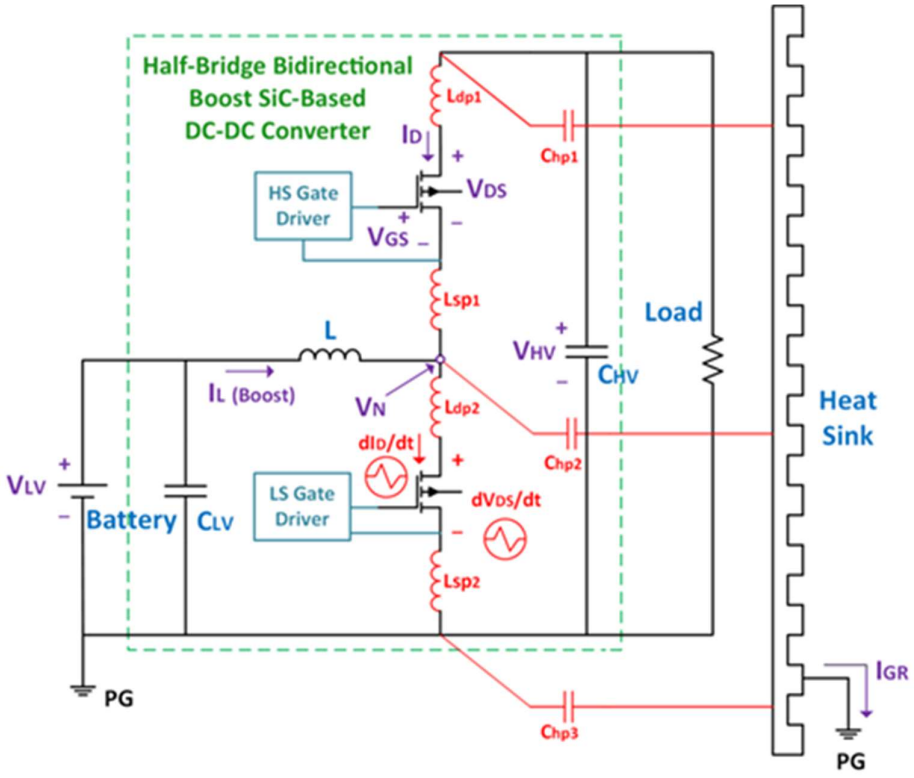

Figure 10 - Half-bridge bidirectional boost SiC-based DC-DC converter

As can be seen in Figure 11, two gate drivers with the same configuration are considered for the HS/LS SiC switching devices. Each gate driver has its own turn-ON and turn-OFF paths and the corresponding gate resistors. So that, there are four gate resistors in the circuit as: $R_{G\text{-}HS\text{-}ON}$, $R_{G\text{-}HS\text{-}OFF}$, $R_{G\text{-}LS\text{-}ON}$ and $R_{G\text{-}LS\text{-}OFF}$. The clamp diodes, DZ_{HS}/DZ_{LS} and D_{HS}/D_{LS}, are used to mitigate the overshoot of the HS/LS gate-source voltages. In order to damp the high frequency ringing of the LC gate driver parasitics, the ferrite beads, FB_{HS} and FB_{LS}, are used with an impedance of Z = 220 Ω at 100 MHz. The gate driver ICs are Si8271 manufactured by Silicon Labs. High integration, low propagation delay, small installed size, flexibility, and cost effectiveness make Si8271 ideal for SiC or GaN devices [40]. In this study, two gate driver ICs are used separately as the single gate drivers for each switching devices in order to increase the reliability of the gate driver design. The topology of the gate driver ICs is totem-pole with a fully isolated

configuration, using bipolar power supplies (+20/-4 V) to drive the gate-source voltage (V_{GS}) of the switching devices.

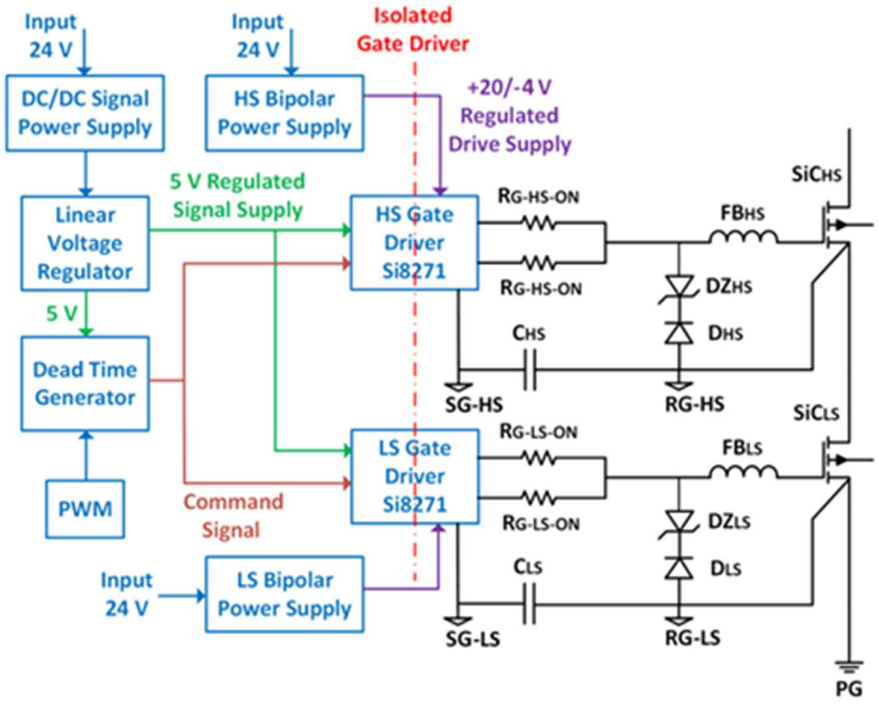

Figure 11 - High side (HS) and low side (LS) gate drivers

The bipolar power supply circuits are identical for the both gate drivers (Figure 12). The -HS/-LS indices are used to refer to the HS/LS bipolar power supplies respectively. The Zener diode (*DZ*) in series with the resistor R_2 realize the ON/OFF gate-source voltages of +20/-4 V. The connection point between *DZ* and R_2 are the reference ground (*RG*) for the switching devices in both Figure 11 and Figure 12. The low voltage signal ground for the gate drivers is indicated with *SG* as well. For the bipolar power supply design, the reference is the GaN gate driver design application note [41], while the values of circuit parameters are suitably modified for the SiC switching device.

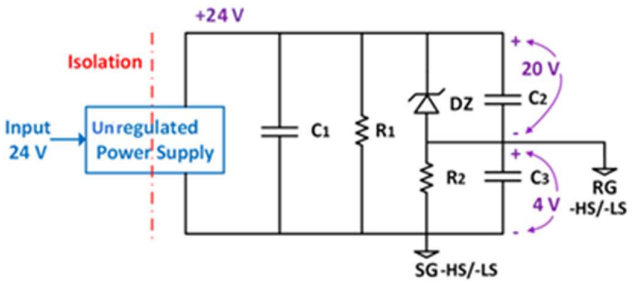

Figure 12 - High side (HS) and low side (LS) power supplies

In order to find the objective functions, first it is needed to define the optimization problem as below:

$$\text{minimize } f_1(x), f_2(x)$$

$$x \in R, R = \{R_{G-HS-ON}, R_{G-HS-OFF}, R_{G-LS-ON}, R_{G-LS-OFF}\} \quad (1)$$

where $f_1(x)$ is the efficiency of the converter with a negative mathematical sign (-η). In another words, finding the minimum value of -η, is in fact finding the maximum value of η. Moreover, $f_2(x)$ is the EMI level of the converter ($\hat{I}_{GR}$).

The objective functions can be obtained in an analytical or in a numerical way. In the analytical way, a circuit analysis is needed where all parameters of the circuit, such as parasitics and the circuit model of the switching devices, are known. In the numerical way, the circuit is considered as a black-box system, where the inputs of the system are the gate resistors and the output of the system are the efficiency and the EMI level. Then, some experiments should be performed to obtain a number of input-output pairs of the system. To perform the experiments, the circuit is already designed and implemented. Therefore, while the final goal is to modify the gate resistors, the other parameters of the circuit such as parasitic inductances/capacitances are already set up. It means that the gate resistor optimization is fitted to the other parameters of the circuit. In this sense, the approach of this study has the same advantage of that of the [33], where the parasitic parameters of the circuit are considered in the final design/control of the gate driver. Once the input-output pairs are obtained, the objective functions can be estimated by applying a regression method on the input-output pairs. As a result, the objective functions can be named regression functions as well. In this study, the numerical way is considered.

The number of experiments, which can be performed in order to obtain the input-output pairs, are technically limited. If we consider all four gate resistors as the inputs of the system and if we want to perform the experiments with, for example, five different values for each resistor, we need $5^4 = 625$ experiments to map the input-output pairs in a five-dimension space (four independent variables and one output). Such a high number of experiments is technically out of reach. To solve this problem, we can consider a two-phase optimization approach in which only two gate resistors are considered as the input of the system for each phase. In this way, the number of the experiments will be reduced by $5^2 = 25$ for each phase of the optimization approach to map the input-output pairs in a three-dimension space (two independent variables and one output).

Now, the question is that which two gate resistors should be selected for each phase of the optimization approach. Technically, there are three options: $\{R_{G-HS-ON}, R_{G-HS-OFF}\}$ for one phase and $\{R_{G-LS-}\ , R_{G-LS-OFF}\}$ for the other phase; $\{R_{G-HS-ON}, R_{G-LS-}\ \}$ for one phase and $\{R_{G-HS-OFF}, R_{G-LS-OFF}\}$ for the other phase; and $\{R_{G-HS-OFF}, R_{G-LS-}\ \}$ for one phase and $\{R_{G-HS-}\ , R_{G-LS-OFF}\}$ for the other phase. Among these three options, the last one is selected in this study based on Miller effect crosstalk between the HS/LS switches in the half-bridge configuration. In the first section, the Miller effect crosstalk has been introduced. In [42], based on the circuit analysis of the half-bridge configuration respect to the Miller effect crosstalk, it is explained how the gate resistors $R_{G-HS-OFF}$ and R_{G-LS-O} should be designed coordinated to each other to minimize the Miller effect crosstalk loss during the turn-ON process of the LS switch and evade a spurious turn-ON of the HS switch. Relatively, the gate resistor pairs, $R_{G-HS-ON}$ and $R_{G-LS-OFF}$ should be designed accordingly to minimize the Miller effect crosstalk loss during the turn-ON process of the HS switch and evade a spurious turn-ON of the LS switch. In this work, only one phase of the optimization approach is studied where the inputs of the system are the gate resistor pairs $R_{G-HS-OFF}$ and R_{G-LS-} . The second phase of the optimization approach, where the inputs of the system are the gate resistor pairs R_{G-HS-} and $R_{G-LS-OFF}$, is considered as the future work. As a result, we can rewrite the multi-objective optimization problem of the Equation 1 as below:

$$\begin{aligned} &\text{minimize } -\eta = f_1(x),\ \hat{I}_{GR} = f_2(x) \\ &x \in R,\ R = \{R_{G-HS-OFF}, R_{G-LS-ON}\} \end{aligned} \tag{2}$$

Details about the experiments are discussed in the next section. In the next step, when the experiment results are available and the input-output pairs are obtained, a regression method should be applied on the input-output pairs to estimate the objective functions $f_1(x)$ and $f_2(x)$. From now, the objective functions can be called regression functions as well. Since there are two independent variables, $R_{G-HS-OFF}$ and R_{G-LS-} a multivariate regression method should be performed. In this research, the *fitlm* solver from the *Statistic and Machine Learning Toolbox* of MATLAB is used for which, the model of the regression function should be specified. To this aim, a quadratic polynomial model is selected for the objective functions to minimize the regression modelling error:

$$\begin{gathered} f_1(x) = a_0 + a_1x_1 + a_2x_2 + a_3x_1x_2 + a_4{x_1}^2 + a_5{x_2}^2 \\ f_2(x) = b_0 + b_1x_1 + b_2x_2 + b_3x_1x_2 + b_4{x_1}^2 + b_5{x_2}^2 \\ x_1 = R_{G-HS-OFF},\ x_2 = R_{G-LS-ON} \end{gathered} \tag{3}$$

where the purpose of the regression step is to estimate the coefficients of the models: a_i and b_i for i = {1, 2, 3, 4, 5}.

In the next step, a multi-objective optimization solver should be used, using the regression functions, to solve the optimization problem of Equation 2, considering a boundary for the independent variables as:

$$R = \{R_{G-HS-OFF}, R_{G-LS-ON}\}, R_{bound} = [R_{min}, R_{max}] \tag{4}$$

Here, the *gamultiobj* non-linear multi-objective optimization solver from the *Optimization Toolbox* of MATLAB is used. This multi-objective optimization solver plots a *Pareto Front* where there are optimum points in a two-dimension space, representing the two objective functions. These points indicate the optimum value choices for the both objective functions. Then, it is the designer's decision to select one optimum point among all the suggestions. Obviously, the higher efficiency costs a higher EMI level and vice versa. Each optimum point is correspondent to the optimum value of the independent variables, which are the gate resistors. Finally, the efficiency and the EMI level in the case of the optimum design should be compared with those of a conventional design to validate the effectiveness of the proposed approach. All the steps are summarized in the flowchart of Figure 13.

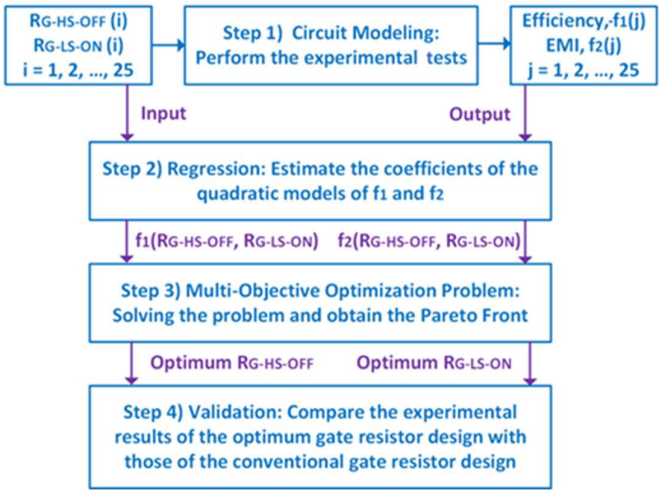

Figure 13 - Flow chart of the multi-objective optimization design approach

3.1.3 Experimental Results and Discussion

Here, at the first subsection, the test set-up, the measurement tools, and the test conditions are presented. Then, the 25 experiments are performed for different values of the gate resistors to obtain the input-output pairs of the system. In the second subsection, the regression functions are estimated and plotted, using the experimental results of the first subsection. At the third subsection, the multi-objective optimization problem is solved, the *Pareto Front* is plotted, and an optimum point is selected. In the fourth subsection, the set-up is tested, mounting the corresponding gate resistors of the selected optimum point of the third subsection. Then, the results are compared with those of a conventional gate resistor design. In the conventional gate resistor design, the gate resistor values are selected based on the application note suggestions for the SiC devices. At the fifth subsection, the experimental results are discussed in depth and the future works are suggested.

3.1.3.1 Test Set-up, Measurement Tools, and Test Conditions

In Figure 14, the the set-up of the converter and the measurement tools are shown. In Figure 6, the 3D PCB board of the converter, designed by Altium, is depected. The specifications of the power stage, of the gate drivers, and of the measurement tools are presented in Table 2, Table 3, and Table 4 respectively. The conventional design refers to the selection of the gate resistor values based on the suggestion of the application notes for SiC [38] [42]. So that, the conventional design gate resistor values are:

$$R_{G-LS-ON} = R_{G-LS-ON} = 4.7\ \Omega,\ R_{G-HS-OFF} = R_{G-LS-OFF} = 2.2\ \Omega \quad (5)$$

It is considered $5^2 = 25$ experimental tests, 5 different values for each of $R_{G-HS-OFF}$ and R_{G-LS-} , while R_{G-LS-} and $R_{G-LS-OFF}$ are remained unchanged. The five different test values are selected as:

$$R_{G-HS-OFF}, R_{G-LS-ON} = \{1\ \Omega, 5\ \Omega, 10\ \Omega, 20\ \Omega, 50\ \Omega\} \quad (6)$$

For each of the 25 experiments (indicated with *j* in Figure 13), the corresponding gate resistors (indicated with *i* in Figure 13) are mounted on the PCB board. Since the aim of this work is just to study the proposed multi-objective optimization approach, the tests are performed at a low input voltage and a low output power to evade the risk of damaging the circuit. The test conditions are summarized in Table 5 then. The output load, as can be seen in Figure 14, consists of three resistances, 10 Ω and 150 W each, connected in series and mounted on a heat-sink. Each test should be performed when the switching devices reach their steady-state temperature, in order to keep the test condition equal for all the experiments in the term of R_{DS-O} and the corresponding P_{Cond}. The ambient temperature also should be kept as constant as possible for all the tests; as the resistance of the load, the corresponding operation point, and the total loss are dependent to the ambient temperature.

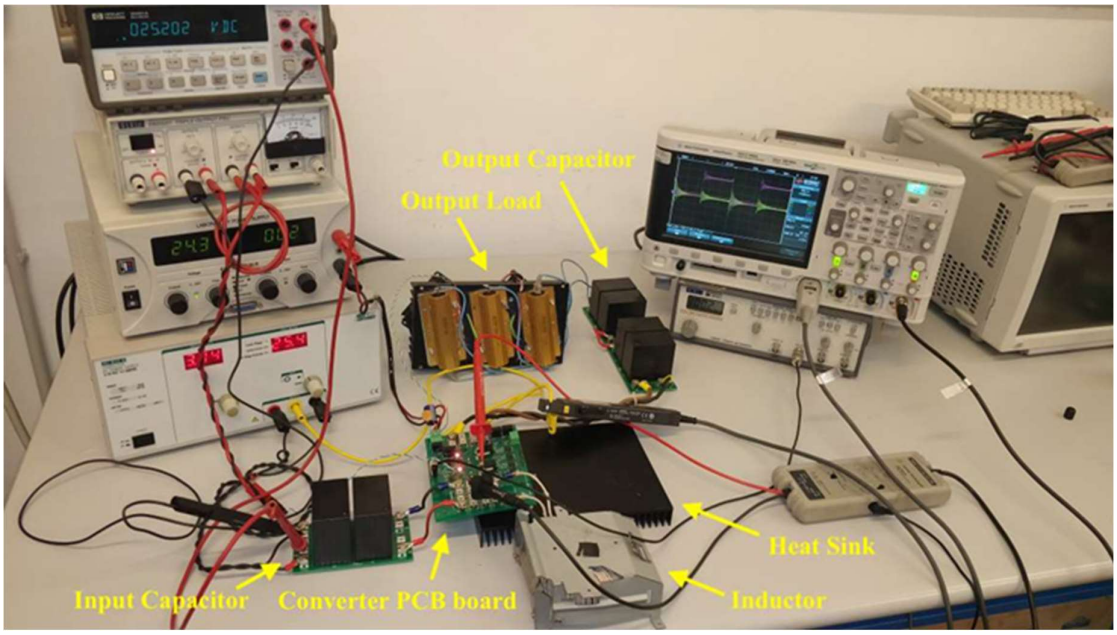

Figure 14 -Test set-up and measurement tools

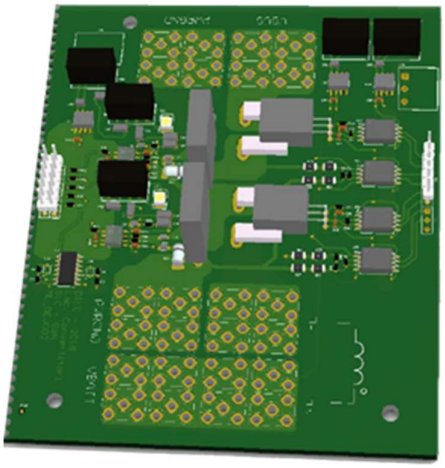

Figure 15 - 3D PCB board (Altium)

Parameter	Value
SiC MOSFET [V, A]	SCT3022AL (650, 93)
Inductor L [mH]	2.55
Low Voltage C_{LV} [μF]	50
High Voltage C_{HV} [μF]	100
Maximum Input Voltage [V]	300

Maximum Output Voltage [V]	600
Switching Frequency [kHz]	100

Table 2 - Power stage specifications of the converter

Parameter	Value
Gate Driver IC	**Si8271**
Input Voltage Range	3.3/5 V
Peak Current	4 A
Output	Sink/Source
Gate Driver Parameters	
Ferrite Beads (FB_{HS}/FB_{LS})	MPZ1608S221A 220 Ω @ 100 MHz
Zener Diodes (DZ_{HS}/DZ_{LS})	2.4 V
Diodes (D_{HS}/D_{LS})	20 V
Capacitors (C_{HS}/C_{LS})	1 μF
Bipolar Power Supply	
Drive Voltage	+20/-5 V
Resistors (R_1/R_2)	1 $k\Omega$
Capacitors (C_1/C_2/ C_3)	4.7 μF
Zener Diode (DZ)	20 V

Table 3 - Gate driver specifications of the converter

Parameter	Value
Input/output Current Probe	**Agilent 1146A**
Current Range	100 mA – 100 A
Bandwidth	100 kHz
Ground Current Probe	**Agilent N2893A**
Maximum Current	15 A
Bandwidth	100 MHz
Differential Voltage Probe	**Agilent N2791A**
Bandwidth	25 MHz
Oscilloscope	**DSO-X 3054A**

Table 4 - Specifications of the measurement tools

Parameter	Value
Input Voltage [V]	25
Duty Cycle [%]	50
Output Power [W]	75
Switching Frequency [kHz]	100

Table 5 - Test condition

3.1.3.2 Regression Functions

For each experiment, there are two independent variables, $R_{G-HS-OFF}$ and $R_{G-LS-ON}$, and two dependent variables, the efficiency and the EMI level. The efficiency is the overall efficiency of the converter which is obtained by measuring the input/output current/voltage of the converter. The EMI level is obtained by measuring the heat-sink ground current of the converter, applying Fourier transform, plotting the *spectra* diagram, and considering the maximum amplitude of the spectra diagram in μAdB ($\hat{I}_{GR}$) as the EMI level. The spectra diagram of the ground current for the case of the conventional gate resistor design is shown in Figure 16.

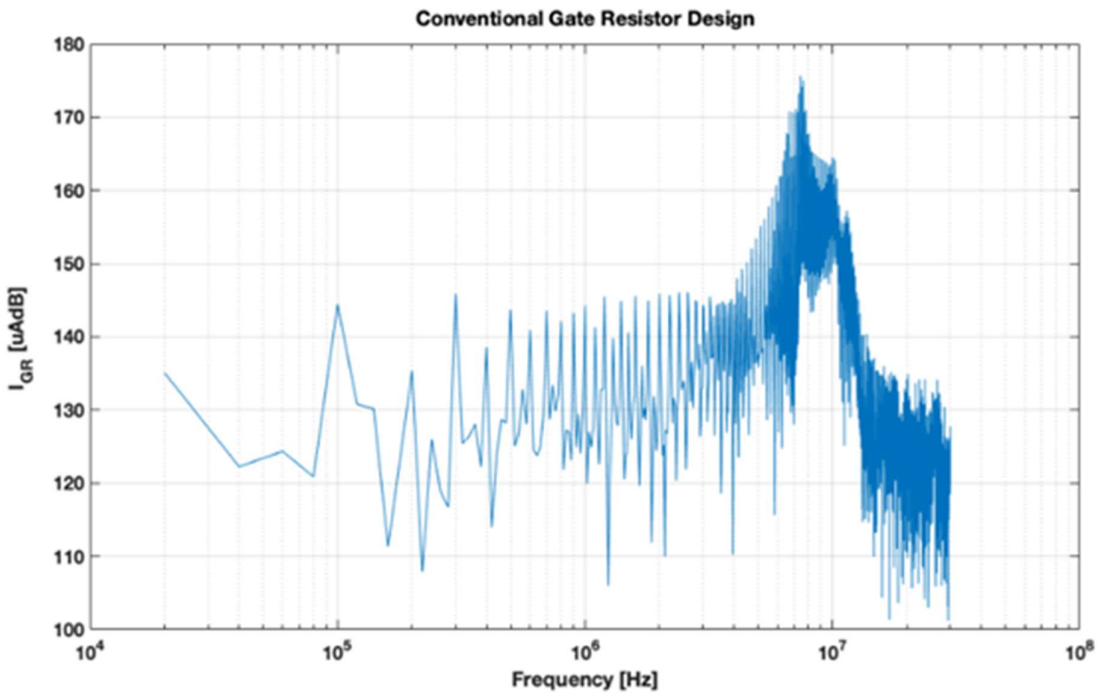

Figure 16 - Spectra diagram of the ground current in the conventional gate resistor design

Once all the 25 input-output pairs are obtained from the experiments, the *fitlm* solver from the *Statistic and Machine Learning Toolbox* of MATLAB can be applied to estimate the coefficients of the regression functions as it is described in Equations 3. In Figure 17 and Figure 18, the 3D mesh plots of the regression functions are shown.

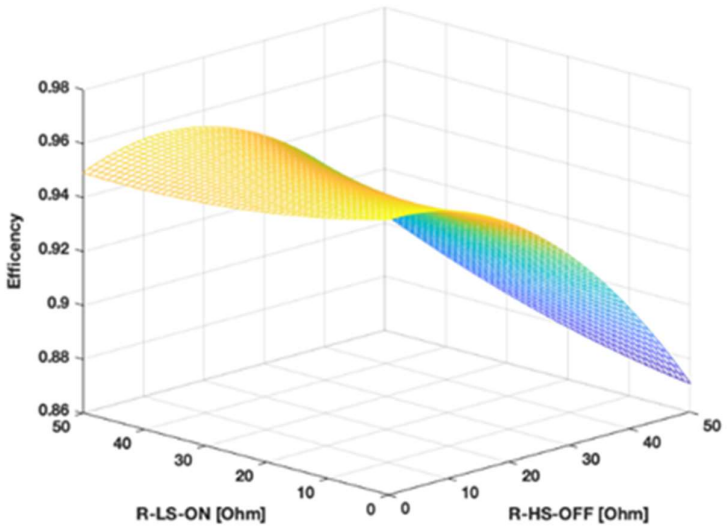

Figure 17 - 3D mesh plot of the regression functions Efficiency (η)

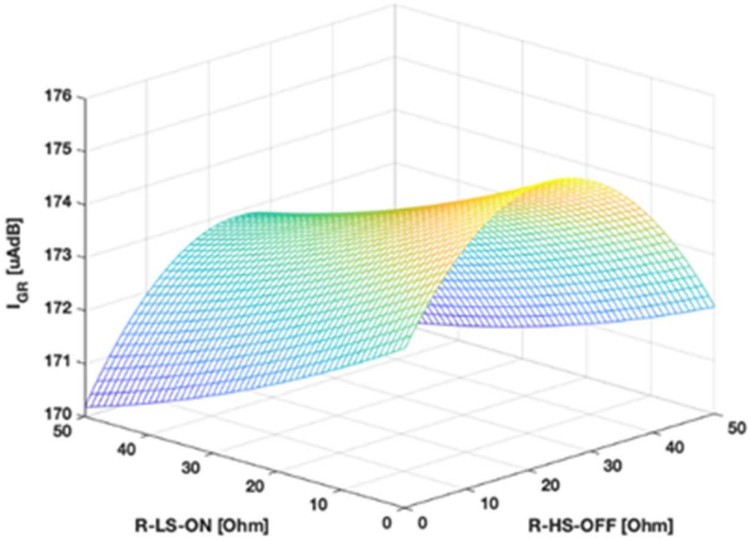

Figure 18 - 3D mesh plot of the regression functions EMI Level ($\hat{I}_{GR}$)

3.1.3.3 Multi-Objective Optimization Problem and Pareto Front

In this step, the multi-objective optimization problem of Equation 2 should be solved. The boundary of the independent variables, as described in Equation 4, is selected as R_{bound} = [1 Ω, 50 Ω]. The multi-objective optimization problem is solved using the *gamultiobj* non-linear multi-objective optimization solver from the *Optimization Toolbox* of MATLAB. The solver provides the *Pareto Front* as well, where a number of optimum points are achieved (Figure 19). Then, it is the designer's decision to choose the desired optimum point that is more matched with the design goals. Here, the indicated optimal point, as it can be seen in Figure 19, is selected. The expected efficiency and EMI level of the selected optimum point are 0.9504 and 170.4 μAdB respectively. The values of the corresponding independent variables of the selected optimum point are $R_{G-HS-OFF}$ = 1.5 Ω and $R_{G-LS-ON}$ = 14 Ω as well.

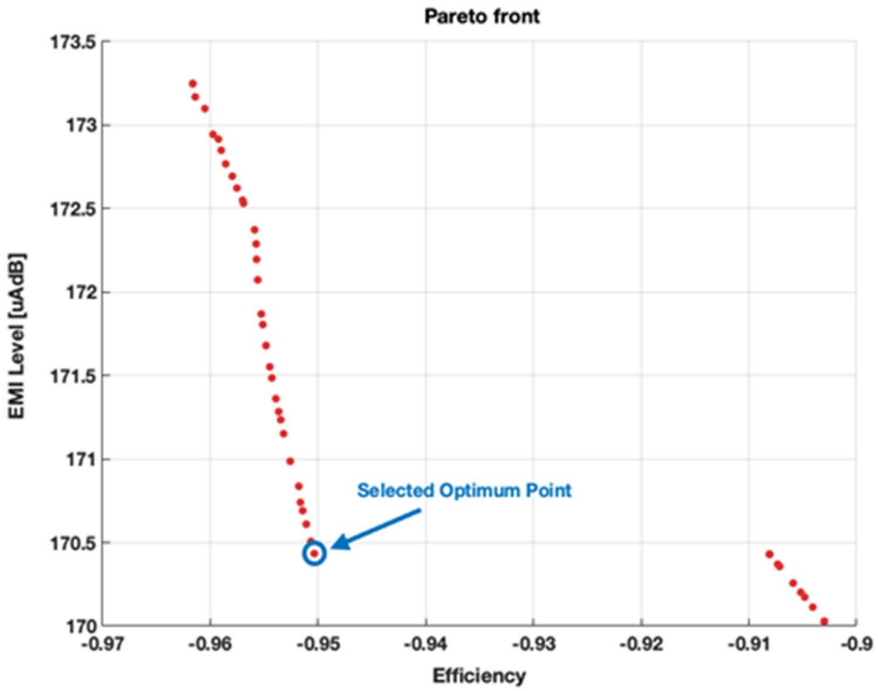

Figure 19 - Pareto Front of the solved multi-objective optimization problem

3.1.3.4 Optimum Gate Resistor Design

Here, the optimum gate resistors are mounted and the measurements are performed to obtain the efficiency and the EMI level. In Table 6, the experimental results are compared between the two design cases: conventional and optimum. An improvement of 0.986 % for the efficiency and an improvement of 1.84 % for the EMI level are achieved in the case of the optimum design compared to the conventional design. It should be noticed that the experimental results of the optimum design are not equal to those of the Pareto Front; as there are always error of measuring, of regression, of optimization problem solving, etc. in the design procedure. In addition, the spectra diagram of the optimum gate resistor design is shown in Figure 20. The maximum amplitude of $\hat{I}_{GR}$ has a corresponding frequency of 7.4 MHz, the same as that of the conventional design of Figure 16.

Design	$R_{HS\text{-}OFF}$	$R_{LS\text{-}ON}$	Efficiency	EMI Level
Conventional	2.2 Ohm	4.7 Ohm	0.9530	175.56 μAdB
Optimum	1.5 Ohm	14 Ohm	0.9624	172.33 μAdB

Table 6 - Result Comparison for the two design cases

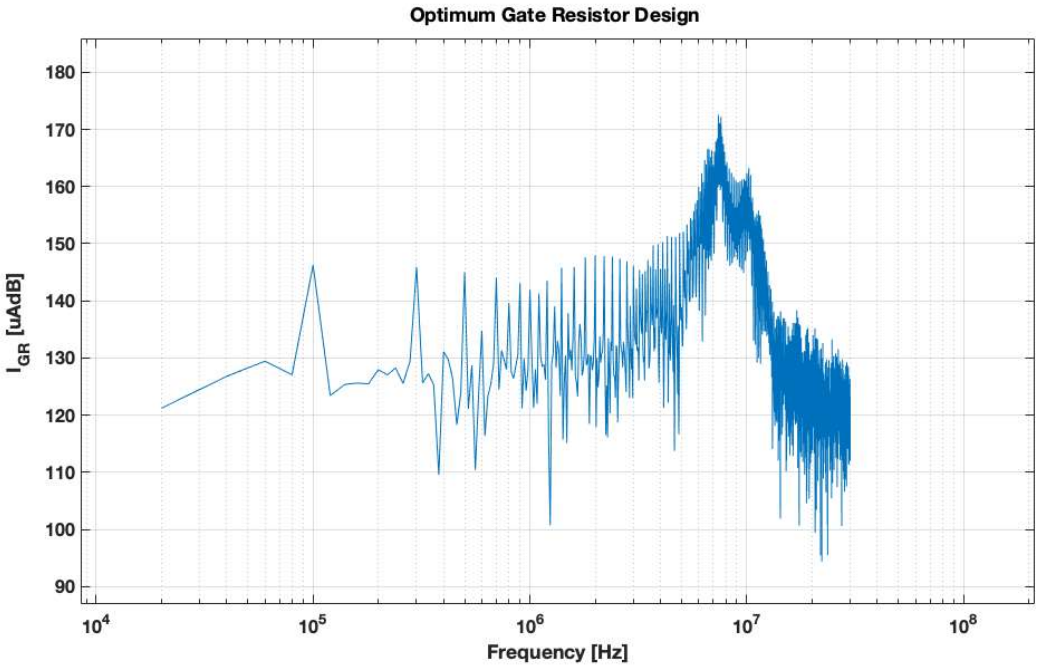

Figure 20 - Spectra diagram of the ground current in the optimum gate resistor design

3.1.4 Experimental Results and Discussion

In this section 3.1, an optimum gate resistor design approach is proposed for a SiC-based DC-DC converter in the application of EVs. In the proposed design approach, a multi-objective optimization problem is solved to maximize the efficiency and minimize the EMI level of the converter. The objective functions of the optimization problem are obtained numerically by means of the experimental tests. The independent variables of the objective functions, one gate resistor pair from the all four HS/LS ON/OFF gate resistors in the half-bridge configuration, are selected on the base of the Miller effect crosstalk suppression. The optimum values of the gate resistors are achieved by solving the optimization problem and plotting the Pareto Front. The experimental results validate both efficiency and EMI level improvements in the case of the proposed design approach compared to the conventional design approach. Final discussion on the experimental results shows that the further improvements can be achieved in the future works, where the second gate resistor pair is also optimized, using the same proposed design approach.

3.2 Multi-Objective Gate Driver Design for a GaN-Based Half-Bridge Converter to Optimize Efficiency and Near-Field EMI

3.2.1 Introduction

In this chapter also a gate driver resistors parameterization is studied. The presented research can be considered as a complementary investigation to the work presented in the previous chapter, where some principles are continual, and some new ideas are contributed.

The primary methodology is the same as that of chapter 3.1, where the idea is to find the compromised value of gate resistors by the means of a multi-objective optimization approach. In a traditional design, however, the gate driver resistor values come from the switching device application notes. Such values, offered by the manufacturers, are optimized for the switching device in the specific circuit of the application note, and not for any circuit in general. For example, as the PCB design of our circuit is different from that of the application note circuit, the parasitic inductance loops of our circuit is consequently different from that of the application note circuit. Therefore, with the same gate driver resistors of the application note circuit we will not obtain the same EMI level for our own circuit. In the proposed multi-objective optimization approach, on the contrary, the gate driver resistors are parameterized and optimized on the basis of experimental tests of any individual circuit.

Another advantage of the proposed multi-objective optimization approach respect to that of the traditional design, is the ability of compromising the values of the gate driver resistors to obtain different objectives. For example, in the previous chapter, the objectives were maximization of efficiency and minimization of conducted EMI. While here, the objectives are considered as maximization of efficiency and minimization of near-field EMI.

As both SiC and GaN are very important and are being inevitably the future of power electronics, in this chapter a GaN-based converter is studied, different from the previous one, where the converter was SiC-based. In this manner, the proposed method is evaluated for a different optimization objective (near-field EMI instead of conducted EMI) and for a different switching device (GaN instead of SiC).

A comprehensive literature review on near-field EMI in power electronics is also presented in the paragraph 1.4.

The rest of the chapter is organized as follow: In section 3.2.2, first the circuit characteristics of the both power stage and gate driver of the GaN-based half-bridge converter are presented. Then, the multi-objective optimization methodology for the gate driver design is proposed. In section 3.2.3, the experimental tests, in order to find the optimized gate driver parameter values are provided. Then, the results are discussed to validate the effectiveness of the proposed gate driver design method on both efficiency and near-field EMI. Finally, in section 3.2.4, the paper is concluded.

3.2.2 Circuit characteristics and optimization methodology

Here, the GaN-based DC-DC converter circuit and its gate drivers are presented. Then, the optimization methodology is addressed.

The GaN-based half-bridge bidirectional DC-DC boost converter configuration shown in Figure 21. The converter topology is bidirectional half-bridge DC-DC, which is typical in many applications such as plug-in electric vehicles [37] and battery energy storage systems [43].

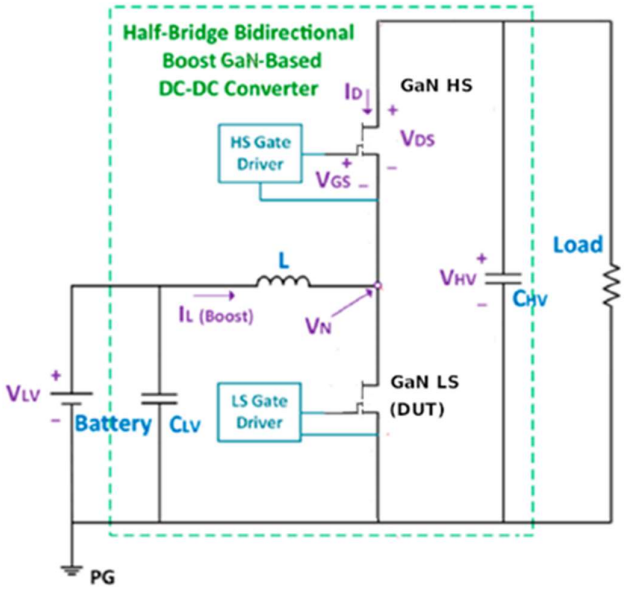

Figure 21 - Half-bridge bidirectional boost GaN-based DC-DC converter

For the near-field EMI measurement, a base was made for the antenna in order to fix it close to the GaN transistor as the device under test (DUT), as shown in Figure 22.

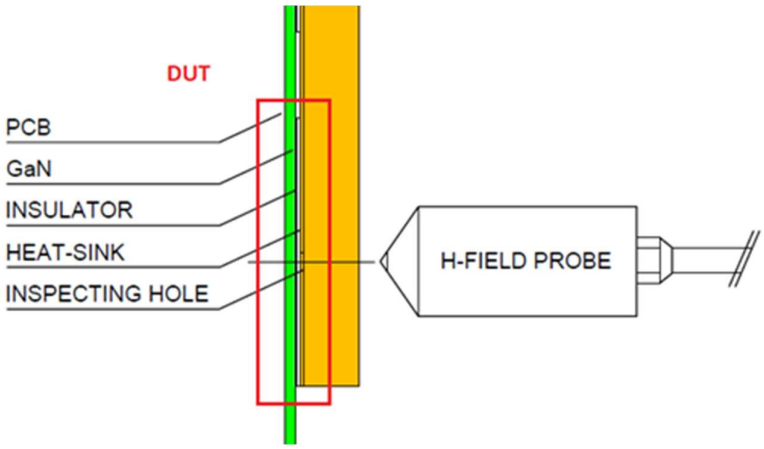

Figure 22 - Cross-section view of the DUT and H-field probe position

In Figure 23 is shown the configuration of the two gate drivers for the high side (HS) and low side (LS) GaN switching devices. Each gate driver has two gate resistors that correspond to the turn-OFF and turn-ON paths, respectively. In total there are four gate resistors in the circuit: $R_{G\text{-}LS\text{-}OFF}$, $R_{G\text{-}LS\text{-}ON}$, $R_{G\text{-}HS\text{-}OFF}$, and $R_{G\text{-}HS\text{-}ON}$. To mitigate and overshoot the HS/LS gate source voltages, the clamp diodes DZ_{HS}/DZ_{LS} and D_{HS}/D_{LS} were used. The ferrite beads (FB_{HS}, FB_{LS}) with

an impedance of Z = 220 Ω (at 100 MHz) was used to damp the high frequency ringing of the LC gate driver parasitics. The Si8271 gate driver integrated circuits used in this study was manufactured by Silicon Labs and its beneficial characteristics such as flexibility, small installed size, high integration, low propagation delay, and cost effectiveness makes it ideal GaN devices [44].

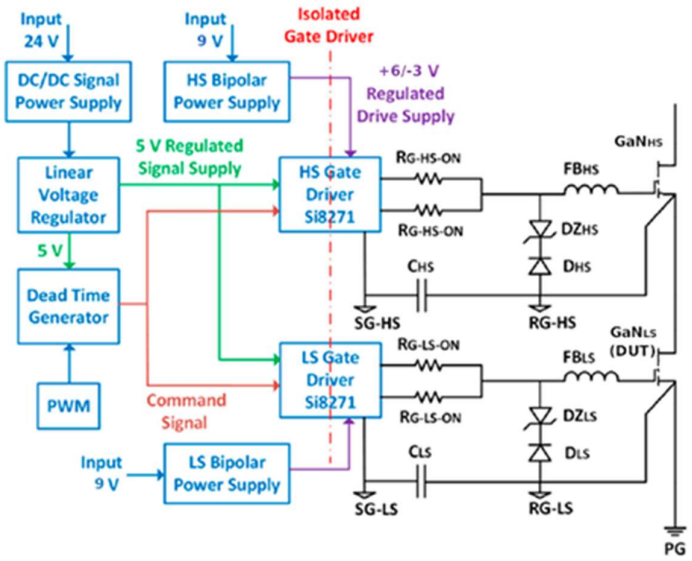

Figure 23 - Low side (LS) and High side (HS) gate drivers

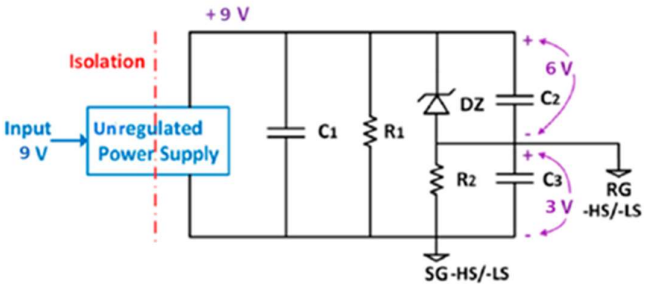

Figure 24 - HS/LS bipolar power supply

With the aim to increase the reliability of the gate driver design, in this work we used two gate driver ICs separately as single gate drivers for the switching apparatus. The gate driver ICs is in a totem-pole topology with a fully isolated configuration, with bipolar power supplies (+20/−4 V) to drive the gate-source voltage of the switching apparatus. Identical bipolar power supply circuits are considered for the gate drivers (Figure 24), where HS/LS indices are used to refer to the HS/LS bipolar power supplies respectively. To achieve the ON/OFF gate-source

voltages of +20/−4 V the Zener diode (DZ) is connected in series with resistor (R2), with the reference ground (RG) being the connection point between them. For the gate drivers the low voltage signal ground is indicated as SG and reference GaN gate driver design application note [45] is followed for the bipolar power design.

The employed optimization approach is similar to the one described in the previous paragraph, where two objective functions, $f_1(x)$ and $f_2(x)$, are defined for the multi-objective optimization problem. In this paragraph $f_1(x)$ representing the efficiency of the converter the same as in 3.1, while $f_2(x)$ is different from that of the other work, representing the near field EMI level of the LS GaN device. Moreover, x, the independent variable(s) of the optimization problem, corresponds to four gate resistors ($R_{G\text{-}LS\text{-}OFF}$, $R_{G\text{-}LS\text{-}ON}$, $R_{G\text{-}HS\text{-}OFF}$, and $R_{G\text{-}HS\text{-}ON}$). If we consider all the four gate resistors as the inputs of the system and with for example five different values for each resistor, the number of experiments to be performed, in order to calculate the regression functions between x and f, becomes $5^4 = 625$, which is technically out of reach. However, this problem can be solved in a reasonable way by utilizing a two-phase optimization approach, where in only two gate resistors are selected as the input of the system. Thus, only $5^2 = 25$ experiments are required to map the input–output pairs in a three-dimension space. In the present study, we investigate one phase of the optimization procedure where only one pair of the resistors are considered as the independent variables. Among the all possibilities of choosing the pairs, in order to make the method effective for the complementary Miller effect crosstalk between the HS and the LS switches in the half-bridge configuration, gate resistor pairs $R_{G\text{–}HS\text{–}OFF}$ and $R_{G\text{–}LS\text{–}ON}$ are chosen [42].

The multi-objective optimization to be performed can be written as:

$$\begin{aligned} &\text{minimize } -\eta = f_1(x),\ EMI = f_2(x) \\ &x \in R, \quad R = \{R_{G\text{-}HS\text{-}OFF}, R_{G\text{-}LS\text{-}ON}\} \end{aligned} \qquad (1)$$

where η is the efficiency of the converter; so that $-\eta$ should be minimized. The objective functions are estimated using the multivariate regression method with the independent variables being $R_{G\text{–}HS\text{–}OFF}$ and $R_{G\text{–}LS\text{–}ON}$. Minimization of the regression modelling error for the objective functions was performed using quadratic polynomial model defined as:

$$f_1(x) = a_0 + a_1x_1 + a_2x_2 + a_3x_1x_2 + a_4x_1^2 + a_5x_2^2$$
$$f_2(x) = b_0 + b_1x_1 + b_2x_2 + b_3x_1x_2 + b_4x_1^2 + b_5x_2^2$$

$$x_1 = R_{G\text{-}HS\text{-}OFF}, \quad x_2 = R_{G\text{-}LS\text{-}ON} \qquad (2)$$

After obtaining the regression function, the multi-objective optimization problem should be solved to plot the *Pareto Front* and find the optimum design point. Finally, to validate the effectiveness of the proposed approach, the efficiency and the near filed EMI levels in the case of the optimum design should be compared with those of a conventional design as we will see in the next section.

3.2.3 Experimental results and discussion

Here, we present in detail the experimental set-up, the measurement tools, and the test conditions. The experimental procedure is performed for each combination of the gate resistors, in order to obtain the input-output pairs of the optimization problem. Then, we discuss and plot the regression functions that are obtained using the measured experimental data. Followingly, the multi-objective optimization problem is solved, the Pareto Front is plotted, and an optimum point is selected. Finally, we examine and discuss the experimental measurements that are performed on the setup with the resistors corresponding to the selected optimum point. Specifically, the results are compared with those of a conventional gate resistor design.

3.2.3.1 Test Set-up, Measurement Tools, and Test Conditions

In Figure 25, the set-up of the DC-DC converter and the measurement tools are shown. In Figure 6, the 3D PCB board of the DC-DC converter, designed by Altium, is depicted on both sides in order to show the top layer, where the gate drivers are placed, and the bottom layer, where the GaN devices are mounted.

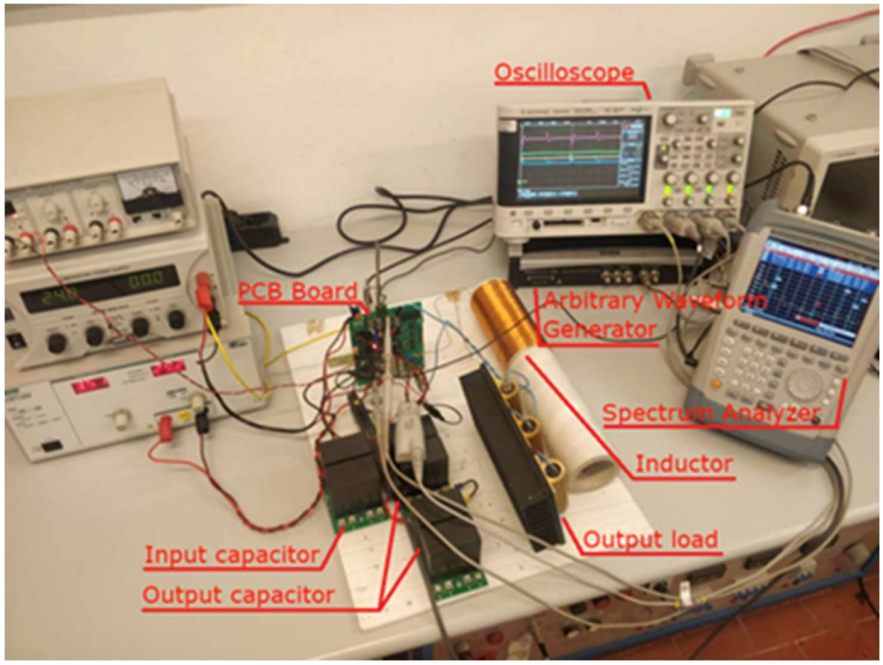

Figure 25 - Experiment set-up and measurement tools

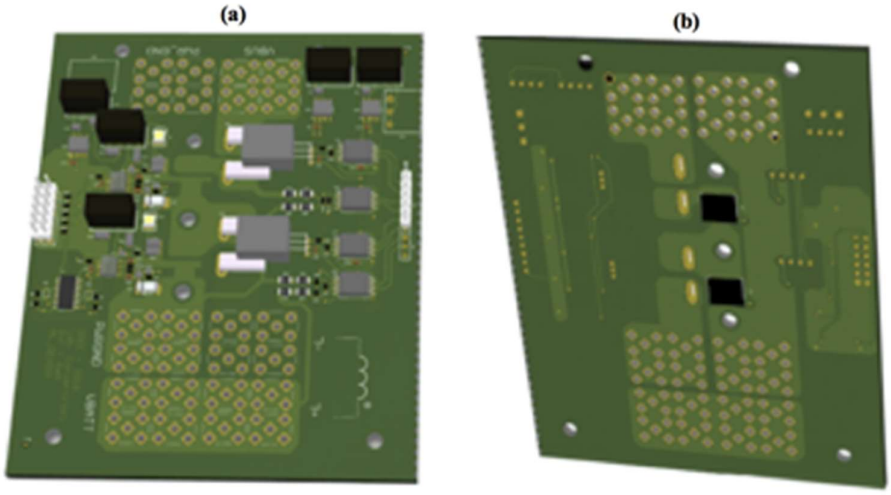

Figure 26 -3D PCB board (Altium): top side (a) and bottom side (b)

The specifications of the power stage, of the gate drivers, and of the measurement tools are presented in Table 7, Table 8, and Table 9 respectively. The conventional design refers to the selection of the gate resistor values based on the suggestion of the application note [45].

The conventional design for the GaN MOSFET used in the present study are $R_{G-LS-ON}$ = 10 Ω, $R_{G-HS-OFF}$ = 1 Ω, $R_{G-LS-ON}$ = 10 Ω, and $R_{G-LS-OFF}$ = 1 Ω.

We performed 25 experiments, with 5 different values for $R_{G-HS-OFF}$ and 5 different values for $R_{G-LS-ON}$, while the value of $R_{G-HS-ON}$ is kept constant to 10 Ω and the value of $R_{G-LS-OFF}$ is kept constant to 1 Ω. The five different resistor values that we considered are:

$$R_{G-HS-OFF}, R_{G-LS-ON} = \{1\ \Omega, 10\ \Omega, 50\ \Omega, 100\ \Omega, 200\ \Omega\}$$

Table 7 - Power stage specifications of the DC-DC converter

Parameter	Value
GaN MOSFET [V, A]	GS66516T (650, 60)
Inductor L [µH]	310
Low Voltage CLV [µF]	50
High Voltage CHV [µF]	100
Maximum Input Voltage [V]	300
Maximum Output Voltage [V]	600
Switching Frequency [kHz]	100

Table 8 - Gate driver specifications of the DC-DC converter

Parameter	Value
Gate Driver IC	Si8271
Input Voltage Range	3.3/5 V
Peak Current	4 A
Output	Sink/Source
Gate Driver Parameters	
Ferrite Beads (FBHS/FBLS)	MPZ1608S221A 220Ω @ 100 MHz
Zener Diodes (DZHS/DZLS)	MMSZ5221BS-7-F
Diodes (DHS/DLS)	TMBYV10
Capacitors (CHS/CLS)	1uF
Bipolar Power Supply	
Drive Voltage	+6/-3 V
Resistors (R1/R2)	1 kΩ
Capacitors (C1/C2/ C3)	4.7 µF
Zener Diode (DZ)	6.2 V

Table 9 - Specifications of the measurement tools

Parameter	Value
Input Current Probe	Agilent N2893A
Maximum Current	15 A
Bandwidth	100 MHz
Output Current Probe	Agilent N2821A+N2822A
Maximum Current	5 A
Bandwidth	3 MHz
Oscilloscope	Agilent DSO-X 3054A
Arbitrary Waveform Generator	LeCroy ArbStudio 1102
Spectrum Analyzer	Rohde & Schwarz FSH8 9kHz-8GHz
H-Field Probe	HZ552 H-Field Probe

Table 10 - Experimental test condition

Parameter	Value
Input Voltage [V]	25-30
Duty Cycle [%]	50
Output Power [W]	75-100
Switching Frequency [kHz]	100

In Table 10, we summarize the test conditions. The gate resistors selected for the 25 experiments were alternatively mounted on the PCB. All the tests were carried out with a low output power and a low input voltage so as to avoid any risk of damaging the circuit. As shown in Figure 25, the output load consists of three series connected resistors (10 Ω and 150 W each) and is mounted on a heatsink. In order to achieve an identical ON drain-source resistor, $R_{DS\text{-}ON}$, and comparable power losses for all tests, each test was performed when the switching devices reach a steady-state temperature. Moreover, since the resistive load and the dissipated power of the DC-DC converter are dependent on the ambient temperature, all the tests were done at constant ambient temperature.

3.2.3.2 Regression Functions

Each experiment is characterized by a pair of independent variables, $R_{G\text{-}HS\text{-}OFF}$ and $R_{G\text{-}LS\text{-}ON}$, and a pair of dependent variables, the efficiency and the near-field radiated EMI level. The efficiency considered is the overall efficiency of the converter, calculated by measuring the

input/output current/voltage of the converter. The near-field radiated EMI level is obtained by measuring the near magnetic field spectrum, plotting the spectra diagram, and considering the maximum amplitude of the spectra diagram in dBμA/m ($\widehat{MF}$) as the EMI level. The spectra diagram of the near magnetic field for the case of the conventional gate resistor design is shown in Figure 27.

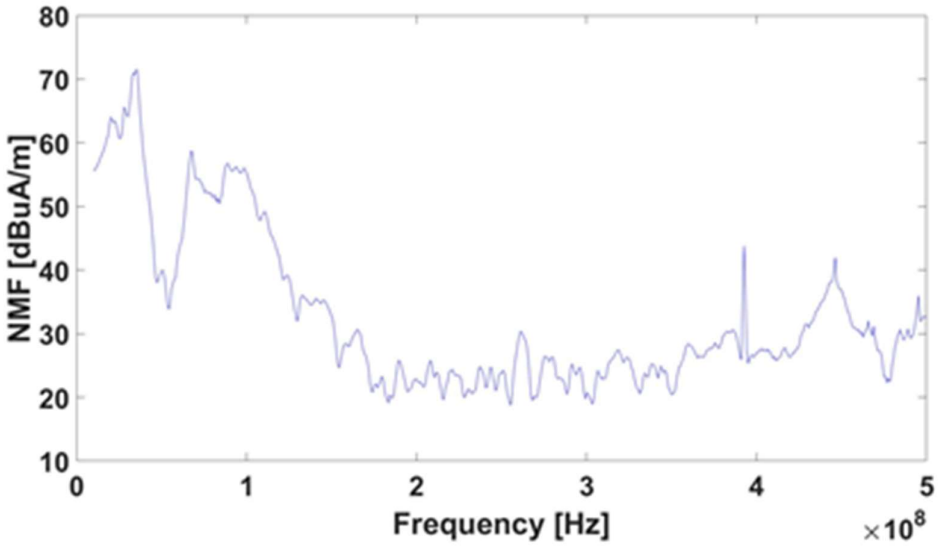

Figure 27 - Spectra diagram of the near magnetic field in the conventional gate resistor design

After performing the 25 experimental tests and measuring the values of the dependent output variables (efficiency and EMI level) for each of them, the *fitlm* solver from the MATLAB *Statistic and Machine Learning Toolbox* can be used to figure out the coefficients of the two regression functions as described in equations 2. Figure 28 shows the 3D mesh plots of the regression functions.

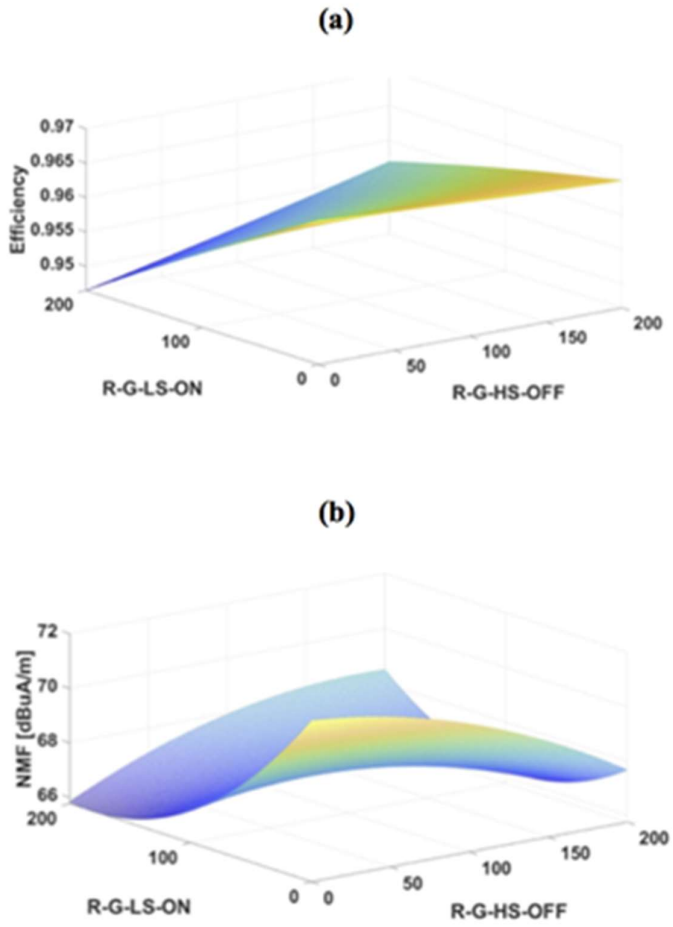

Figure 28 - 3D mesh plot of the regression functions: (a) Efficiency (η); (b) EMI Level

3.2.3.3 Multi-Objective Optimization Problem and Pareto Front

In this step, the multi-objective optimization problem of Equation (1) should be solved. The boundaries of the independent variables, $R_{G\text{-}HS\text{-}OFF}$ and $R_{G\text{-}LS\text{-}ON}$, are defined as follows: R_{bound} = [R_{min}=1Ω, R_{max}=200 Ω]. The multi-objective optimization problem is solved using the *gamultiobj* non-linear multi-objective optimization solver from the MATLAB *Optimization Toolbox*. The solver allows to plot the *Pareto Front* as well, which contains all the optimum points of the multi-variable problem in the range of values of the independent variables (Figure 29). At this step, it is up to the designer to choose the optimum point that best corresponds to the design objectives. In this paper, the selected optimal point, as it can be seen in Figure 29,

corresponds to the knee-point of the Pareto Front. The expected efficiency and EMI level of the selected optimum point are 0.9639 and 66.87 dBµA/m respectively. The values of the corresponding independent variables of the selected optimum point are $R_{G\text{-}HS\text{-}OFF}$ = 196.8 Ω and $R_{G\text{-}LS\text{-}ON}$ = 40.9 Ω as well.

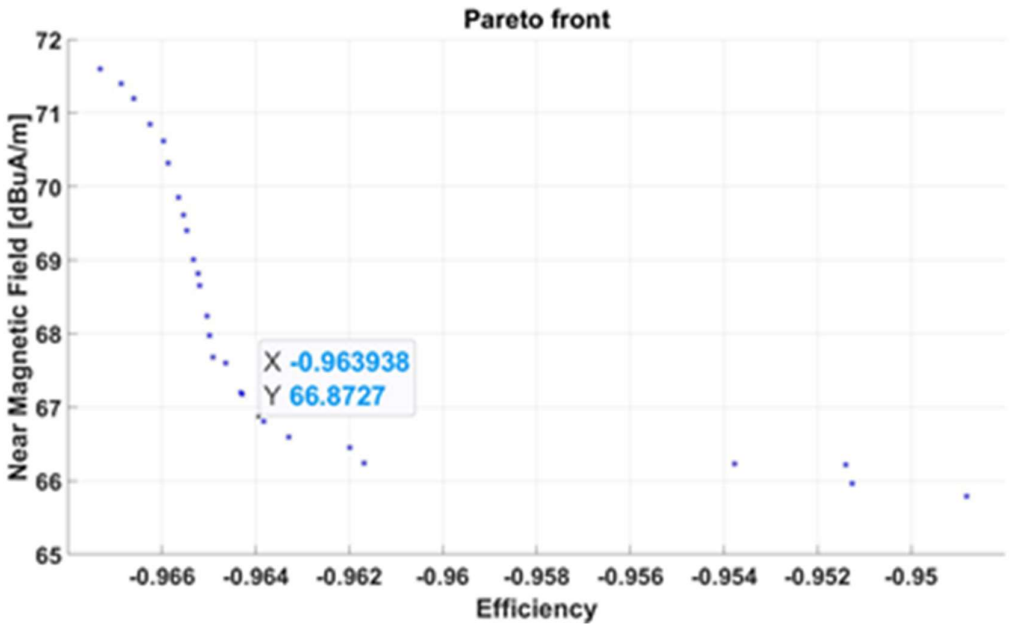

Figure 29 - Pareto Front of the solved multi-objective optimization problem

3.2.3.4 Optimum Gate Resistor Design

In the last step, once the optimum point has been chosen, the corresponding optimum resistors are mounted on the circuit and the measurements are re-performed to obtain the efficiency and the EMI level.

Table 11 - Result Comparison for the two design cases

Design	$R_{G\text{-}HS\text{-}OFF}$	$R_{G\text{-}LS\text{-}ON}$	Eff	EMI Level
Conventional	1 Ω	10 Ω	0.9618	71.81 dBµA/m
Optimum	196.8 Ω	40.9 Ω	0.9754	67.20 dBµA/m

In Table 11, we present the experimental results for both conventional and proposed optimum designs. It can be noted that in the case of optimal design, a 1.7% increase in efficiency and a 6.4% reduction in EMI level have been obtained. It is emphasized that the experimental results differ from the Pareto Front values due to measurement errors, the regression model, calculation errors in the solution of the optimization problem, etc. However, the errors are less than 1.5%. In Figure 27 is shown the spectra diagram of the optimum gate resistor design. The maximum peak of the near magnetic field occurs at the frequency of 35 MHz, as in the case of conventional design in Figure 27.

It is worthy to emphasis here that the proposed design method is a post-prototyping method. It means that all characteristics of the PCB, such as parasitics, that highly affect the EMI level of the converter, can be seen and considered for the gate driver resistor design. On the contrary, in a conventional design, the values of the gate driver resistors, are proposed by the application note, for any converter in general, regardless of its PCB design and its corresponding parasitics.

3.2.4 Conclusion

In this work, the slew rate control of the GaN devices in a half-bridge configuration of a DC-DC converter was studied. The slew rate control is achieved using a post-prototyping multi-objective optimization method to parameterize the gate driver resistors. The efficiency of the converter and the near-field EMI of the GaN device are considered as the objective functions of the optimization problem. The optimum design point was obtained using the experimental measurements and mathematical calculations. Finally, the experimental results showed the improvement in both efficiency and EMI level compared to those of the conventional gate driver resistor design.

3.3 Current source gate driver for GaN e-HEMT in Hard-Switching High Power Applications

3.3.1 Introduction

There are different aspects to be concerned in the gate driver design such as the gate driver circuit, the layout, the gate resistors/inductors design, the ON/OFF gate-source voltage, and the gate current capability. Rather than providing the essential needs of the device, such as the proper gate-source voltage in the case of MOSFETs, the gate driver design intends to reduce the "power loss" and the "ringing" [64] [42]. To this aim, apart from the conventional techniques such as using a ferrite bead [65] or a RC snubber [66], there are innovative methods such as the multi-objective optimization of the parameters [31], the active source inductance [67] [68], etc. Moreover, Wide Band Gap (WBG) devices such as Gallium Nitride (GaN) and Silicon Carbide (SiC) have superiority over Silicon (Si) MOSFETs and Si IGBTs in the term of the power losses and the switching frequency. However, these new devices have characteristics to be concerned in the term of the gate drive design. For example, the GaN device (GS66516T by GaNSystems) has a very low threshold voltage ($V_{GS(th)}$ = 1.1 – 1.3 V) that can cause unwanted turning ON/OFF. Therefore, it needs a special gate driver design [41] [69]. In [70], a novel gate driver circuit is proposed for the GaN device to reduce turn-OFF power loss. In [71], an optimized gate driver parameterization is studied for the GaN device in high frequency application. Another topic in the gate driver design is the current source gate drivers. In a conventional voltage source gate driver, the gate current during the turn-OFF transition of the device doesn't return to the voltage source. Instead, it sinks to the ground, causes the gate driver loss (Figure 30 and Figure 31).

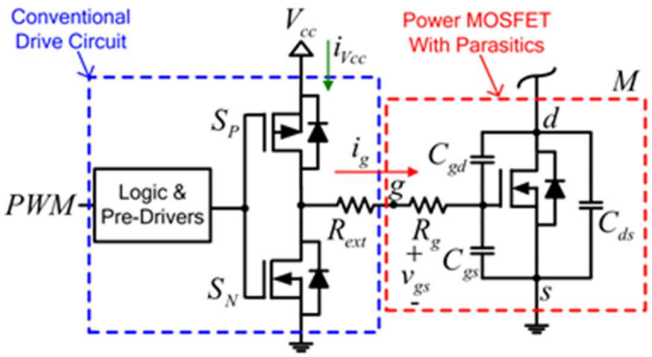

Figure 30 - Conventional voltage source gate driver: gate driver circuit [72]

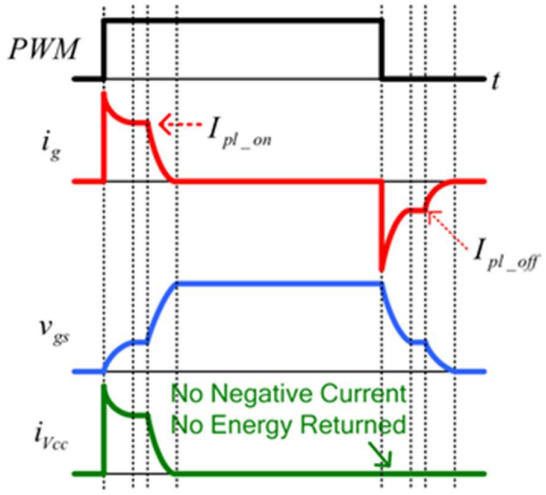

Figure 31 - Conventional voltage source gate driver: waveforms

The initial idea of the current source gate driver was to recover the gate driver energy during the turn-OFF transition by charging a resonant inductor (L) with the gate driver current (Figure 32 and Figure 33).

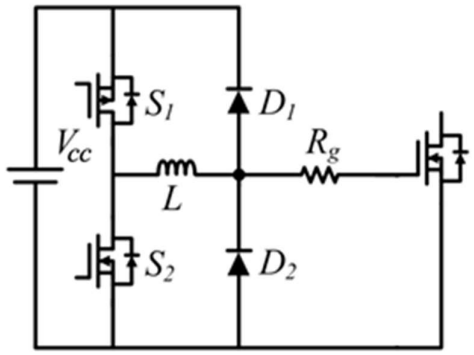

Figure 32 - LS current source gate driver with zero initial inductor current: gate driver circuit [73]

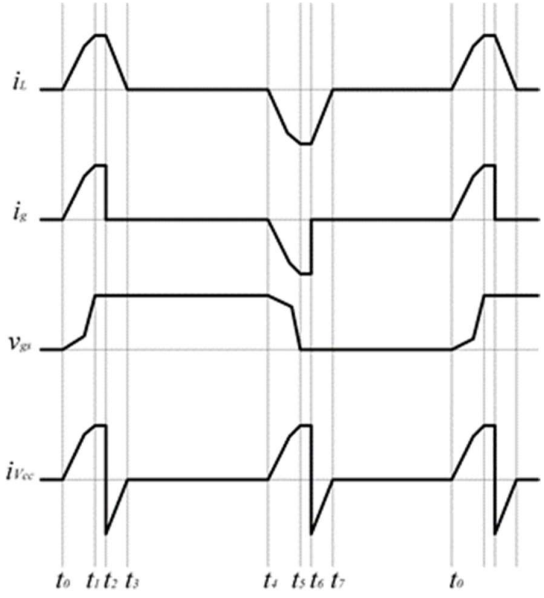

Figure 33 - LS current source gate driver with zero initial inductor current: waveforms [73]

In very high frequency (> 1 MHz) low power (< 100 W) applications, the gate driver loss ($P_G = V_{GS} \times f_{sw} \times Q_{G(tot)}$) is a considerable portion of the total power loss. Therefore, the current source gate driver is well known for the mentioned applications. The limitation of the current source gate driver of Figure 32 and Figure 33 is the slow transition times due to gate charging by the inductor current with an initial value of zero. Another type of current source gate drivers is that with non-zero initial inductor. In such a gate driver, rather than recovering the gate driver loss, the gate is charged/discharged at a higher current results in faster switching time and consequently lower switching power loss (Figure 34 and Figure 35).

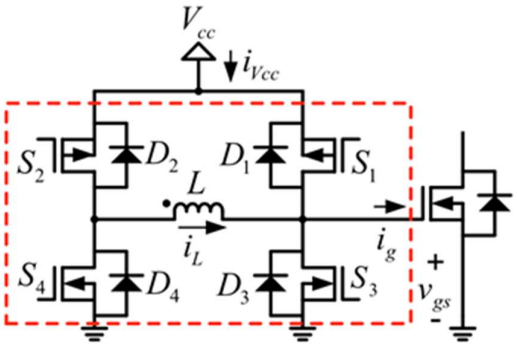

Figure 34 - LS current source gate driver with non-zero initial inductor current: gate driver circuit [74]

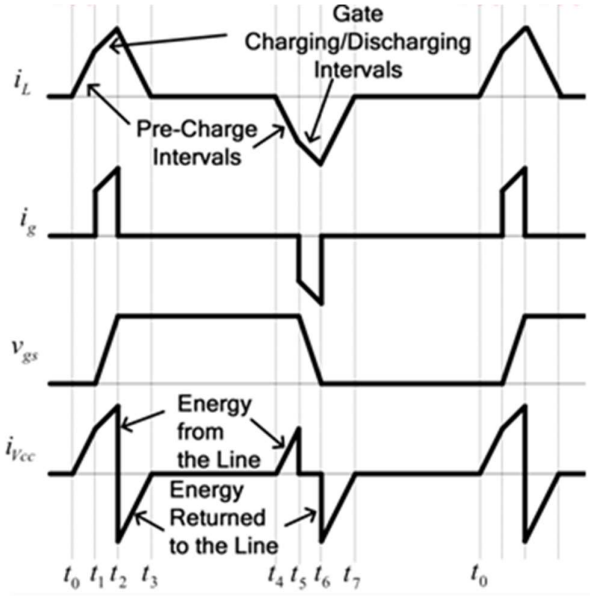

Figure 35 - LS current source gate driver with non-zero initial inductor current: waveform [74]

Current source gate drivers are also a topic of research for the WBG devices. Particularly in the case of GaN devices, the high frequency application and the higher resulted gate driver loss are the concern of researchers where they propose different types of current source gate drivers to reduce the gate power loss [75-79]. However, for medium-to-high voltage/power applications of GaN devices, such as the mentioned GS66516T GaN device in electric vehicles [37] or in battery energy storage systems [80], where the gate driver power loss is negligible and the switching power loss is the main contributor, current source gate drivers are not studied. As a result, in this study current source gate drivers with non-zero initial inductor current are studied and proposed for medium-to-high voltage/power GaN devices.

3.3.2 Current source gate driver

Due to the voltage/current rating of the GaN device, which is 650 V 60 A GS66516T by GaNSystems, only current source gate drivers with non-zero initial inductor current are of our interest. Because, as it is explained before, the non-zero initial inductor current type is able to decrease switching power loss, which is the main power loss contributor in our medium-to-high voltage/power applications.

In this paragraph two current source gate drivers with non-zero initial inductor current are studied. The first current source gate driver is a LS gate driver as it is shown in Figure 34 and Figure 35. Two diodes (D_1 and D_2) in Figure 32 are replaced with two controllable transistors (S_1 and S_3) in Figure 34. For the turn-ON transition of the device, during $t = t_0$ to t_1, the inductor current (i_L) passes through V_{cc}, S_2, S_3, and the ground to charge the resonant inductor (L). Then, at $t = t_1$, S_3 is turned-OFF and the non-zero i_L passes through V_{cc}, S_2 and the gate of the device. When the gate is fully charged ($V_{gs} = V_{gs\text{-}ON}$), S_1 and S_4 are turned-ON at $t = t_2$ and i_L passes through the ground, S_4, S_1, and V_{cc} to discharge the inductor L and to recover i_L to the voltage source V_{cc}.

The same for the turn-OFF transition of the device, during $t = t_4$ to t_5, the inductor current (i_L) passes through V_{cc}, S_1, S_4, and the ground to charge the inductor L in the opposite direction. Then, at $t = t_5$, S_1 is turned-OFF and the negative non-zero i_L passes through the gate of the device, S_4 and the ground. When the gate is fully discharged ($V_{gs} = V_{gs\text{-}OFF}$), S_2 and S_3 are turned-ON at $t = t_6$ and i_L passes through the ground, S_2, S_3, and V_{cc} to discharge the inductor L and to recover i_L to the voltage source V_{cc}.

The second current source gate driver is a HB gate driver as it is shown in Figure 36 and Figure 37.

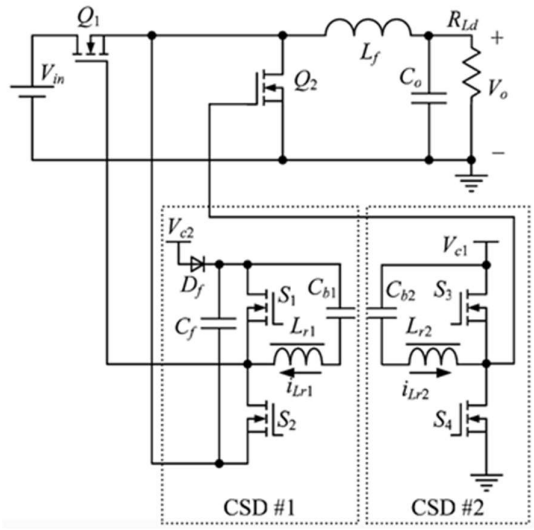

Figure 36 - HB current source gate driver with non-zero initial inductor current: gate driver circuit [81]

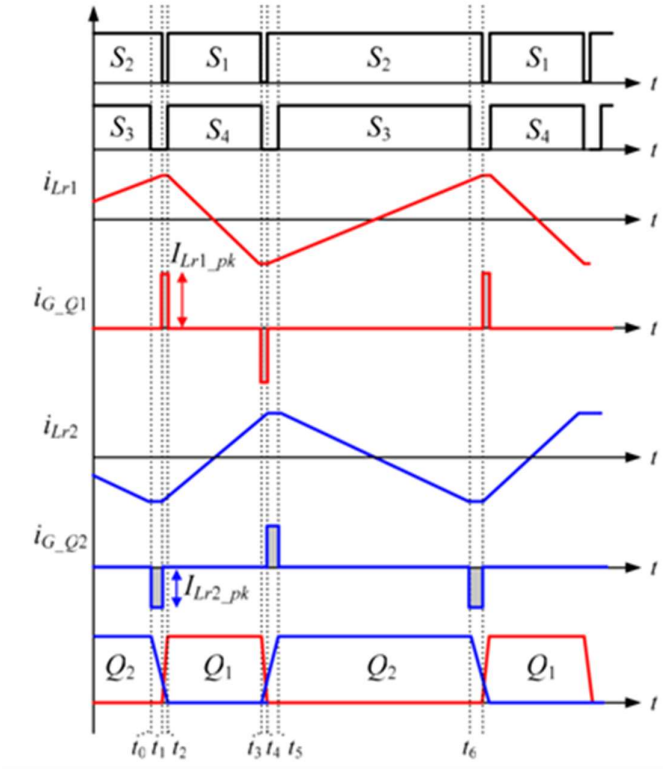

Figure 37 - HB current source gate driver with non-zero initial inductor current: waveforms [81]

Practically, the current source drivers (CSD #1 and CSD #2) work independently for the optimal operation of the both HS and LS transistors (Q1 and Q2). To this aim, the voltage sources (V_{c1} and V_{c1}), the resonant inductors (L_{r1} and L_{r1}), and the blocking capacitors (C_{b1} and C_{b1}) can be designed independently to provide the optimal gate currents (I_{Lr1_pk} and I_{Lr2_pk}) for Q1 and Q2 respectively. The HS CSD #1 has the same configuration of the LS CSD #2 plus the voltage level-shift circuit of the capacitor C_f and the diode D_f. The LS CSD #2 can be compared with the LS gate driver of Figure 34 as well where in the case of the LS CSD #2, only two controllable transistors are applied instead of four transistors and the inductor current is continuous instead of being discontinuous. In all cases, for a larger amount of resonant inductance, the relevant gate driver current will be higher, the switching power loss of the device will be lower, and the gate driver will be higher. Therefore, a trade-off optimal design can be considered for the gate driver where the sum of the switching power loss and the gate driver loss is minimum. However, in our case as the gate driver loss is negligible compared to the switching power loss, the objective is to minimize the switching power loss as much as possible.

3.3.3 Simulation results

In this section the GaN device (650 V 60 A GS66516T by GaNSystems) is simulated in OrCAD Space in two different cases. In the first case, a conventional voltage source gate driver is applied where the gate-source voltages of $V_{GS\text{-}ON}$=6 V, $V_{GS\text{-}OFF}$=-3 V and the gate resistors of $R_{G\text{-}ON}$=5 Ω, $R_{G\text{-}OFF}$=1 Ω are considered for the turn-ON and the turn-OFF intervals respectively [41]. In the second case the LS current source gate driver of Figure 36 (CSD #2) is applied in which the resonant inductor and the blocking capacitor are designed as follow [81]:

$$C_b = \frac{I_{Lr\_pk}}{4 \times k \times V_c \times f_{sw}} \qquad (1)$$

$$L_r = \frac{V_c \times D \times (D-1)}{2 \times I_{Lr\_pk} \times f_{sw}} \qquad (2)$$

In these formulation, the peak inductor current I_{Lr_pk} = $I_{G\text{-}pk}$ =8 A is considered high enough to minimize the ON and the OFF switching transition times (T_{ON} and T_{OFF}) and the corresponding switching power loss. The voltage source V_c=6 V is considered the same as $V_{GS\text{-}ON}$ in the case of voltage source gate driver, k=0.05 is the per unit voltage ripple of the blocking capacitor C_b, f_{sw} = 100 kHz is the switching frequency of the GaN device, and D in fact is the duty cycle of the HB DC-DC converter, but here it is assumed D=0.5. In this way, the blocking capacitor and the resonant inductor are obtained as $C_b = 66.66\ \mu F$ and $L_r = 0.9375\ \mu H$.

The waveforms of the OrCAD Spice simulations are presented in Figure 38, 39, 40, 41, 42, 43, 44, and 45 for both voltage source gate driver (VSD) and current source gate driver (CSD) in both turn-ON and turn-OFF transitions. All figures show a period of 50 ns. In the turn-ON transition, the gate current is much higher for the CSD (around 8 A) respect to that for the VSD (around 1 A). There is no plateau gate voltage for the CSD as well. All together, transition time of drain-source voltage (V_{DS}) and drain current (I_D) are much faster for the CSD (Figure 40) compared to the VSD (Figure 38). In the turn-OFF transition, the gate current is higher for the CSD (around -5 A) respect to that for the VSD (around -2 A) as well. The V_{GS} transition is faster for the CSD respected to that of the VSD. But, there is no considerable transition time difference for the V_{DS} and the I_D for the CSD compared to those of the VSD.

To study the effect of the L_r value and its corresponding $I_{G\text{-}pk}$ value, the CSD is simulated with $L_r = 3.75\ \mu H$ (Figure 46) and $L_r = 0.46875\ \mu H$ (Figure 47). In the first case, the value of the L_r is four times of that of Figure 41. The corresponding peak gate current is $I_{G\text{-}pk}$=2 A, one-forth of that of Figure 41, results in a turn-ON transition time of the V_{GS} around two times slower than that of Figure 41. In the case of Figure 46, the V_{Gs} has almost no overshoot as well. In the second case, the value of the L_r is half of that of Figure 41. But, the corresponding peak gate current doesn't reach more than $I_{G\text{-}pk}$=9 A, which is slightly higher than that of Figure 41, results in the same turn-ON transition time of the V_{GS} as that of Figure 41. Moreover, the overshoot of the V_{GS} is around 30 percent higher than that of Figure 41. As a result, the optimum value of L_r=0.9375 and its corresponding $I_{G\text{-}pk}$ = 8 A is selected for the CSD to obtain a very fast turn-ON transition with a low V_{GS} overshoot.

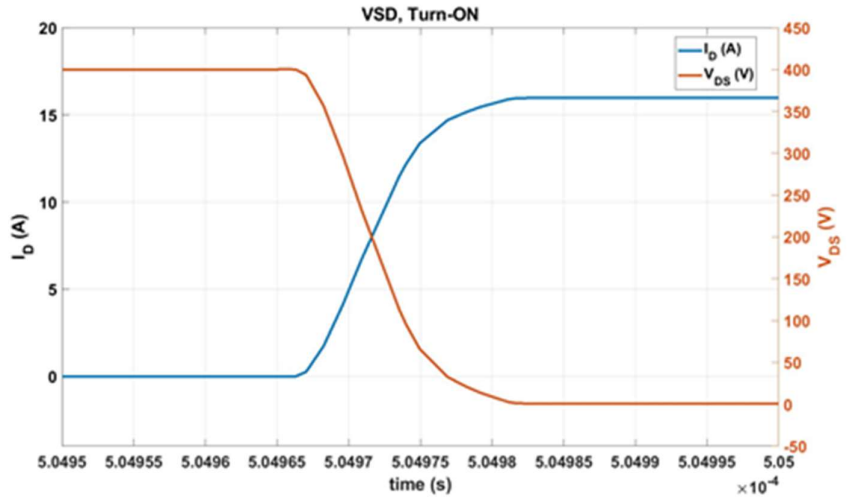

Figure 38 - Turn-ON transition using the voltage source gate driver: I_D, V_{DS}

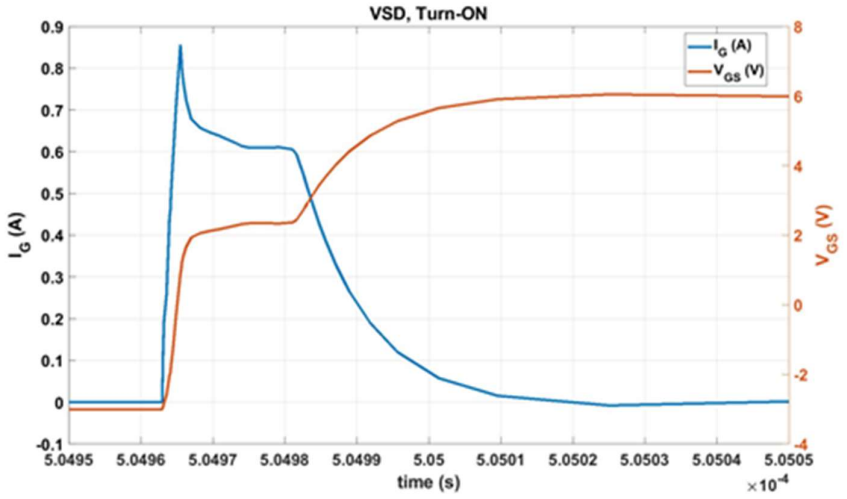

Figure 39 - Turn-ON transition using the voltage source gate driver: I_G, V_{GS}

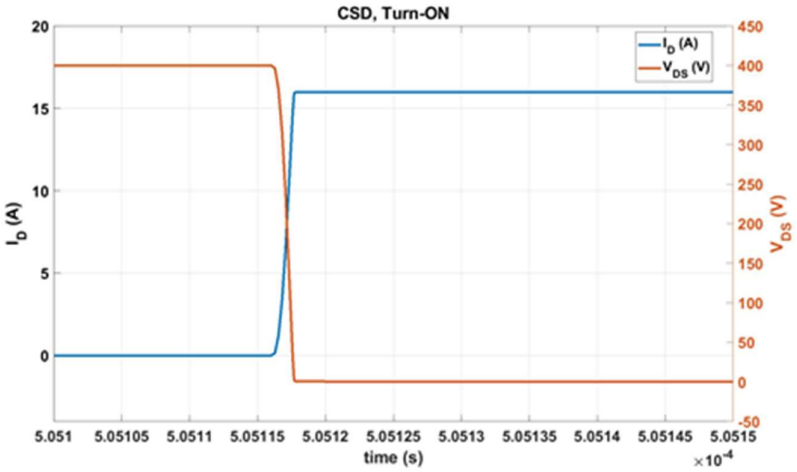

Figure 40 - Turn-ON transition using the current source gate driver: I_D, V_{DS}

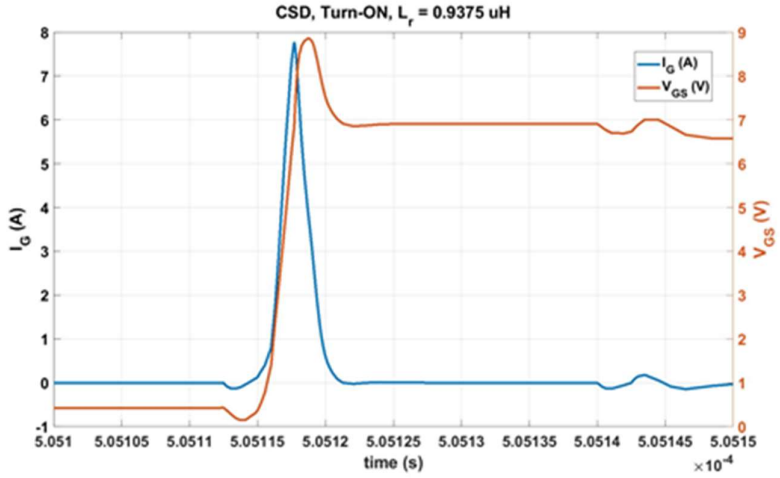

Figure 41 - Turn-ON transition using the current source gate driver: I_G, V_{GS}

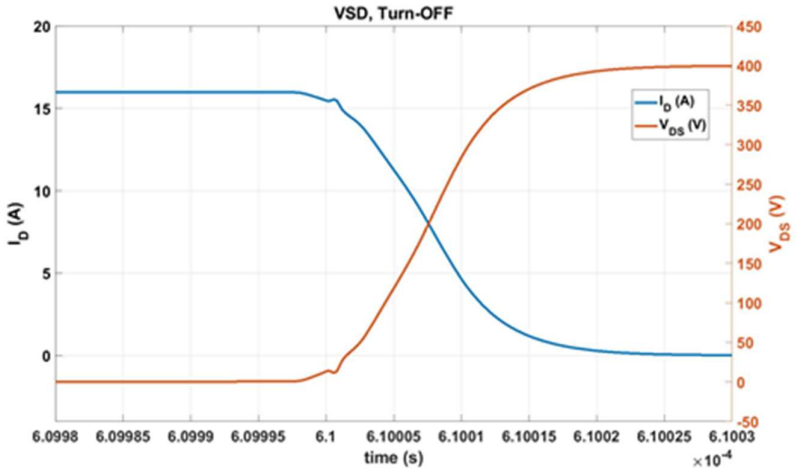

Figure 42 - Turn-OFF transition using the voltage source gate driver: I_D, V_{DS}

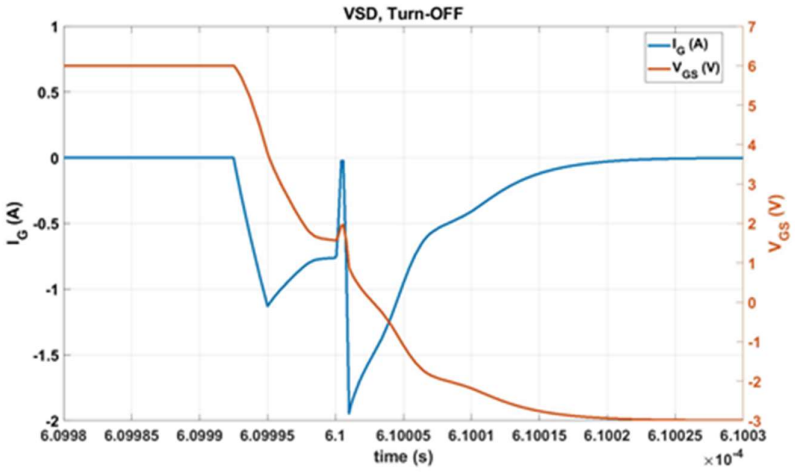

Figure 43 - Turn-OFF transition using the voltage source gate driver: I_G, V_{GS}

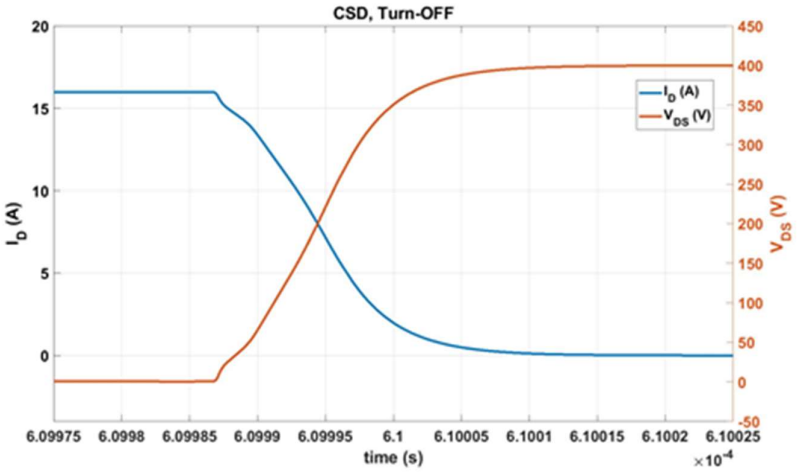

Figure 44 - Turn-OFF transition using the current source gate driver: I_D, V_{DS}

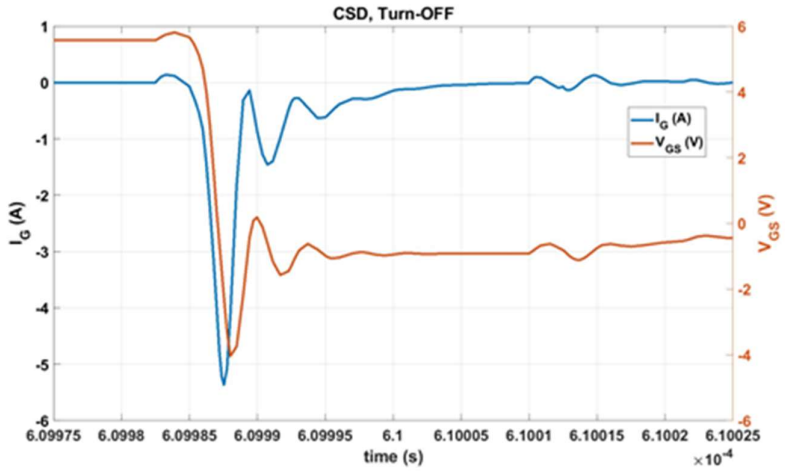

Figure 45 - Turn-OFF transition using the current source gate driver: I_G, V_{GS}

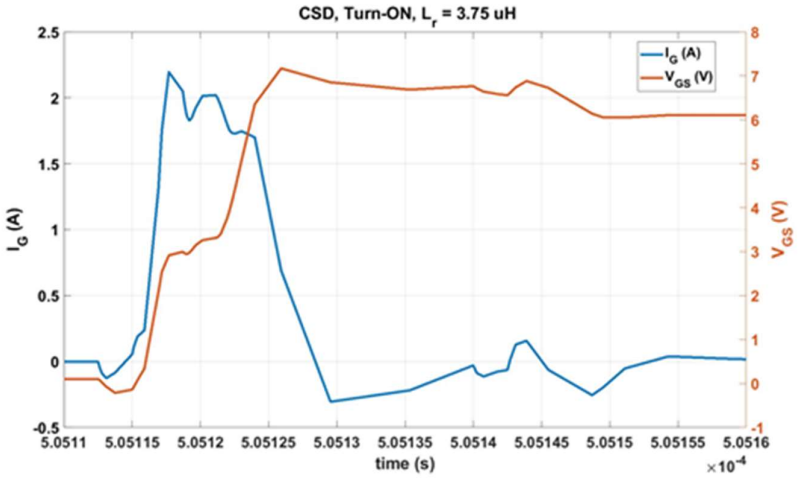

Figure 46 -Turn-ON transition of the gate-source voltage (V_{GS}) and the gate current (I_G) for the CSD with different values of the resonant inductor (L_r=3.75 uH) and its corresponding gate current (I_G)

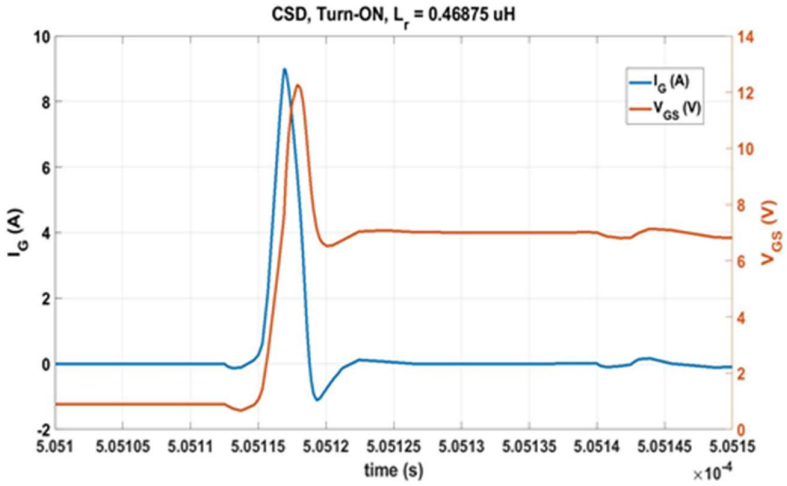

Figure 47 - Turn-ON transition of the gate-source voltage (V_{GS}) and the gate current (I_G) for the CSD with different values of the resonant inductor (L_r=0.46875 uH) and its corresponding gate current (I_G)

Now, the conduction loss (P_{Cond}) and the switching loss (P_{SW}) can be calculated in order to compare the total device power loss for the both VSD and CSD as follow:

$$P_{Cond} = R_{DS-} \times I_{D(rms)}^{2} \qquad (3)$$

$$P_{SW} = V_{DS} \times I_D \times f_{SW} \times \frac{T_{ON} + T_{OFF}}{2} \qquad (4)$$

As it is explained in [72], the CSD has smaller source impedance compared to that of the VSD. Therefore, for the same amount of the gate driver voltage (V_{cc}), there is a higher gate-

source voltage (V_{GS}) in the case of the CSD. As a higher V_{GS} results in lower $R_{DS\text{-}ON}$, the conduction loss is also lower in the case of the CSD.

The values of $R_{DS\text{-}ON}$, T_{ON}, and T_{OFF} as well as the resulted P_{Cond} and P_{SW} are summarized in Table I. To obtain the value of the $R_{DS\text{-}ON}$, the average of the all OrCAD Spice simulation samples of the V_{DS} and the I_D during the conduction time interval of the device are calculated. Then, $R_{DS\text{-}ON}$ is considered as $V_{DS\text{-}AVG}/I_{D\text{-}AVG}$ where AVG stands for "average". T_{ON} and T_{OFF} are obtained from the OrCAD Spice simulation results as well. Based on the simulations and the calculations, the total power losses are 10.6 W and 14.7 W for the case of CSD and the case of VSD respectively. It validates the superiority of the CSD over the VSD in the term of device power losses (28 % improvement).

Table 12 - Power loss analysis

Parameters	VSD	CSD
$\boldsymbol{T_{ON}}$ $[\boldsymbol{ns}]$	11 ($R_{G-ON} = 5\ \Omega$)	1.5
$\boldsymbol{T_{OFF}}$ $[\boldsymbol{ns}]$	15 ($R_{G-OFF} = 1\ \Omega$)	12
$\boldsymbol{P_{Cond}}$ $[\boldsymbol{W}]$	6.4 ($R_{DS-ON} = 25.2\ m\Omega$)	6.3 ($R_{DS-ON} = 24.8\ m\Omega$)
$\boldsymbol{P_{SW}}$ $[\boldsymbol{W}]$	8.3	4.3
$\boldsymbol{P_{tot}}$ $[\boldsymbol{W}]$	14.7	10.6

3.3.4 Conclusion

Current source gate drivers (CSDs) are studied in this chapter for wide band gap (WBG) Gallium Nitride (GaN) devices in the hard-switched medium-to-high voltage/power applications such as electric vehicle (EV) and battery energy storage system (BESS). The configuration and the operation of a zero initial inductor current CSD, a low side (LS) non-zero initial inductor current CSD, and a half-bridge non-zero initial current CSD are presented and compared. A power loss analysis is performed to compare the conventional voltage source gate driver (VSD) to the CSD using OrCAD Spice for the GaN device 650 V 60 A GS66516T by GaNSystems. The power loss analysis validates the faster switching time, the lower switching loss, the lower ON drain-source resistance, and the lower conduction loss of the CSD compared

to those of the VSD. Finally, the simulation results prove a total device power loss improvement of 28 % in the case of CSD.

3.4 A GaN-Based Battery Energy Storage System for Three-Phase Residential Application with Series- Stacked devices and Three-Level Neutral Point Clamped Topology

3.4.1 Introduction

The penetration of distributed power generation (DG) based on renewable energy reduces the transmission power losses and the power system infrastructure expenses. Environmental benefits are also obtained regarding the clean nature of renewable energy resources such as photovoltaic solar energy and wind energy. However the renewable energy resources have a stochastic and unpredictable nature. Therefore, the injected power of the DG units to the grid causes fluctuation and other power quality problems. In addition, the power management of the DG units is another concern. As a solution, battery energy storage systems (BESSs) can be used beside DG units to improve the reliability and the controllability of the injected power. Moreover, applying BESSs, it is possible to make economical benefit in the deregulated power markets [46- 47]. As a result, BESSs are being studied and developed for example in Italy [48] and in the central Europe [49].

As said several times, in the last decade, wide band gap (WBG) devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are introduced as the future of power electronic for high efficiency, high frequency, and high voltage applications. Particularly in BESS application, WBG devices are being studied in the recent years as well.

In [50], SiC-based isolated bidirectional dc-dc converter is proposed in a medium power three-phase BESS. In [51], SiC device are compared with Si IGBT for the same application. In [52], SiC device is applied in a BESS with multi-level converter topology for mega watt (MW) power, distribution system voltage (13.8 kV) application. In [53], 650 V GaN devices are discussed for BESSs in the application of 400 V DC micro grids.

The comparison of SiC with GaN is the subject of some recent research [54]. The current available GaN devices have lateral structure results in limited current rating. The expected GaN devices with vertical structure will solve this problem in the future [37]. The superiority of GaN over SiC is its lower switching power losses. Since the *rms* value of the voltage at the three-

phase AC grid side of the BESS is 400 V, a regulated DC bus voltage of 800 V is needed. The voltage rating of the available GaN devices in the market is limited to 650 V which is not applicable for the three-phase residential application. On the contrary, there are SiC devices with voltage rating of 1200 V make them suitable for this application.

A solution to overcome the voltage limitation of switching devices is to apply them in series in a so-called series- connected or "series-stacked" structure. In [55], two series-connected 650 V GaN devices are studied in term of switching power losses to be used in the applications of 1.2 kV. In [56], two series-stacked 650 V GaN devices are applied using an integrated gate driver for the application of electric vehicles. The series-stacked GaN devices with a voltage rating of 650x2 = 1.3 kV are compared with a SiC device (1.2 kV) in the term of power losses. To have the advantage of lower switching power loss and solve the limitation of voltage rating at the same time, series-stacked devices are proposed in this paper as well.

GS66516T by GaNSystems is a state-of-the-art GaN device with high current rating and high efficiency compared to other GaN devices in the voltage range of 650 V. SCT3030KL by ROHM has the same situation among SiC devices in the voltage range of 1200 V. These two devices are compared in Table 12. The SiC device has lower drain-source ON resistance ($R_{DS(on)}$) 30 mΩ respect to that of the two series GaN devices 25x2 = 50 mΩ and relatively lower conduction power loss.

Table 13 - Parameters comparison between GaN and SiC

Parameters	**GaN Transistor GaNSystems (GS66516T)**	**SiC MOSFET ROHM (SCT3030KL)**
V_{DS} $[V]$	650	1200
$R_{DS(on)}$ $[m\Omega]$	25	30
I_D $[A]$	60	72
$Q_{G(tot)}$ $[nC]$	12.1	131
Q_{rr} $[nC]$	0	135
C_{iss} $[pF]$	520	2222
C_{oss} $[pF]$	130	180

Its current rating is also 20% more than that of the GaN device. Instead, the GaN device has a very low gate charge ($Q_{G(tot)}$), zero reverse recovery charge (Q_{rr}), lower input and output

parasitic capacitance (C_{iss} and C_{oss} respectively). Consequently, the GaN device has a very lower switching power loss and relatively higher efficiency in hard-switched applications.

In Figure 30, the configuration of the energy storage system (ESS) in the power system and the position of residential load are shown by ABB [56]. In [57], commercial ABB BESSs are presented where ESI-S model is a three-phase BESS with a power rating of 20 kW. Considering the limited current of the GaN devices and the voltage/power rating of the BESSs, in this study a three-phase BESS is proposed for residential application with a power rating of 15 kW.

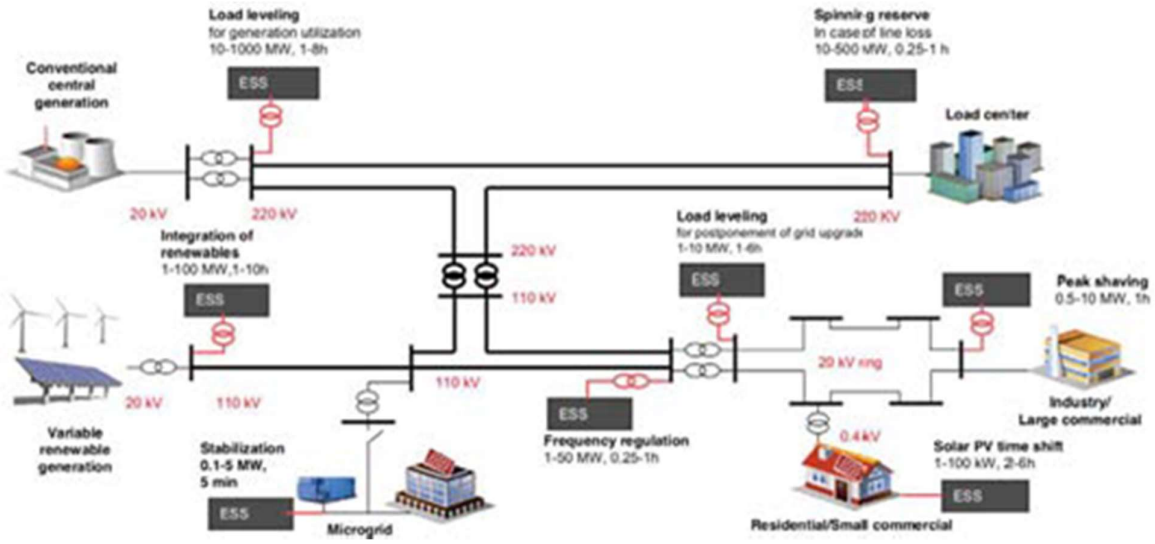

Figure 48 - Configuration of the ESS in the power system by ABB [15]

The proposed GaN-based BESS includes two power electronic stages. The first stage of the BESS is a half-bridge bidirectional dc-dc converter with series-stacked GaN devices. The second stage of the BESS is a three-phase grid-connected inverter with three-level (3L) neutral point clamped (NPC) topology. In the DC-DC converter, it needs a maximum DC current of 60 A in the low voltage (LV) battery side for full load operation of 15 kW. The two series-stacked GaN devices provide a voltage rating of 1.2 kV while the DC bus has a regulated voltage of 800 V. In the DC-AC inverter, it needs a maximum AC current in the full load with a peak value of 31 A at the ac grid side. The both high side (HS) and low side (LS) devices should tolerate a voltage of 800 V. Therefore, two series-stacked GaN devices are needed. The 3L NPC topology not only

uses two series devices for the both HS and LS, but also has the advantage of low dv/dt and THD at the output AC voltage. As a result, 3L NPC inverter is selected in this study.

The rest of this chapter is organized as follow: in section 3.4.2, the configuration of the BESS, the power stage design, and the control design are discussed. In section 3.4.3, the series-stacked GS66516T GaN devices are compared with SCT3030KL SiC device in the term of power losses based on OrCAD Spice simulations. Then, the GaN-based BESS is simulated with MATLAB SIMULINK to validate the satisfactory performance of the controller system. Finally, the conclusion is presented in section 3.4.4.

3.4.2 Battery Energy Storage System

3.4.2.1 Configuration

The configuration of the GaN-based BESS is shown in Figure 2.

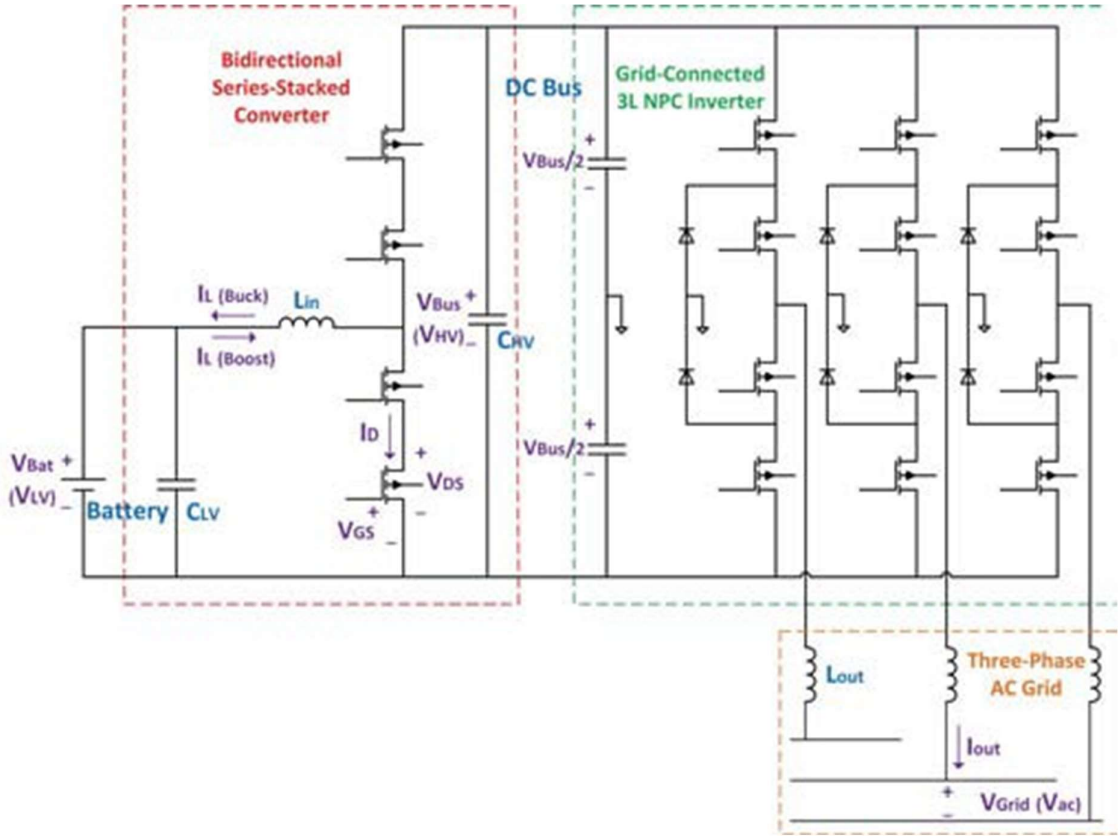

Figure 49 - Configuration of the GaN-based BESS

It consists of the battery pack, the DC-DC converter, the DC-AC inverter, and the three-phase AC grid. The DC-DC converter is a bidirectional converter with a half-bridge topology. The voltage level of the battery and the DC bus are 250 V and 800 V respectively. In both HS and LS of the half-bridge converter, two series-stacked GaN devices are applied. In this way, a drain-source voltage V_{DS} = 800/2 = 400 V should be provided by each GaN devices which is satisfactory due to their voltage rating of 650 V. At the power rating of 15 kW, the DC value of the input inductor current (I_L) is 15000/250 = 60 A. Therefore, the DC value of the drain current (I_D) of the GaN devices during the ON intervals is equal to their current rating of 60 A. As we can see in formula (1), the input inductor current ripple is only 1.2 A, that is not a problem for the GaN devices.

The DC-AC three-phase grid-connected inverter has a three-level (3L) neutral point clamped (NPC) topology. Nabae introduced 3L NPC inverter at 1992 for the first time. In this

topology, the DC bus voltage is divided into three levels of voltage (-, +, N). The main advantage of 3L NPC inverter is the low dv/dt and THD at its output ac voltage. It is usually used in the medium/power applications [58]. In our case, the series-stacked devices are another advantage of this topology where each GaN device needs to tolerate only a voltage of $V_{Bus}/2 = 800/2 = 400$ V.

The input inductor [59], the low voltage (LV) capacitor [60], the output filter [61], and the high voltage (HV) capacitor [62] can be designed as follow:

$$L_{in} = \frac{V_{HV} \cdot \left(1 - \frac{V_{LV}}{V_{HV}}\right) \cdot \left(\frac{V_{LV}}{V_{HV}}\right)^2}{\Delta I_{L(P.U.)} \cdot I_{L(min)} \cdot f_{s1}} \qquad (1)$$

where V_{LV} = 250 V is the voltage of the battery, V_{HV} = 450 V is the voltage of the regulated DC bus, $\Delta I_{L(P.U.)}$ = 0.3 A is the per unit current ripple of the inductor, $I_{L(min)}$ = 4 A is the minimum inductor current which happens at a minimum power of 1 kW, and f_{s1} = 100 kHz is the switching frequency of the DC-DC converter. In this way, the DC-DC converter operates at continuous conduction mode (CCM) even at a minimum power of 1 kW result in L_{in} = 514 µH.

$$C_{LV} = \frac{\frac{V_{LV}}{V_{HV}}}{8 \cdot L_{in} \cdot \Delta V_{LV} \cdot f_{s1}} \qquad (2)$$

Where $\Delta V_{LV} = \Delta V_{LV(P.U.)} \times V_{LV}$ and $\Delta V_{LV(P.U.)}$ is the per unit ripple which considered as 0.05 and result in C_{LV} = 108 µF.

$$L_{out} = \frac{\frac{V_{HV}}{2}}{8 \cdot \Delta I_{out} \cdot f_{s2}} \qquad (3)$$

Where $\Delta I_{out} = \Delta I_{out(P.U.)} \times I_{out(max)}$ and $\Delta I_{out(P.U.)}$ is the per unit output current ripple which considered as 0.05; $I_{out(peak)}$ is the peak value of the output AC current and is calculated as:

$$I_{out(peack)} = \frac{P_{rating}}{\sqrt{3} \cdot V_{grid(rms)} \cdot PF} = \frac{15000}{\sqrt{3} \cdot 400 \cdot 0.7} = 31\ A$$

and f_{s2} = 100 kHz is the switching frequency of the inverter. Moreover, PF = cosφ is the power factor limited to 0.7 which satisfactory for the demanded reactive power of residential loads and φ is the phase angle between the voltage and the current of each phase. Finally, the inductance of the output filter will be obtained as L_{out} = 322 µH.

$$C_{HV} = \frac{I_{L(min)} \cdot \left(1 - \frac{V_{LV}}{V_{HV}}\right)}{\Delta V_{HV} \cdot f_{s1}} \qquad (4)$$

where $I_{L(max)}$ = 60 A is the maximum input inductor current, $\Delta V_{HV} = \Delta V_{HV(P.U.)} \times V_{HV}$ and $\Delta V_{HV(P.U.)}$ is the per unit ripple which considered as 0.01 and result in C_{HV} = 52 µF.

The clamp diodes should switch at f_{s2} = 100 kHz, conduct the peak of current of $I_{out(peak)}$ = 31 A, and tolerate the voltage of $V_{BUS}/2$ = 800/2 = 400 V. Based on this characteristics, SCS240AE2 SiC by ROHM is selected which is a schottky barrier diode (SBD).

Table 8 summarizes the specifications of the proposed GaN-based BESS.

Table 14 - Specifications of the GaN-based BESS

GaN Transistors Part Number by GaNSystems	GS66516T
SiC SBD Part Number by ROHM	SCS240AE2
Battery Input Voltage V_{Bat} (V_{LV}) [V]	250
Regulated DC Bus Voltage V_{Bus} (V_{HV}) [V]	800
Three-Phase AC Grid Voltage $V_{Grid\ (rms)}$ [V]	400
Power rating P_{rating} [kW]	15
Input Inductor L_{in} [uH]	514
Output Inductors L_{out} [uH]	322
Low-Voltage Capacitor C_{LV} [μF]	108
High-Voltage Capacitor C_{HV} [μF]	52
Switching Frequency of the DC-DC Converter f_{S1} [kHz]	100
Switching Frequency of the DC-AC Inverter f_{S2} [kHz]	100

3.4.2.2 Control Method

In the GaN-based BESS there are two control systems. The first controller is aimed to control the DC-DC converter. The block diagram of the DC-DC converter controller is shown in Figure 32.

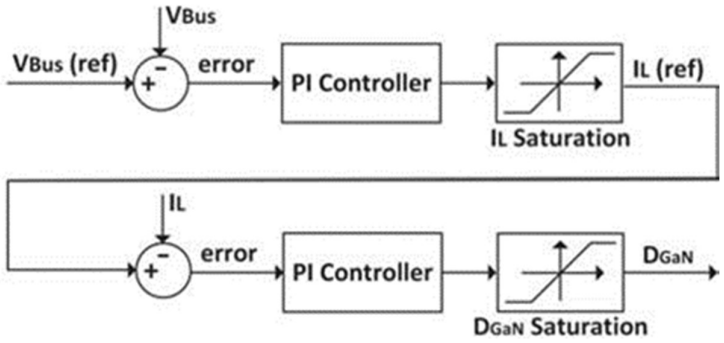

Figure 50 - Cascade PI controller of the bidirectional DC-DC converter

It is a cascade PI controller with an inner loop for current control and an outer loop for voltage control. The block in the inner loop should control the current of the input inductor L_{in} since the drain current of the HS and the LS GaN devices should not exceed the current rating

of 60 A. The PI block in the outer loop should regulate the voltage of the DC bus at the value of 800 V. To regulate the PI parameters, two steps should be followed as it is described in [63].

The second controller is supposed to control the DC-AC inverter. The injected/received power to/from the grid and the demanded power of the local load should be controlled. The reactive power of the local load should be compensated as well. To this aim, a three-phase *d-q* controller is selected for the grid-connected inverter [61]. The block diagram of the three-phase *d-q* controller is shown in Figure 33.

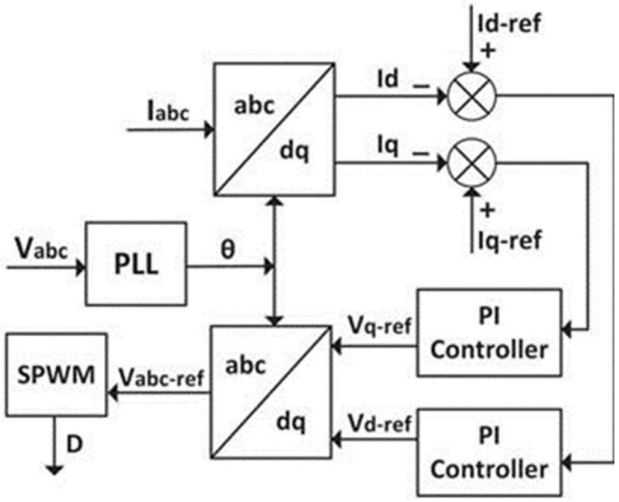

Figure 51 - Three-phase d-q controller of the grid-connected inverter

In the three-phase *d-q* controller, the output current of the inverter (I_{abc}) is transformed to the *d-q* system using:

$$I_{dq} = \begin{bmatrix} I_d \\ I_q \end{bmatrix} = T_{abc} \cdot I_{abc} = \begin{bmatrix} sin(\omega t) & sin(\omega t - 2\pi/3) & sin(\omega t + 2\pi/3) \\ cos(\omega t) & cos(\omega t - 2\pi/3) & cos(\omega t + 2\pi/3) \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \quad (5)$$

where $\omega t = 2\pi f = \theta$ is the phase of the grid voltage and f = 50 Hz is the grid frequency. θ is obtained using voltage sensors and PLL block. Then, the resulted *d-q* components are compared with the current reference *d-q* components to obtain the output current error, where the current reference *d-q* components should be calculated considering the demanded active/reactive power. Using the output current error, the PI controllers of Figure 33 can control the both active (d) and reactive (q) components of the power and produce the reference

modulation voltage in *d-q* system. Then, the reference modulation voltage in *abc* system can be obtained as follow:

$$V_{abc-ref} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = T_{dq-abc} \cdot V_{dq-} = \begin{bmatrix} sin(\omega t) & cos(\omega t) \\ sin(\omega t - 2\pi/3) & cos(\omega t - 2\pi/3) \\ sin(\omega t + 2\pi/3) & cos(\omega t + 2\pi/3) \end{bmatrix} \begin{bmatrix} V_{d-ref} \\ V_{q-ref} \end{bmatrix} \quad (6)$$

Finally, $V_{abc\text{-}ref}$ is used as the reference of the SPWM block to produce the duty cycles of the inverter's switches.

3.4.3 Simulation results

In the first part of this section OrCAD Spice is applied for a power loss comparison between the GS66516T GaN device and the SCT3030KL SiC device. The advantage of OrCAD Spice is the possibility of using precise spice model of the devices, which are released by the manufactures (GaNSystems and ROHM). To this aim, first, the DC-DC converter is simulated using series-stacked GaN devices. Then, the simulation is repeated where the series-stacked GaN devices are replaced with one SiC device for each HS and LS part of the half-bridge converter. Both simulations are performed at the power rating of 15 kW in boost mode, where the input battery voltage is 250 V and the regulated DC bus voltage is 800 V. In the case of the GaN-based converter, the gate-source voltages of $V_{GS\text{-}ON}$ = 6 V, $V_{GS\text{-}OFF}$ = -3 V and the gate resistors of $R_{G\text{-}ON}$ = 10 Ω, $R_{G\text{-}OFF}$ = 1 Ω are considered in the gate driver for the turn-ON and the turn-OFF intervals respectively [41]. In the case of the SiC-based converter, the gate-source voltages of $V_{GS\text{-}ON}$ = 20 V, $V_{GS\text{-}OFF}$ = -4V and the gate resistors of $R_{G\text{-}ON}$ = 5 Ω, $R_{G\text{-}OFF}$ = 1 Ω are considered in the gate driver for the turn-ON and the turn-OFF intervals respectively.

The V_{DS} and the I_D of one of the LS GaN devices (Figure 34) and those of the LS SiC device (Figure 35) during the turn-ON switching transition are presented at the same period of time. The V_{DS} and the I_D of one of the LS GaN devices (Figure 36) and those of the LS SiC device (Figure 37) during the turn-OFF switching transition are presented at the same period of time.

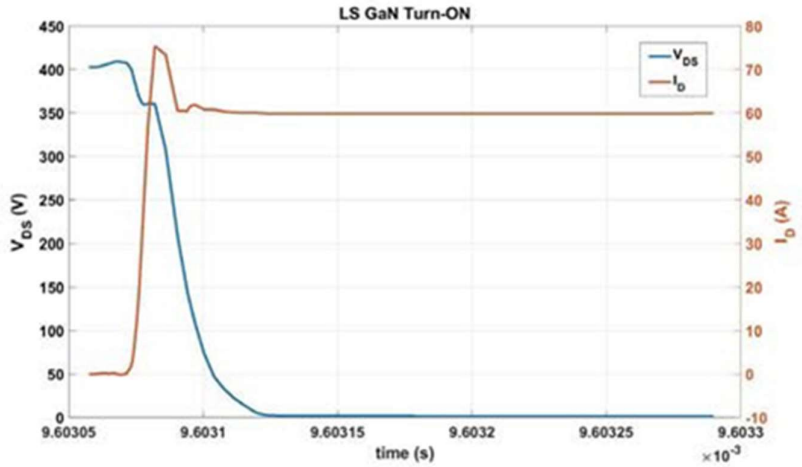

Figure 52 - Turn-ON transition of the GaN devices in the DC-DC converter

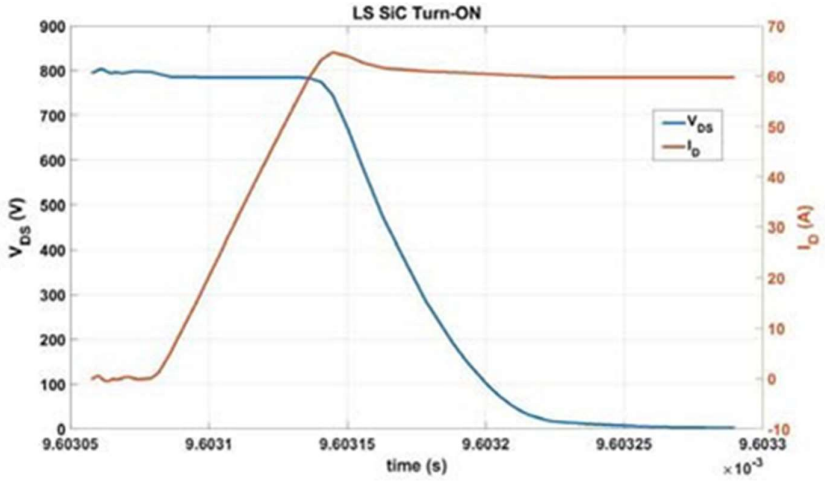

Figure 53 - Turn-ON transition of the SiC devices in the DC-DC converter

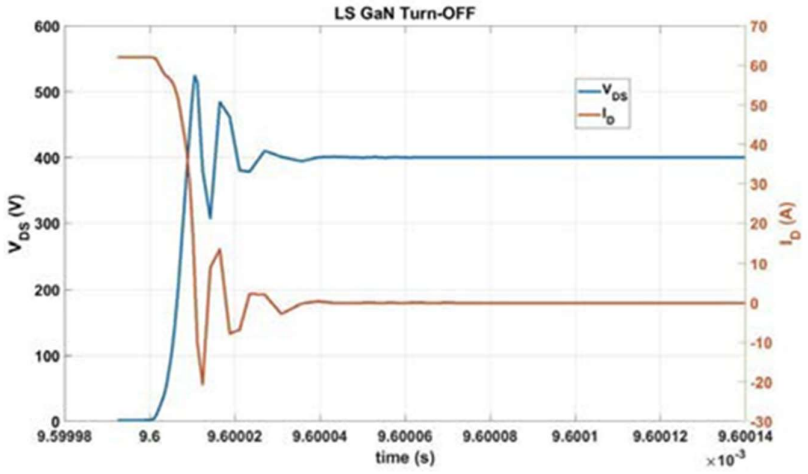

Figure 54 - Turn-OFF transition of the GaN devices in the DC-DC converter

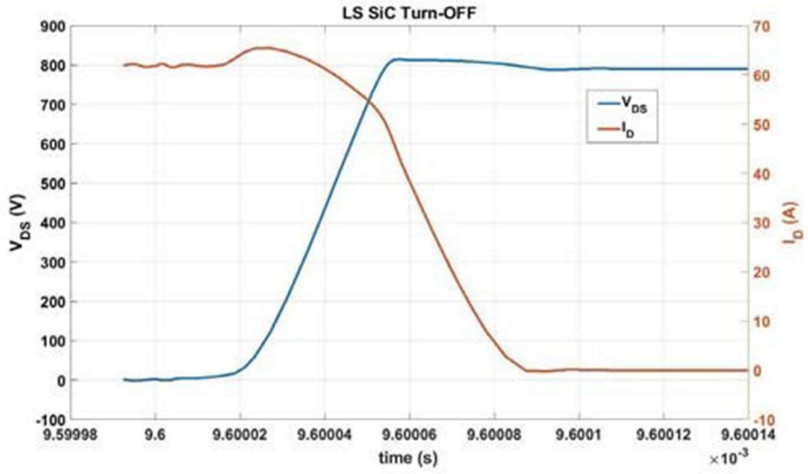

Figure 55 - Turn-OFF transition of the SiC devices in the DC-DC converter

Now, it is possible to calculate the conduction loss (P_{Cond}) and the switching loss (P_{SW}) for both cases as follow:

$$P_{Cond} = R_{DS(ON)} \cdot {I_{D(rms)}}^2 \qquad (7)$$

$$P_{SW} = V_{DS} \cdot I_D \cdot f_{s1} \cdot \frac{T_{ON} + T_{OFF}}{2} \qquad (8)$$

The values of T_{ON} and T_{OFF} (obtained from OrCAD Spice simulations) as well as the resulted P_{Cond} and P_{sw} are summarized in Table 14. Based on the simulations and the calculations, the total power losses (P_{tot}) are 246 W for the case of the GaN and 462 W for the case of the SiC. It

validates the superiority of the GaN-based DC-DC converter over the SiC-based DC-DC converter with an improvement of 47% in the term of efficiency. It is worthy to notice that the total power loss of the GaN-based DC-DC converter is lower even with its two series devices (cause higher conduction loss) and its larger amount of gate resistors (cause higher switching loss) because of the very low switching loss of the GaN device that result in the lower total power loss.

Table 15 - Power loss analysis

Parameters	GaN	SiC
T_{ON} [ns]	35 (R_{G-ON} = 10 Ω)	115 (R_{G-ON} = 5 Ω)
T_{OFF} [ns]	30 (R_{G-OFF} = 1 Ω)	55 (R_{G-OFF} = 1 Ω)
P_{Cond} [W]	90	54
P_{SW} [W]	156	408
P_{Tot} [W]	246	462

The larger gate resistors are selected since the oscillations and consequently EMI level are higher in the case of the GaN device compared to the case of the SiC device. The values of the gate resistors (high-side, low-side, turn-ON, and turn-OFF) can be also optimally selected in order to minimize the EMI level and to maximize the efficiency at the same time using a multi-objective optimization procedure presented in the previous chapters.

In the following the performance of the controllers are evaluated. To this aim, the proposed BESS of Figure 31 is simulated in MATLAB Simulink.

In this simulation, for t = 0 to 0.2 seconds, the BESS is supposed to provide the demanded active power of the local load and to inject power to the AC grid. In this period of time, the BESS works in boost mode and at the power rating of 15 kW. It provides 7.5 kW to the local load and injects 7.5 kW to the AC grid (Figure. 40, t = [0-0.2] s). The output AC voltage (V_{abc}) and the output AC current (I_{abc}) have the same phase (Figure 38 and Figure 39, t = [0-0.2] s).

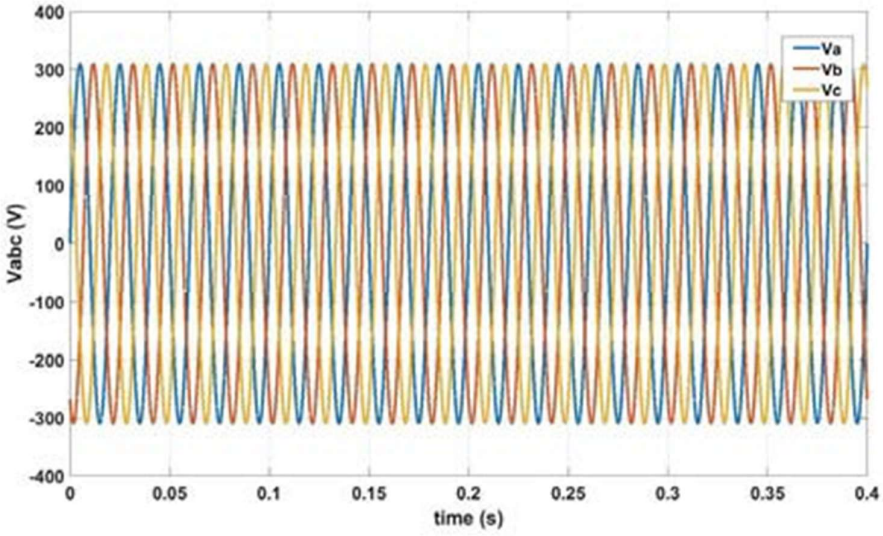

Figure 56 - Three-phase output voltage of the grid-connected inverter

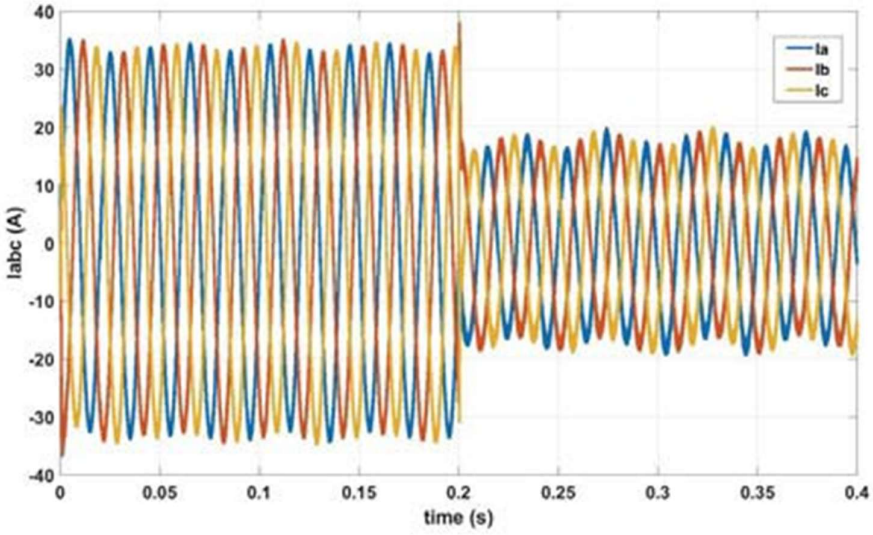

Figure 57 - Three-phase output current of the grid-connected inverter

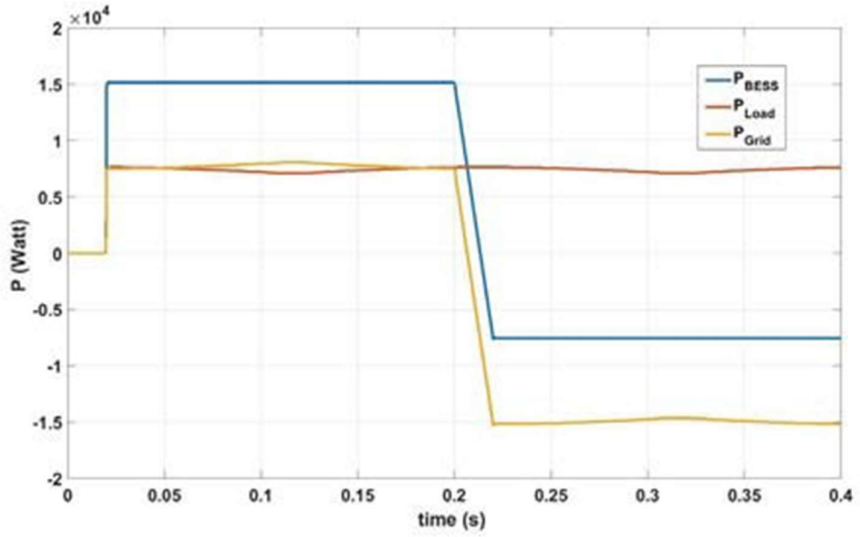

Figure 58 - Active power of the BESS, of the load, and of the grid

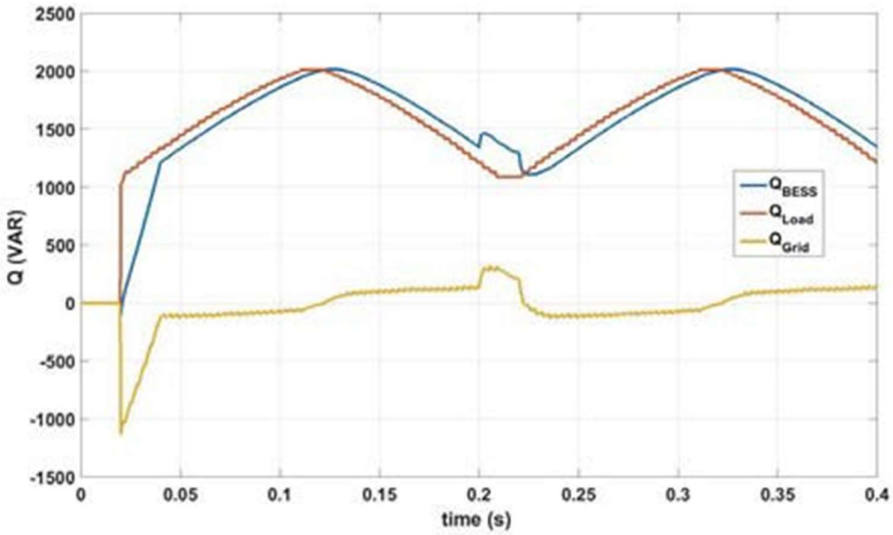

Figure 59 - Reactive power of the BESS, of the load, and of the grid

The other part of the simulation is aimed to evaluate the buck mode operation of the BESS. For t = 0.2 to 0.4 seconds, the AC grid is supposed to provide the demanded active power of the local load and to charge the battery of the BESS. In this period of time, the BESS works in buck mode and at the power rating of 7.5 kW. The AC grid provides 7.5 kW to the local load and deliver 7.5 kW to the BESS (Figure. 40, t = [0.2-0.4] s). The output AC voltage (V_{abc}) and the output AC current (I_{abc}) have a phase shift of 180° (Figure 38 and Figure 39, t = [0.2-0.4] s).

For whole simulation time period (t = [0 0.4] s), the BESS is supposed to compensate the demanded reactive power of the local load. In Figure. 41, the BESS is tracking the variable demanded reactive power of the local load. In this way, the injected/received reactive power of the AC grid is supposed to be zero. As it is discussed before, the reactive power of the BESS is limited to a power factor of PF = 0.7 which is satisfactory for the residential applications.

Figure 42 also shows the regulated DC bus voltage (V_{Bus}) and the input inductor current (I_L). V_{Bus} is regulated to 800 V during both boost and buck operation modes of the BESS. During the boost mode, when the battery provides the demanded power of the local load and injects power to the AC grid, the voltage of the DC bus is decreasing slightly. During the buck mode, when the battery receives power from the AC grid, the voltage of the DC bus is increasing slightly. I_L follows the d-q reference currents without harmful overshoots to control both active and reactive powers as well.

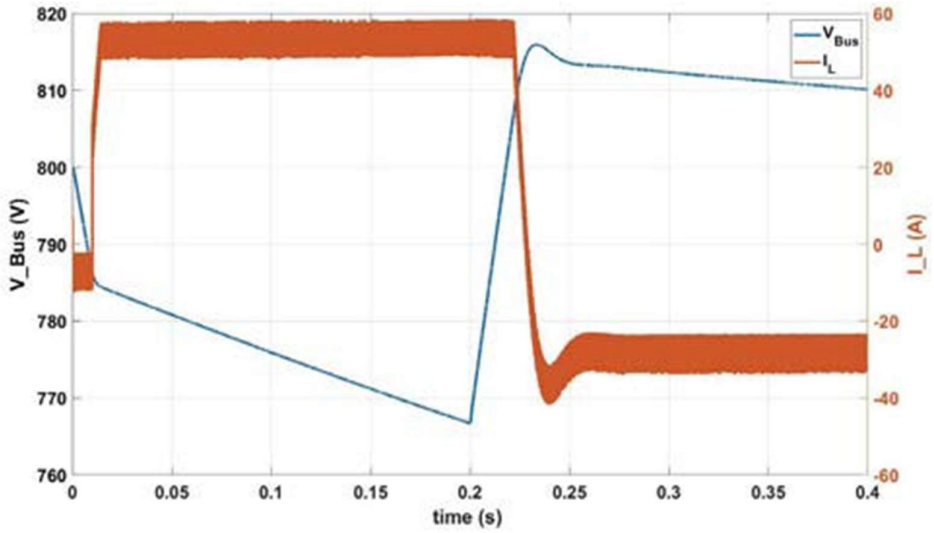

Figure 60 - Regulated DC bus voltage V_{Bus} and input inductor current I_L

3.4.4 Conclusion

A GaN-based BESS is proposed in this work for three-phase residential applications with a power rating of 15 kW. For the power stage design, due to the limited voltage rating of the GaN device (650 V), series-stacked devices are used in the DC- DC converter and 3L NPC

topology is chosen for the DC-AC inverter. The controller design (cascade PI controller for the bidirectional DC-DC converter and three-phase *d-q* controller for the DC-AC grid-connected inverter) is presented. A power loss analysis is performed to compare the GaN device with a possible alternative SiC device (voltage rating of 1200 V) using OrCAD Spice to validate the higher efficiency of the GaN device. Moreover, the MATLAB SIMULINK simulation results present the satisfactory performance of the controllers in both boost and buck modes in the term of the injecting/receiving power tracking, the reactive power compensation, the DC bus voltage regulation, and the input inductor current overshoot elimination.

4. CONCLUSIONS

My research activity aims to understand and investigate the importance of gate drive parameters in a wide band gap material-based DC-DC converters for high power applications. An important figure of merit of the semiconductor devices is the product of drain-source ON resistance and the gate charge. A lower value of drain-source results in lower conduction loss, while lower value of gate charge leads to a faster switching transient and lower switching loss. The faster switching transient of wide band gap devices provides higher efficiency, but sharp voltage/current transients cause high frequency noises and deteriorate the electromagnetic compatibility performance of the converter. Design of gate drivers parameters becomes a challenging task for wide band gap power electronic devices that operate at high switching speeds. Therefore, my thesis aims to investigate the values of these parameters using a multi-objective optimization method to optimize efficiency and electromagnetic interference. The objective functions of the optimization problem are obtained numerically by means of the experimental tests.

In this light, we present an optimum gate resistor design approach for two wide band gap material based (SiC, GaN) DC-DC converters in the application of Electric Vehicles. Furthermore, the current source gate drivers for GaN devices in the hard-switched medium-to-high voltage/power applications such as an electric vehicle (EV) and battery energy storage system (BESS) is investigated in my thesis work.

4.1 Optimization of the Gate Driver Parameters in a SiC-Based DC-DC Converter

In the proposed design, the independent variables of the objective functions, one gate resistor pair from all four High Side/Low Side ON/OFF gate resistors in the half-bridge configuration, are selected on the base of the Miller effect crosstalk suppression. The optimum values of the gate resistors are achieved by solving the optimization problem and plotting the Pareto front. The effectiveness of the proposed gate resistor design is validated at low voltage/power for the rating values to evade putting high stresses on the implemented

converter. Both the efficiency and EMI level improvements are validated using the experimental results.

4.2 Optimization of the Gate Driver Parameters in a GaN-Based DC-DC Converter

The change of voltage/current per unit time (slew rate) of the GaN-based electronic device in a half-bridge configuration of a DC-DC converter is studied. The slew rate control is achieved using a post-prototyping multi-objective optimization method to parameterize the gate driver resistors. The objective functions of the optimization problem considered in this case are the efficiency of the converter and the near-field EMI of the GaN device. The optimum design point is obtained using experimental measurements and mathematical calculations. Compared to the conventional gate driver resistor design, the experimental results highlighted the improvement in both efficiency and EMI level.

4.3 GaN e-HEMT in Hard-Switching High Power Applications

A power loss analysis is performed to compare the conventional voltage source gate driver to the CSD using OrCAD Spice for the GaN device. The configuration and the operation of a zero initial inductor current CSD, a low side non-zero initial inductor current CSD, and a half-bridge non-zero initial current CSD are presented and compared. The power loss analysis confirms the faster switching time, the lower switching loss, the lower ON drain-source resistance, and the lower conduction loss of the CSD compared to those of the VSD. A total device power loss improvement of 28 % in the case of CSD is shown from the simulation results.

4.4 A GaN-Based Battery Energy Storage System for Three-Phase Residential Application

A GaN-based BESS is proposed for three-phase residential applications with a power rating of 15 kW. DC-DC converter and 3L NPC topology are chosen for the DC-AC inverter for the power stage design. The controller design comprises a cascade PI controller for the

bidirectional DC-DC converter, and a three-phase *d-q* controller for the DC-AC grid-connected inverter is presented. A power loss analysis validates the higher efficiency of the GaN device and compares the GaN device with a possible alternative SiC device (voltage rating of 1200 V) using OrCAD Spice. The satisfactory performance of the controllers in both boost and buck modes in terms of the injecting/receiving power tracking, the reactive power compensation, the DC bus voltage regulation, and the input inductor current overshoot elimination is shown from simulation results using the MATLAB SIMULINK.

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