Peculiar Failure Mechanisms in GaN Power Transistors

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Abstract – Commercial GaN power amplifiers for RF applications, made of a pair of discrete transistors for operation in Doherty configuration, failed during the HAST tests. Failure Analysis pointed out a layout-specific issue related to thermal expansion at the level of the field plates. Anyway, the search for initial degradation stages using Optical Beam Induced Resistance Change and Photon Emission Microscopy revealed a subtle second mechanism, involving Ga interdiffusion into the gate metal lines, coming from hollow pipes in GaN. Both mechanisms are discussed.

1. Introduction

The pervasive employment of GaN on SiC Power Transistors in several fields, ranging from power management to wireless telecommunications, from radars up to security applications [1], followed the availability of commercial devices since 2005. Entering the market stated the achievement of a technology mature enough to pass the qualification requirements for electronics, that is the demonstration of Reliability levels suitable for the required mission profiles, even in harsh environments [2]. The continuous technological evolution of such devices along the past decade prompted a growing parallel research on Reliability, as recently summarized by Zanoni [3]. The key challenging point is the large amount of novelty introduced by GaN devices: higher current, voltage and temperature limits, and then higher electrical and thermal stresses; a complex vertical epitaxial structure, never perfectly lattice matched, an uncommon high density of native defects; the strong piezoelectricity of GaN itself; the introduction of a special element as a Field Plate (FP) to improve the breakdown figures [4,5,6]. Even one single element of that list can defy the standard protocols for reliability assessment as those developed for Silicon devices. Failure Physics required to investigate new failure mechanisms, as the Converse Piezoelectric Effect [7] or electrochemical phenomena specific of GaN [8], or the physical cause of time-dependent phenomena whose effects (failure modes) recall the breakdown kinetics in MOSFETs [9].

Qualification tests have been accordingly extended, in order to include stress levels not usual for other devices, in term of temperature, current and voltage, and keeping the standard environmental tests as HAST (Highly Accelerated Stress Test) and Temperature, Humidity Bias (THB) mostly unchanged.

Within that framework, each new discovered mechanism that can be specifically attributed to the GaN HEMT materials and technology is a contribution to the improvement of their Reliability.

This paper deals with a Failure Analysis case history of a family of commercial GaN on SiC Power Amplifiers for RF applications during an off-state biased HAST, having that family passed all other kinds of dry tests, including High Temperature Operating Life (HTOL) in both the on and the off states, and the RF tests.

The analysis started with the demonstration of a rather trivial problem of strong Gate-Source leakage due to dielectric cracking, whose specificity for GaN HEMTs was only given by the direct involvement of the Field Plate. It seemed a result worth of just a technical report, useful for some adjustment of the passivation process.

Unexpectedly, the following search for the nucleation point of the failures revealed a completely different interaction mechanism, that is GaN-specific under several aspects, and has never been reported before, at Authors' knowledge.

The paper aims to give the first experimental evidence for that mechanism, describing step by step the chain of experiments and interpretations that brought to its discovery.

The first section will then describe the devices, the HAST and THB test conditions and the failures under the HAST and THB tests and their first analysis, driven by direct inspection at the Optical Microscope (OM) or at the Scanning Electron Microscope (SEM), followed in several cases by cross-sectional SEM after FIB (Focused Ion Beam) milling of the damaged regions.

The protocol changed after repeating the environmental tests at much weaker stress, which excluded all mechanism known to require high current or high voltages, or extreme temperatures. Failures accumulated again, without any evident damage directly distinguishable at the OM or the SEM. This moved to replace OM and SEM by a set of Photon Emission Microscopy (PEM) [10], Optical Beam Induced Resistance Change (OBIRCH) [11] and TIVA [12] analyses. Several critical points have then be revealed along the Gate fingers, where FIB/SEM was applied again. Here in two different devices, both failed because of the Source-Field Plate short circuit, the weakest PEM spots were not connected to the main failure mechanism, but to an extended conducting vertical path between a Gate finger and the semiconductor. Droplets of liquid Gallium give evidence of GaN dissolution along a vertical pipe, and Ga interdiffusion inside the Gate gold metal characterize the device at the PEM emission spot.

The final discussion will point out the scarce relationship of the new mechanism with humidity, and its probable occurrence

2. Devices

The devices are commercial GaN on SiC Power Transistors. Each device was made (

*Fig.*1) by two GaN on SiC chips of the same technology and different power, mounted in a same package for power amplification in Doherty configuration [13].

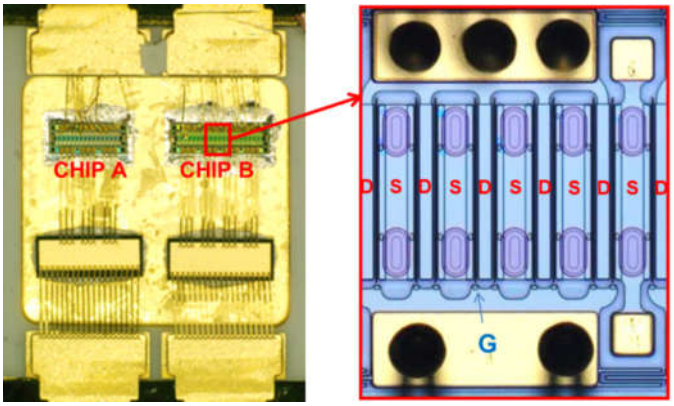

Fig.1. The two chips A and B mounted in the package, and a detail of the visible interdigitated Source (S), Drain (D) and Gate (G) structure at the optical microscope. Sources are connected to the common backside of the chip through the visible elliptic vias.

The vertical structure of each of the interdigitated transistor elements shows (fig.2) the presence of a Field Plate (FP), connected to the Source by two thin bridges. The role of the FP is to improve the breakdown performances of the device, by a simple electrostatic effect [4,5,6]. It is designed to bring a ground voltage reference close to the channel surface between Gate and Drain.

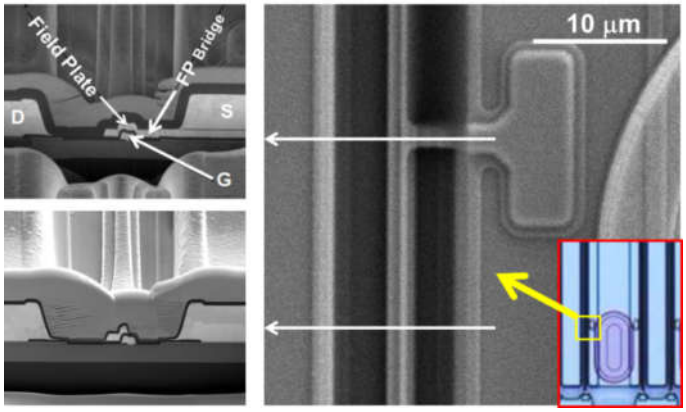

Fig.2. Planar view (right side) and two cross-sections of the transistor structure, corresponding to the arrowed lines, at the same magnification. The Field Plate is shown, partially overlapped with the gate, and connected to the Source by means of a bridging strap.

The bare chips are manufactured by one Company, and are assembled and mounted in a non-hermetic ceramic package by another Company, who also was in charge of performing the qualification tests required by the Customer.

3. Tests and device modifications

3.1 Initial HAST and THB

Devices underwent a complete qualification campaign, passing all test but the environmental ones: HAST (Highly Accelerated Stress Test) and Temperature, Humidity Bias (THB) performed according with the JEDEC JESD22-A110 and JEDEC JESD22-A101 standards, respectively. In particular, for HAST the environmental conditions were 130°C with Vapor Pressure 230kPa, while for THB the temperature was fixed at 85°C and the relative humidity at 85%RH.

Both tests require DC biasing of the devices, that for the GaN transitors under test corresponds to V_{DS}=55V, V_{GS}=-8V (fig.3). In this configuration, the channel is closed, and no current flows across any part of a regularly working device.

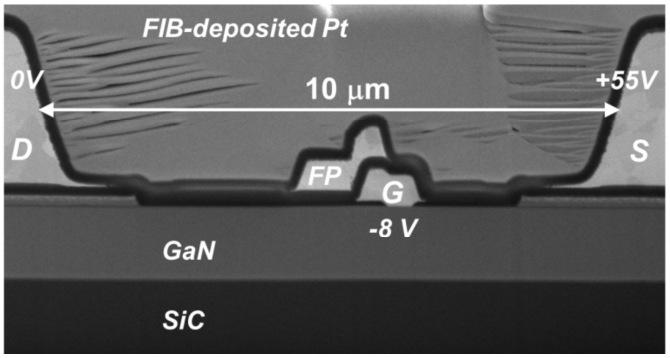

Fig.3. Enlarged view of one of the cross-sections in fig.3, with the bias conditions for the HAST and THB tests.

In fig.3, it is worth noticing that the maximum field occurs between Gate and Field Plate and is in the order of 300 kV/cm.

The results of the first tests have been severe: 100% failures within 10 hours for HAST, while during THB failures started to occur after 200 hours.

The failure modes were a resistive short circuit between gate and source, with a measured resistance ranging from few tens to some hundreds of a Ohm.

The observation of the failed devices, first at the OM, and then at the SEM (fig.4) showed an extended damage of the overlaying FP and Gate metals, that will be discussed in the next session.

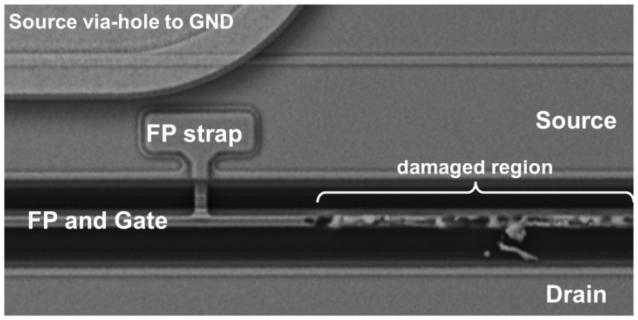

Fig.4. A typical damage along the gate finger, after the HAST test..

3.2 Device modification

The evident role of humidity in causing failures prompted the vendor to improve both the sealing glue of the ceramic package and the passivation of the chips (fig.5).

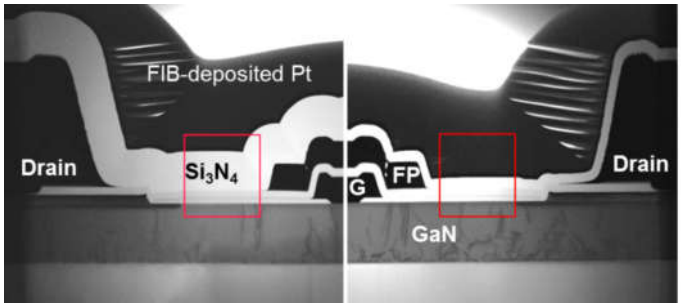

Fig.5. Specular TEM images of the Gate-Drain region of two devices with different thickness of the Si_3N_4 passivation layer (boxed).

Despite a relevant improvement in device survival, none of the corrective actions was able to solve the problem. Glue and passivation have been modified three more times. After the last adjustment, a lot of 177 devices passed the HAST, surviving 96 hours. But, allowing the test to continue, two devices failed after about 100 additional hours, and two more devices, that passed HAST, failed at a supplementary THB test. Monitoring the gate leakage current at the nominal bias during the HAST continuation, revealed that failures are not sudden, but follow gradual kinetics (fig.6). The corrective actions only delayed the timing of the failure mechanism, but not solved the problem.

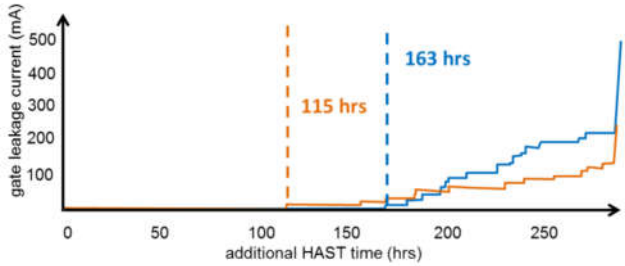

Fig.6. Gate leakage current for two devices under HAST conditions after additional test hours beyond the required 96 hours.

3.3 The test board

Within this framework, it is useful to spend some words on the biasing circuitry used for HAST and THB. Both tests apply DC voltage to gate and drain. Each chip in each device was driven by two separate circuits, one for biasing and monitoring the Drain, and one for the Gate.

The Drain controller includes a LED and a fuse, calibrated at 500 mA. The current limit is inserted because the channel is normally open and, in case of accidental loss of control of even a single gate finger, a huge current could flow between drain and source.

The gate controller, on the other hand, has been designed for keeping the gate constantly biased at -8 V (fig.7), but in case of leakage between Gate and Ground (dashed resistor) the gate voltage can become less negative, and then some current can flow across the channel, only limited by the fuse on the Drain controller. This effect introduces an uncontrolled variable to the problem of explaining the damage as in fig.4: the contribution of the uncontrolled channel current to the thermal effects associated with the gate-source short circuit.

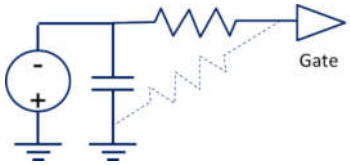

Fig.7. The (simplified) gate driving circuit for the HAST and THB tests (bold lines) and the parasitic path between gate and ground (dashed line).

3.4 Partially biased THB

In order to clarify the possible role of the drain current in the observed phenomena, and looking for the initial stages of the failures, a new set of moderate environmental test was planned at partial bias. More specifically, the test was performed keeping the humidity and temperature of the THB test (85%RH/85°C), the gate was reversely biased, V_{GS}=-8V, and both source and drain were grounded, V_{DS}=0.

The test was planned for a duration of 96 hrs on four sets of 5 devices each, differing for two different passivation thickness and for entering the test with the package sealed or open. A current limit of 10 mA was set to the gate current.

Two devices, both of the weakest group (thinner passivation, open package) failed, showing evident gate damage as in fig.5. It was then decided to perform a second identical test on a new set of that specimens, setting the current limit to 1 mA. The three survivors of the first experiment were also added to the new test. A summary of the results is given in Table I, where the label "fail" indicates a gate current reaching the compliance (10 mA or 1 mA, for the first and the second test, respectively).

TABLE I.
Summary of the results of the partially biased THB tests

	Device #	I Test	II Test	evidence
I_G limit 10 mA	1	pass	fail	gate damage
	2	pass	pass	*not observed*
	3	pass	unstable	*not observed*
	4	fail		gate damage
	5	fail		gate damage
I_G limit 1 mA	6		fail	none
	7		high leak	none
	8		pass	*not observed*
	9		pass	*not observed*
	10		pass	*not observed*

The second test then seemed to achieve the goal of causing the FP-Gate short circuit without inducing an overcurrent. The physical analysis was accordingly planned on failed devices at different degrees of visible damage, aiming to reveal the nucleation point of the failure mechanism.

4. Physical Analysis

4.1 Techniques

Leaky points were identified at a glance, by simple inspection at the OM and the SEM, of the devices failed during the first test, where the gate current was allowed to reach 10 mA, and then confirmed at the SEM (Fig.8 to be compared with fig.4).

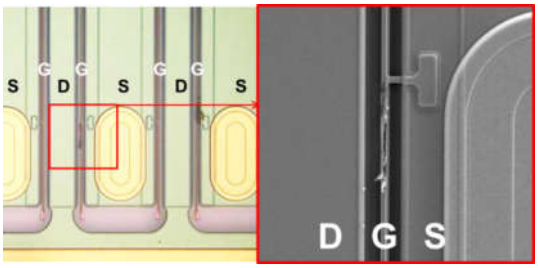

Fig.8. a) Optical image and b) SEM imagnification of a damaged region in a device failed during the partially biased 85°C/85%RH test.

At the damaged points, vertical analysis was performed by sequential slicing by means of FIB milling, up to reveal the contact point between the Gte and the Field Plate metal lines (Fig.9)

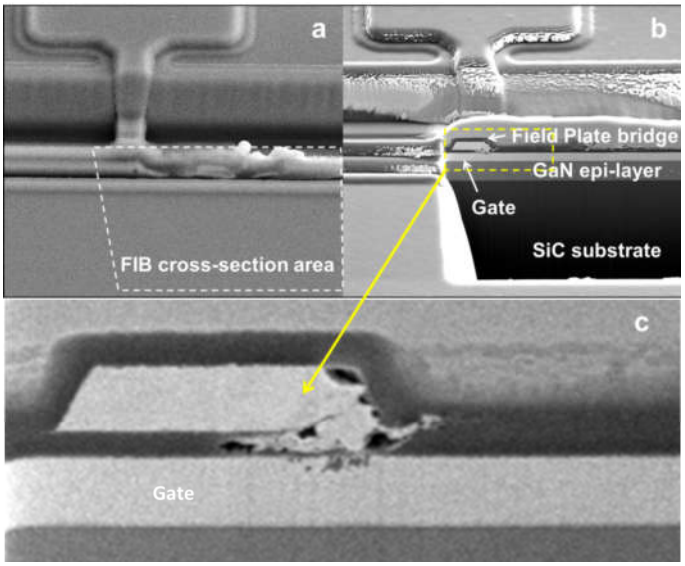

Fig.9 a) Surface view and b) FIB cross-section of the damaged region in fig.9, revealing a contact point between metal lines c).

When weaker test produced electrical shorts (Table I) without evidence at the OM and SEM, the analysis protocol was refined, including PEM, OBIRCH and TIVA inspection. The goal was to localize small contact points between metal and semiconductor (PEM) or between metal lines (OBIRCH and TIVA), or both.

Sequential FIB slicing and SEM observation was then kept as the final step.

4.2. Mechanisms

4.2.1 Dielectring cracking

The extended thermal damage in fig. 4,8 and 9 should be considered a side effects of the root cause: the short circuit between Gate and Field Plate, whose evidence is in the circled part of fig.9b. The point is to understand the reason for that short circuit.

Several clues were found: the Field Plate displays a steep step when climbing over the gate. Two phenomena occur at that step: *i*) the step coverage is not uniform, resulting in metal with relevant porosity (fig.10); *ii*) the upper passivation easily cracks locally, where a cusp forms in coverage of the steepest step (fig.11).

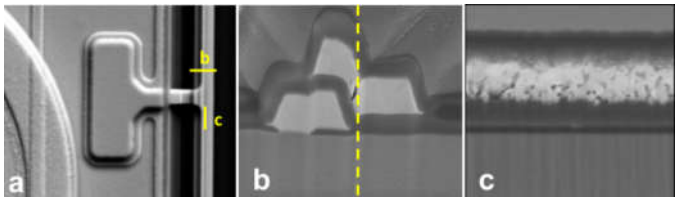

Fig.10 a) Plan view, b) cross-section and c) longitudinal cross section of a FP-Gate structure showing the porosity of FP at the step.

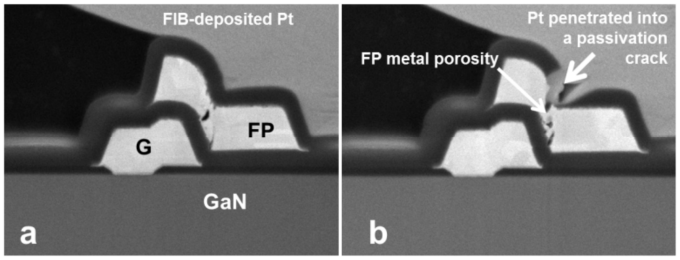

Fig.11 a) reference cross-section and b) evidence for passivation crack at the FP steps.

Passivation cracks are not a surprise in such devices. Fig.12 shows the discoloration visible at the optical microscope in devices after HAST or THB, while fig.13 correlates discoloration with surface cracks. None of the discoloured areas was present before the tests.

The systematic occurrence of delamination at the curved edges of the vias (that are metal pillars passing through the whole chip thickness) and at the pads of the Field Plate on the Source large finger strongly addresses the origin of fractures towards thermomechanical stresses.

An independent analysis, at the beginning of the qualification campaign, proposed the reverse piezoelectric effect in GaN as the leading stress able to crack the passivation.

The hypothesis is questionable in itself, because it should be demonstrated how a mechanical stress inside the semiconductor can focus on the top of the passivation, as reported in fig. 13. Anyway, switching off the Drain voltage during the test, only leaves the -8 V bias applied to the Gate, which seems a too weak stress to cause any damage in few hours at 85°C [7].

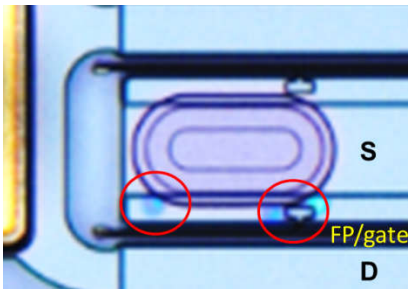

Fig.12 Delamination of the passivation layer, revealed at the optical microscope by discoloration at the circled areas.

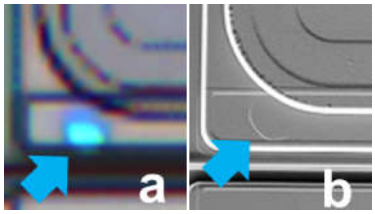

Fig.13 Optical (a) and SEM (b) plan views of a delaminated passivation point (arrowed).

Going back to fig.10 and 11, they tell that passivation cracks and metal porosity jointly build direct access to the maximum field region between Field Plate and Gate.

Two further elements supported the growing belief that the cause of the Gate-Source short circuits was caused by humidity penetration into the interspace between Gate and Field Plate: the occurrence of anodic gold corrosion and the intensification of the mechanical damage after modifying the layout of the Field Plates.

Fig.14 shows the optical image of the location and a detail of a leakage point of a device failed during the first HAST tests. The point stands outside the GaN area, at the end of both gate and FP lines. This evidence should be sufficient for excluding GaN-specific mechanisms from the possible explanations of the observed failures.

Anyway, the interesting point is the FIB cross-section in fig.14c. It is evident as the anode of the metal couple, that is the Field Plate, is completely corroded, while the Gate electrode is nearly intact. This image should be compared with images of nearly 40 years ago [14] dealing with Anodic Gold corrosion in microelectronics. The key point is that in presence of humidity, temperature and a high electric field, as that between Gate and FP at the given conditions, gold can react with water and create a brittle hydroxide that grows in volume, cracks the surrounding dielectrics and still preserves conductivity high enough to create resistive short circuits with the neighbouring metal lines.

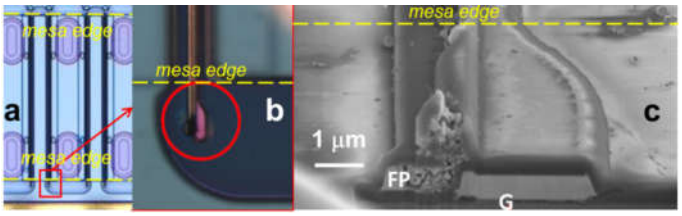

Fig.14.Location (a) and detail (b) of a leakage spot, outside the GaN area (the dashed lines indicate the boundaries of the mesa region). In (c) the FIB cross section of the leaky point shows the corrosion of the anode of the Gate-FP pair.

The second additional element supporting the thermomechanical hypothesis comes from the results of another HAST performed on a further modified family of devices. The new family (fig.15) had an increased number of straps bridging the FP to the Source metallization.

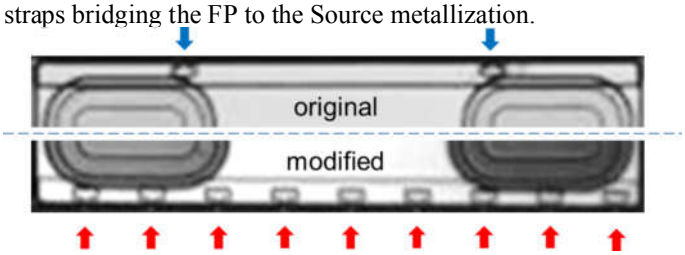

Fig.15. The modified layout of the devices of the last HAST tests. The number of bridging straps (arrowed) from FP to Source has been increased from 2 to 9 per finger.

The resulting effect has been that failures occur as in the previous tests, but the mechanical damage is much more distributed, which causes many more contact points (fig.16), not visible at the OM or at the SEM, but revealed by OBIRCH

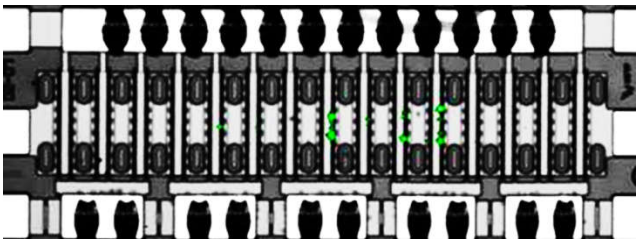

Fig.16 Optical Beam Induced Resistance Change (OBIRCH) of the leakage points (green spots) in devices with modified layout as in fig.15, after a HAST test.

Also the local intensity of the damage results intensified (fig.17), with the dielectric not only cracked but also delaminated from the semiconductor surface.

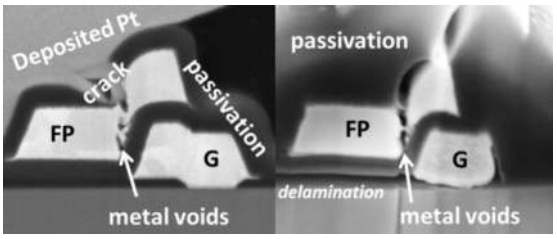

Fig. 17. Transversal FIB cross-section of a Gate/FP structure in two devices, showing metal voiding at FP and different levels of dielectric cracks. On the left, a device with the original layout; on the right, a device with the modified one.

At this point, the analysis seemed nearly concluded. The hypothesis was that thermomechanical stresses during the tests caused local fractures in the steep steps of the passivation covering the Field Plates, in particular, close to the bridging straps. The metal porosity, intrinsic of the manufacturing process of the FP itself, would then drive moisture in the maximum field region, where or other thermomechanical cracks, or the expansion of corrosion products leads FP and Gate to touch.

4.2.2 Ga/Au interdiffusion

In order to conclude the previous analysis, it was only necessary to find a leakage point not corresponding to any visible effect of overcurrent, and possibly with the minimum mechanical damage. In summary, it was necessary to find something putting together a contact point between metals as in in fig.9, a porous step in the Field Plate as in fig.10 and a crack in the upper passivation as in fig.11.

Two candidates were found in the two devices #6 and #7 of Table I.

Fig.18 shows indeed the intact appearance of one of the two devices at that same point where Photon Emission Microscopy locates a leakage spot. It was then decided to try a sequential FIB cross-section, one transversal and one parallel to the gate length.

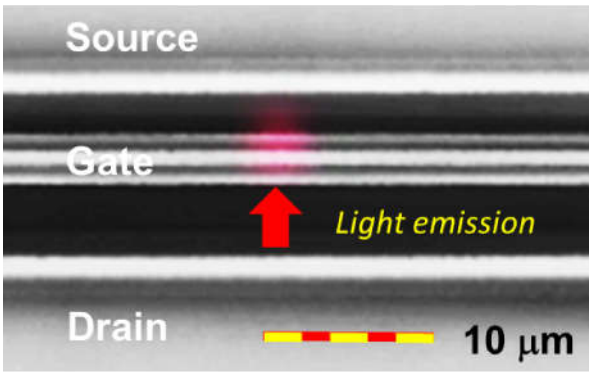

Fig.18. Optical plan view of the GaN power transistor under investigation, and the detected light emission spot.

This is the point where the history deviates from expectations. The first result was disconcerting: a complete sequence of longitudinal cuts across the overlap region of FP and gate at the leakage point did not show anything abnormal (fig.19 a,b). It was then decided to simply ultimate the sequence, in order to analyse also the final edge of the gate, not covered by the Field Plate. Here, on the edge (fig.19c), a strong contrast appeared in the Au layer, that was demonstrated to be rich of Gallium by Energy Dispersive x-ray spectroscopy at the SEM (fig.20).

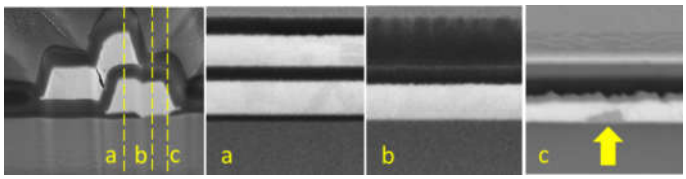

Fig.19 Sequence of longitudinal cross sections (located for reference on a transversal cross section o the leftmost image) of a leaky point not corresponding to FP-Gate physical contact..

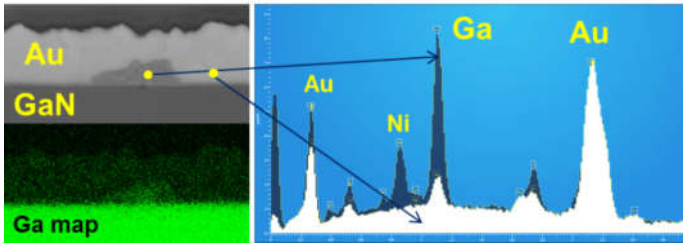

Fig.20 EDS analysis of the contrast area of fig.19c, that is identified in a Ga rich region inside the gate Au metal.

Even more intriguing, the cross section sequence, perpendicular to the gate length, at the second PEM emission point, fig.21 and fig. 22, showed a complex structure, where Ga/Au interdiffusion in Gate is vertically aligned with a hollow vertical pipe, where even a droplet of liquid Ga forms during the observation at the SEM after FIB milling.

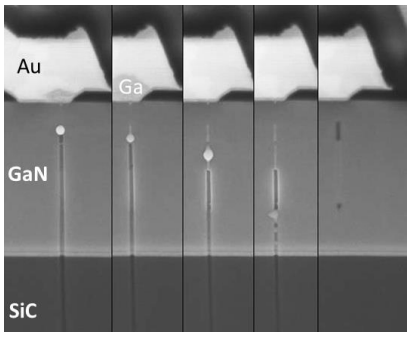

Fig.21 Sequence of sectioning planes across the second PEM emission spot

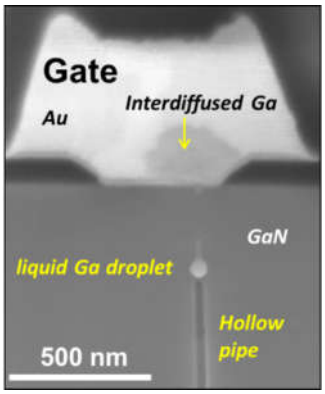

Fig.22. Enlarged view of one of the cross sections in fig.21

The Ga liquid droplet is not rare in SEM imaging of GaN or also GaAs devices, at the non-polished sides of the FIB trenches. It simply indicates that, at that points, the GaN or GaAs structure has been so damaged that the electron beam energy is sufficient to lead the nearly unbound Ga to liquefy.

In a polished surface as in fig. 21 and 22,the droplet points out the intrinsic local dissolution of GaN along the pipe.

Discussion and Conclusions

The relevance of the two mechanisms is significantly different.

The first is essentially a thermomechanical issue, strictly related to several peculiarities in the FP/Gate system: a) the steep step of the FP and its poor coverage, leading to voids not relevant for the electrostatic performances of that element, but essential for leading moisture down to the FP/Gate gap; b) the known fragility of the SiN_x dielectric under mechanical stress; c) the transversal expansion stress exerted by the FP bridges onto the FP/Gate structure. The many attempts to mitigate the problem by changing the thickness of the passivation look inadequate, and a different design of the FP/Gate element should be considered.

It was said that the devices have been manufactured by one Company and packaged and distributed by a second one. It is quite possible that such devices passed all tests, including THB and even HAST at level of bare chips, and then fail because of improper packaging. The check of that hypothesis is beyond the possible action range of the Authors. Anyway, the corrective action should focus on the thermomechanical criticalities at the vias and at the FP steps, rather than on passivation.

The second mechanism is much more subtle, and potentially lethal only in long term operation. For the moment it has only been found in devices where other areas, involved by FP-Gate leakage, completely masked the electrical signatures of the new mechanism.

The existence of an electric path between Gate and channel, if not revealed by the electrical measurements because of the dominating leakage due to the FP/Gate short, is demonstrated by the PEM images, and then a current flows along that path when the gate is biased.

About the pipes, their presence in GaN is known, even if their formation mechanism is not completely clear, and they are recognized as open core screw dislocations [15-20].

The incomplete bonds on the walls of the pipe leave some Ga atoms nearly unbound, up to the point that the energy of the electron or the ion beam is sufficient to liquefy their clusters. This indicates that in normal operation, when the temperature rises because of power dissipation, or during tests as HAST and THB, it is possible to have some locally liquid Ga encapsulated along the hollow pipes. The occurrence of such pipes anywhere else than under a gate should be of minor relevance. On the contrary, cases as in Fig.19 to 22 indicate that only the Nickel layer of the Ni/Au metal stack of Gate interposes to prevent Ga from inter-diffusing inside Au. In case of barrier crack, nothing could avoid the formation of a shunting path that is likely to evolve, during operating life, slowly.

The probability that a hollow pipe stands just below a weak Ni barrier looks low at a glance. Anyway, the phenomenon was observed in all devices where the analysis has been performed, at the faint light emission spots. This suggests that the pipe itself is sufficient to lead the Ni barrier to break. Hypotheses to be investigated can consider the role of hydrostatic pressure on liquid Ga, possibly coupled with that piezoelectric effect during real operating life. A fascinating suggestion comes from a completely different kind of devices, GaN laser diodes, where it has been recently demonstrated [21, 22] that their catastrophic failure under overcurrent stress is caused by GaN dissociation, with gaseous Nitrogen ejecting liquid Gallium from the core of the device at high speed.

Finally, it should be considered that pipes, even if present in fresh devices, would not be detected by the current screening protocols, but could be revealed by PEM inspection.

To conclude, we have reported on two mechanisms that, under different point of view, are peculiar for GaN Power HEMTs.

Both deal with topics that have been extensively studied in the mentioned literature, as the role of Field Plate or the formation of hollow pipes. Anyway, the thermal expansion at the Field Plate as the cause of a thermomechanical fatal stress, when combined with humidity, has never been pointed out as a Failure Mechanism. This belief is supported by the many corrective efforts spent by the Manufacturer pointing towards passivation issues rather towards the FP design.

Similarly, the possibility of Ga diffusion into the Gate metal from hollow pipes, with the creation of a leakage path, is here shown as a potential long term risk, whose kinetics, activation energy and screening protocols should be investigated.

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