# Current Distortion Mitigation in Grid-Connected Three Phase NPC Converter in Presence of Grid Harmonic Voltage Pollution

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***Abstract*—The present paper reports the design of a grid-connected three-phase neutral point clamped (NPC) converter. Specifically, the voltage balancing, the LCL filter and the control system have been modelled and experimentally validated. Finally, the effect of the grid voltage harmonics on the NPC output currents was investigated, taking into account the voltage distortion defined according to the quality standard. The mitigation of the current distortions induced by the fifth and the seventh voltage harmonics was carried out using a notch filter compensator that has been specifically designed for this purpose. The mitigation of the proposed harmonic compensator under different operating conditions characterised by the presence of these voltage harmonics has been evaluated by means of an experimental test bench.**

***Index Terms*—Grid connected converter, NPC Converter, power quality, harmonic compensation.**

## I. Introduction

The deployment of Renewable Energy Sources (RES) is leading the transformation of the power system. The expected energy scenario requires the implementation of innovative management models that guide the ongoing transition of power system from a centralized to a distributed configuration. In this context, Voltage Source Converters (VSCs), and in particular those dedicated to grid-connection of RES and Energy Storage Systems (ESSs), play a key role. A survey of the relevant VSC literature reveals the predominance of Pulse Width Modulation (PWM) converters characterised by the use of LCL filters [1]. This is due to the effective attenuation of switching harmonics achievable [2]. However, the integration of LCL filters within grid-connected converters results in a more complex digital current control synthesis, necessitating particular attention to ensure compliance with the stability condition [3], [4]. Specifically, VSCs that rely on their output current as feedback for digital control (i.e., ICF – inverter current feedback) necessitate a sampling frequency that is six times higher than the LCL filter resonant one. Conversely, converters that utilize the output grid current as feedback (i.e., GCF – grid current feedback) require a sampling frequency that is six times lower than the LCL filter resonant one [5]. Consequently, if the design target of the grid connected inverter requires the sampling frequency to be above the LCL resonance constraints, the implementation of an effective damping mechanism is mandatory to ensure system stability. [6]. The technical literature propose solutions in the form of passive and active damping, which have been demonstrated to be efficacious in mitigating stability issues [7], [8]. It is also possible to achieve attenuation of switching harmonic components by acting directly on their source. Specifically, the augmentation of the voltage levels provided by the multilevel converter renders it feasible to reduce the current ripple and consequently enhance the power quality [9]. Therefore, the multilevel configuration is conducive to enhancing the voltage power quality of converters improving in the mean time the effectiveness of current filtering. This, in turn, results in enhancements to cost, performance and size of the converter and any associated maintenance requirements.

The present paper reports on the design of a three-phase NPC converter that is characterised by grid current feedback. Furthermore, an investigation has been conducted into the impact of grid voltage pollution on the current quality delivered by the proposed NPC inverted configuration. Indeed, the voltage quality standards of each country define the maximum harmonic contents of grid voltage in accordance with the classification of power system. Within the Italian contexts, the voltage quality standard is defined by CEI EN 50160. This standard establishes that grid voltage may contain harmonics components the magnitude of which must not exceed specified values. In particular, the fifth and seventh harmonics, which are the greater ones in this instance, must be no more than 6% and 5%, respectively. In consideration of these operative conditions, an investigation was conducted into the impact of

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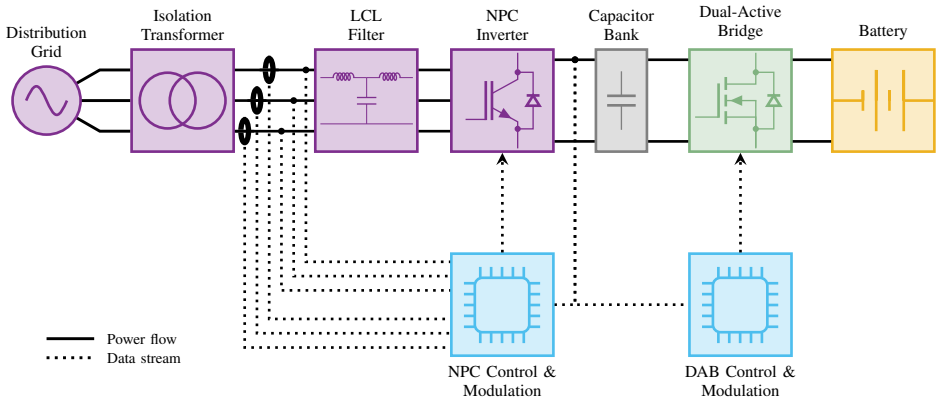


Fig. 1. Schematic of proposed Energy Storage System.

grid voltage pollution on NPC current quality, and a mitigation control strategy was implemented. Specifically, a digital notch filter compensator on a synchronous reference frame has been designed with the purpose of counteracting the fifth and seventh current harmonics introduced by voltage ones.

The paper is structured as follows: Section II describes the NPC converter, Section III present the digital control algorithm design. Finally, Section IV presents and discusses the experimental tests and performance evaluation.

## II. Grid-Connected NPC Converter

The NPC converter is designed to act as a power conditioning and interface system between an electrochemical battery and the grid. The topological configuration of the proposed grid-connected energy storage system is shown in Fig.1. The system under discussion consists of a battery connected to the NPC DC bus via a Dual Active Bridge (DAB). The purpose of the DAB is twofold. Firstly, it galvanically isolates the battery from the DC bus. Secondly, it regulates the battery voltage during the charging and discharging processes, ensuring a constant voltage on the NPC DC bus. The design of the three-phase NPC converter has been carried out in accordance with the design specification given in Table I. The NPC converter employs IGBT switches and includes an LCL filter. The schematic representation of the three-phase grid-connected NPC inverter is displayed in Fig.2. An 8 kVA insulation transformer has been interposed between the filter and the main grid to prevent zero-sequence current. The NPC converter is accomplished by paralleling three NPC half-bridges (PEN8010) manufactured by Imperix. The main characteristics of these components are reported in Table II. The half-bridge PEN8010 is equipped with P924F33 module manufactured by Vincotech. The salient characteristics of this module are in Table III. It is evident that each half-bridge has a DC bus, which is constituted by two banks of capacitors, named $C_H$ and $C_L$ each characterised by a capacitance of $517\mu F$. It can thus be concluded that, in view of the parallel connection of the three NPC half-bridges, the final values of $C_H$ and $C_L$ are 1.55 $mF$, respectively.

### A. LCL filter design

The current switching frequency harmonics of NPCs are subject to limits imposed by power quality standards. In this case, the LCL filter was designed with reference to the specifications given in Table I. An iterative procedure was used to evaluate the LCL parameters. This procedure was carried out with the aim of ensuring compliance with the design target and achieving the following objectives: (i) to obtain the maximum power factor; (ii) to minimise the voltage drop across the total value of the inductance; (iii) to comply with the constraints imposed by the switching and mains frequencies with regard to the LCL filter resonant frequency; (iv) to achieve a current ripple in compliance with the power quality standards [10]. The LCL filter design results in parameters whose values are given in Table IV.

TABLE I
Design Specifications

| | | | |
|---|---|---|---|
| **Rated power** | $P_r$ | 8 | kVA |
| **Rated grid voltage** | $V_g$ | 400 | $V_{RMS}$ |
| **Rated current** | $I_r$ | 11.5 | $A_{RMS}$ |
| **Ratel grid frequency** | $f_g$ | 50 | Hz |
| **Rated switching frequency** | $f_{sw}$ | 20 | kHz |
| **DC-link voltage** | $V_{DC}$ | 700 | V |

TABLE II
NPC Half-Bridge PEN8018 module rating

| | | | |
|---|---|---|---|
| **DC Bus voltage** | $V_{DC}$ | 800 | V |
| **Maximum continuous current** | $I_{DC}^{max}$ | 18 | $A_{RMS}$ |
| **Maximum pulsed current** | $I_{DC}^{pulsed}$ | 90 | A |
| **Reference switching frequency** | $f_{sw}$ | 20 | kHz |
| **DC bus capacitances** | $C_H\, C_L$ | 517 | $\mu$ F |
| **Maximum switching frequency** | $f_{sw}^{max}$ | 50 | kHz |

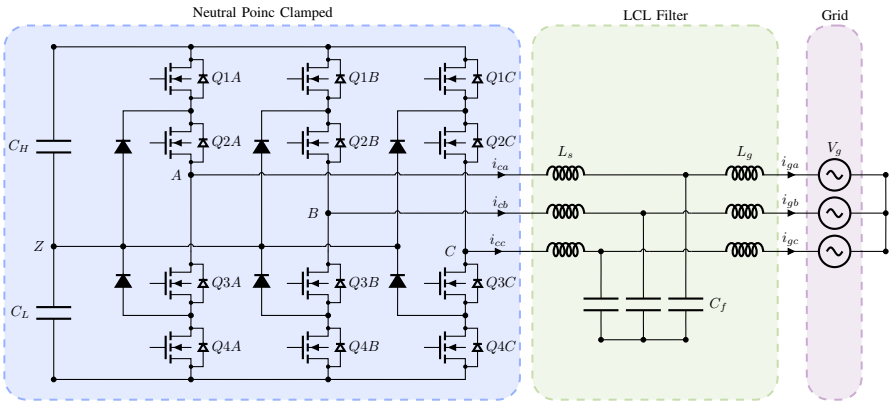


Fig. 2. Schematic of Neutral Point Clamped converter.

TABLE III
MODULE VINCOTECH P924F33 RATINGS

| | | | |
|---|---|---|---|
| **Collector-emitter Voltage** | $V_{ce}$ | 600 | V |
| **Collector Current** | $I_c$ | 33 | A |
| **Total power dissipation** | $P_d$ | 64 | W |
| **Gate-emitter voltage** | $V_{ge}$ | $\pm 20$ | V |
| **Turn-on delay time** | $t_{d(on)}$ | $101,6$ | ns |
| **Turn-off delay time** | $t_{d(off)}$ | $158,2$ | ns |

## III. ACTIVE DAMPING CURRENT CONTROL DESIGN

The synchronous rotating frame (SRF) control strategy of the NPC has been synthesised according to the model described in (1). The estimation of the instantaneous position $\theta$ of the grid voltage space vector is achieved by a phase-locked loop (SRF-PLL) [11]. Currents $i_d\, i_q$ and voltages $v_d\, v_q$ on axes $d-q$, synchronous with the voltage space vector, can be evaluated by implementing Clark and Park transformations. The decoupling of the $d$ and $q$ current loops is facilitated by the implementation of the grid voltage feed-forward together with the cancellation of the current cross-coupling components. In this way, the PI current controller synthesis can be performed in accordance with linear theory as reported in the block diagram in Fig. 3A.

The s-domain LCL filter transfer function can be evaluated from (2), where the parameters $\omega_{res}$ and $L'$ take the form reported in (3) according to the per-phase LCL equivalent circuit shown in Fig.4 [12]. Under this assumption, knowing the values of the filter and transformer parameters $L_s$, $L_g$ and $L_t$, the PI current controller parameters $k_p$ and $T_i$ given in (4) can be set to fix the current loop crossover frequency $\omega_c$. As shown in Fig. 3A), the sampling and computation time delay $\alpha\, T_s$ is taken into account in the current control system. It is assumed that the value of $\alpha\, T_s$ is not greater than one sampling period $T_s$, so that $\alpha$ is less than one or at most equal to one. To account for the PWM time delay, the ZOH model (5) has been introduced. Consequently, as a reference for the digital controller design [4], a global time delay of $1.5T_s$ was assumed.

TABLE IV
LCL FILTER PARAMETERS

| | | | |
|---|---|---|---|
| **Insulation transformer inductance** | $L_t$ | $0,68$ | mH |
| **Grid side inductance** | $L_g$ | $2,2$ | mH |
| **Resistance of grid side inductance** | $R_g$ | 65 | m$\Omega$ |
| **Converter side inductance** | $L_s$ | $2,2$ | mH |
| **Resistance of converter side inductance** | $R_s$ | 65 | m$\Omega$ |
| **Capacitor - Wye connection** | $C_f$ | 10 | $\mu$ F |

$$\begin{aligned} v_d &= R\, i_d + L\, \frac{d\, i_d}{dt} + \omega_s\, L\, i_q + u_d; \\ v_q &= R\, i_q + L\, \frac{d\, i_q}{dt} - \omega_s\, L\, i_d + u_q; \end{aligned} \tag{1}$$

$$G_{12}(s) = \frac{I_2(s)}{V_1(s)} = \frac{1}{(L_s + L_g + L_t)}\, \frac{1}{s\,(L' C_f\, s^2 + 1)} \tag{2}$$

$$\omega_{res} = \frac{1}{\sqrt{L' C_f}}; \quad L' = \frac{L_s\,(L_g + L_t)}{L_s + L_g + L_t}; \tag{3}$$

$$G_{PI}\,(s) = k_p \left(1 + \frac{1}{T_i\, s}\right) \tag{4}$$

The investigation of the open-loop transfer function of the current control system in the $s$-domain, reported in Fig.3 A, reveals a critical issue. It is evident that the resonant frequency of the LCL filter, denoted by $f_{res}$, exceeds $f_s/6$. Therefore, the system is susceptible to instability, as evidenced by the Nyquist criteria. It can thus be concluded that, the implementation of damping control schemes is imperative for successfully overcoming the constraint imposed by LCL resonance frequency. The solution that is analysed in this study is the introduction, as shown in Fig. 3 B), of a notch filter characterised by the transfer function reported in (6). It must first be noted that, in order to guarantee that no negative 180° crossing with the gain above 0 dB occurs, the proper tune of the notch frequency $f_n = \omega_n/2\pi$ is required.

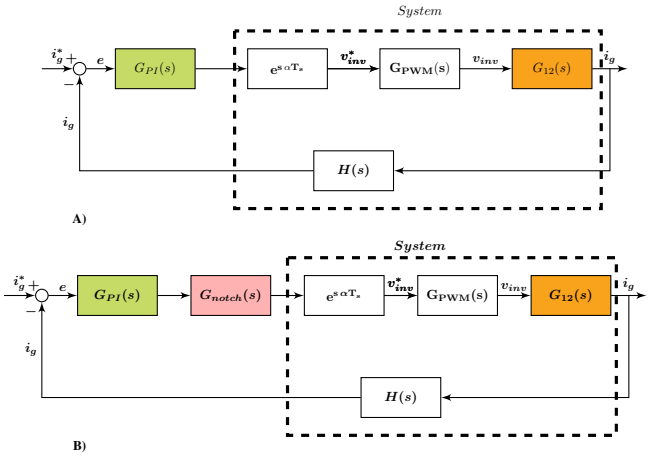


Fig. 3. Block diagrams ofd-q current control grid connected VSC: A) W/O active damping and B) with active damping.

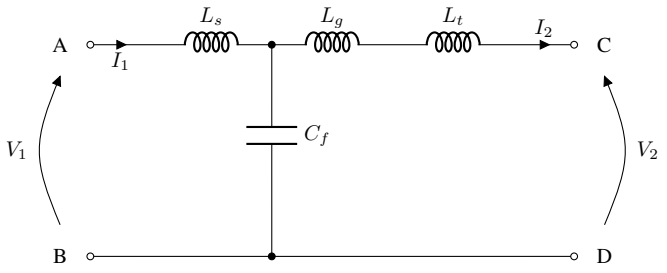


Fig. 4. Per-phase equivalent circuit of LCL filter.

The technical literature proposes a solution that entails the implementation of the notch filter frequency $f_n$ which is equal to LCL resonant one $f_{res}$. Nevertheless, the observed variations in grid impedance and LCL parameters suggest to select a higher value for $f_n$ than for $f_{res}$ in order to ensure the robustness of the current control system. Moreover, the digital implementation introduces a delay that must be considered to ensure that the phase margin attains values congruent with those required to achieve the settled dynamic performances [8]. In order to reach this objective, it is imperative to allocate particular attention to the discretisation of the notch filter. This is a necessary measure to prevent the introduction of undesired effects.

$$G_{\mathrm{PWM}}(s) = \frac{1 - e^{-sT_s}}{s}. \tag{5}$$

$$G_{\mathrm{notch}}(s) = \frac{s^2 + +\omega_n^2}{s^2 + 2\xi\omega_n\, s + \omega_n^2} \tag{6}$$

### A. Digital Controller Design

As previously stated, the implementation of active damping is mandatory in this case study to guarantee the stability of current control. An investigation has been conducted into the notch filter's functionality as an active damping system when it is cascade connected to the PI current controller. The initial phase of the design process for the notch filter involves the establishment of the cutting frequency, $f_n$. In this particular instance, $f_n$ has been set at 1660 Hz.

The aforementioned value has been defined with reference to the most unfavourable possible condition associated to parameter variations. In particular, the situation of grid impedance of $L_g$ equal to zero and a simultaneous drift of 5 % of the LCL passive components has been assumed as worst-case for the evaluation of $f_n$ . The parameters of the PI controller have been configured to achieve a crossover frequency $f_c$ of 100 Hz. Consequently, the $k_p$ and $T_i$ assume the values of 3.14 V/A and 16 ms, respectively. The discretisation of the notch filter and the PI current controller has been developed by implementing the Tustin transformation to $G_{notch(s)}$ and $G_{PI(s)}$, respectively. In relation to the digital notch filter, the transfer function in the $z$-domain assumes the form reported in equation (7),

$$G_{notch}(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}}; \tag{7}$$

where the coefficients assume the values reported in (8) and $k_1$ $k_2$ are functions of both the natural frequency $\omega_n$ and the bandwidth $BW$, as reported in (9) [8].

$$\begin{cases} a_0 = 1 \\ a_1 = k_1(1 + k_2) \\ a_2 = k_2 \end{cases} \qquad \begin{cases} b_0 = \frac{1}{2}(1 + k_2) \\ b_1 = k_1(1 + k_2) \\ b_2 = \frac{1}{2}(1 + k_2) \end{cases} \tag{8}$$

$$\begin{cases} k_1 = -\cos(\omega_n) \\ k_2 = \frac{1-\tan\left(\frac{BW}{2}\right)}{1+\tan\left(\frac{BW}{2}\right)} \end{cases} \tag{9}$$

The digital notch filter $G_{notch}(z)$ can be implemented by using the Direct-Form II transposed (DFIIt) structure whose block diagram is shown in Fig.5. To analyse the performance of the synthesised controller and notch filter, the open-loop transfer function in $z$-domain of the grid current control scheme reported in Fig.3B) has been evaluates referring to (10).

$$G_o(s) = G_{PI}(z) \cdot G_{notch}(z) \cdot Z\left\{e^{s\alpha T_s} \cdot G_{PWM}(s) \cdot G_{12}(s)\right\} \tag{10}$$

The usage of the notch filter with the designed values of $f_n$ and bandwidth $BW$ introduces a phase shift and a zero -pole cancellation that improve the phase in correspondence of $f_{res}$. The gain margin in proximity of $f_{res}$ and the phase margin at $f_c$ achieve 10 dB and 78 degree, respectively. Moreover, the closed loop current $z$-transformation $W(z) = G_o(z)/[1 + G_o(z)]$ confirms the stability because its poles are all placed into the circle of radius equal to one.

### B. Harmonic Current Compensation

The experimental investigation into power quality demonstrated the occurrence of low frequency current harmonics corresponding to the presence of grid voltage ones [11]. In order to surmount this issue, it is recommended that the PI regulator be integrated with a harmonic compensator (HC).

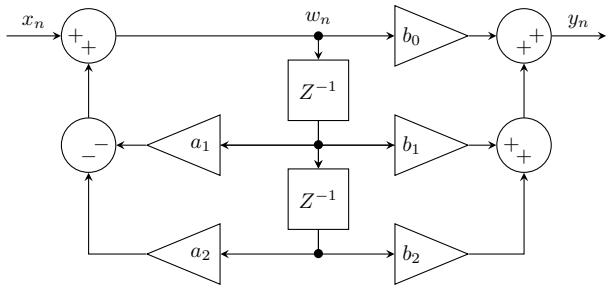


Fig. 5. Digital structure of implemented Notch Filter.

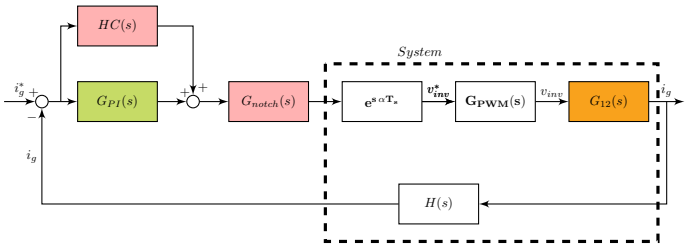


Fig. 6. Block diagrams of NPC current loop control with HC integration.

Specifically, the analysis of grid voltage has revealed significant contributions to NPC's output grid current by both the fifth and the seventh voltage harmonic components. Referring to the synchronous reference frame, these two harmonics possess the same absolute frequency equal to $6\omega_g$. Therefore, a single harmonic compensator (HC) operating on a single frequency has the capacity to mitigate the voltage effects engendered by the fifth and seventh harmonics. In accordance with this assumption, an HC founded upon the proposed notch filter has been designed imposing the frequency $f_n^{HC}$ at 6 $\omega_g$. Hence, the block diagram of the current control system assumes the form schematically depicted in Fig.6.

### C. DC-link Voltage Balancing

A challenge associated with NPC converters relates to potential unbalance phenomena occurring between the capacitors making up the DC bus. This phenomenon is associated with the use of specific switching state of NPC that cause average current circulation on the floating point Z of the DC Bus. These conditions are known to cause voltage imbalance between capacitors $C_H$ and $C_L$.

The control strategies reported in the scientific literature for balancing the neutral point Z can be classified according to the PWM algorithm used. It is known that the zero-sequence voltage is the only degree of freedom that can be adjusted in the modulation process to compensate for this effect [13]. In the present paper, the injection of a zero-sequence voltage component has been chosen as the balancing algorithm to compensate for the unbalance occurring on the $V_H$ and $V_L$ [14]. Specifically, considering the implementation of space vector PWM, the zero-sequence has been directly added to the normalised reference voltage after the Clark anti-transformation. The normalised zero-sequence voltage used to mitigate the voltage unbalance is evaluated using (11).

$$V_o^{pu} = \frac{V_H - V_L}{V_{DC}}\, sign(I_d). \tag{11}$$

## IV. Experimental Results

The proposed control algorithms have been implemented on the prototype according to the design procedure reported in Section III, using a rapid prototyping controller (B-Box RCP 3.0) employing Matlab/Simulink [15]. The B-Box RCP 3.0 is equipped with a dual-core 1 GHz ARM processor, which allows for a closed-loop control frequency up to 250 kHz. The sampling frequency has been set at 20 kHz. Three isolated voltage sensors with a measurement bandwidth of 60 kHz, an accuracy of 0,15 % and input voltage ranging till 800 V have been installed on the PCC. Three isolated current measurement sensors (LAH 50-P) provide the feedback signals for current loop control. A four-quadrant grid simulator (Regatron TC.ACS) with a rated power of 50 kVA is used as a grid voltage source. The test bench is shown in Fig.7.

To perform the test, a symmetrical sinusoidal three-phase voltage of 100 $V_{RMS}$ at a frequency of 50 Hz was imposed as the mains voltage. The DC bus voltage $V_{DC}$ was set at 350 V. The performances were evaluated for different operating current and grid voltage conditions.

In order to evaluate the expected performance of the implemented NPC converter without harmonic compensator the evolution of the grid currents was carried out for an $i_d$ set-point of 10 A. The experimental results are shown in Fig.8. As expected the current harmonic content associated with the switching frequency is 0.1% at 20kHz and reaches its maximum amplitude of 0.2 % at 60 kHz. The $THD_i$ shown

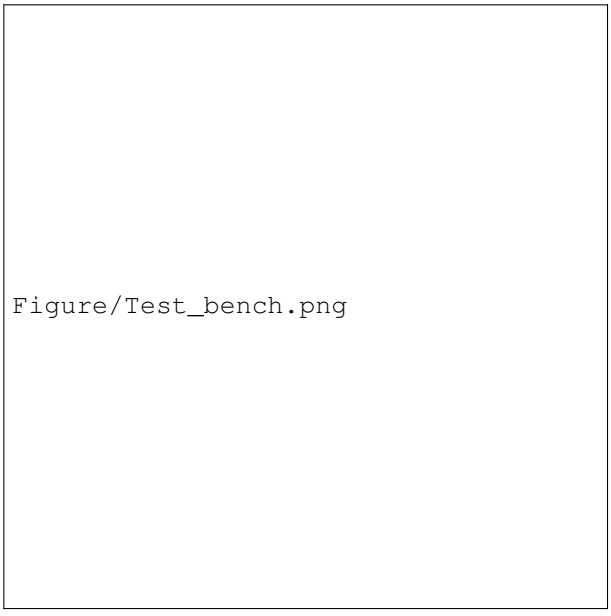


Fig. 7. The Test bench used for the experimental validation

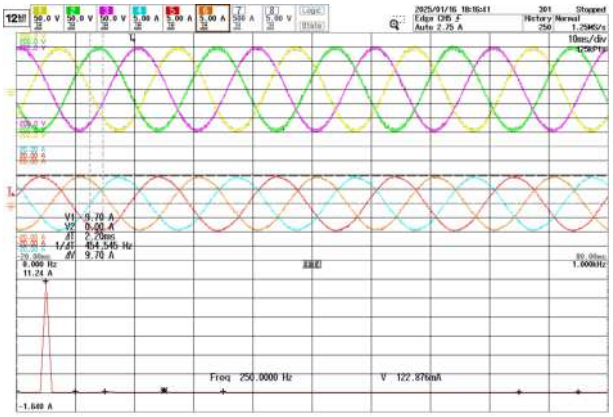

Fig. 8. Grid side currents during a $i_d$ set-point of 10 A when grid voltages are not affected by any harmonic pollution

in Fig.8 reveals the presence of $5^{th}$ and $7^{th}$ current harmonics whose amplitudes are of 1.3% and 0.3%, respectively.

Subsequently the same test has been performed injecting $5^{th}$ and $7^{th}$ harmonics on the grid voltages with the same amplitude of 4% concerning the fundamental one. The results are reported in Fig.9. The currents THD shows the presence of $5^{th}$ and $7^{th}$ harmonics whose amplitudes are of 1.5% and 3.4%, respectively. However, these values increase significantly if the $i_d$ set-point is reduced, as shown in Fig.10, achieving for a set-point of 2 A the 19% for the $5^{th}$ current harmonic and 14% for the $7^{th}$. Therefore an experimental investigation on the evolution of the $THD_i$ concerning the current set-point on the NPC converter in presence of grid voltage distortion on the $5^{th}$ and $7^{th}$ harmonics whose amplitudes are of 4%, in accordance with the Italian power quality standards CEI EN 50160, has been developed. The results are summarised in Fig.11 and reveal that the $THD_i$ limit of 5%, recommended by current quality standards, is overcome for current set-point lower than 10A. To evaluate the effects of single harmonic component on the output NPC current the same tests has been performed

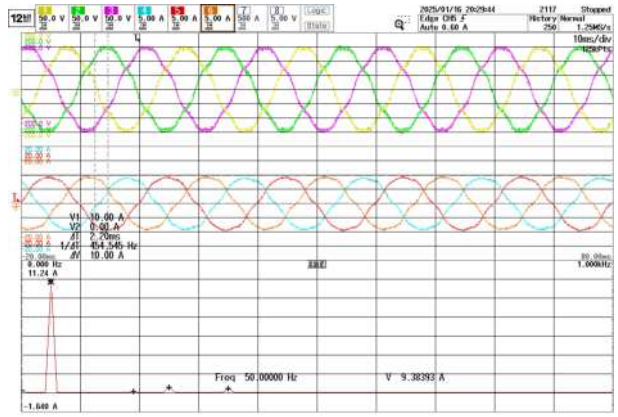

Fig. 9. Grid side currents during a $i_d$ set-point of 10 A when grid voltages are affected by an $5^{th}$ and $7^{th}$ harmonics distortion of 4%.

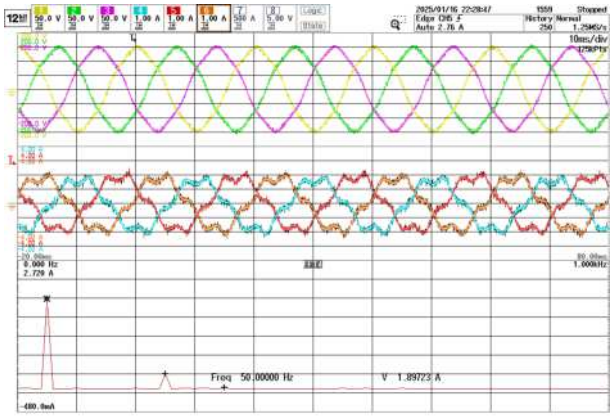

Fig. 10. Grid side currents during a $i_d$ set-point of 2 A when grid voltages are affected by an $5^{th}$ and $7^{th}$ harmonics distortion of 4%.

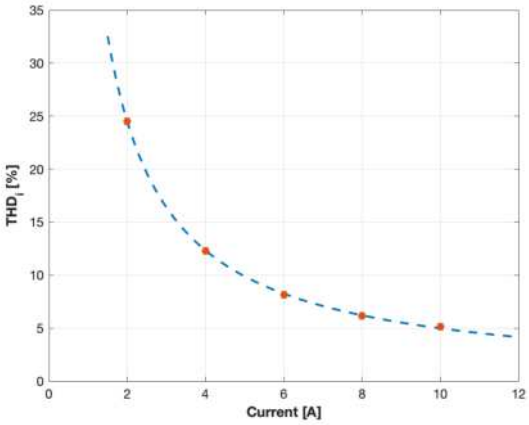


Fig. 11. Evolution of $THD_i$vs current set point on SRF under a voltage $5^{th}$ and $7^{th}$ harmonic distortions of 4% in magnitude concerning the fundamental one.

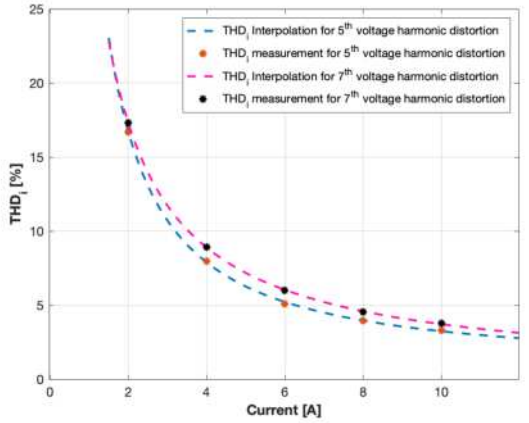


Fig. 12. Comparison of $THD_i$ vs current set point on SRF under the application of a voltage harmonic distortions of 4% in magnitude concerning the fundamental one for the $5^{th}$ and the $7^{th}$.

injecting one harmonic component in the grid voltage. The results, reported in Fig.12, highlight that the impact on the $THD_i$ is almost the same.

Subsequently, the proposed harmonic compensator has been activated and the comparison between the $THD_i$ with and without HC is reported in Fig.13. The mitigation achieved

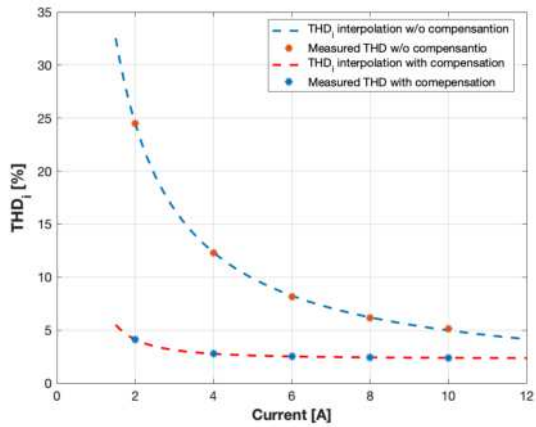


Fig. 13. Comparison of $THD_i$ vs current set point on SRF under a voltage $5^{th}$ and $7^{th}$ harmonic distortions of 4% in magnitude with and without harmonic compensator.

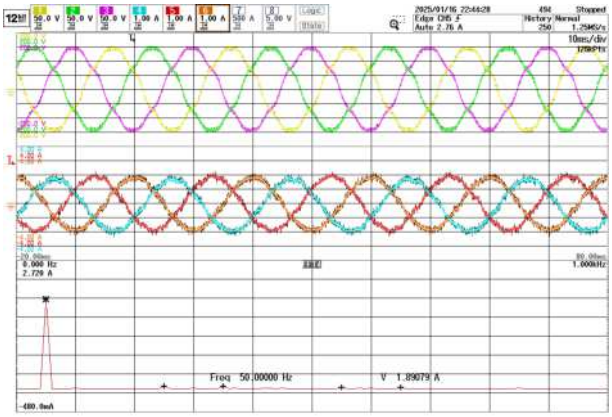

Fig. 14. Grid side currents during a $i_d$ set-point of 2 A when grid voltage is affected by an $5^{th}$ and $7^{th}$ harmonics distortion of 4% and harmonic compensator is on.

by the implementation of digital harmonic compensator on the $THD_i$ in presence of $5^{th}$ and $7^{th}$ grid voltage harmonic distortion is so efficacious to keep the currents into the power quality standard till a current of 2 A. This is also confirmed by the comparison of current evolutions, reported in Fig.14, recorded when the harmonic compensator is activated with those reported in Fig.10.

## V. Conclusion

The design of a grid-connected three-phase Neutral Point Clamp (NPC) converter is reported. In particular, the digital control system, the LCL filter and the DC voltage compensation, aimed at the grid connection of an energy storage system characterised by a rated power of 8 kVA, have been modelled and experimentally validated. Furthermore, the effect of the distortion of the grid voltage harmonics on the NPC has been experimentally investigated, highlighting the difficulties of meeting the power quality standards when the fifth and seventh grid voltage harmonics assume values that comply with the voltage quality standard. The reduction of the current distortions was achieved by means of a notch filter compensator designed for this purpose. The experimental results show the significant improvement especially for low values of the current setpoint. In particular, the current quality standard is met throughout the operating range when a voltage distortion of 4% occurs in the fifth and seventh harmonic components of the mains voltage.

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