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A HV-CMOS integrated circuit for neural stimulation in prosthetic applications

Lorenzo Bisoni, Caterina Carboni, Luigi Raffo *Member, IEEE*, Nicola Carta, Massimo Barbaro *Member, IEEE*

***Abstract*—An integrated neural stimulator for prosthetic applications, realized with a High Voltage (HV) CMOS $0.35\mu m$ process, is presented. The device is able to provide bi-phasic current pulses to stimulate 8 electrodes independently. A voltage booster generates a $17V$ voltage supply in order to guarantee the programmed stimulation current even in case of high impedances at the electrode-tissue interface. Pulse parameters such as amplitude, frequency and width can be programmed digitally. The device has been successfully tested by means of both electrical and *in-vivo* tests and the results show its capability to provide currents in the order of hundreds of μA with impedances in the order of tens of $k\Omega$.**

***Index Terms*—Neural stimulation, PNS stimulation, Biomedical interfaces, voltage booster, high voltage stimulator**

I. Introduction

NEURAL electrical stimulation has been widely used in the latest years in different biomedical applications, from cochlear implants to neurological disorders treatment [1]. In neural prosthetics, the stimulator is needed to provide sensory feedback to the patient, who will have thus more chances to feel the robotic limb as a natural extension of his/her body. Our work belongs to this latter field and proposes an integrated neural stimulator aimed to restore the sensory feedback in patients with upper limb amputation.

There are basically two different approaches to provide electrical stimuli to the nerves: generating voltages or currents. In both approaches the objective is to transfer a given charge through the electrode. While the generation of voltage pulses can be very efficient in terms of power consumption, the actually delivered charge depends on the highly variable electrode-tissue interface impedance. For this reason, it has poor performances in terms of amplitude resolution of the stimulus. On the contrary, with current-mode stimulation the amount of delivered charge depends entirely on controllable parameters (injected current and duration of the pulse), thus it can be designed with excellent amplitude resolution and high safety for the patient [2]. The major issue, in this case, is the high variability of electrode-tissue impedance whose value depends on the electrode placement inside the nerve and varies in the range $10k\Omega - 1M\Omega$ [3] from electrode to electrode and during the lifetime of the implant. Therefore, reproducibility of the current stimuli requires the use of a high voltage supply and, thus, high voltage transistors in order to accommodate the large voltage drops required even by low stimulation currents. The paper is a development of [4], in which a first design was sketched and the simulation results were presented. This paper describes in details the circuits used to implement the booster and the stimulator and presents the measured results obtained with electrical tests and acquired with in-vivo experiments.

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The authors are with the Department of Electrical and Electronic Engineering, Università di Cagliari, Cagliari I-09123, Italy. Corresponding author: Lorenzo Bisoni (email: lorenzo.bisoni@diee.unica.it).

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II. Motivation and aim

This work is aimed at the realization of an integrated stimulator for the implementation of a bi-directional neural interface to be used in experiments on human amputees. The stimulator should generate programmable current waveforms [5][6] with amplitude resolution of $10\mu A$ and a time resolution of $0.8\mu s$. Typical neural stimulation patterns are bi-phasic current pulses, shown in Fig. 1, with programmable amplitude (A) in the range $10\mu A - 300\mu A$, period (T) from $2.5ms$ to $1s$ and pulse width (W) from $50\mu s$ to $150\mu s$. Bi-phasic pulses are needed since it has been demonstrated that the charge accumulation at the tissue interface can produce severe damages to the cells [7]. To prevent these risks, bipolar active or passive waveforms should be used, in this way the charge accumulated in the first phase is compensated in the opposite phase. Any residual charge due to mismatch between the pulses must be eliminated by connecting the terminals through a resistor or using other techniques such as blocking capacitors [8]. As shown in Fig. 1, each pulse is therefore characterized by 4 phases: cathodic, anodic, charge-cancellation and a final resting phase in which the electrode terminal is disconnected from the stimulator. The pulse phases are independently generated and can differ in duration if necessary. A complete integration of the stimulator is required to reduce the encumbrance of the electronics and let the patient move freely, without impeding connections to lab instrumentation. The electronics will be connected by transcutaneous wirings to the implanted TIME electrodes as those used in [5]. For this reason, a voltage booster able to provide a voltage supply up to $17V$ is needed

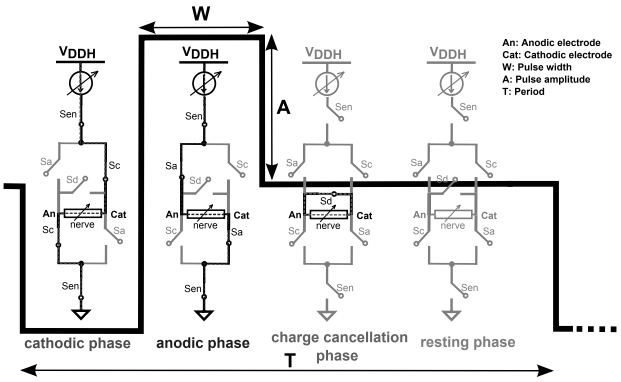


Fig. 1: Stimulation phases and switch configuration.

to deliver currents in the order of hundreds of μA even in case of impedances in the range of tens of $k\Omega$. Experimental sessions will last up to $6-8$ hours during which the stimulator should be powered by a battery.

III. Circuit Design

The architecture of the proposed high voltage stimulator is presented in Fig. 2. The device embeds a programmable voltage booster that increases the stimulation voltage up to $17V$ starting from a $3.3V$ power supply. The generated high voltage is shared between 8 independent stimulation channels. Each channel includes a low voltage pulse generator based on a 5-bit current DAC followed by an output stage that converts the generated pulse from a low into a high voltage current stimulus ready to be injected/sinked to/from the nerve. The IC was realized in a $0.35\mu m$ HV CMOS process from

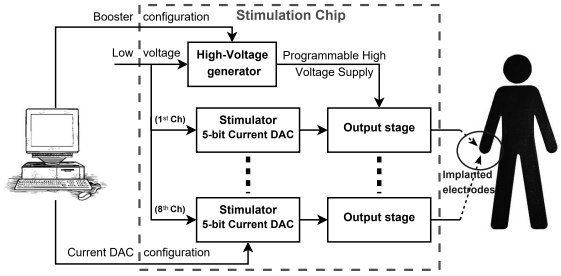


Fig. 2: Block diagram of the neural stimulation system.

AMS including both low voltage and high voltage transistors able to support up to $50V$. The stimulation circuits and the switch configuration used to generate each phase have been represented in Fig. 1 overlapped to the corresponding pulse phase. The stimulation is enabled by closing switches S_{en}; when also switch S_{c} is closed, the cathodic phase is started; closing S_{a} and opening S_{c} the anodic current is delivered to the electrode. Switches S_{en} stay open in the last two phases: during charge-cancellation S_{d} is closed to short the electrode terminals and, finally, when all the switches are open the electrode is disconnected from the stimulator (resting state). The anodic electrode in Fig. 1 is shared by all the 8 stimulation channels (the catodic electrodes) and represents a reference electrode properly placed inside the nerve or in the patient

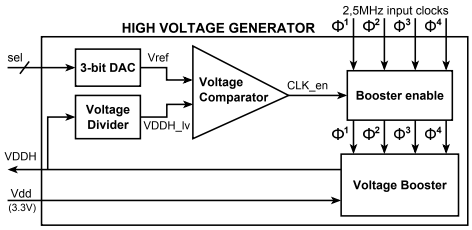


Fig. 3: Block diagram of the high voltage generator.

body. All the switches are driven by an external controller that handles the different pulse phases through a 16-bit SPI interface clocked at $20MHz$. The SPI clock frequency sets the time resolution of the stimulus pattern at $0.8\mu s$ which is the time required for a single write operation.

A. High voltage generator

As depicted in Fig. 3, the high voltage generator is comprehensive of a voltage booster and a voltage regulator. The voltage booster is the core module that generates the required voltage level programmed through the 3-bit signal (*sel*). It is based on a Dickson charge pump circuit in which each cell contains a MOSFET-based diode and a charge-transfer capacitor. The specifications for the voltage booster were calculated trying to minimize the chip area and to reduce the boosting time. In order to reach the target output voltage of $17V$ and to minimize the area, 9 stages are required ($N = 2 \times (Vout/Vdd - 1)$)[9]. Since only $2.35ms$ are available to recover the charge between two subsequent pulses (in case of maximum stimulation frequency), one more stage was added to reduce recovery time. Fig. 4 shows two cells of the charge pump connected together. The diodes are implemented with HV-PMOS transistors [10]: M_1 is the transistor responsible of the charge transfer, M_2 and M_3 connect the wafer substrate to the maximum voltage between those at M_1 drain and source. M_4 with C_g capacitor guarantees that the V_{gs} of M_1 does not exceed the $3.3V$ power supply so that the transistor M_1 can be turned on/off by means of a low voltage ϕ_i signal. The gate of M_4 is controlled by the clock signal ϕ_3, for the first cell and, for all the other stages, by the clock at the M_1 gate of the previous stage. These connections allow to open M_1 diode connection during the charge phase and to connect it in diode-mode during charge transfer to the subsequent cell.

The operating principle of the boosting chain is the turnover of two different phases by means of four $2.5MHz$ clocks ($\phi_1, \phi_2, \phi_3, \phi_4$) depicted in the inset in Fig. 4. Clock frequency was chosen for compatibility with the requirements of a recording chip driven by the same signal that completes the bi-directional interface. Clocks ϕ_1 and ϕ_2 drive to the odd cells while ϕ_3 and ϕ_4 control the even cells. In Fig. 4 the circuit of the first two Booster's cells is shown in details: during phase 1, $\phi_1 = 0V$ and $\phi_2 = 0V$ the transistor M_{1a} is on and current flows from V_{in} charging C_{ta}. In phase 2, $\phi_1 = 3.3V$, M_{1a} turns off, isolating C_{ta} from V_{in} and $\phi_2 = 3.3V$ forces the C_{ta} charge to move through M_{1b} on C_{tb}, this is allowed by the clocks ϕ_3 and ϕ_4 in cell b that are both low. The charge transfer described for the first cells

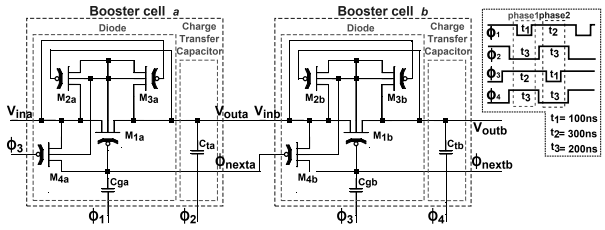
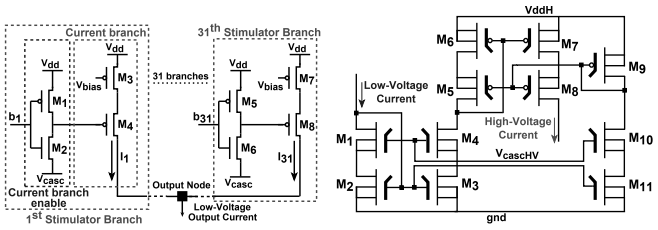


Fig. 4: Schematic diagram: voltage booster cells.



(a) (b)

Fig. 5: Schematic diagram: (a) stimulator module and (b) output stage diagram.

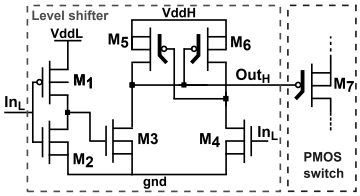


Fig. 6: HV PMOS switch: $17V$ level shifter and HV PMOS.

is replicated for all cells. Continuously switching the two phases, small amounts of charge are transferred from one stage to the next one until when the charge reaches the final accumulation capacitor (C_{acc}). Its dimension has been chosen considering the maximum stimulation current of $300\mu A$ and the maximum pulse width of $150\mu s$, in this case, the maximum amount of charge to be delivered to the nerve is $45nC$ for each pulse side (positive and negative). As a consequence and for a given electrode impedance of $50k\Omega$ the booster needs to charge an accumulation capacitor C_{acc} of, at least, $20nF$. The transfer capacitance has been chosen minimizing the area, according to [9], the optimum value is calculated as $C_t = N \times \frac{I_L T}{(N+1V_{dd}-V_{out})}$ that results in a $C_t = 62pF$, we tuned this value simulating the circuit and obtained the same boosting rate using a $C_t = 50pF$. Moreover, to balance the stimulus phases and to increase the maximum stimulation frequency, two independent boosters were embedded in the chip and two different accumulation capacitors were used. One booster is used in the anodic phase and the other in the cathodic phase. Thus, during each phase the booster that is not involved in the stimulation can recover the charge delivered to the nerve in the previous phase getting ready for the next stimulation.

The size of the diode-transistor M_1, has been chosen considering the charge delivered during each stimulation pulse and the minimum time between two subsequent pulses. As already mentioned, within a stimulation pulse, the maximum charge delivered to the electrode is $45nC$ for each phase (with current amplitude of $300\mu A$ and duration of $150\mu s$). Since the maximum work frequency is $400Hz$ ($T = 2.5ms$), in the worst case, the charge transferred to the nerve must be recovered in $2.35ms$. During this time, with the booster clock frequency of $2.5MHz$, 5875 clock cycles occur, therefore $7.6pF/cycle$ are transferred to recover the consumed charge ($45nC$). This corresponds to a current of $76\mu A$ (since $T_{on} = 100ns$). Considering the technology parameters, to achieve such current a $W/L = 25$ has been calculated. This is valid for a single channel stimulation, to allow the parallel simulation of at least 4 channels a $W/L = 100$ was used. Since for the HV transistors $L_{min} = 2.8\mu m$ a $W = 300\mu m$ was chosen. The voltage booster is regulated by means of a voltage regulator that compares the booster output with a target voltage generated by a 3-bit DAC. In order to save area, the regulation circuitry was completely designed with low voltage transistors and, as a consequence, the booster high voltage output is scaled into a low voltage range between $0V$ and $3.3V$ before being compared. Depending on the comparison result, the voltage comparator enables/disables the generation of the four clock signals turning on/off the booster.

B. Stimulator

This module generates the stimulation current pattern in a low voltage domain on the base of the selection bit programmed by an off-chip controller. The stimulator is based on a 5-bit current DAC that can generate currents in a range from $10\mu A$ up to $310\mu A$ with a resolution of $10\mu A$. The stimulator diagram is depicted in Fig. 5(a). The base current is generated by a common bias circuit and mirrored into 31 equal branches (thermometric code) switching the gate voltage of the enabler pmos transistor (M4 and M8 in Fig. 5(a)) from V_{dd} to V_{casc}. Both voltages, V_{bias} and V_{casc}, are generated by the on chip bias circuit.

C. Output stage

The output stage converts the stimulation current from a low into a high voltage domain using the high voltage generated by the boosters. It is implemented as a current mirror that copies the low voltage current from the stimulator in a branch with high voltage transistors connected between the high voltage (*VddH*) and *gnd* as depicted in Fig. 5(b). The voltage VcascH used to polarize the HV NMOS transistor is generated by the on-chip common bias circuit. This module includes also high voltage switches to implement S_1, S_2 and S_3 from Fig. 1 whose functionalities are described in Sec. III. As depicted in Fig. 6, switching from *gnd* to *VddH* and viceversa requires a HV NMOS or PMOS and a voltage level shifter. It converts the switch driving signals from a low ($0V - 3.3V$) into a high ($0 - 17V$) voltage domain.

IV. Experimental Results

The IC layout was designed reducing, as much as possible, the mismatch among the 8 stimulation channels. The two

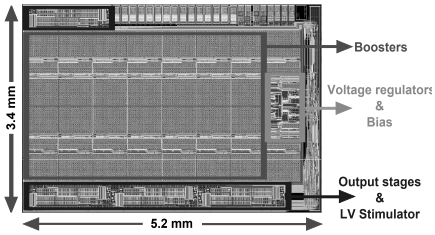


Fig. 7: Designed IC layout.

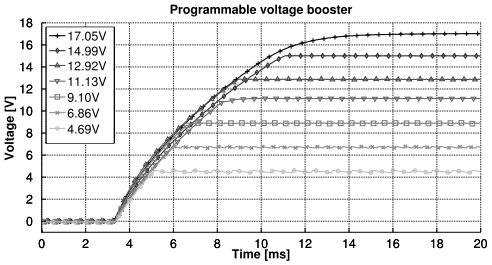


Fig. 8: Booster programmable output voltage.

$20nF$ booster charge-accumulation capacitors were placed off-chip, in this way an overall IC area of about $17.68mm^2$ as depicted in Fig. 7, was obtained. The experimental setup used to test the realized stimulator is comprehensive of a custom PCB and a Xilinx FPGA Spartan-6 LX45. The former hosts the IC, the external charge-accumulation capacitors and a $3.3V$ voltage regulator whereas the latter is used to configure the parameters of the stimulator by using the $20MHz$ SPI protocol. In particular, the stimulus pattern and the high voltage level must be defined. The FPGA also provides the $20MHz$ clock to generate the 4 clock signals for the boosters. The entire system was completely tested, firstly, by means of laboratory measurements and then with *in-vivo* experiments. To start with, both boosters were completely characterized in terms of high voltage programmability and boosting time. As depicted in Fig. 8, they can effectively generate an output voltage in the range $4.69 - 17V$ with steps of about $1V$, showing a boosting time of $9ms$ to reach the maximum voltage level. Then, each stimulation channel was tested generating and delivering different current patterns to resistors with different values chosen to emulate the electrode impedance. Fig. 9(a) refers to the injection of current pulses with an increasing amplitude into a $33k\Omega$ resistor and shows a stimulation current programmability from about $10\mu A$ to $310\mu A$ with steps of $10\mu A$. To conclude with the IC characterization, a $400Hz$ pulse train with $152\mu s$ cathodic and anodic phase duration was delivered to a $33k\Omega$ resistor. The complete pulse train with the C_{acc} discharge in correspondence of each cathodic (lower plot) and anodic (upper plot) phase is depicted in Fig. 9(b). Finally, the system was tested *in-vivo* on rats using TIME electrode implanted in the sciatic nerve. Different current patterns were injected into the rat nerve and the evoked plantar and tibial EMG response was measured by means of a commercial EMG recorder. In particular Fig. 10 shows an increasing response from the rat tibial muscle by rising the stimulation current from $10\mu A$ up to $310\mu A$. This is a very important result because it proves that our system can overcome the problem of the high impedance at the electrode-tissue interface injecting enough level of current into the nerve.

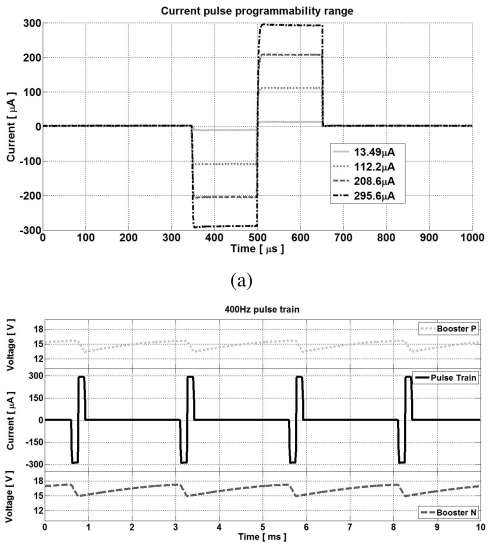


Fig. 9: Current stimulus delivered to a $33k\Omega$ resistor with $152\mu s$ anodic and cathodic phases: (a) current programmability range and (b) a $400Hz$ pulse train (central plot) with the correspondent booster discharges (top and bottom curves).

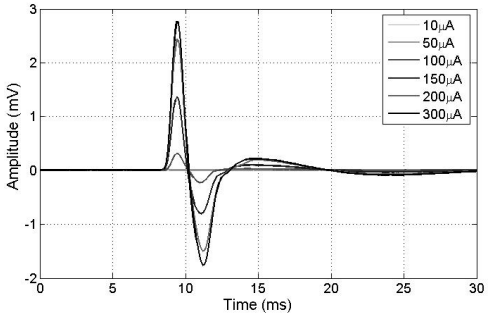


Fig. 10: In-vivo test: tibial EMG response obtained by increasing the stimulation current of a single TIME active site.

V. Discussion and Conclusion

The device performances are summarized in Table I and compared with other papers on the same topic. The circuit can deliver relatively high currents to impedances up to $50k\Omega$ which is a considerably higher value than that achieved with other approaches. The electrode contact impedance is a crucial aspect in peripheral neural stimulation, considering that it increases during the implant lifetime due to electro-chemical reactions at the tissue interface. Even a few days/weeks after the implant the impedance can grow up to tens of $k\Omega$[5], thus silencing the active site. In order to keep most of the electrodes alive, the supply voltage should be increased properly. This was the main aim of the proposed work and it was achieved thanks to the high voltage generator that

	[12]	[13]	[14]	This work
Tech.	CMOS $0.35\mu m$	HV-CMOS $0.18\mu m$	CMOS $0.18\mu m$	HV-CMOS $0.35\mu m$
I [μA]	$0-450$	$0-500$	$0-320$	$0-310$
Load [$k\Omega$]	1.5	6	n.a.	50
V [V]	3	$3-11.5$	$8-0$	$2.5-17$
N	–	–	6	10
Ch.	1	8	1	8
A [mm^2]	0.58	5.4	1.27	17.68
Pw [mW]	n/A	n/A	3.8	$5-29$

TABLE I: Comparison between different stimulator.

provides voltages up to $17V$ in a boosting time of $9ms$. The programmable voltage regulator allows to increase the desired supply voltage following the degradation of the contact and preventing saturation of the output current.

The drawback of such approach is the higher power consumption mainly due to the large number of stages in the Dickson charge pump. Power consumption reported in Table I was measured in different working conditions: the static power is $5mW$, while the total power (static and dynamic), measured during a bi-phasic pulse stimulation of $300\mu A$ in amplitude and a duration of $150\mu s$, is $29mW$. More than 50% of such power is lost in the transfer capacitors C_t, because of the large number of stages. Moreover, a large amount of power is dissipated because the chosen HV-CMOS process has large parasitic capacitances: around 30% of power is dissipated by the bottom-plate parasitics of transfer capacitors. The achieved power efficiency is slightly lower than 10% which is the theoretical efficiency limit of a charge pump with 10 stages realized in a process with bottom-plate capacitors equal to 14% of the main capacitor, as calculated in [11].

Anyhow, power efficiency was not the main concern of the current implementation, which is aimed at experimental sessions with human volunteers lasting no more than 6-8 hours. Therefore, the design was not optimized in terms of power consumption, but rather in terms of delivered current, boosted voltage, area and recovery time. Nevertheless, even with present power consumption levels the device could be continuously operated for more than 70 hours with commercially available rechargeable batteries with a capacity in the order of $650mAh$. In future versions of the chip power consumption can be largely reduced optimizing design choices and process selection.

In conclusion, the implemented system has shown the capability to deliver completely configurable current pulses to a peripheral nerve in the range from $10\mu A$ to $310\mu A$ with steps of $10\mu A$. The *in-vivo* tests proved that our neural stimulator can inject bi-phasic current pulses into rat sciatic nerve exhibiting a good intraneural stimulation selectivity.

REFERENCES

[1] C. O. Oluigbo, A. Salma, and A. R. Rezai, "Deep brain stimulation for neurological disorders," *IEEE Reviews in Biomedical Engineering*, vol. 5, pp. 88–99, 2012.

[2] C.-S. Gong, K.-W. Yao, J.-Y. Hong, and M.-T. Shiue, "On investigation into a cmos-process-based high-voltage driver applied to implantable microsystem," in *VLSI Design, Automation, and Test (VLSI-DAT), 2012 International Symposium on*, April 2012, pp. 1–4.

[3] C. H. Chen, D. J. Yao, S. H. Tseng, S. W. Lu, C. C. Chiao, and S. R. Yeh, "Micro-multi-probe electrode array to measure neural signals," *Biosensors and Bioelectronics*, vol. 29, pp. 1911–1917, 2009.

[4] C. Carboni, L. Bisoni, N. Carta, and M. Barbaro, "Compact, multi-channel, electronic interface for pns recording and stimulation," *Proceedings of the IASTED International Conference Biomedical Engineering (BioMed 2014)*, pp. 65–71, 23-25 June 2014.

[5] S. Raspopovic, M. Capogrosso, F. M. Petrini, M. Bonizzato, J. Rigosa, G. Di Pino, J. Carpaneto, M. Controzzi, T. Boretius, E. Fernandez, G. Granata, C. M. Oddo, L. Citi, A. L. Ciancio, C. Cipriani, M. C. Carrozza, W. Jensen, E. Guglielmelli, T. Stieglitz, P. M. Rossini, and S. Micera, "Restoring natural sensory feedback in real-time bidirectional hand prostheses," *Science Translational Medicine*, vol. 6, no. 222, p. 222ra19, 2014.

[6] D. Loi, C. Carboni, G. Angius, G. N. Angotzi, M. Barbaro, L. Raffo, S. Raspopovic, and X. Navarro, "Peripheral neural activity recording and stimulation system," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 4, pp. 368–379, 2011.

[7] C. Huang, P. Carter, and R. Shepherd, "Stimulus induced ph changes in cochlear implants: An in vitro and in vivo study," *Annals of Biomedical Engineering*, vol. 29, no. 9, pp. 791–802, 2001. [Online]. Available: http://dx.doi.org/10.1114/1.1397793

[8] X. Liu, A. Demosthenous, and N. Donaldson, "An integrated implantable stimulator that is fail-safe without off-chip blocking-capacitors," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 2, no. 3, pp. 231 –244, sept. 2008.

[9] G. Palumbo and D. Pappalardo, "Charge pump circuits: An overview on design strategies and topologies," *Circuits and Systems Magazine, IEEE*, vol. 10, no. 1, pp. 31–45, First 2010.

[10] T. Yamazoe, H. Ishida, and Y. Nihongi, "A charge pump that generates positive and negative high voltages with low power-supply voltage and low power consumption for non-volatile memories," in *Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on*, May, pp. 988–991.

[11] M. R. Hoque, T. Ahmad, T. R. McNutt, H. A. Mantooth, and M. M. Mojarradi, "A technique to increase the efficiency of high-voltage charge pumps," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 5, pp. 364–368, 2006.

[12] S. Arfin and R. Sarpeshkar, "An energy-efficient, adiabatic electrode stimulator with inductive energy recycling and feedback current regulation," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 6, no. 1, pp. 1–14, Feb 2012.

[13] I. Williams and T. Constandinou, "An energy-efficient, dynamic voltage scaling neural stimulator for a proprioceptive prosthesis," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 7, no. 2, pp. 129–139, April 2013.

[14] Y.-C. Huang, M.-D. Ker, and C.-Y. Lin, "Design of negative high voltage generator for biphasic stimulator with soc integration consideration," in *Biomedical Circuits and Systems Conference (BioCAS), 2012 IEEE*, Nov 2012, pp. 29–32.